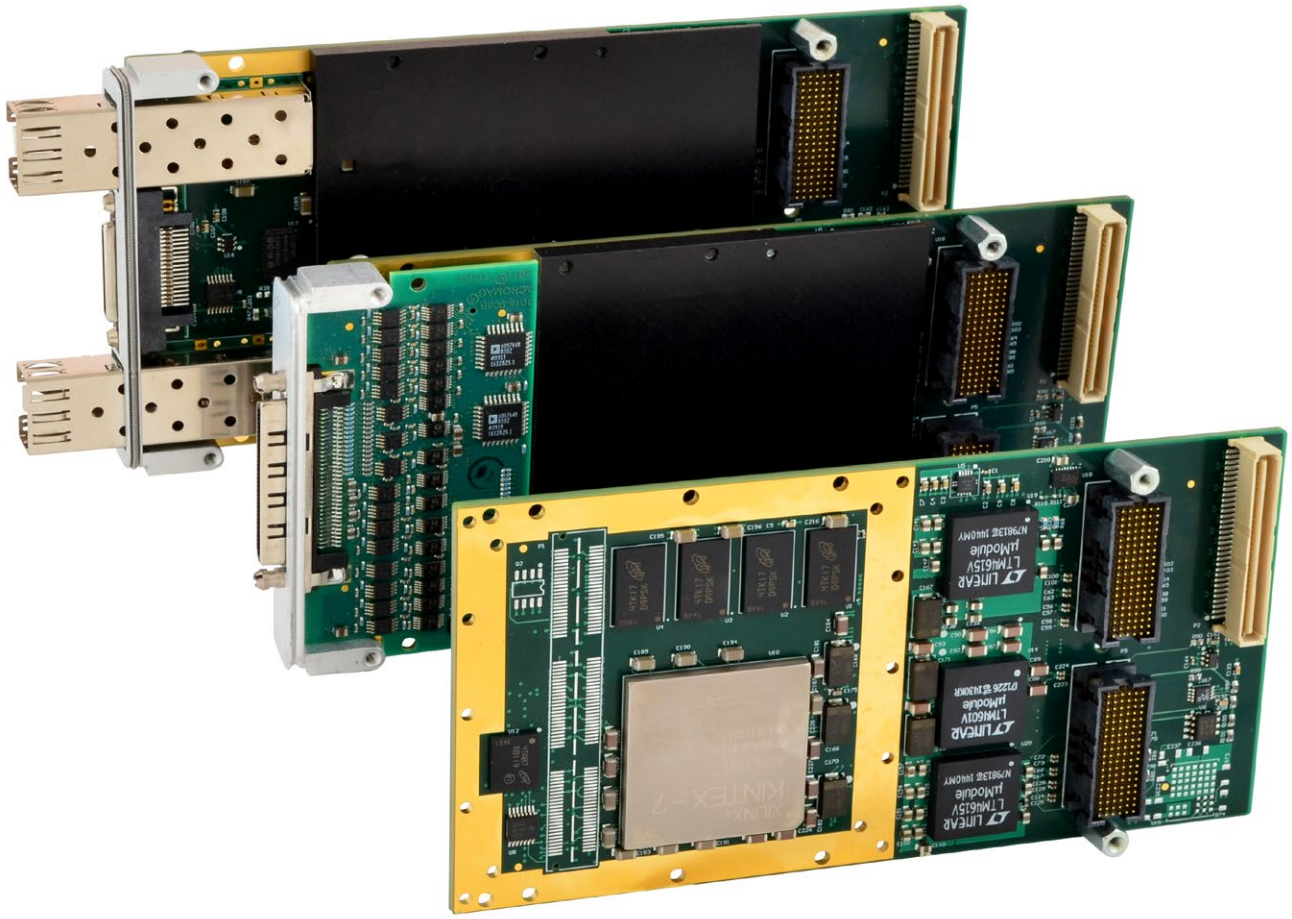
APPLICATION GUIDE

Acromag
THE LEADER IN INDUSTRIAL I/O

Programming AMD (Xylinx) Acromag XMC-7 FPGA Series with Vivado™

Products:

XMC-7A Series
XMC-7K Series



Bulletin # 8401093

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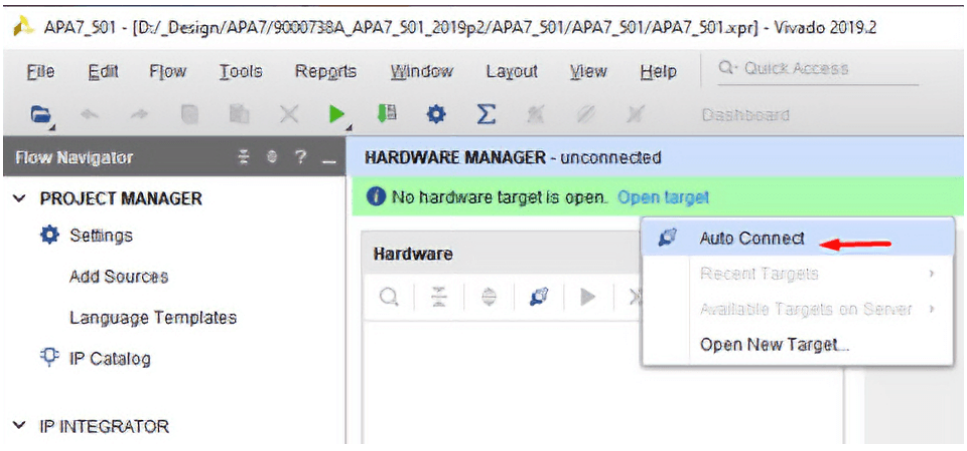
Overview

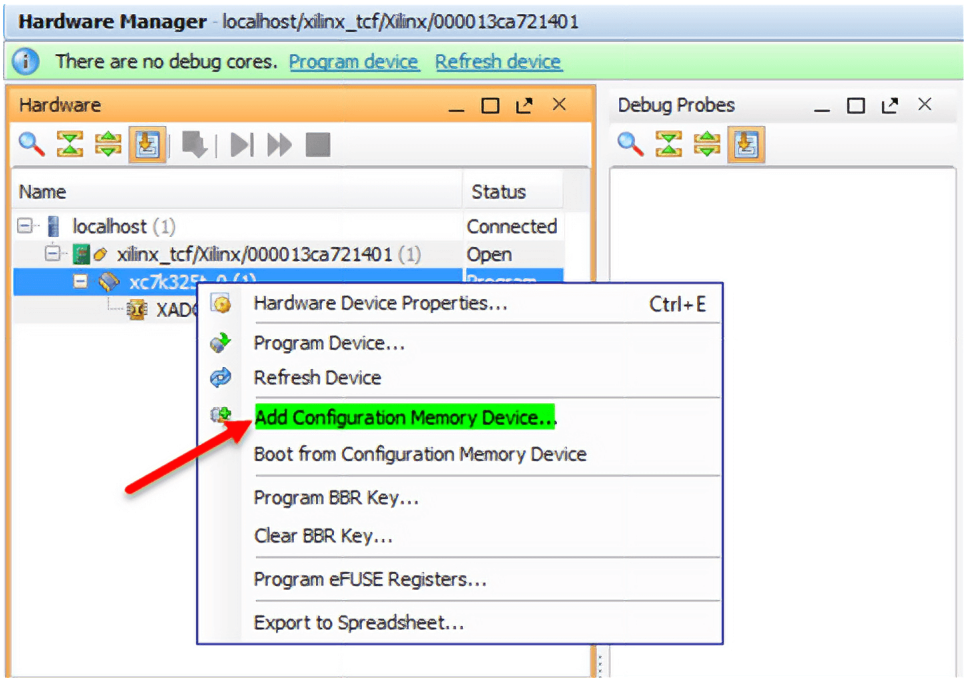
It is assumed that the user is familiar with FPGA programming via JTAG, and that you have the necessary JTAG programmer. One such programmer is the Xilinx Platform Cable USB II:

The XMC-7 Series FPGA mezzanine board is hosted on a carrier. To program the on-board FPGA, you will need to attach the JTAG cable to the carrier's 14-pin JTAG connector, then turn the host's power ON. Connect the USB cable from the JTAG programmer to the PC running Vivado. Once the JTAG programmer is recognized, locate and run Vivado.

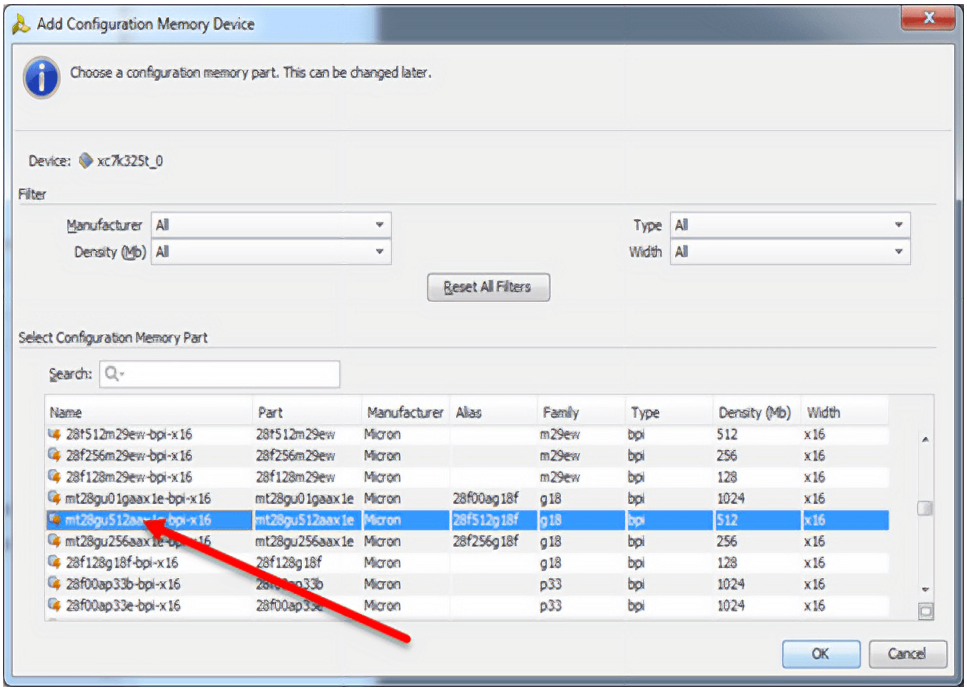
Once in Vivado, open the hardware manager. In hardware manager, click on **Open Target => Auto Connect:**



The Vivado hardware manager should detect the presence of the JTAG programmer and the AMD Xilinx FPGA. The following hierarchy should be displayed in the hardware pane.

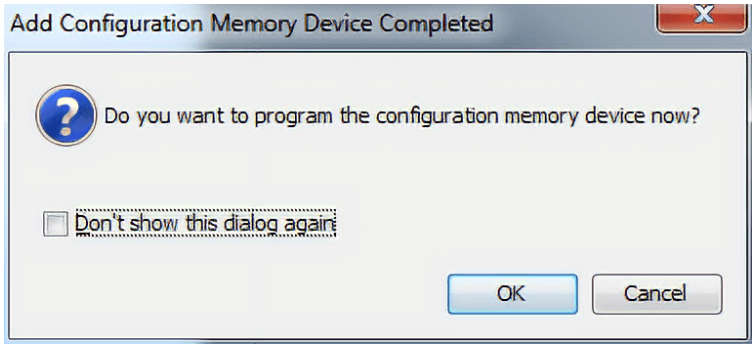


For XMC-7 series boards, you'll see xc7a200t, xca7k325t, or xca7k410t. Right-click on the appropriate **xc7** device in the hierarchy and then select "Add Configuration Memory Device..." command. An "Add Configuration Memory Device" dialog box appears. Scroll and select the configuration memory device present on your module. Select the following memory device: **Micron MT28GU512A.**



Select **OK**

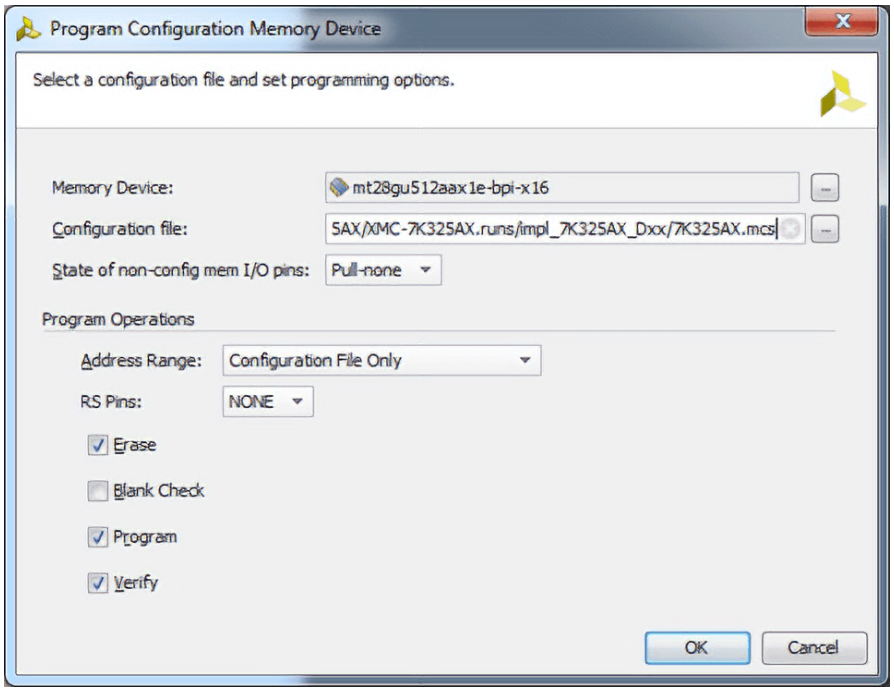
The following dialog box appears:



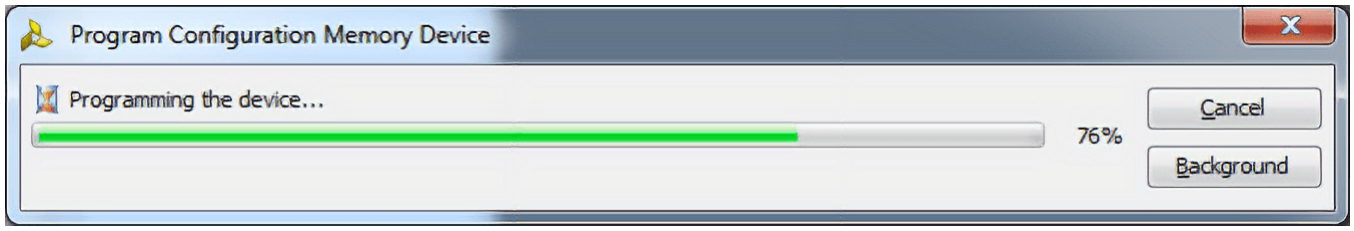
Select **OK**

The following dialog box appears. Click the ... button on the **Configuration file** line and browse to the location of the configuration file.

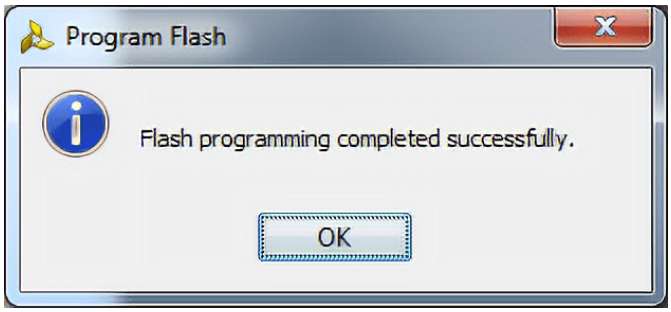
Select **OK**



The flash write progress is displayed.



The flash erase/program operation will begin.



Select **OK**

The flash is now programmed with the configuration file. **Cycle the power to the XMC-7 FPGA board (completely turn off the chassis hosting the board, wait a few seconds, then power back on)** to initiate the FPGA's bitstream load.