



APTIO™ HASWELL CORE BIOS MANUAL

For Acromag® Products

using the

Haswell Processor

ACROMAG INCORPORATED

30765 South Wixom Road

Wixom, MI 48393-2417 U.S.A.

Tel: (248) 624-1541

Fax: (248) 624-9234

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1.0 GENERAL INFORMATION

1.1 Intended Audience

This users' manual was written for technically qualified personnel who will need working information for the system BIOS used with Acromag® I/O devices that are based upon the Intel® Haswell 4th Generation core processor. It is not intended for a general, non-technical audience that is unfamiliar with the Haswell core processor or the devices that use this core processor..

1.2 About Aptio™

Aptio™ is AMI's next-generation BIOS firmware based on the UEFI Specifications and the Intel® Platform Innovation Framework for EFI. Aptio™ is specifically designed to address firmware portability and extensibility to future platforms. Along with silicon enabling components, Aptio™ can be expanded using a variety of drivers, development tools, support utilities and pre-boot application solutions. (*Aptio™ TSE User Manual, pg. 6*).

1.3 About Aptio™ Text Setup Environment (TSE)

Aptio™ Text Setup Environment (TSE) is a text-based basic input and output system. The purpose of Aptio™ TSE is to empower the user with complete system control at boot. AMI Text Setup Environment (TSE) provides advance UEFI functionality with a familiar BIOS interface. AMI TSE is an AMI firmware user interface designed to work in conjunction with Aptio™. It is made up of a series of drivers, applications and images, which can be customized according to an OEM's requirements, or can use AMI's default interface. In Aptio™, as in any firmware project, lack of flash space is always one of the biggest obstacles. One of the goals of Aptio™ is to offer a complete solution in 512 KB of flash ROM. In order to satisfy customers who require small ROM footprint without sacrificing the ability to use setup to configure the system, AMI offers space-optimized setup environment components called AMI Text Setup Environment (TSE). This document explains the basic navigation of Aptio™ TSE. (*Ibid, pg. 6*).

1.4 Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag,

1.5 Trademark, Trade Name and Copyright Information

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Acromag Incorporated
30765 South Wixom Road
P.O. BOX 437
Wixom, MI 48393-7037 U.S.A.

All rights reserved. Acromag and Xembedded are registered trademarks of Acromag Incorporated. All other trademarks, registered trademarks, trade names, and service marks are the property of their respective owners. The text information used in this manual in support of the specifications, screen, implementation, and use of the Aptio BIOS has been reprinted by permission from the public document *Aptio™ Text Setup Environment (TSE) User Manual*, Document Revision 1.00, Copyright © 2010 by American Megatrends, Inc (AMI). In addition, the figures, tables and all other visuals that appear in this manual are also taken from, or are based upon, content from the *Aptio™ Text Setup Environment (TSE) User Manual*, again with the permission of AMI. Because of the extent of the use of the AMI-supplied material in this material, that use is referenced in this paragraph in lieu of using individual in-text citations.

The images (figures, tables and screen shots) shown in this manual that are not from the *TSE User Manual* were also provided by AMI for the expressed purpose of inclusion in this Acromag-provided Core BIOS user manual.

1.6 Related Material

The following manuals and part specifications provide the necessary information for in-depth understanding of the XCOM-6400 module.

- *Aptio™ Text Setup Environment (TSE) User Manual*, Document Revision 1.00, Copyright © 2010 by American Megatrends, Inc.
- Intel® document No. 328901, “Mobile 4th Generation Intel® Core™ Processor Family Datasheet – Volume 1 of 2”, Rev: 002; September, 2013.

<http://www.intel.com/content/www/us/en/processors/core/CoreTechnicalResources.html>

1.7 Disclaimer

Changing BIOS setup parameters carries risks. It can lead to system instability and data loss or even cause the system to no longer boot. It is recommended that only advanced users change these settings.

Please proceed at your own risk. In no event shall Acromag be held liable for any loss, expenses, or damages of any kind, whether direct, indirect, incidental, or consequential, arising from the modification of BIOS settings or any other support materials provided in our products.

2.0 Aptio™ BIOS Setup

2.1 Main Menu

The Aptio™ TSE BIOS setup menu is the first screen that you can navigate. Each BIOS setup menu option is described in this user's manual. To enter the Aptio™ TSE screens, follow the steps outlined below:

Table 2.1.a Entering the Aptio™ TSE Screens

Step	Description
1	Power on the motherboard
2	Press the <Delete> key on your keyboard when you see the following text prompt: "Press DEL or F2 to enter Setup"
3	After selecting <Delete> key, the Aptio™ TSE main BIOS setup menu is displayed. You can access the other setup screens from the main BIOS setup menu, such as the Chipset and Power menus.

In most cases, the <Delete> key is used to invoke the Aptio™ TSE screen. There are a few cases where other keys are used, such as <F1>, <F2>, and so on. The user can press the <TAB> key during boot to switch from the boot splash screen (logo) to see the keystroke messages. The Aptio™ TSE BIOS setup menu (see Figs. 2.1.b-d below) is the first screen that you can navigate. Each BIOS setup menu option is described in this user's manual. The Main Setup menu is shown in Figs. 2.1.b through 2.1.d below.

Fig. 2.1.b Main Menu (Screen 1 of 3)

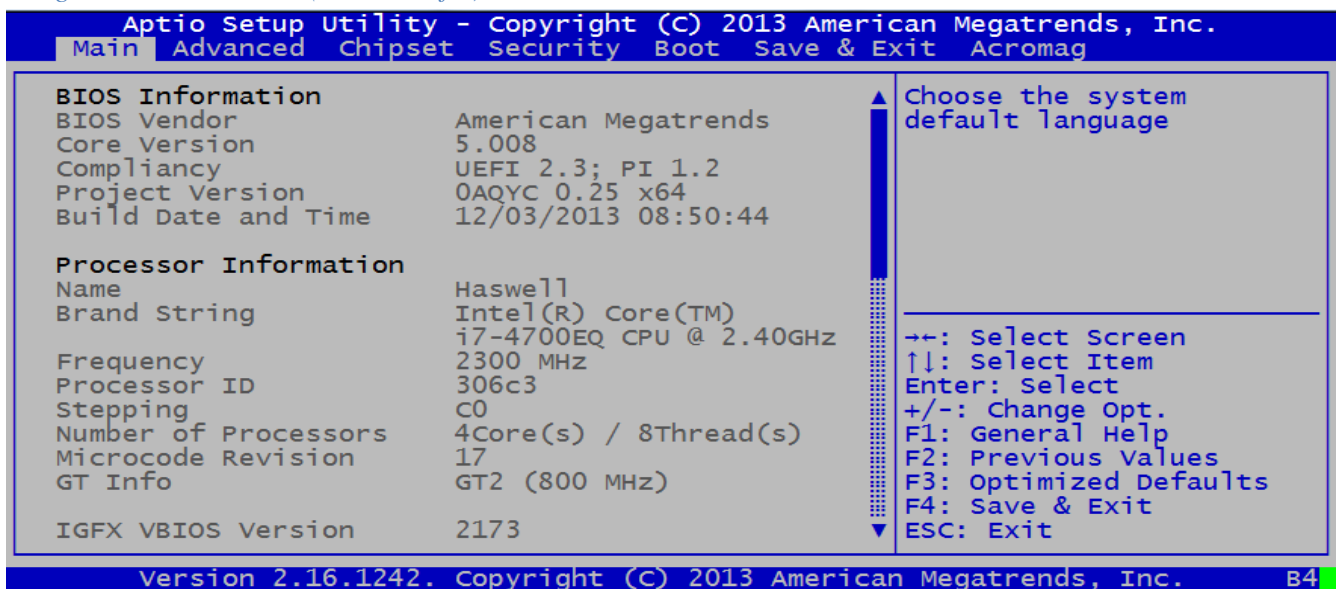


Fig. 2.1.c Main Menu (Screen 2 of 3)

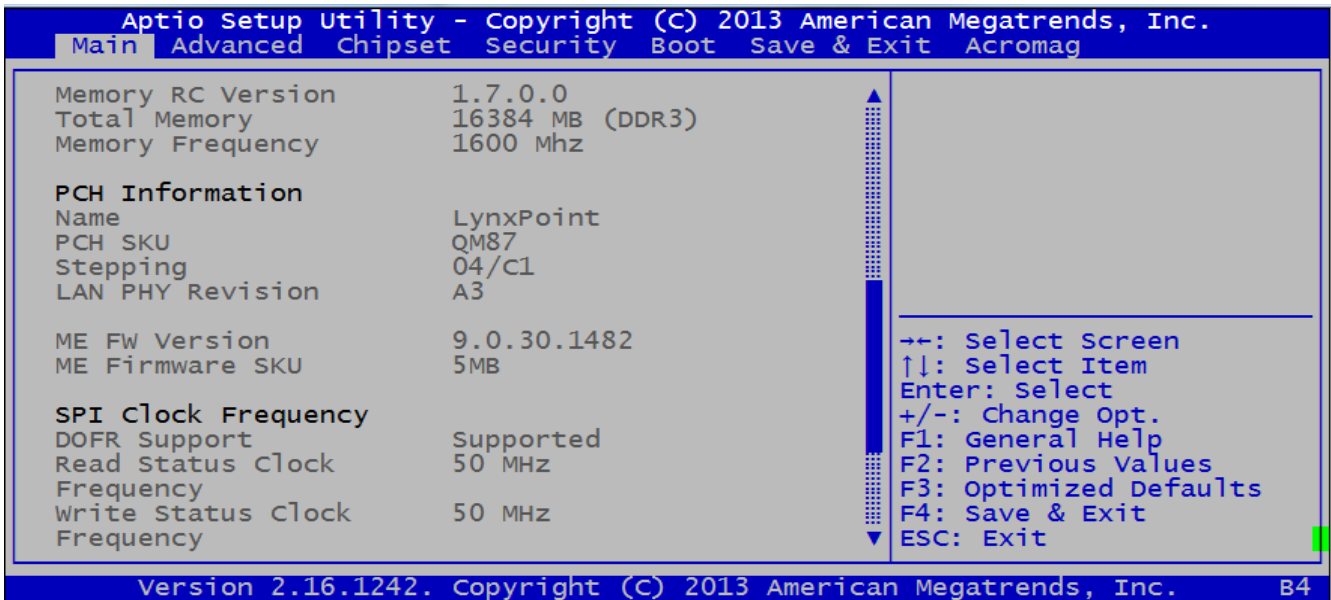
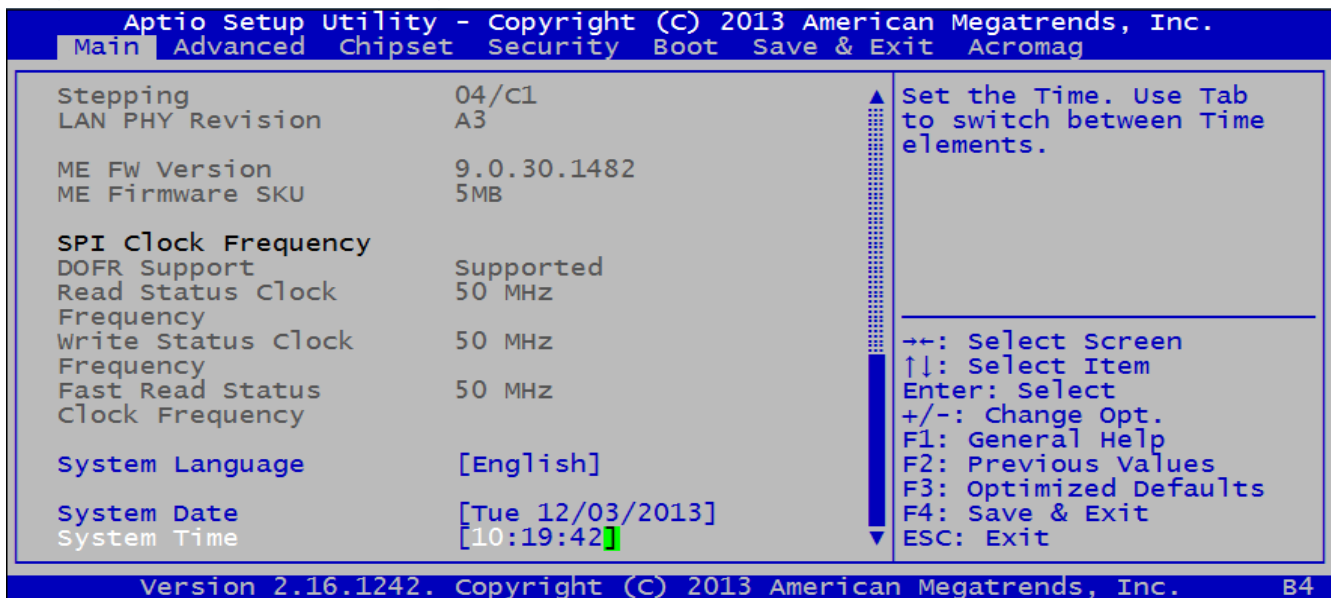


Fig. 2.1.d Main Menu (Screen 3 of 3)



The “System Date” option allows the user to set the date on the system real-time clock RTC. Simply navigate to the month, day, or year and type in the correct numeric value.

The “System Time” option allows the user to set the time on the RTC. Simply navigate to the hour, minute, or second and type in the correct numeric value. Note that the time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

2.1.1 Keyboard-Based Navigation of the TSE BIOS Screens

The Aptio™ TSE keyboard-based navigation can be accomplished using a combination of the keyboard keys (<FUNCTION> keys, <ENTER>, <ESC>, <ARROW> keys, etc.). See figure 2.1.1.a below.

Fig. 2.1.1.a Keyboard-Based Navigation

Keystroke	Description
<Enter>	The <i>Enter</i> key allows the user to select an option to edit its value or access a sub menu.
<Left Arrow Key> and <Right Arrow Key>	The <i>Left and Right</i> <Arrow> keys allow you to select an Aptio™ TSE screen. For example: Main screen, Advanced screen, Chipset screen, and so on.
<Up Arrow Key> and <Down Arrow Key>	The <i>Up and Down</i> <Arrow> keys allow you to select an Aptio™ TSE item or sub-screen.
“+” and “-“ (plus and minus keys)	The <i>Plus and Minus</i> keys allow you to change the field value of a particular setup item. For example: Date and Time.
<Tab>	The <Tab> key allows you to select Aptio™ TSE fields.
<F1>	This key displays the general help window for the user.
<F2>	This key enables users to load pervious values in TSE.
<F3>	This key enables users to load optimized default values in TSE.
<F4>	This key enables users to save the current configuration and exit TSE.
<ESC>	The <Esc> key allows you to discard any changes you have made and exit the Aptio™ TSE. Press the <Esc> key to exit the Aptio™ TSE without saving your changes. The following screen will appear: Press the <Enter> key to discard changes and exit. You can also use the <Arrow> key to select <i>Cancel</i> and then press the <Enter> key to abort this function and return to the previous screen.
Function Keys	When other function keys are available, they are displayed in the help screen along with their intended function.

2.2 Advanced Menu

Select the *Advanced* menu item from the Aptio™ TSE screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen.

Fig. 2.2.a Advanced Menu (Screen 1 of 2)

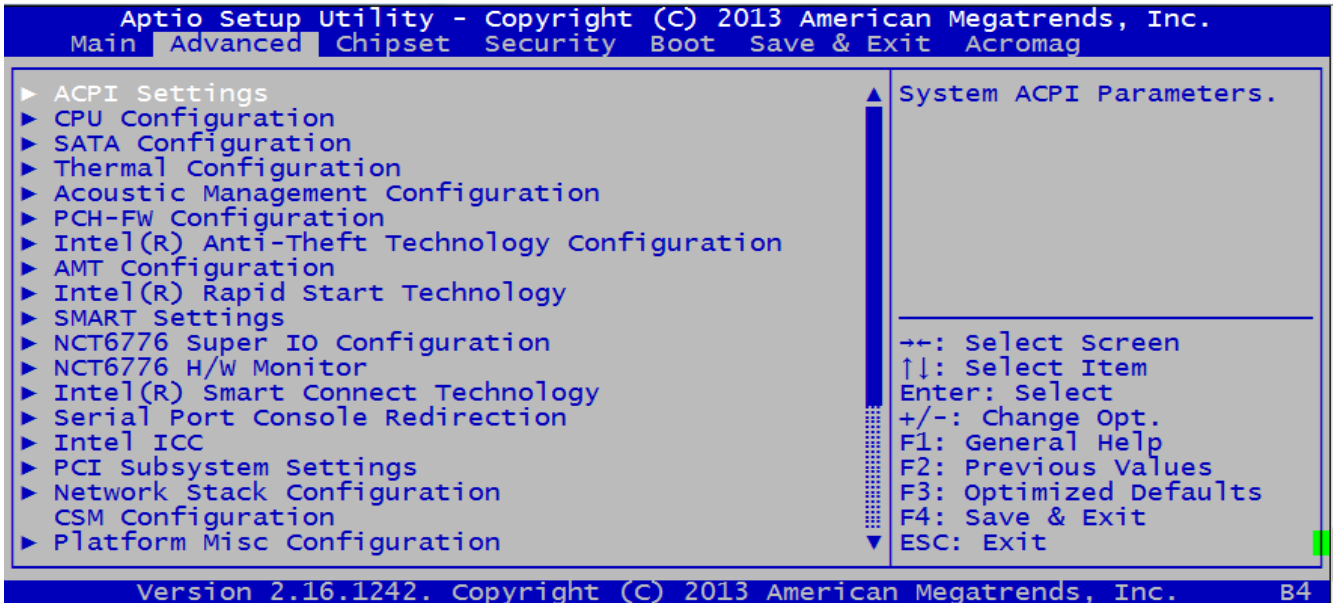
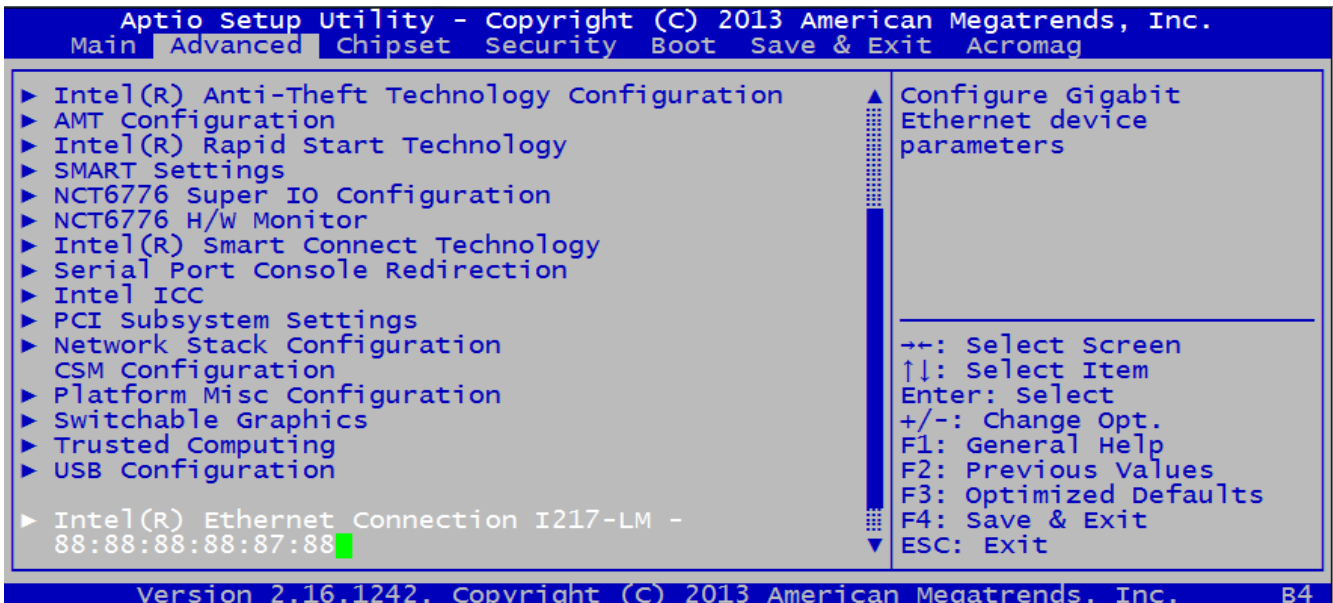
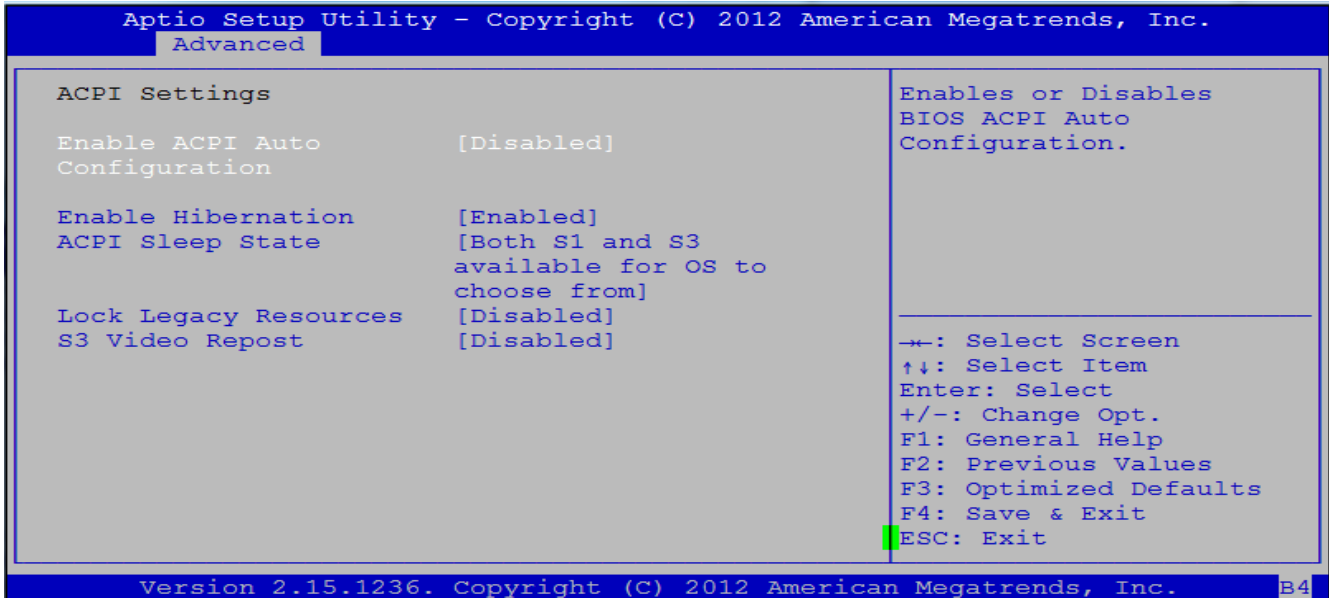


Fig. 2.2.b Advanced Menu (Screen 2 of 2)



2.2.1 ACPI Settings

Fig. 2.2.1.a ACPI Settings



This option allows the user to view and configure the system Advanced Configuration and Power Interface (ACPI) parameters.

Feature	Options	Description
Enable ACPI Auto Configuration	<i>Enabled</i> <i>Disabled</i>	Enables or Disables BIOS ACPI Auto Configuration.
Enable Hibernation	<i>Enabled</i> <i>Disabled</i>	Enables or disables system ability to Hibernate (OS/S4 Sleep State).
ACPI Sleep State	<i>Suspend Disabled</i> <i>S1 (CPU Stop Clock)</i> <i>S3 (Suspend to RAM)</i> <i>Both S1 and S3 available for OS to choose from</i>	Select the highest ACPI sleep state the system will enter when the SUSPEND button is Selected.
Lock Legacy Resource	<i>Enabled</i> <i>Disabled</i>	Enables or Disables Lock of Legacy Resources.
blah		
S3 Video Repost	<i>Enabled</i> <i>Disabled</i>	Enables or Disables S3 Video Repost.

2.2.2 CPU Configuration

Fig. 2.2.2.a CPU Configuration (Screen 1 of 5)

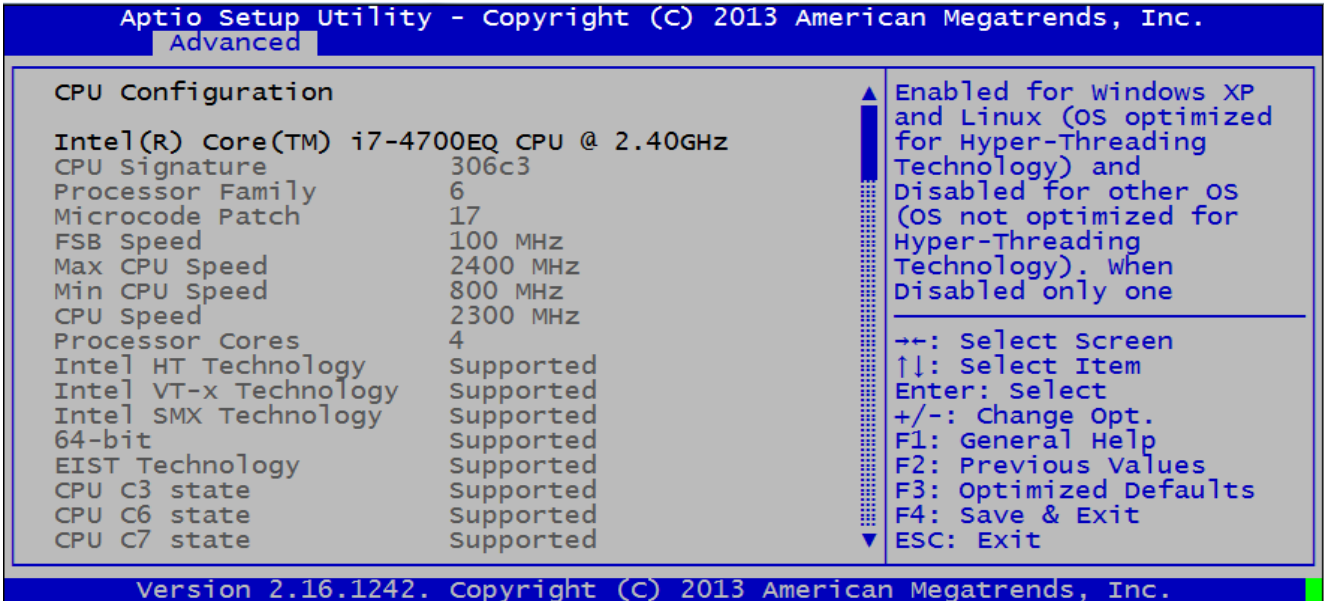


Fig. 2.2.2.b CPU Configuration (Screen 2 of 5)

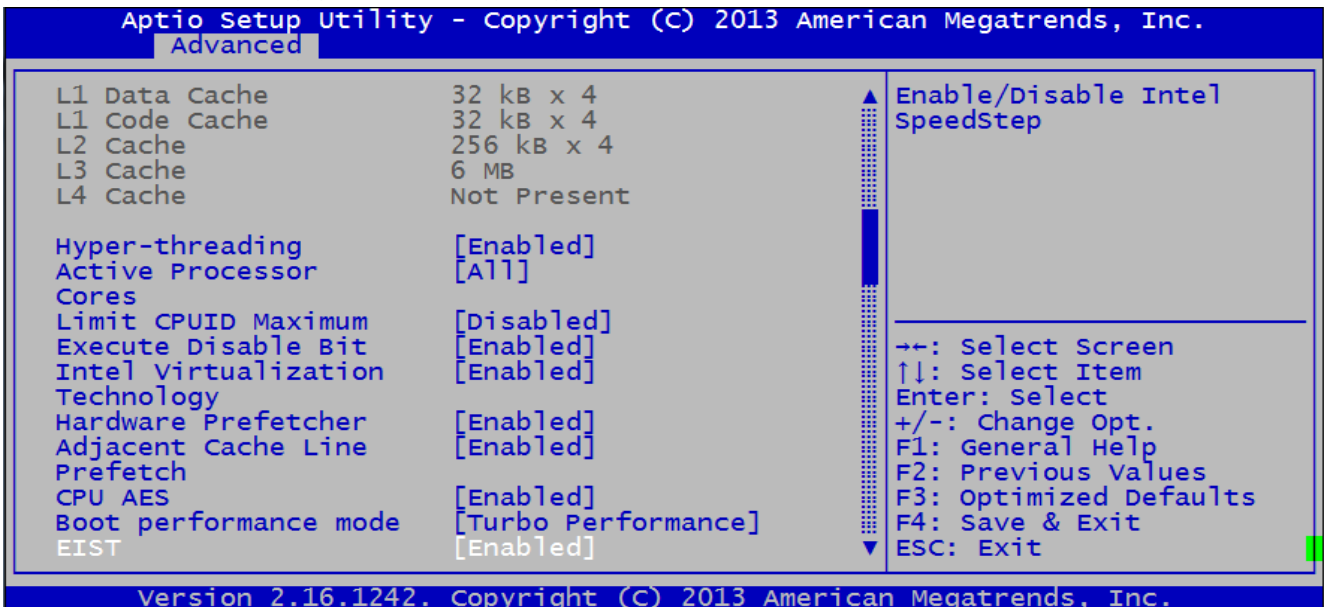


Fig. 2.2.2.c CPU Configuration (Screen 3 of 5)

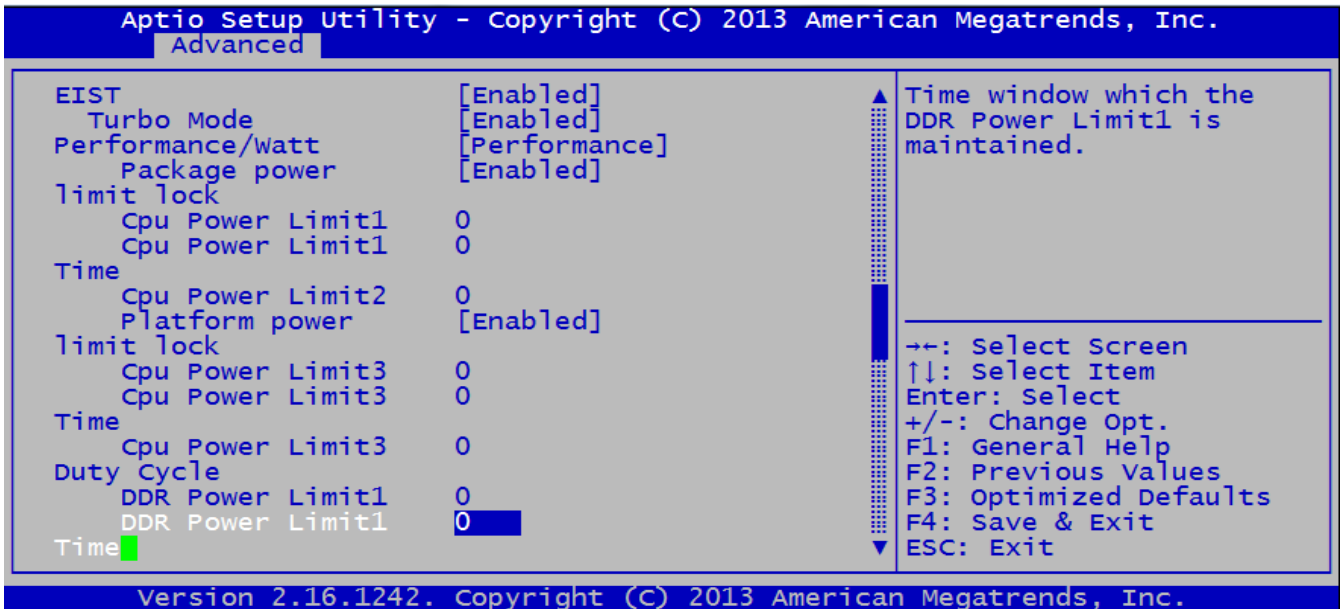


Fig. 2.2.2.d CPU Configuration (Screen 4 of 5)

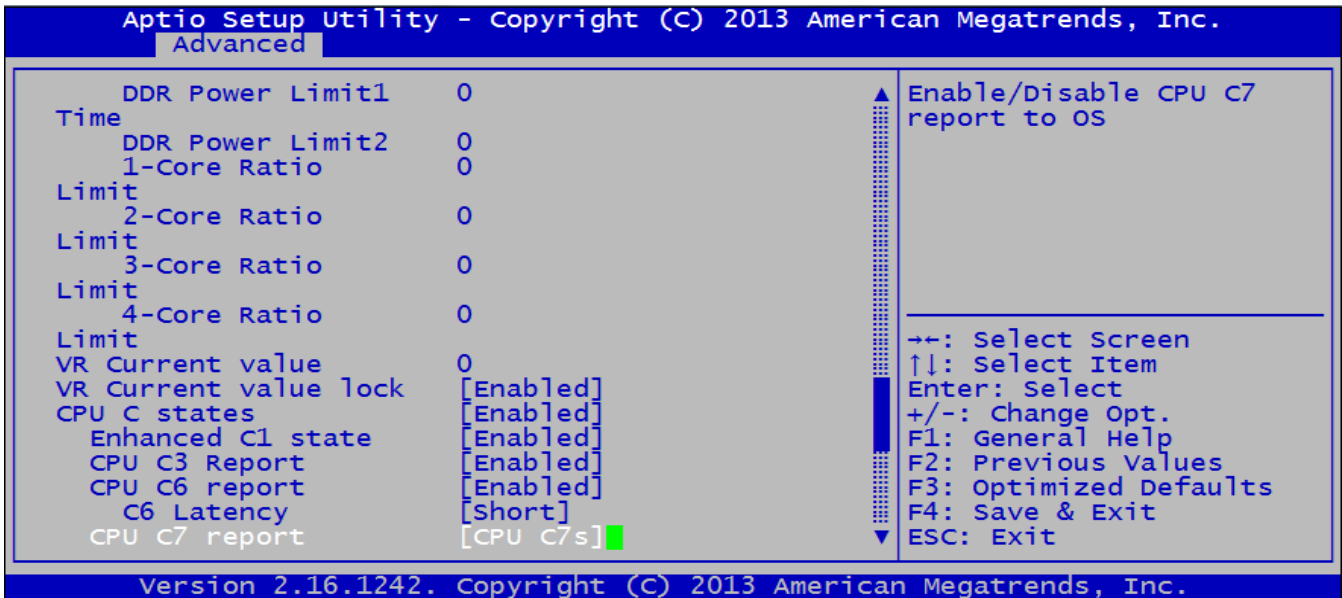
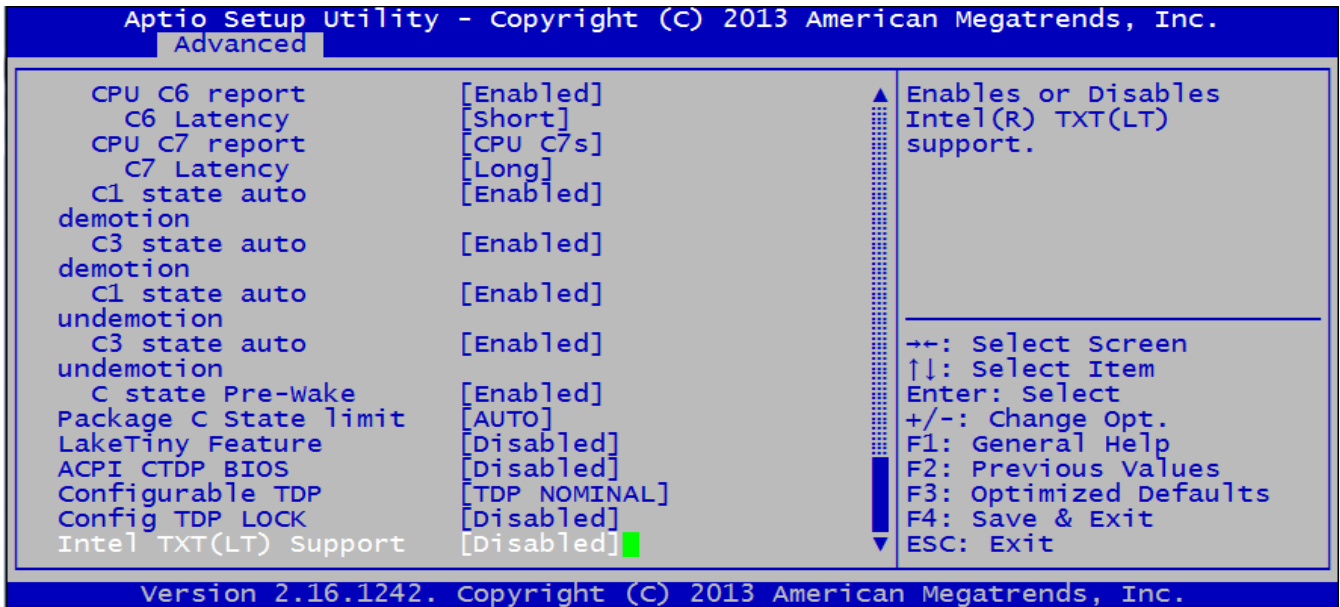


Fig. 2.2.2.e CPU Configuration (Screen 5 of 5)



This option allows the user to view and configure the settings of the CPU installed on the computer system.

Feature	Options	Description
		The initial information is for view only purpose, this includes Processor Type, CPU Speed, L1, L2, and L3 Cache RAM
Hyper-threading	<i>Enabled</i> <i>Disabled</i>	Enabled for Linux, most Windows versions (OS Optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When disabled only one thread per enabled core is enabled. Note: This setting should be disabled in Windows 2000.
Active Processor Cores	<i>All</i> <i>1</i> <i>2</i> <i>3</i> <i>4</i>	Number of cores to enable in each processor package.
Limit CUID Maximum	<i>Disabled</i> <i>Enabled</i>	When CUID instruction is executed, the CPU may return a value greater than 3 which causes certain problem with specific operating systems. Enabling "CUID Maximum Value Limit" in the CPU configuration of BIOS setup menu will limit the returned value to 3 and less to get rid of the problem. The problem is not seen with newer Windows series operating systems such as XP and higher so the default is set to <i>Disabled</i> .
Execute Disable Bit	<i>Enabled</i> <i>Disabled</i>	Execute Disable Bit (XD) is an Intel hardware-based security feature that can help reduce system exposure to viruses and malicious code. XD allows the processor to

		classify areas in memory where application code can or cannot execute. When a malicious worm attempts to insert code in the buffer, the processor disables code execution, preventing damage and worm propagation. To use Execute Disable Bit you must have a supporting OS.
Intel Virtualization Technology	<i>Enabled</i> <i>Disabled</i>	Formerly known as Vanderpool, this technology enables a CPU to act as if it is several different computers, in order to enable several operating systems to run at the same time on the same machine.
Hardware Prefetcher	<i>Enabled</i> <i>Disabled</i>	This option operates transparently, without programmer intervention, to fetch streams of data and instruction from memory into the unified second-level cache. The prefetcher is capable of handling multiple streams in either the forward or backward direction. It is triggered when successive cache misses occur in the last-level cache and a stride in the access pattern is detected, such as in the case of loop iterations that access array elements. The prefetching occurs up to a page boundary.
Adjacent Cache Line Prefetch	<i>Enabled</i> <i>Disabled</i>	The Adjacent Cache-Line Prefetch mechanism, like automatic hardware prefetch, operates without programmer intervention. When enabled through the BIOS, two 64-byte cache lines are fetched into a 128-byte sector, regardless of whether the additional cache line(L2) has been requested or not. In applications with relatively poor spatial locality, the cache miss ratio is higher.
CPU AES	<i>Enabled</i> <i>Disabled</i>	Enables or Disables CPU Advanced Encryption Standards.
Boot performance mode	<i>Max Non-Turbo</i> <i>Max Battery</i> <i>Turbo Performance</i>	Selects the performance state that the BIOS will set before OS handoff.
EIST	<i>Enabled</i> <i>Disabled</i>	Enable or Disable Enhanced Intel SpeedStep Technology. Enhanced Intel SpeedStep Technology allows the system to dynamically adjust processor voltage and core frequency, which can result in decreased average power consumption and decreased average heat production.
Turbo Mode	<i>Enabled</i> <i>Disabled</i>	Also known as Intel Turbo Boost Technology, this option automatically allows the processor cores to run faster than the rated operating frequency if they're operating below power, current, and temperature specification limits. This option is not available unless EIST is enabled.
Performance/Watt	<i>Performance</i> <i>Balanced Performance</i> <i>Balanced Energy</i> <i>Energy Efficient</i>	Depending on the setting, this BIOS option parameterizes the internal "Power Control Unit (PCU)" of the processors and optimizes the power management functions of the processors between performance and

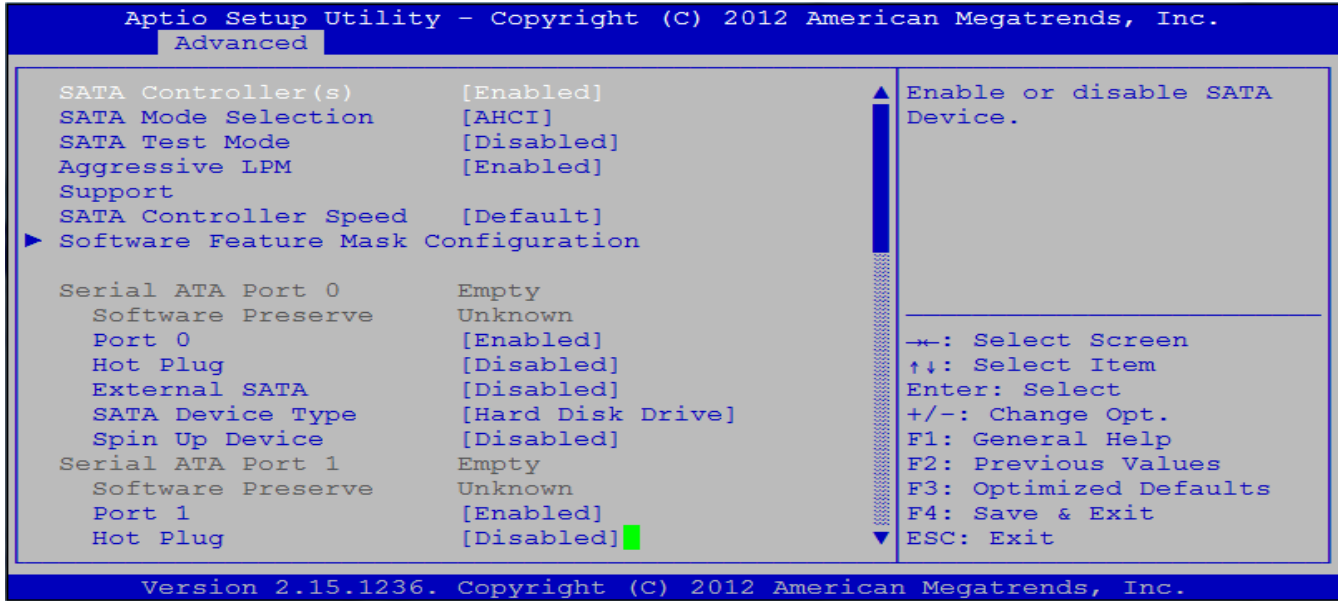
		energy efficiency. The default engages Turbo Boost immediately when possible.
Package power limit lock	<i>Enabled</i> <i>Disabled</i>	When Enabled, Package_Power_Limit MSR will not locked and a reset will be required to unlock the register.
Cpu Power Limit 1		CPU Power Limit1 value. Default is <i>0</i> .
Cpu Power Limit 1 Time		Time window which the Power Limit1 is maintained. Default is <i>0</i> .
Cpu Power Limit 2		CPU Power Limit2 value. Default is <i>0</i> .
Platform power Limit lock	<i>Enabled</i> <i>Disabled</i>	When enabled, PLAT_FORM_POWER_LIMIT MSR will be locked and a reset will be required to unlock the register.
Cpu Power Limit 3		CPU Power Limit3 value. Default is <i>0</i> .
Cpu Power Limit 3 Time		Time window which the Power Limit3 is maintained. Default is <i>0</i> .
Cpu Power Limit 3 Duty Cycle		Specify the duty cycle in percentage that the CPU is required to maintain over the configured Power Limit3 time windows. Default is <i>0</i> .
DDR Power Limit 1		DDR Power Limit1 Value. Default is <i>0</i> .
DDR Power Limit 1 Time		Time window which the DDR Power Limit1 is maintained. Default is <i>0</i> .
DDR Power Limit 2		DDR Power Limit2 Value. Default is <i>0</i> .
1-Core Ratio Limit		This limit is for 1 core active. 0 means using the factory-configured value. Default is <i>0</i> .
2-Core Ratio Limit		This limit is for 2 cores active. 0 means using the factory-configured value. Default is <i>0</i> .
3-Core Ratio Limit		This limit is for 3 cores active. 0 means using the factory-configured value. Default is <i>0</i> .
4-Core Ratio Limit		This limit is for 4 cores active. 0 means using the factory-configured value. Default is <i>0</i> .
VR Current value		Voltage Regulator Current Limit. 0 means AUTO. Default is <i>0</i> .
VR Current value lock	<i>Enabled</i> <i>Disabled</i>	Locks VR Current Value from further writes until reset.
CPU C states	<i>Enabled</i> <i>Disabled</i>	Enable or disable CPU C states.
Enhanced C1 state	<i>Enabled</i> <i>Disabled</i>	Enhanced C1 state.
CPU C3 Report	<i>Enabled</i> <i>Disabled</i>	Enable/Disable CPU C3 Report to OS.
CPU C6 Report	<i>Enabled</i> <i>Disabled</i>	Enable/Disable CPU C6 Report to OS.
C6 Latency	<i>Short</i> <i>Long</i>	Configure Short/Long latency for C6.
CPU C7 Report	<i>Disabled</i>	Enable/Disable CPU C7 Report to OS.

	<i>CPU C7</i> <i>CPU C7s</i>	
C7 Latency	<i>Short</i> <i>Long</i>	Configure Short/Long latency for C7.
C1 state auto demotion	<i>Enabled</i> <i>Disabled</i>	Processor will conditionally demote C3/C6/C7 requests to C1 based on uncore autodemote information. Default is <i>Enabled</i> .
C3 state auto demotion	<i>Enabled</i> <i>Disabled</i>	Processor will conditionally demote C6/C7 requests to C3 based on uncore autodemote information. Default is <i>Enabled</i> .
C1 state auto undemotion	<i>Enabled</i> <i>Disabled</i>	Un-demotion from Demoted C1.
C3 state auto undemotion	<i>Enabled</i> <i>Disabled</i>	Un-demotion from Demoted C3.
C state Pre-Wake	<i>Enabled</i> <i>Disabled</i>	Enable or Disable C State Pre-Wake feature.
Package C State Limit	<i>C0</i> <i>C2</i> <i>C3</i> <i>C6</i> <i>C7</i> <i>C7s</i> <i>AUTO</i>	Select Auto for the AMI BIOS to automatically set the limit on the C-State package register..
LakeTiny Feature	<i>Disabled</i> <i>Enabled</i>	Select Enabled for LakeTiny feature support for C-State configuration. Default is <i>Disabled</i> .
ACPI CTDP BIOS	<i>Disabled</i> <i>Enabled</i>	Enable/Disable Advanced Configuration and Power Interface (ACPI) Configurable Thermal Design Power (cTDP) support. Default is <i>Disabled</i> .
Configurable TDP	<i>TDP NOMINAL</i> <i>TDP DOWN</i> <i>TDP UP</i> <i>Disabled</i>	Allows re-configuration of the Configurable Thermal Design Power (TDP) levels based on current power and thermal delivery capabilities of the system. When the processor runs at its rated frequency and TDP. When a cooler or quieter mode of operation is desired, this mode specifies a lower TDP and lower guaranteed frequency versus the nominal mode. TDP UP is not currently supported. This option disabled TDP.
Config TDP Lock	<i>Disabled</i> <i>Enabled</i>	This feature allows the lock the Configurable Thermal Design Power Control Register.
Intel TXT(LT) Support	<i>Disabled</i> <i>Enabled</i>	Enables or Disables Intel's Trusted Execution Technology (TXT). This technology was formerly known as LaGrande Technology (LT). This feature provides dynamic root of trust for measurement (DRTM), data protection in case of improper shutdown, and measurement and verification of launched environment.
ACPI T State	<i>Disabled</i> <i>Enabled</i>	ACPI T States are a way of clock-gating the computer's cores as a way of cooling the machine when all other methods fail. Intel asserts that T States are no longer

		relevant, and offers a more detailed explanation of T States on their website.
CPU DTS	<i>Disabled</i> <i>Enabled</i>	When Disabled, ACPI thermal management uses EC reported temperature values. When Enabled, ACPI Thermal management uses Digital Thermal Sensors (DTS) to obtain CPU Temperature values.
Debug Interface	<i>Disabled</i> <i>Enabled</i>	Enable or Disable CPU debug feature.
Debug Interface Lock	<i>Enabled</i> <i>Disabled</i>	Lock CPU Debug feature setting.

2.2.3 SATA Configuration

Fig. 2.2.3.a SATA Configuration



The general SATA options allow the user to view and configure the SATA settings of the system.

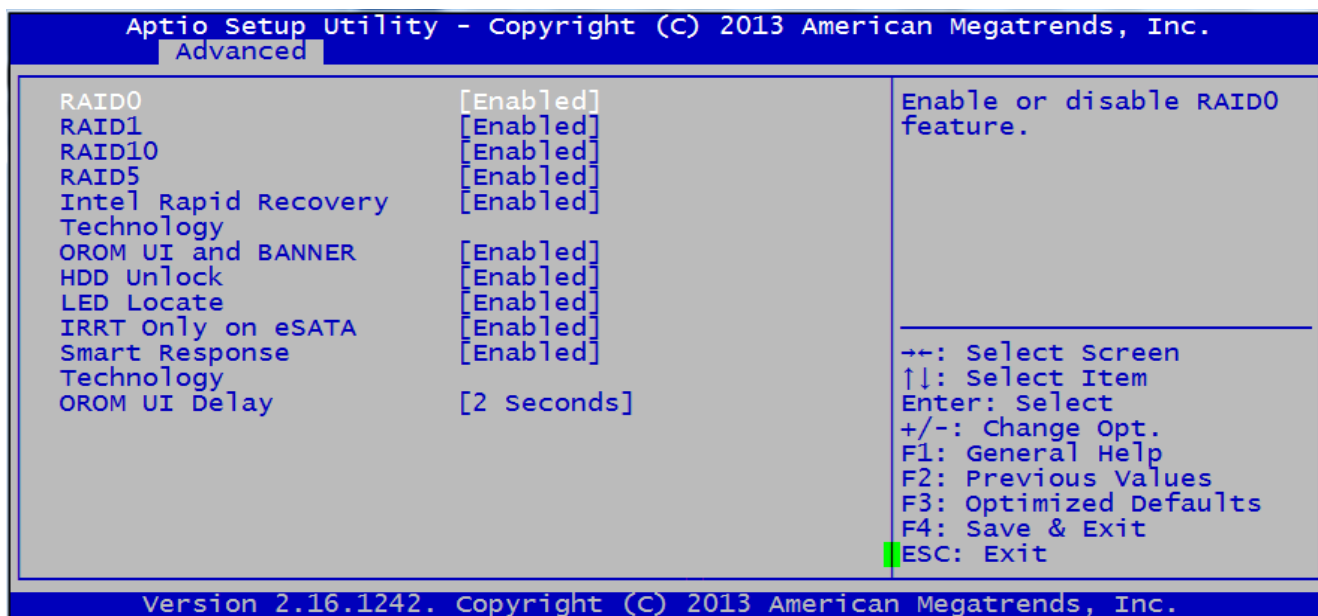
Feature	Options	Description
SATA Controllers(s)	<i>Enabled</i> <i>Disabled</i>	Enable or Disable the onboard SATA controller.
SATA Mode Selection	<i>IDE</i> <i>AHCI</i> <i>RAID</i>	Determines how SATA controller(s) operate. Please note that modifying this option after installation may require you to reinstall Windows.
SATA Test Mode	<i>Enabled</i> <i>Disabled</i>	Enable or Disable Test Mode.
Aggressive LPM Support	<i>Enabled</i> <i>Disabled</i>	Enable PCH to aggressively enter link power state. <i>Aggressive Link Power Management (ALPM)</i> is a power-saving technique that helps the disk save power by setting a SATA link to the disk to a low-power setting during idle time (that is when there is no I/O). ALPM automatically sets the SATA link back to an active power state once I/O requests are queued to that link. Power savings introduced by ALPM come at the expense of disk latency. As such, you should only use ALPM if you expect the system to experience long periods of idle I/O time.
SATA Controller Speed	<i>Default</i> <i>Gen1</i> <i>Gen2</i> <i>Gen3</i>	Indicates the maximum speed the SATA controller can support. Please select based on your SATA device.

The SATA port setting options allow the user to view and configure individual SATA devices on each of the SATA ports from 0 to 5.

Feature	Options	Description
Serial ATA Port X		This option is view only and identifies the SATA drive and size of the SATA device connected to this port. i.e. <i>MKNSSDAT120GB (120.0GB)</i>
Software Preserve		This is a view only option that specified whether the SATA device supports Software Preserve.
Port X	<i>Enabled</i> <i>Disabled</i>	Enable or Disable SATA Port. Please consult your specific board's user manual for what SATA Ports are available.
Hot Plug	<i>Enabled</i> <i>Disabled</i>	Designates whether this port is hot pluggable.
Mechanical Presence Switch	<i>Enabled</i> <i>Disabled</i>	Controls reporting if this port has an optional Mechanical Presence switch. This option is currently not supported.
External SATA	<i>Enabled</i> <i>Disabled</i>	Identifies if the drive needs External SATA (eSATA) Support.
SATA Device Type	<i>Hard Disk Drive</i> <i>Solid State Drive</i>	Identify if the SATA port is connected to a Solid State Drive (SSD) or a mechanical Hard Disk Drive.
Spin Up Device	<i>Enabled</i> <i>Disabled</i>	When enabled, on an edge detect from 0 to 1, the PCH starts a COMRESET initialization sequence to the device.

2.2.3.1 SATA Software Feature Mask Configuration

Fig. 2.2.3.1.a SATA Software Feature Mask Configuration



This option allows the user to view and configure the SATA Software Feature Mask Configuration options.

Feature	Options	Description
RAID0	<i>Enabled</i> <i>Disabled</i>	Enable or disable RAID0 feature.
RAID1	<i>Enabled</i> <i>Disabled</i>	Enable or disable RAID1 feature.
RAID10	<i>Enabled</i> <i>Disabled</i>	Enable or disable RAID10 feature.
RAID5	<i>Enabled</i> <i>Disabled</i>	Enable or disable RAID5 feature.
Intel Rapid Recovery Technology	<i>Enabled</i> <i>Disabled</i>	Enable or disable Intel Rapid Recovery Technology.
OROM UI and BANNER	<i>Enabled</i> <i>Disabled</i>	If enabled, then the Option ROM (OROM) User Interface (UI) is shown. Otherwise, no OROM banner or information will be displayed if all disks and RAID volumes are Normal.
HDD Unlock	<i>Enabled</i> <i>Disabled</i>	If enabled, indicates that the Hard Disk Drive (HDD) password unlock in the OS is enabled.
LED Locate	<i>Enabled</i> <i>Disabled</i>	If enabled, it indicates that the LED/SGPIO hardware is attached and the <i>ping to locate</i> feature is enabled on the OS.
IRRT only on eSATA	<i>Enabled</i> <i>Disabled</i>	If enabled, then only IRRT volumes can span internal and eSATA drives. If disabled, then any RAID volume can span internal and eSATA drives.
Smart Response Technology	<i>Enabled</i> <i>Disabled</i>	Enable or Disable Smart Response Technology.

OROM UI Delay	<i>2 Seconds</i> <i>4 Seconds</i> <i>6 Seconds</i> <i>8 Seconds</i>	If enabled, indicates the delay of the Option ROM (OROM) User Interface (UI) Splash Screen in a normal status. .

2.2.4 Thermal Configuration

Fig. 2.2.4.a Thermal Configuration

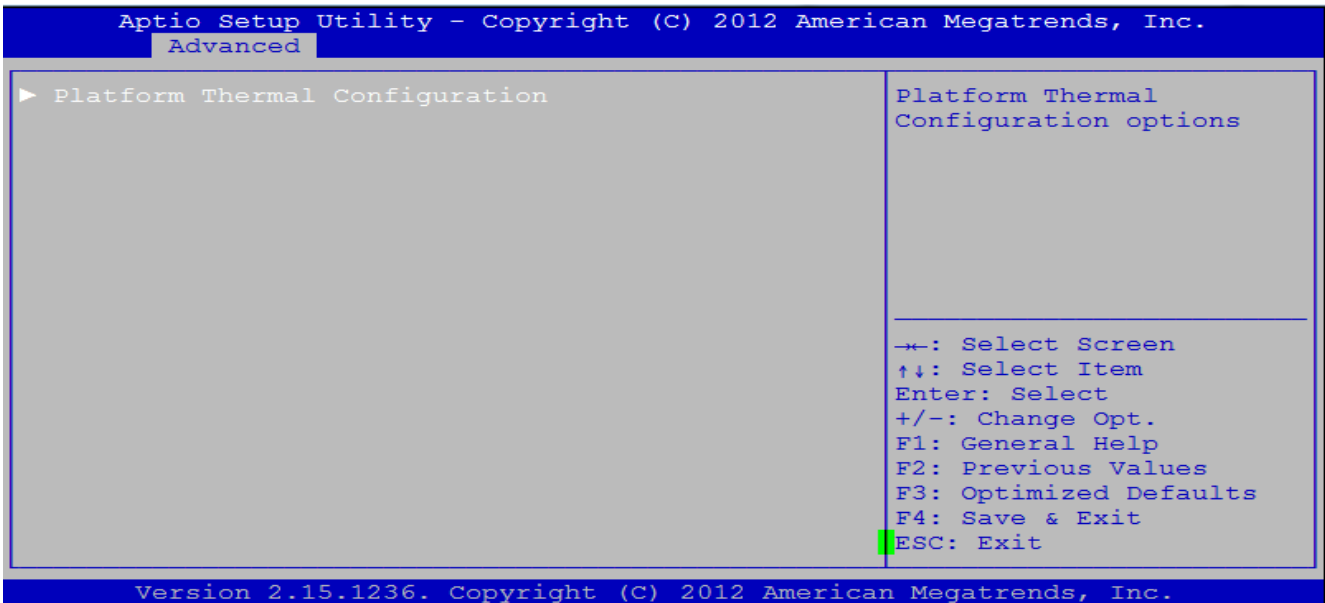
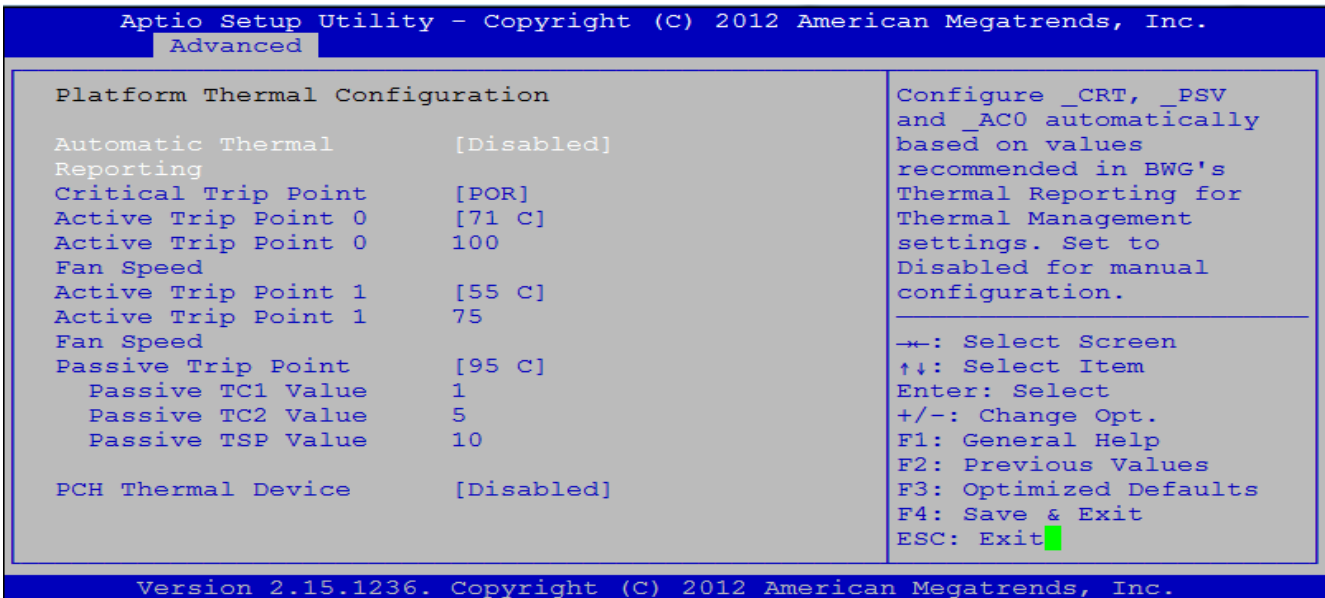


Fig. 2.2.4.b Platform Thermal Configuration

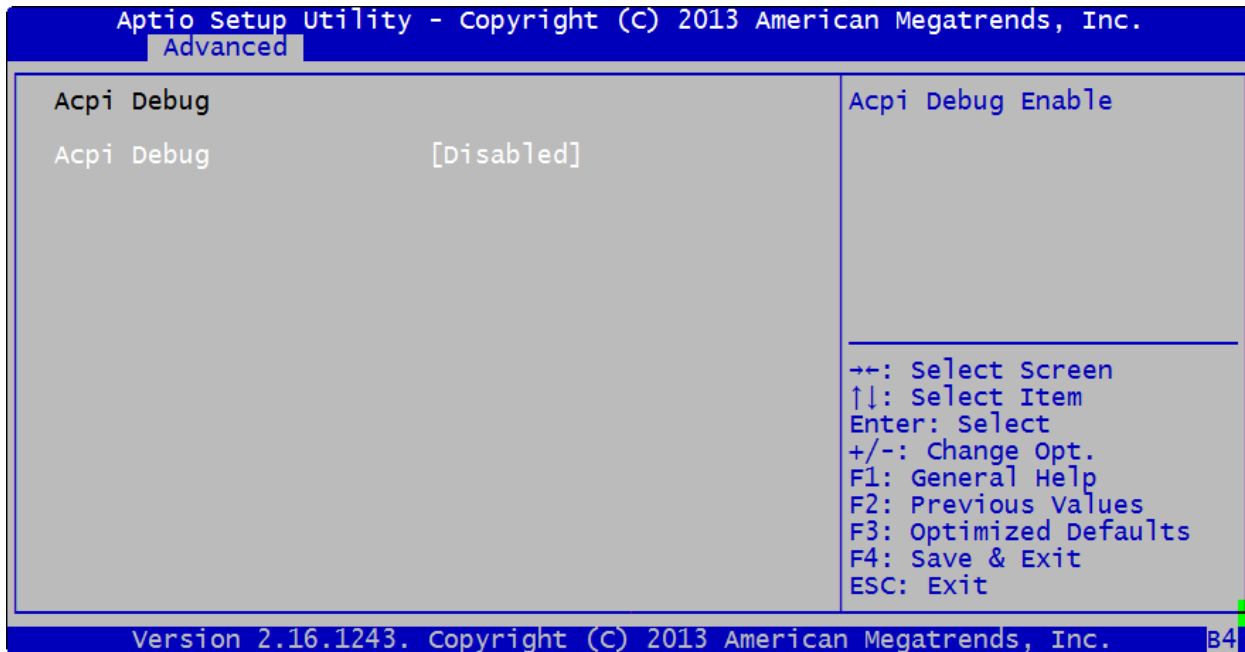


This option allows the user to view and configure the Platform Thermal Configuration options.

Feature	Options	Description
Automatic Thermal Reporting	<i>Enabled</i> <i>Disabled</i>	Configure _CRT, _PSV, and _ACO automatically based on values recommended in BWG's Thermal Reporting for Thermal Management settings. Set to Disabled for manual configuration.
Critical Trip Point	<i>POR</i> <i>15 °C</i> <i>23 °C</i> ... <i>127 °C</i>	This value controls the temperature of the ACPI Critical Trip Point – the point in which the OS will shut the system off. The temperature range is from 15 °C to 127 °C. Please note that this feature is only available when Automatic Thermal Reporting is Disabled. NOTE: 100 °C is the Plan of Record (POR) for all Intel mobile processors. Default value is <i>POR</i> .
Active Trip Point 0	<i>Disabled</i> <i>15 °C</i> <i>23 °C</i> ... <i>71 °C</i> <i>119 °C</i>	This value controls the temperature of the ACPI Active Trip Point 0 – the point in which the OS will turn the processor fan on Active Trip Point 0 Fan Speed. Please note that this feature is only available when Automatic Thermal Reporting is Disabled.
Active Trip Point 0 Fan Speed	<i>0%</i> ... <i>100%</i>	Active Trip Point 0 Fan speed in percentage. Value must be between 0 (Fan off) – 100 (Max fan speed). This is the speed at which fan will run when Active Trip Point 0 is crossed.
Active Trip Point 1	<i>Disabled</i> <i>15 °C</i> <i>23 °C</i> ... <i>55 °C</i> <i>119 °C</i>	This value controls the temperature of the ACPI Active Trip Point 1 – the point in which the OS will turn the processor fan on Active Trip Point 1 Fan Speed.
Active Trip Point 1 Fan Speed	<i>0%</i> ... <i>75%</i> <i>100%</i>	Active Trip Point 1 Fan speed in percentage. Value must be between 0 (Fan off) – 100 (Max fan speed). This value must be less than Active Trip Point 0 Fan Speed. This is the speed at which fan will run when Active Trip Point 1 is crossed.
Passive Trip Point	<i>Disabled</i> <i>15 °C</i> <i>23 °C</i> ... <i>95 °C</i> <i>119 °C</i>	This value controls the temperature of the ACPI Passive Trip Point – the point in which the OS will begin throttling the processor down. Please note that this feature is only available when Automatic Thermal Reporting is Disabled.
Passive TC1 Value		This value sets the TC1 value for the ACPI Passive Cooling Formula. Range 1 – 16. Default is <i>1</i> .
Passive TC2 Value		This value sets the TC2 value for the ACPI Passive Cooling Formula. Range 1 – 16. Default is <i>5</i> .
Passive TSP Value		This item sets the TSP value for the ACPI Passive Cooling Formula. It represents in tenths of a second how often the OS will read the temperature when passive cooling is enabled. Range 2 – 32. Default is <i>10</i> .
PCH Thermal Device	<i>Enabled</i> <i>Disabled</i>	Enable or Disable the PCH Thermal Device (D31:F6). Default is <i>Disabled</i> .

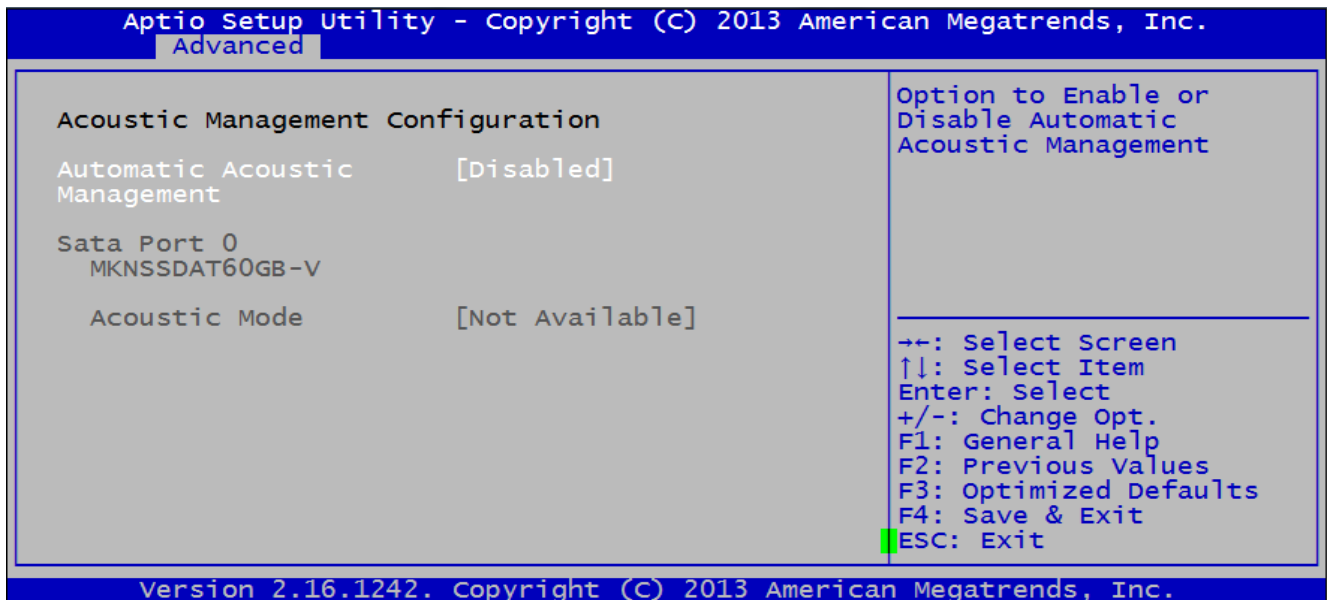
2.2.5 Acpi Debug Configuration

Fig. 2.2.5.a ACPI Debug Configuration



2.2.6 Acoustic Management Technology Configuration

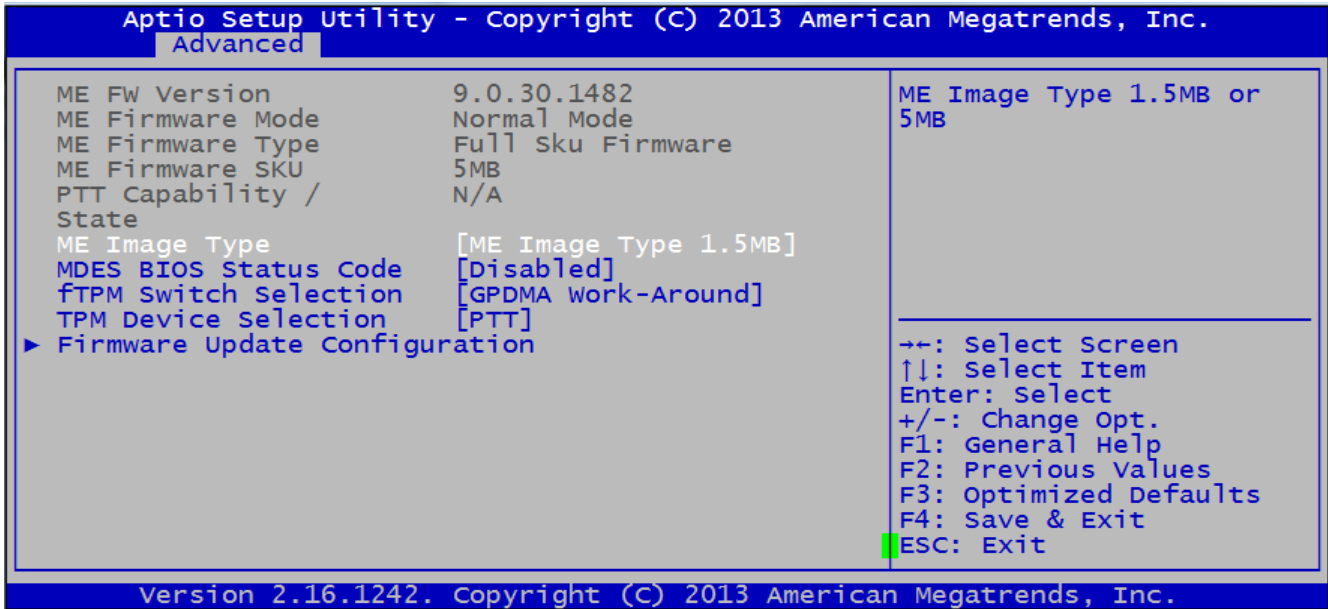
Fig. 2.2.6.a Acoustic Management Technology Configuration



Acoustic management is a form of hard-drive power management that allows for the adjustment of noise, performance, temperature, power requirements, and life expectancy.

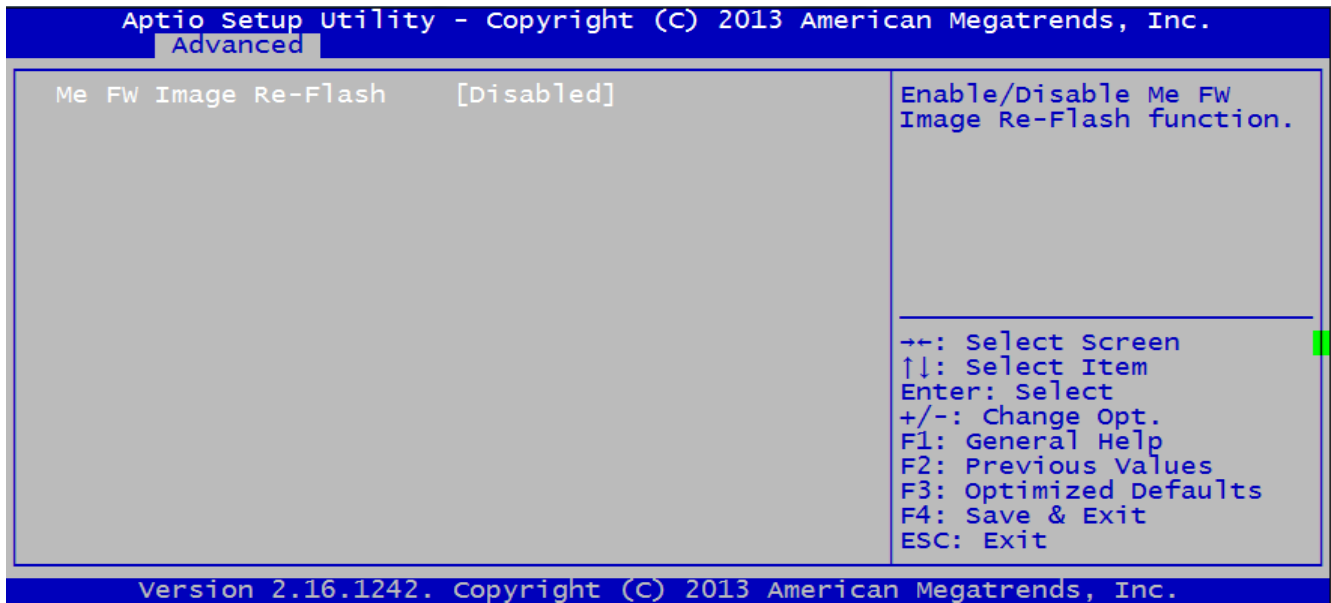
2.2.7 PCH-FW Configuration

Fig. 2.2.7.a PCH-FW Configuration



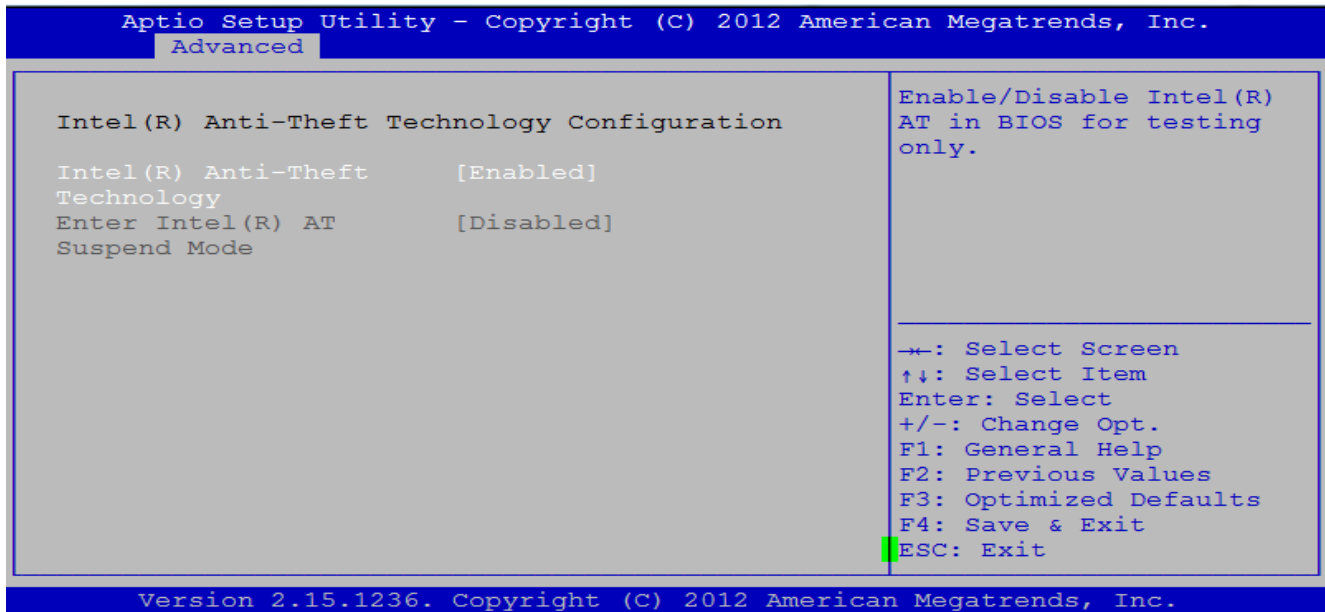
Feature	Options	Description
fTPM Switch Selection		Firmware-based Trusted Platform Module (fTPM). It is a firmware implementation of a TPM chip, which is a microcontroller that stores keys, passwords, and digital certificates for the machine.
TPM Device Selection	PTT dTPM	This option allows the user to select the preferred TPM device: PTT or discrete TPM (dTPM). PTT is the firmware implementation of TPM, and dTPM is the hardware implementation on a chip that is separate from other system elements, which communicates with the system on a dedicated hardware bus.

Fig. 2.2.7.b Firmware Update



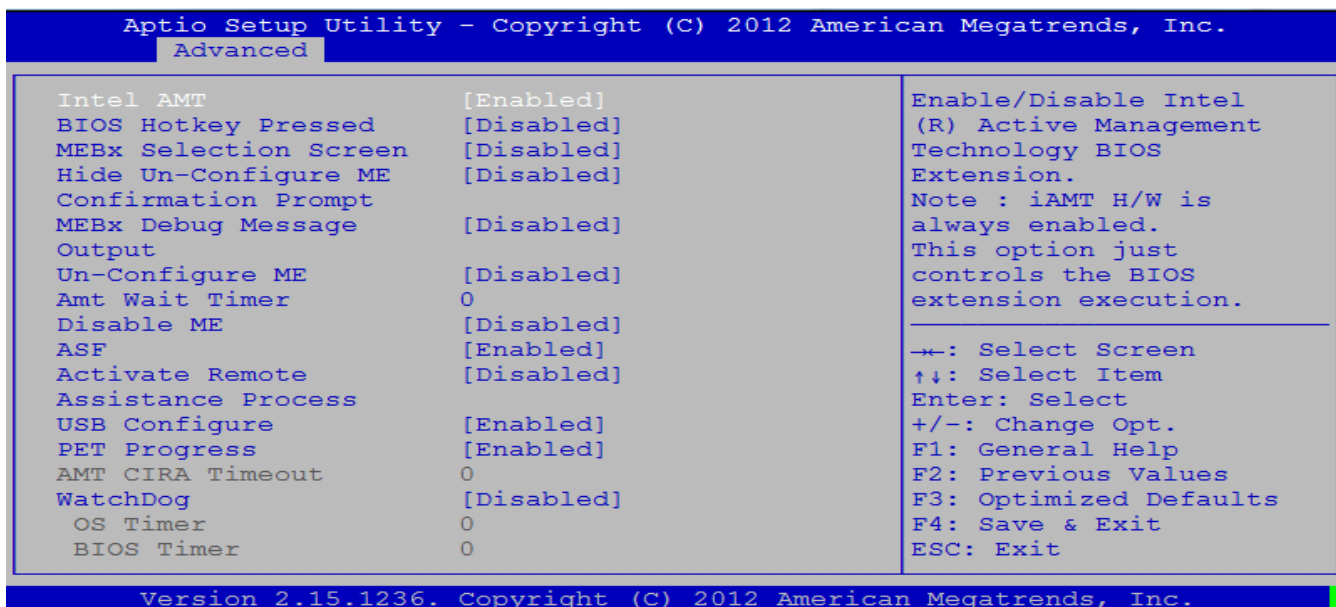
2.2.8 Intel® Anti-Theft Technology Configuration

Fig. 2.2.8.a Intel® Anti-Theft Technology Configuration



2.2.9 AMT Configuration

Fig. 2.2.9.a AMT Configuration



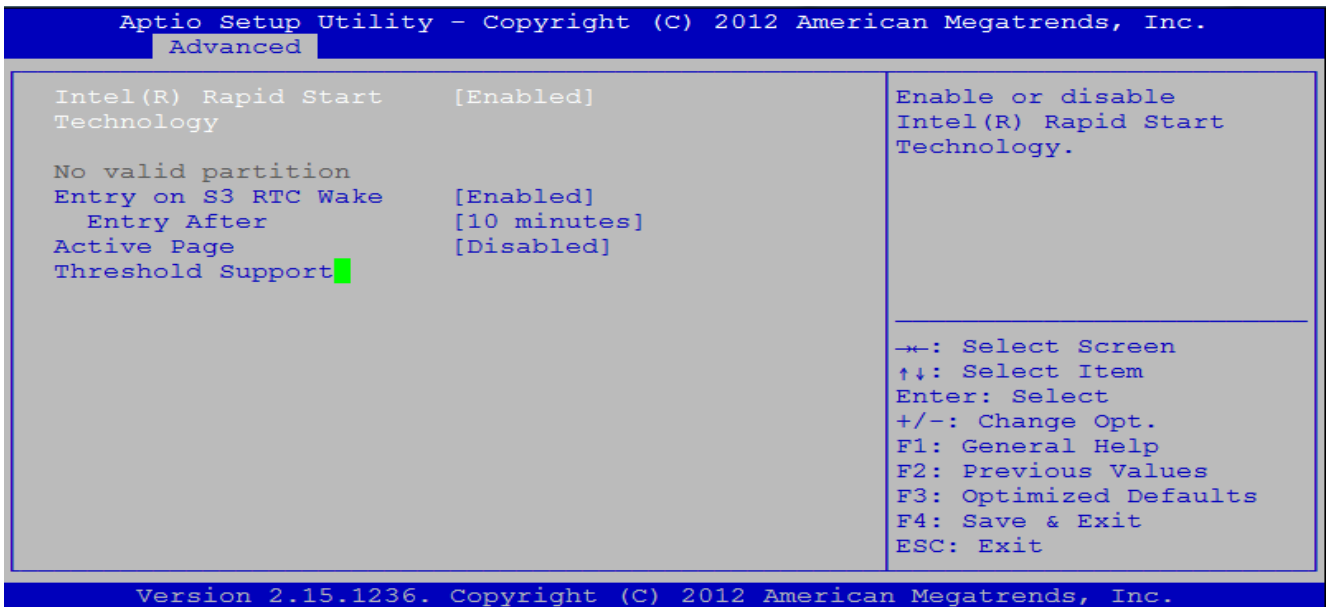
This option allows the user to view and configure the Intel Activate Management Technology (AMT) parameters.

Feature	Options	Description
Intel AMT	<i>Enabled</i> <i>Disabled</i>	Use this item to enable or disable the Intel Active Management Technology (iAMT) BIOS Extension. Note: iAMT Hardware is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.
BIOS Hotkey Pressed	<i>Enabled</i> <i>Disabled</i>	Use this item to enable/disable BIOS hotkey press. (OEMFlag Bit 1)
MEBx Selection Screen	<i>Enabled</i> <i>Disabled</i>	Use this item to enable/disable the Management Engine BIOS Extension (MEBx) selection screen. (OEMFlag Bit 2)
Hide Un-Configure ME Confirmation Prompt	<i>Enabled</i> <i>Disabled</i>	Use this item to enable/disable hide un-configure Management Engine (ME) without password confirmation prompt. (OEMFlag Bit 6)
MEBx Debug Message Output	<i>Enabled</i> <i>Disabled</i>	Use this item to enable/disable the Management Engine Bios Extension (MEBx) debug message output. (OEMFlag Bit 14)
Un-Configure ME	<i>Enabled</i> <i>Disabled</i>	Use this item to enable/disable un-configure Management Engine (ME) without password. (OEMFlag Bit 15)
AMT Wait Timer		Set the Active Management Technology (AMT) timer to wait before sending ASF_GET_BOOT_OPTIONS. Default is <i>0</i> .
Disable ME	<i>Enabled</i> <i>Disabled</i>	Use this item to enable/disable set Management Engine (ME) to Soft Temporary Disabled.
ASF	<i>Enabled</i> <i>Disabled</i>	Use this item to enable/disable Alert Specification Format (ASF).

Activate Remote Assistance Process	<i>Enabled</i> <i>Disabled</i>	Use this item to enable/disable trigger Client Initiated Remote Access (CIRA) boot.
USB Configure	<i>Enabled</i> <i>Disabled</i>	Use this item to enable/disable USB configure function.
PET Progress	<i>Enabled</i> <i>Disabled</i>	When Enabled, the Intel(R) AMT firmware receives all progress Platform Event Trap (PET) events.
AMT CIRA Timeout		This option is only available when Activate Remote Assistance Process is Enabled. This is the amount of time to wait to establish a Client Initiated Remote Access (CIRA) connection. Default is <i>0</i> . 0 – Use the default timeout value of 60 seconds 255 – MEBX waits until the connection succeeds.
WatchDog	<i>Enabled</i> <i>Disabled</i>	Use this item to enable or disable the WatchDog Timer.
OS Timer	<i>0</i>	Sets the Operating System (OS) Watchdog Timer.
BIOS Timer	<i>0</i>	Sets the BIOS Watchdog Timer.

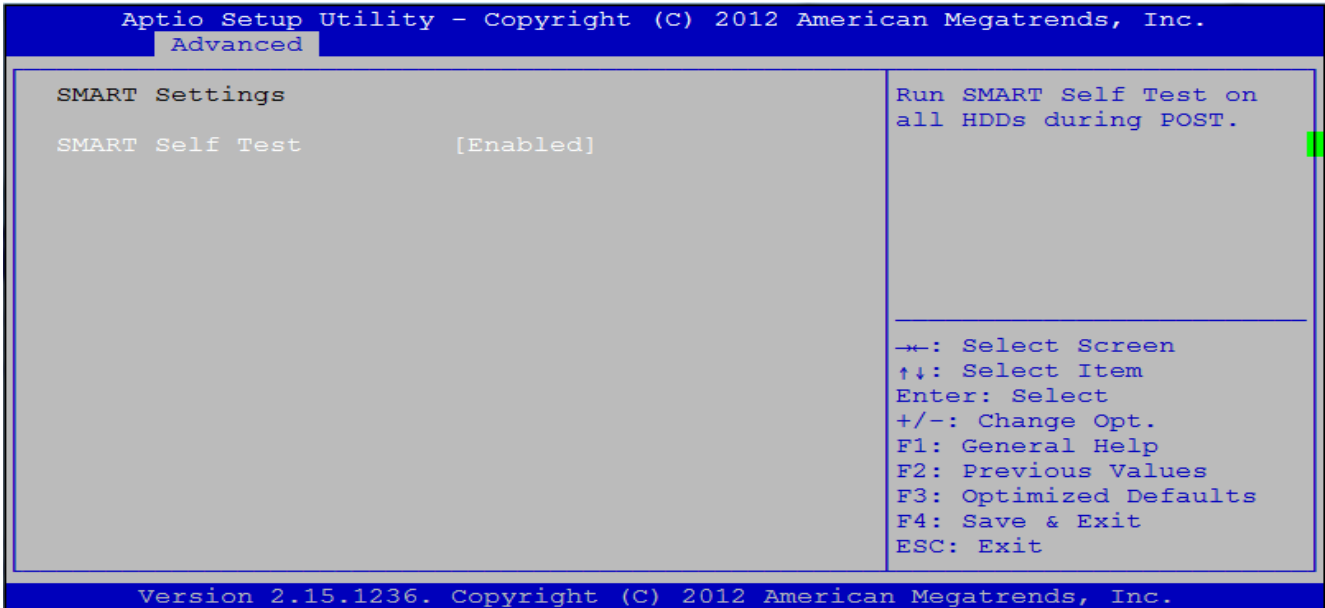
2.2.10 Intel® Rapid Start Technology

Fig. 2.2.10.a Intel® Rapid Start Technology



2.2.11 Smart Settings

Fig. 2.2.11.a Smart Settings



SMART stands for Self-Monitoring, Analysis and Reporting Technology. SMART keeps track of hard-drive stats in an attempt to anticipate hard drive hardware failure. The SMART Self-Test checks up on the recorded data levels, and provides an on-demand overview of the drive’s health.

2.2.12 NCT6776 Super IO Configuration

Fig. 2.2.12.a NCT6776 Super IO Configuration

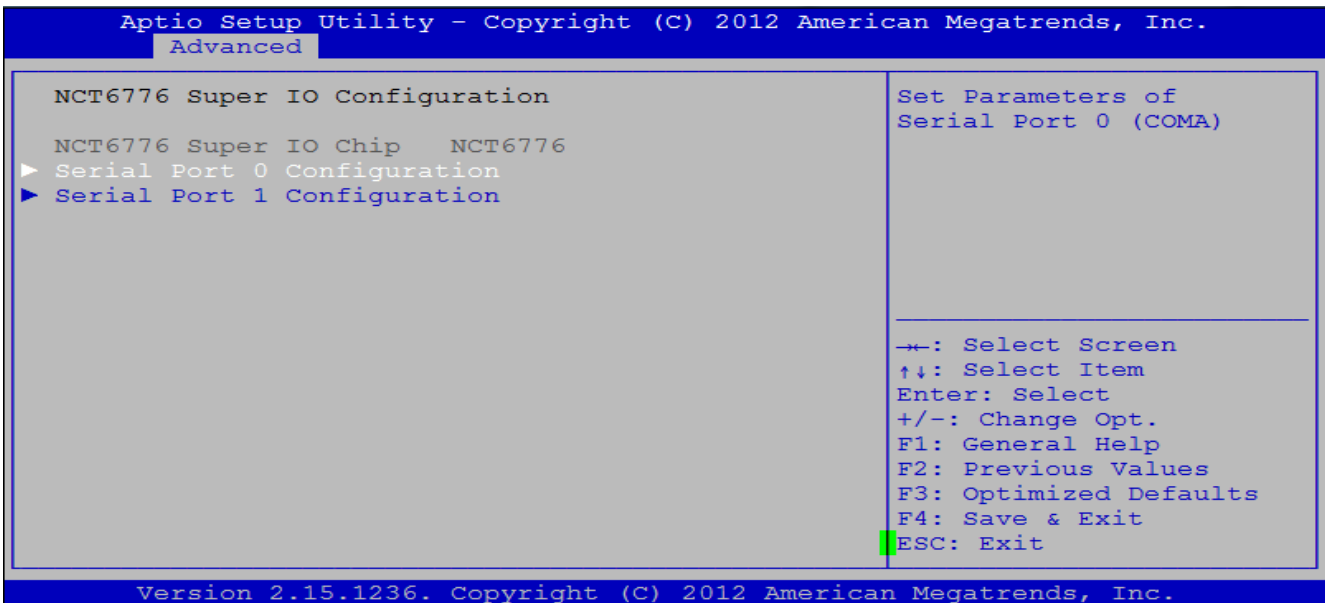
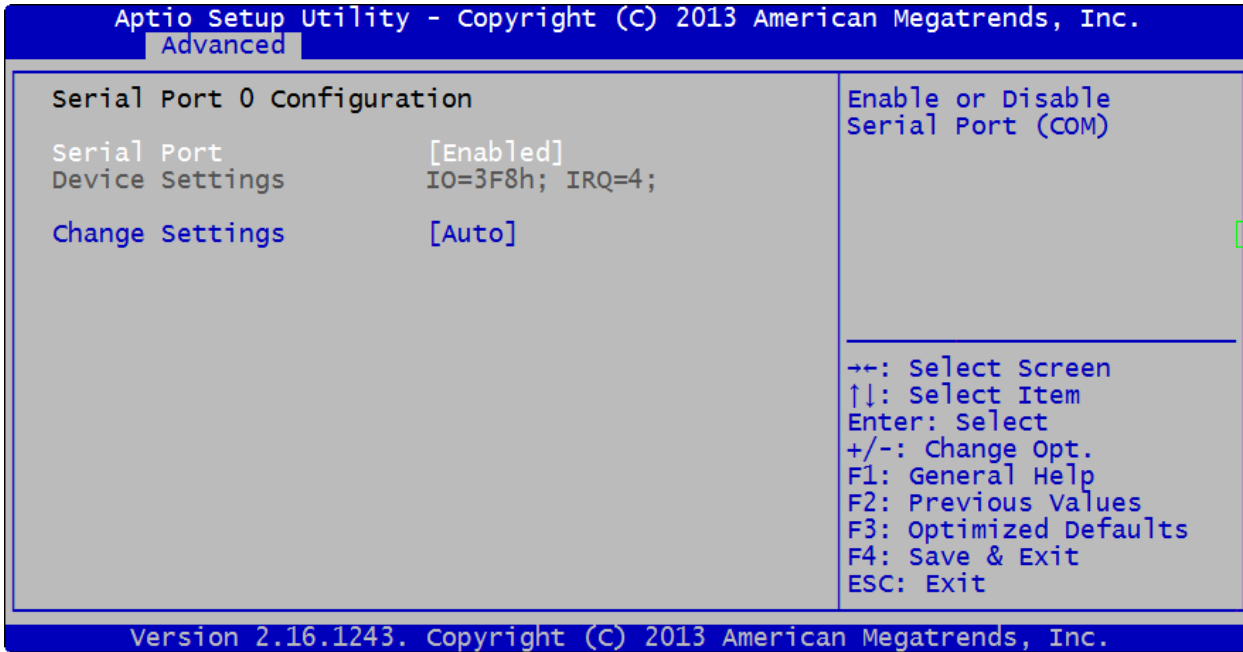


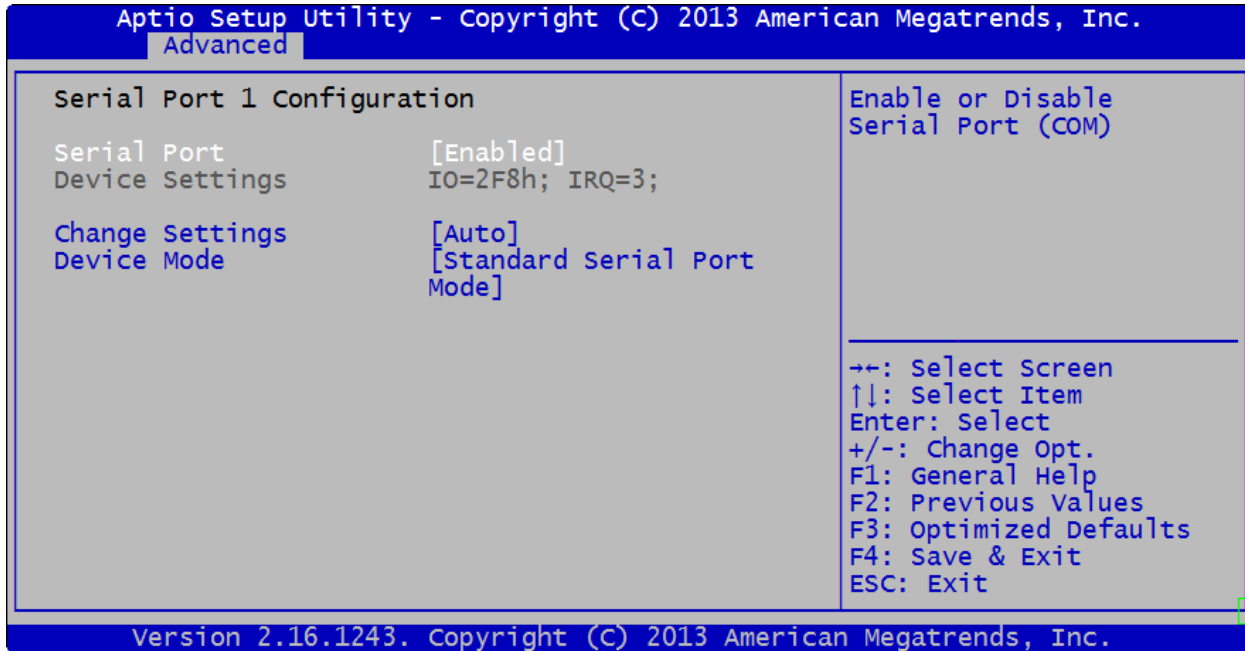
Fig. 2.2.12.b Serial Port 0 Configuration



This option allows the user to view and configure Serial Port 0.

Feature	Options	Description
Serial Port	<i>Enabled</i> <i>Disabled</i>	Enable or Disable Serial Port (COM)
Change Settings	<i>Auto</i> <i>IO=3F8h; IRQ=4;</i> <i>IO=3F8h; IRQ=3,4,5,6,7...;</i> <i>IO=2F8h; IRQ=3,4,5,6,7...;</i> <i>IO=3E8h; IRQ=3,4,5,6,7...;</i> <i>IO=2E8h; IRQ=3,4,5,6,7...;</i>	Select an optimal setting for Serial IO Device

Fig. 2.2.12.c NCT6776 Super IO Serial Port 1 Configuration

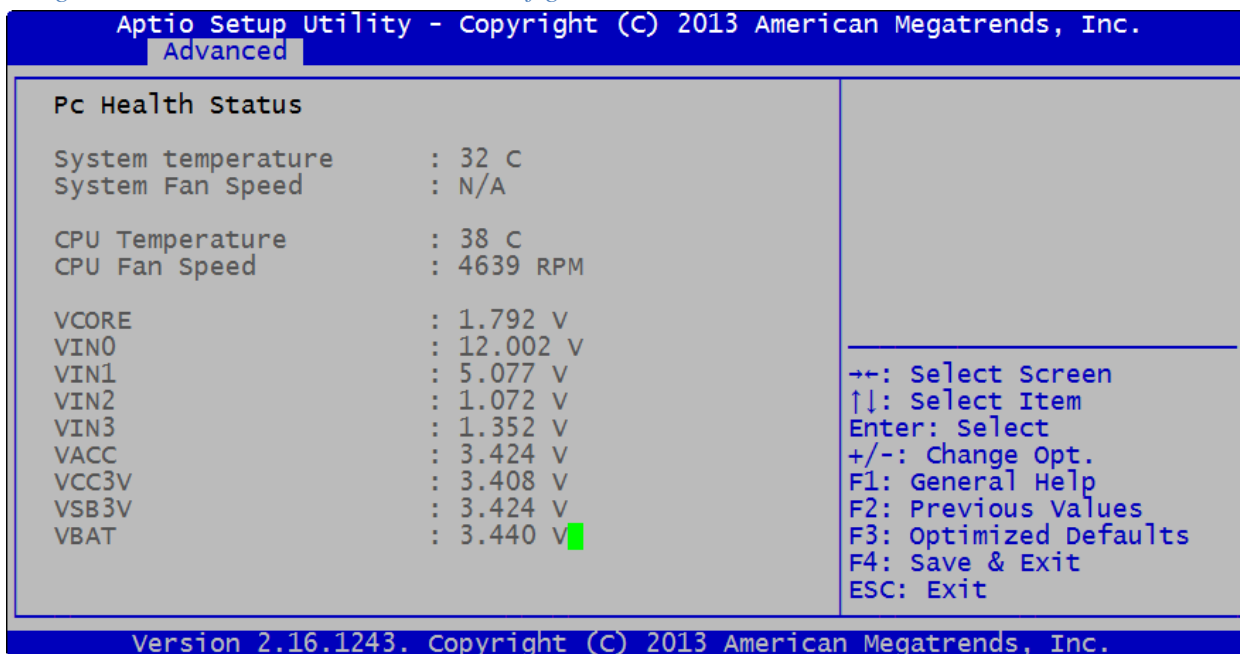


This option allows the user to view and configure Serial Port 1.

Feature	Options	Description
Serial Port	<i>Enabled</i> <i>Disabled</i>	Enable or Disable Serial Port (COM)
Change Settings	<i>Auto</i> <i>IO=2F8h; IRQ=3;</i> <i>IO=3F8h; IRQ=3,4,5,6,7...;</i> <i>IO=2F8h; IRQ=3,4,5,6,7...;</i> <i>IO=3E8h; IRQ=3,4,5,6,7...;</i> <i>IO=2E8h; IRQ=3,4,5,6,7...;</i>	Select an optimal setting for Serial IO Device
Device Mode	<i>Standard Serial Port Mode</i> <i>IrDA 1.0 (HP SIR) Mode</i> <i>ASKIR Mode</i>	Change the Serial Port mode. Please note that our current hardware only supports Standard Serial Port Mode.

2.2.13 NCT6776 HW Monitor Configuration

Fig. 2.2.13.a NCT6776 HW Monitor Configuration

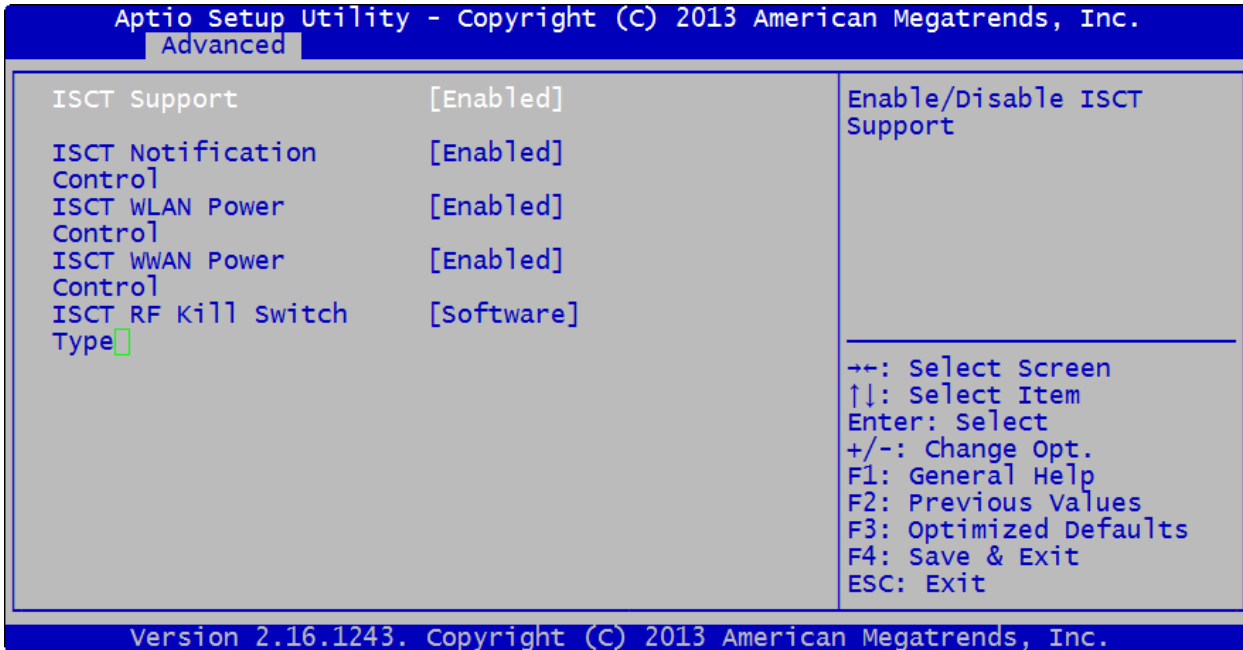


This option allows the user to view system and CPU temperatures, voltages, and the FAN speed.

Option	Description
System Temperature	This reports the 'ambient' temperature of the PCB in Celsius.
System Fan Speed	This option is not available since the system fan is not connected.
CPU Temperature	This reports the CPU temperature in Celsius.
CPU Fan Speed	This value reports the CPU Fan Speed.
VCORE	This value reports the Core CPU voltage.
VIN0	This value reports the 12V Input voltage.
VIN1	This value reports the 5V_standby voltage.
VIN2	This value reports the 1.05V PCH supply voltage.
VIN3	This value reports the supply voltage to the SODIMMs.
VACC VCC3V VS3V VBAT	All of these values report the 3.3V supply voltage.

2.2.14 Intel Smart Connect Technology

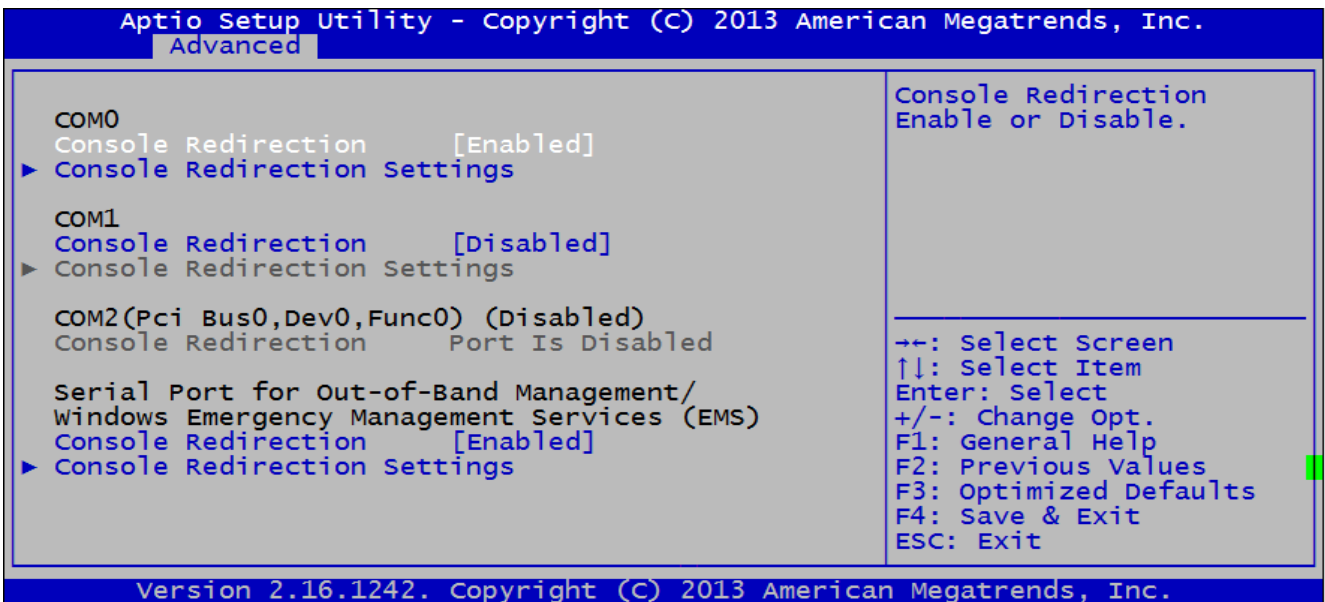
Fig. 2.2.14.a Intel Smart Connect Technology



Intel Smart Connect Technology (ISCT) is a feature designed to periodically wake the computer from sleep or standby mode so that certain programs and features can update themselves automatically.

2.2.15 Serial Port Console Redirection

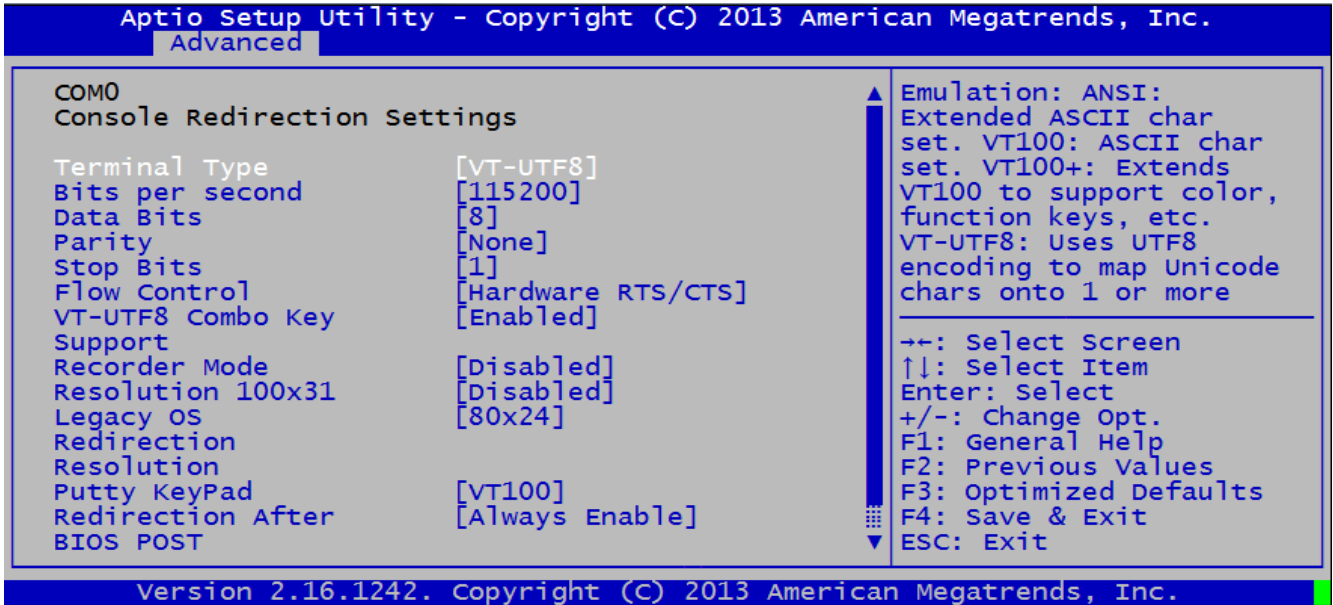
Fig. 2.2.15.a Serial Port Console Redirection



Serial Port Console Redirection allows a user to remotely control the computer’s keyboard and mouse through the computer’s serial port.

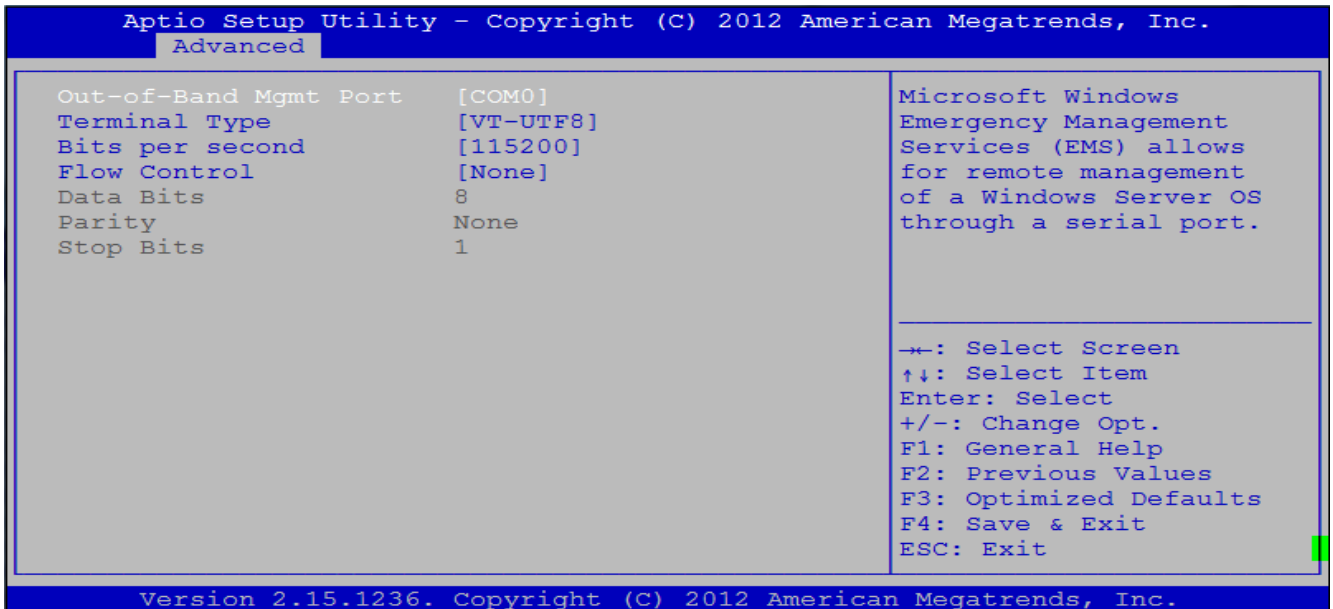
2.2.15.1 Console Redirection Settings

Fig. 2.2.15.1.a Console Redirection Settings (Screen 1 of 2)



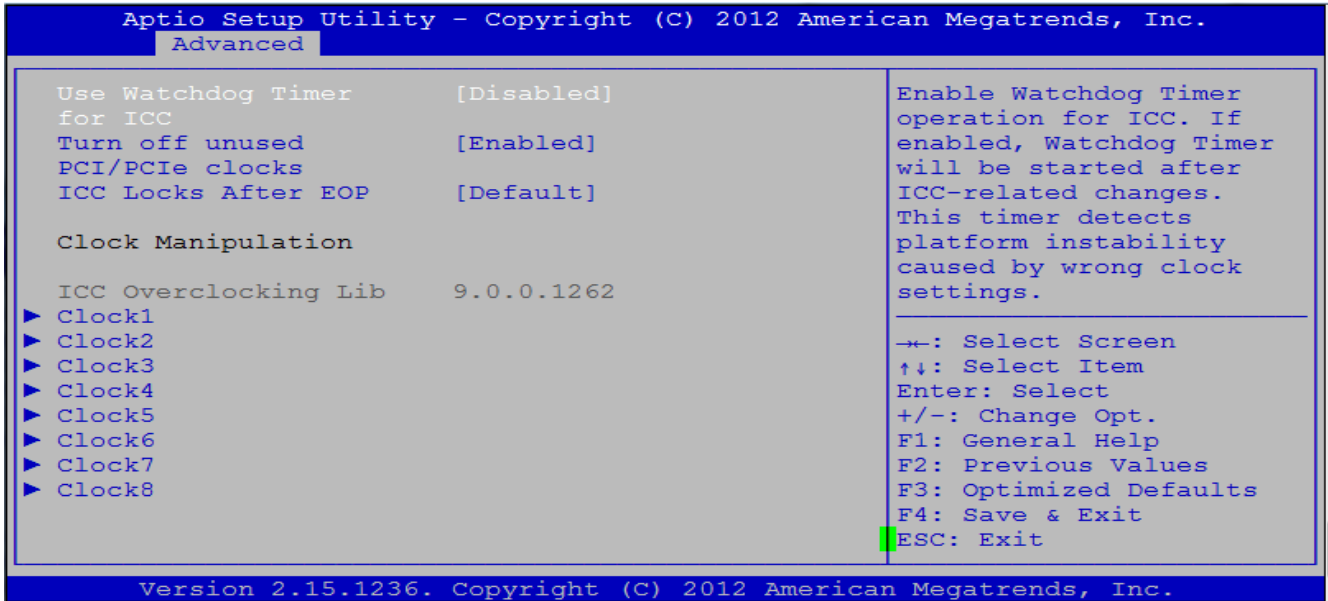
The options include Enable/Disable for each COM port.

Fig. 2.2.15.1.b Console Redirection Settings (Screen 2 of 2)



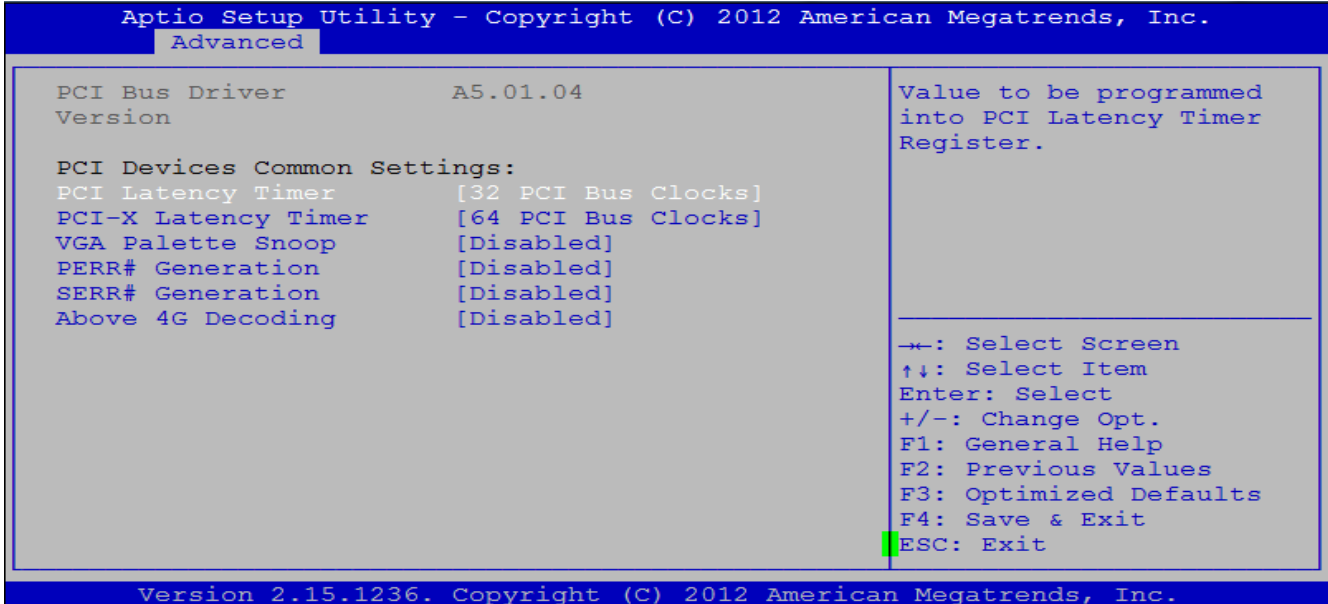
2.2.16 Intel® ICC (Watchdog Timer)

Fig. 2.2.16.a Intel® ICC (Watchdog Timer)



2.2.17 PCI Subsystem Settings

Fig. 2.2.17.a PCI Subsystem Settings

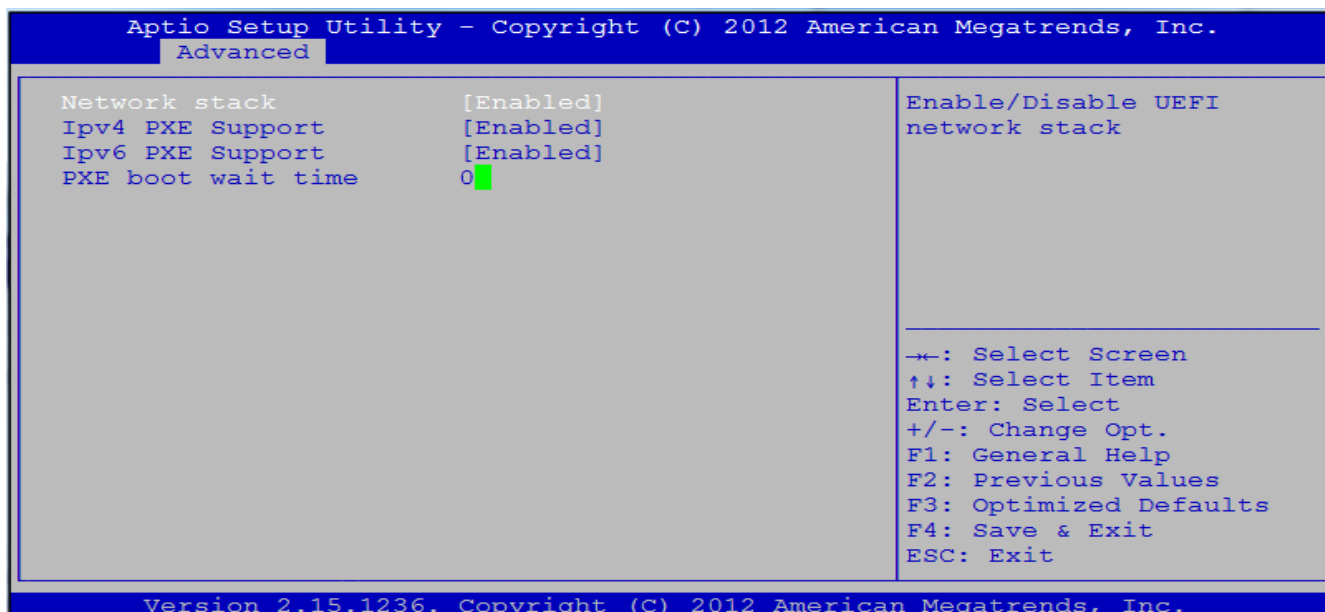


2.2.18 AMI Graphic Output Protocol Policy

Feature	Options	Description
AMI Graphic Output Protocol Policy		When outputting graphics, and there are multiple graphics devices, specify a device order, a brightness setting, and enable or disable the Built-In Self Test (BIST)

2.2.19 Network Stack

Fig. 2.2.18.a Network Stack

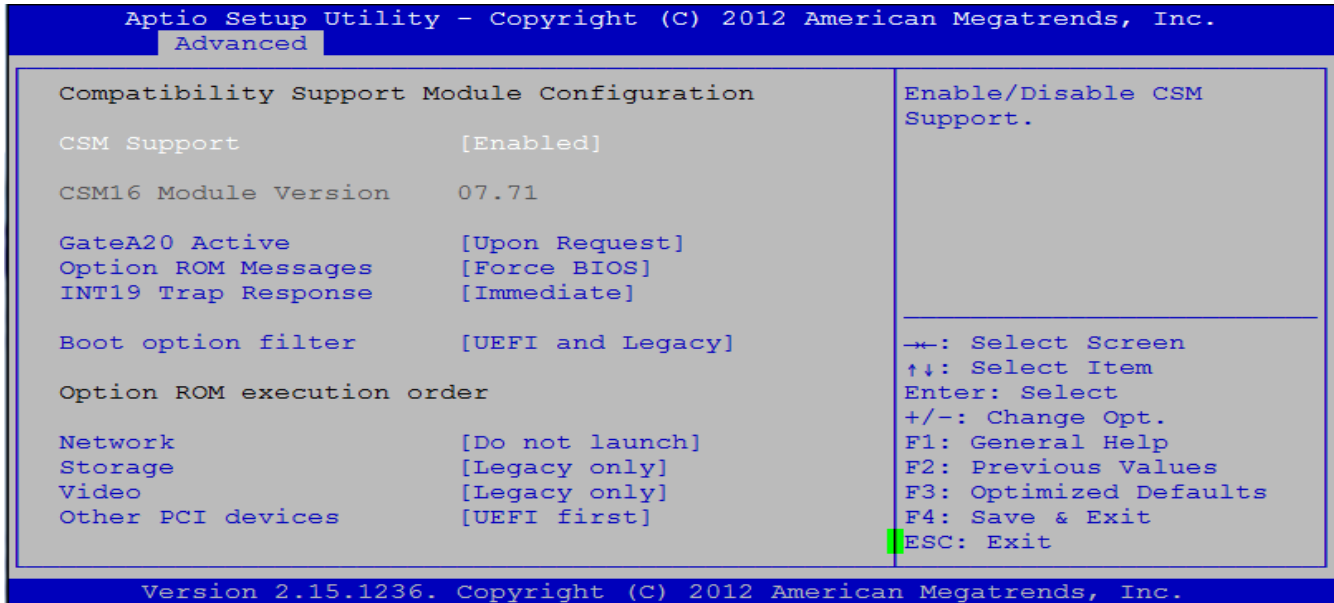


PXE stands for Preboot Execution Environment. PXE allows networked computers to be configured and booted remotely via Ethernet before their Operating System is booted.

Feature	Options	Description
IPv4 PXE Support	<i>Enabled</i> <i>Disabled</i>	This option, when enabled, allows for PXE booting via IPv4.
IPv6 PXE Support	<i>Enabled</i> <i>Disabled</i>	This option, when enabled, allows for PXE booting via IPv6.
PXE Boot Wait Time		This specifies how long this remote (client) computer will delay before accepting PXE boot requests from the server.

2.2.20 Compatibility Support Mode (CSM) Configuration

Fig. 2.2.20.a CSM Configuration



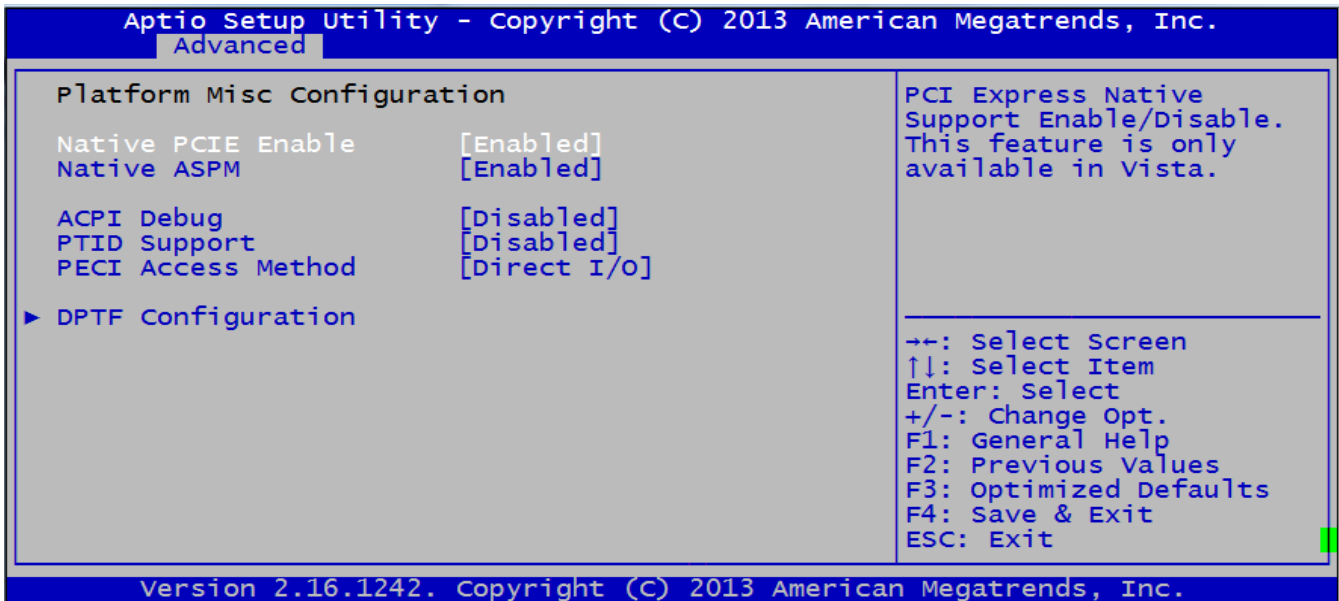
This option allows the user to view and configure the Compatibility Support Mode (CSM) Configuration.

Feature	Options	Description
CSM Support	<i>Enabled</i> <i>Disabled</i>	Enable or Disable Compatibility Support Mode (CSM) Support.
CSM16 Module Version		Displays CSM Module Version
GateA20 Active	<i>Upon Request</i> <i>Always</i>	GateA20 (GA20) can be disabled using BIOS Services. Do not allow disabling GA20; This option is useful when any RT code is executed above 1MB.
Option ROM Messages	<i>Force BIOS</i> <i>Keep Current</i>	Set display mode for Option ROM.
INT19 Trap Response	<i>Immediate</i> <i>Postponed</i>	BIOS reaction on INT19 trapping by Option ROM. Execute the trap right away. Execute the trap during legacy boot.
Boot Option filter	<i>UEFI and Legacy</i> <i>Legacy only</i> <i>UEFI only</i>	This option filters which ROM type(s) will be available during boot
Network	<i>Do not launch</i> <i>UEFI</i> <i>Legacy</i>	Controls the execution of UEFI and Legacy PXE Option Rom.

Storage	<i>Do not launch</i> <i>UEFI</i> <i>Legacy</i>	Controls the execution of UEFI and Legacy Storage Option Rom (OpROM).
Video	<i>Do not launch</i> <i>UEFI</i> <i>Legacy</i>	Controls the execution of UEFI and Legacy PXE Option Rom (OpROM).
Other PCI devices	<i>UEFI</i> <i>Legacy</i>	Determines Option ROM (OpROM) execution policy for devices other than Network, Storage, or Video.

2.2.21 Platform Miscellaneous Configuration

Fig. 2.2.21.a Platform Miscellaneous Configuration



The options in this menu allow users to configure the platform-related features.

Feature	Options	Description
Native PCIe Enable		Enabling this provides native support for PCIe. This feature is only available in Windows Vista.
Native ASPM		When enabled, Windows Vista will control the Active State Power Management (ASPM), when disabled, BIOS controls it.
ACPI Debug		This option opens a memory buffer for storing debug strings, and uses the Advanced Configuration and Power Interface (ACPI) debug method to write strings to the buffer.
PTID Support		Enable/Disable the Power and Temperature Instrumentation Details SSDT table in ACPI.

2.2.21.1 DPTF Configuration

Fig. 2.2.21.1.a DPTF Configuration (Screen 1 of 5)

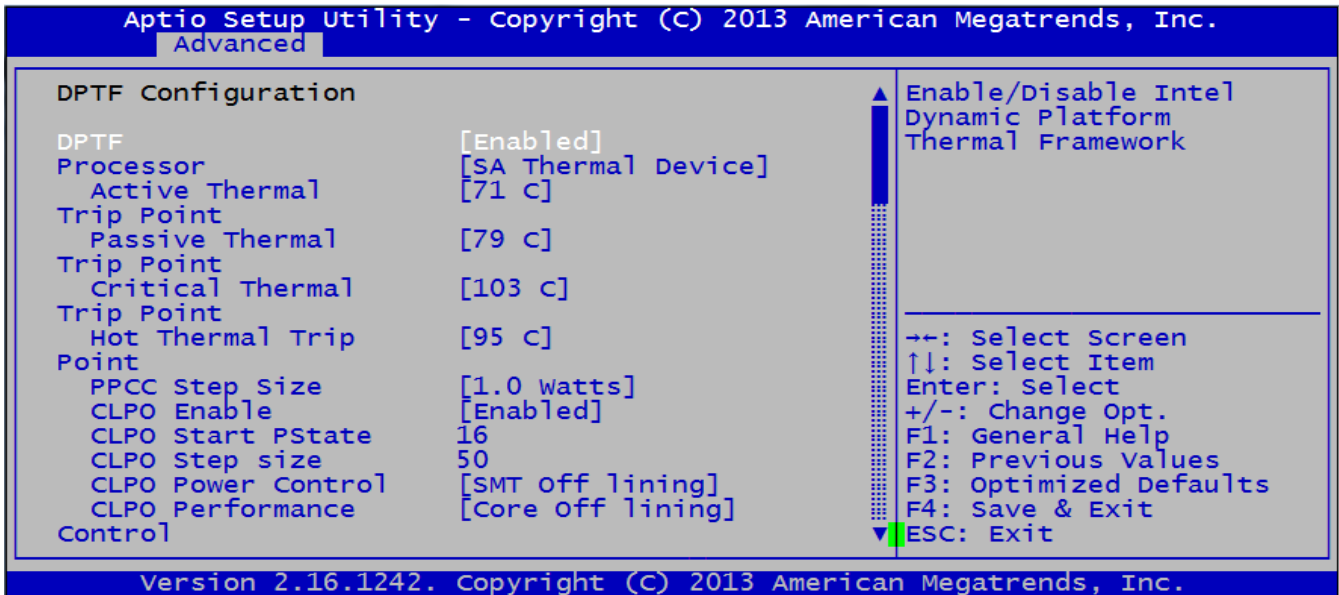


Fig. 2.2.21.1.b DPTF Configuration (Screen 2 of 5)

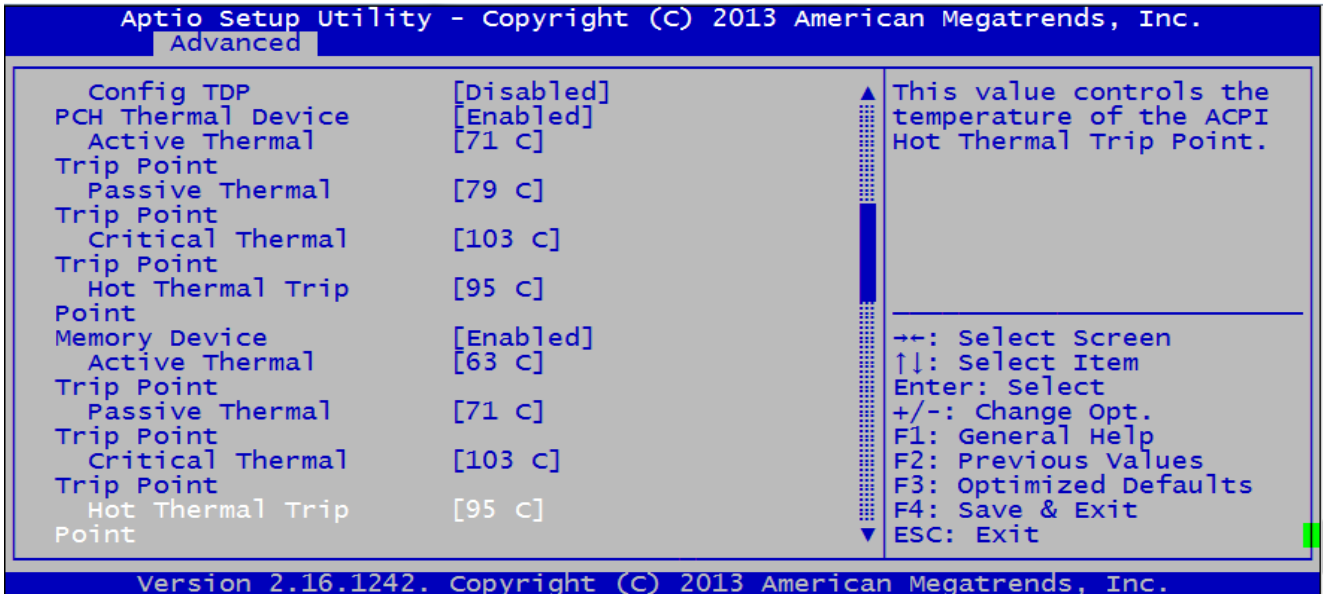


Fig. 2.2.21.1.c DPTF Configuration (Screen 3 of 5)

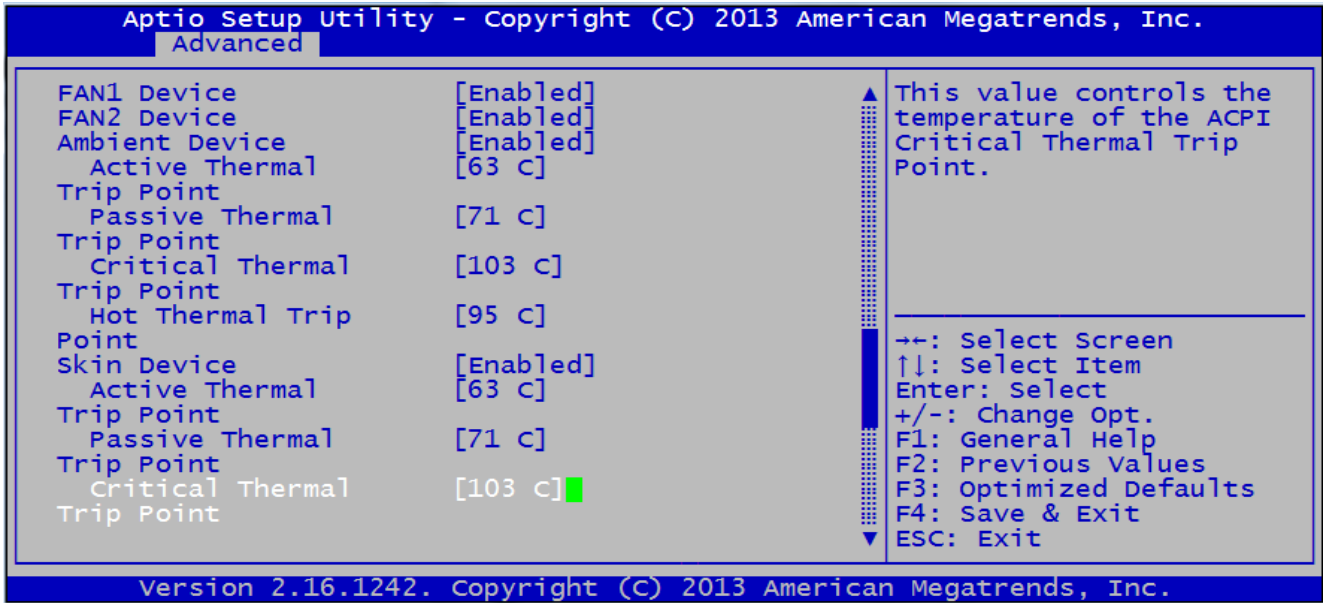
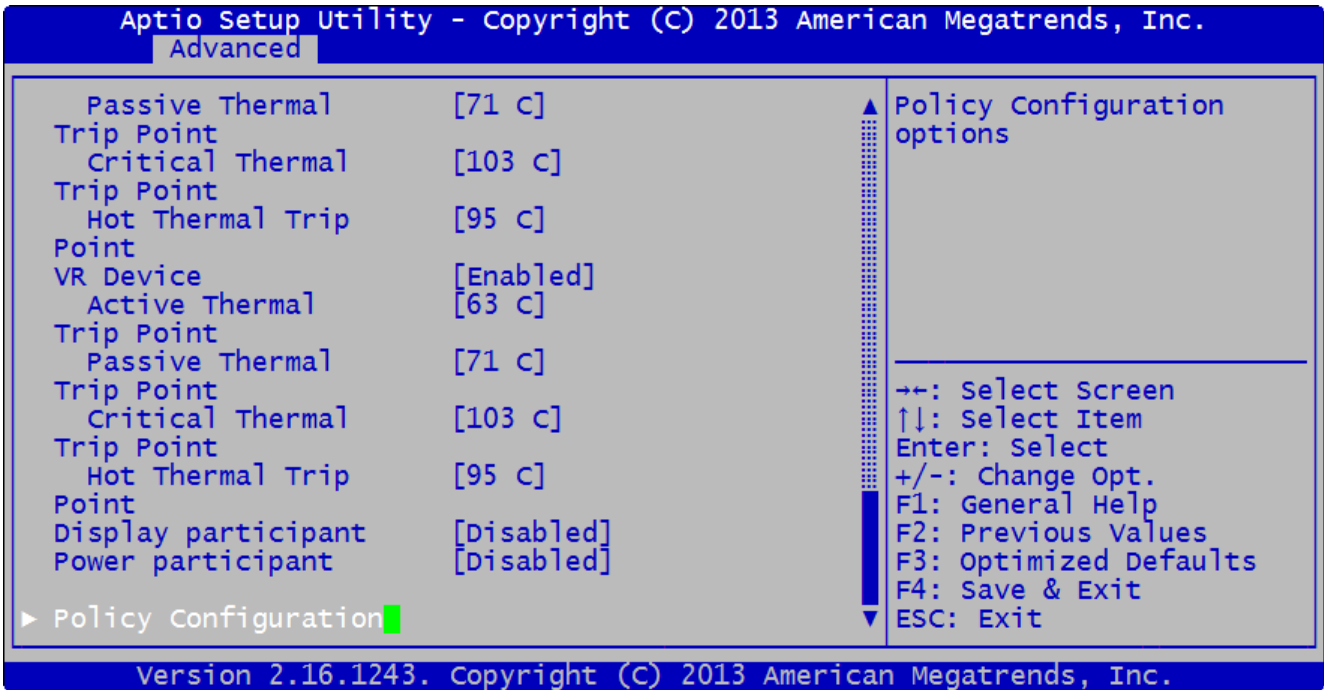


Fig. 2.2.21.1.d DPTF Configuration (Screen 4 of 5)



This option allows the user to view and configure the Dynamic Platform Thermal Framework (DPTF) Configuration.

Feature	Options	Description
DPTF	<i>Enabled</i> <i>Disabled</i>	Enable or Disable Compatibility Support Mode (CSM) Support.
Processor	<i>Disabled</i> <i>SA Thermal Device</i> <i>CPU Thermal Device</i>	Enable or Disable Processor Thermal Device
Active Thermal Trip Point	<i>Disabled</i> <i>15 °C</i> <i>23 °C</i> ... <i>71 °C</i> <i>119 °C</i>	This value controls the temperature of the ACPI Active Thermal Trip Point.
Passive Thermal Trip Point	<i>Disabled</i> <i>15 °C</i> <i>23 °C</i> ... <i>79 °C</i> <i>119 °C</i>	This value controls the temperature of the ACPI Passive Thermal Trip Point.
Critical Thermal Trip Point	<i>Disabled</i> <i>15 °C</i> <i>23 °C</i> ... <i>103 °C</i> <i>119 °C</i>	This value controls the temperature of the ACPI Critical Thermal Trip Point.
Hot Thermal Trip Point	<i>Disabled</i> <i>15 °C</i> <i>23 °C</i> ... <i>95 °C</i> <i>119 °C</i>	This value controls the temperature of the ACPI Hot Thermal Trip Point.
PPCC Step Size	<i>0.5 Watts</i> <i>1.0 Watts</i> <i>1.5 Watts</i> <i>2.0 Watts</i>	Step size for Turbo power Limit (RAPL) control.
CLP0 Enable	<i>Enabled</i> <i>Disabled</i>	Instructs the policy to use Active Cores if they are available.
CLP0 Start PState	<i>16</i>	Instructs the policy when to initiate Active Core control if enabled. Note: 16=LFM
CLP0 Step size	<i>50</i>	Instructs the policy to take away logical processors in the specified percentage steps.
CLP0 Power Control	<i>Disabled</i> <i>SMT Off lining</i> <i>Core Off lining</i>	Instructs the policy whether to use Core off lining or SMT off lining if Active core control is enabled to be used in P0 or when power control is applied.
CLP0 Performance Control	<i>Disabled</i> <i>SMT Off lining</i> <i>Core Off lining</i>	Instructs the policy whether to use Core off lining or SMT off lining if Active core control is enabled

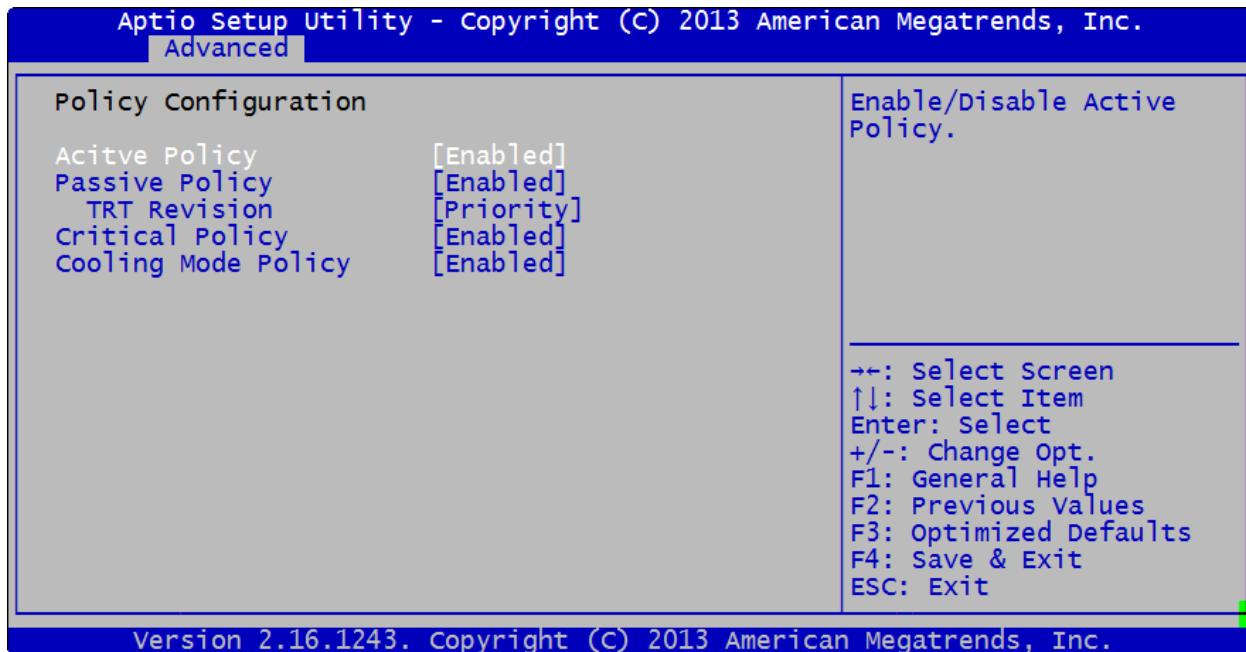
		to be used in P1 or when performance control is applied.
Config TDP	<i>Disabled</i> <i>Enabled</i>	Enable or Disable Configurable Thermal Design Power (TDP).
PCH Thermal Device	<i>Enabled</i> <i>Disabled</i>	Enable or Disable Platform Control Hub (PCH) Thermal Device.
Active Thermal Trip Point	<i>Disabled</i> 15 °C 23 °C ... <i>71 °C</i> 119 °C	This value controls the temperature of the ACPI Active Thermal Trip Point.
Passive Thermal Trip Point	<i>Disabled</i> 15 °C 23 °C ... <i>79 °C</i> 119 °C	This value controls the temperature of the ACPI Passive Thermal Trip Point.
Critical Thermal Trip Point	<i>Disabled</i> 15 °C 23 °C ... <i>103 °C</i> 119 °C	This value controls the temperature of the ACPI Critical Thermal Trip Point.
Hot Thermal Trip Point	<i>Disabled</i> 15 °C 23 °C ... <i>95 °C</i> 119 °C	This value controls the temperature of the ACPI Hot Thermal Trip Point.
Memory Device	<i>Enabled</i> <i>Disabled</i>	Enable or Disable Memory Device.
Active Thermal Trip Point	<i>Disabled</i> 15 °C 23 °C ... <i>71 °C</i> 119 °C	This value controls the temperature of the ACPI Active Thermal Trip Point.
Passive Thermal Trip Point	<i>Disabled</i> 15 °C 23 °C ... <i>79 °C</i> 119 °C	This value controls the temperature of the ACPI Passive Thermal Trip Point.
Critical Thermal Trip Point	<i>Disabled</i> 15 °C 23 °C ...	This value controls the temperature of the ACPI Critical Thermal Trip Point.

	<i>103 °C</i> <i>119 °C</i>	
Hot Thermal Trip Point	<i>Disabled</i> <i>15 °C</i> <i>23 °C</i> ... <i>95 °C</i> <i>119 °C</i>	This value controls the temperature of the ACPI Hot Thermal Trip Point.
Fan1 Device	<i>Disabled</i> <i>Enabled</i>	Enable the Fan1 device. There is no Fan1 or System Fan connected to this system.
Fan2 Device	<i>Enabled</i> <i>Disabled</i>	Enable the Fan2 or CPU Fan device.
Ambient Device	<i>Enabled</i> <i>Disabled</i>	Enable or Disable the Ambient Thermal Device.
Active Thermal Trip Point	<i>Disabled</i> <i>15 °C</i> <i>23 °C</i> ... <i>71 °C</i> <i>119 °C</i>	This value controls the temperature of the ACPI Active Thermal Trip Point.
Passive Thermal Trip Point	<i>Disabled</i> <i>15 °C</i> <i>23 °C</i> ... <i>79 °C</i> <i>119 °C</i>	This value controls the temperature of the ACPI Passive Thermal Trip Point.
Critical Thermal Trip Point	<i>Disabled</i> <i>15 °C</i> <i>23 °C</i> ... <i>103 °C</i> <i>119 °C</i>	This value controls the temperature of the ACPI Critical Thermal Trip Point.
Hot Thermal Trip Point	<i>Disabled</i> <i>15 °C</i> <i>23 °C</i> ... <i>95 °C</i> <i>119 °C</i>	This value controls the temperature of the ACPI Hot Thermal Trip Point.
Skin Device	<i>Enabled</i> <i>Disabled</i>	Enable or Disable the Skin Thermal Device.
Active Thermal Trip Point	<i>Disabled</i> <i>15 °C</i> <i>23 °C</i> ... <i>71 °C</i> <i>119 °C</i>	This value controls the temperature of the ACPI Active Thermal Trip Point.
Passive Thermal Trip Point	<i>Disabled</i> <i>15 °C</i>	This value controls the temperature of the ACPI Passive Thermal Trip Point.

	<p>23 °C</p> <p>...</p> <p>79 °C</p> <p>119 °C</p>	
Critical Thermal Trip Point	<p>Disabled</p> <p>15 °C</p> <p>23 °C</p> <p>...</p> <p>103 °C</p> <p>119 °C</p>	This value controls the temperature of the ACPI Critical Thermal Trip Point.
Hot Thermal Trip Point	<p>Disabled</p> <p>15 °C</p> <p>23 °C</p> <p>...</p> <p>95 °C</p> <p>119 °C</p>	This value controls the temperature of the ACPI Hot Thermal Trip Point.
Exhaust Fan Device	<p>Enabled</p> <p>Disabled</p>	Enable or Disable the Exhaust Fan Thermal Device.
Active Thermal Trip Point	<p>Disabled</p> <p>15 °C</p> <p>23 °C</p> <p>...</p> <p>71 °C</p> <p>119 °C</p>	This value controls the temperature of the ACPI Active Thermal Trip Point.
Passive Thermal Trip Point	<p>Disabled</p> <p>15 °C</p> <p>23 °C</p> <p>...</p> <p>79 °C</p> <p>119 °C</p>	This value controls the temperature of the ACPI Passive Thermal Trip Point.
Critical Thermal Trip Point	<p>Disabled</p> <p>15 °C</p> <p>23 °C</p> <p>...</p> <p>103 °C</p> <p>119 °C</p>	This value controls the temperature of the ACPI Critical Thermal Trip Point.
Hot Thermal Trip Point	<p>Disabled</p> <p>15 °C</p> <p>23 °C</p> <p>...</p> <p>95 °C</p> <p>119 °C</p>	This value controls the temperature of the ACPI Hot Thermal Trip Point.
VR Device	<p>Enabled</p> <p>Disabled</p>	Enable or Disable the VR Thermal Device.
Active Thermal Trip Point	<p>Disabled</p> <p>15 °C</p> <p>23 °C</p> <p>...</p>	This value controls the temperature of the ACPI Active Thermal Trip Point.

	<i>71°C</i> <i>119°C</i>	
Passive Thermal Trip Point	<i>Disabled</i> <i>15°C</i> <i>23 °C</i> ... <i>79°C</i> <i>119°C</i>	This value controls the temperature of the ACPI Passive Thermal Trip Point.
Critical Thermal Trip Point	<i>Disabled</i> <i>15°C</i> <i>23 °C</i> ... <i>103°C</i> <i>119°C</i>	This value controls the temperature of the ACPI Critical Thermal Trip Point.
Hot Thermal Trip Point	<i>Disabled</i> <i>15°C</i> <i>23 °C</i> ... <i>95°C</i> <i>119°C</i>	This value controls the temperature of the ACPI Hot Thermal Trip Point.
Display participant	<i>Disabled</i> <i>Enabled</i>	Enable or Disable the Display participant.
Power Participant	<i>Disabled</i> <i>Enabled</i>	Enable or Disable the Power participant.
► Policy Configuration		Policy Configuration Options Menu

Fig. 2.2.21.1.e Policy Configuration (Screen 5 of 5)

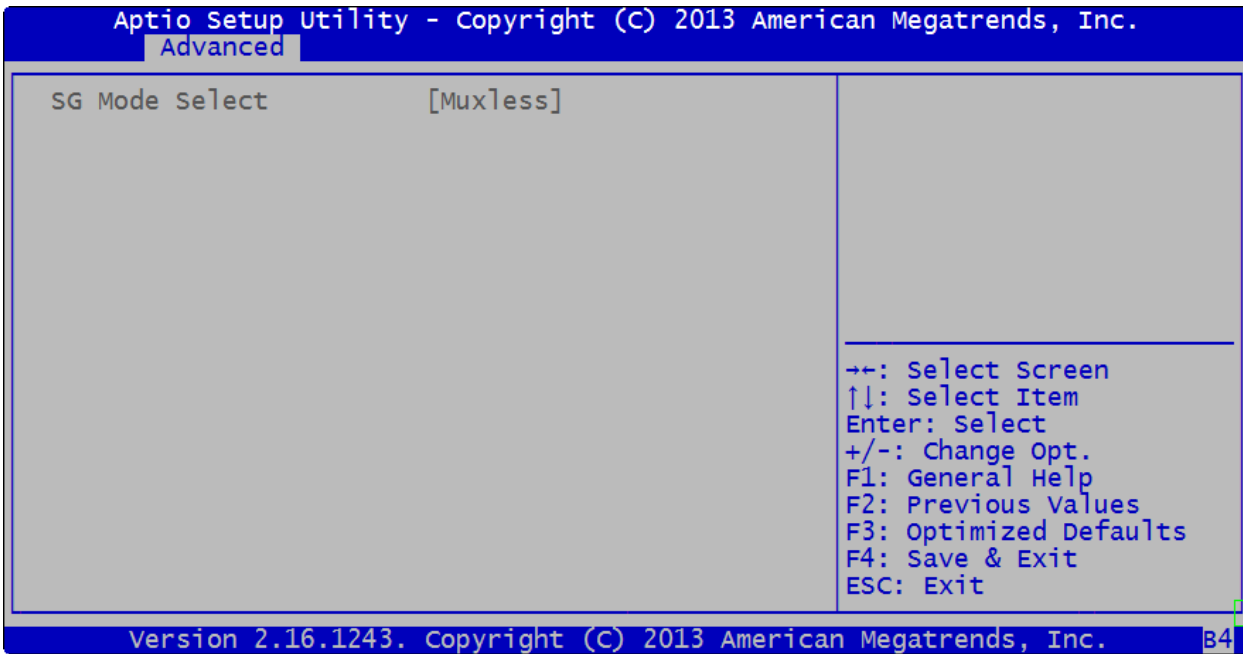


This option allows the user to view and configure Serial Port 1.

Feature	Options	Description
Active Policy	<i>Enabled</i> <i>Disabled</i>	Enable or Disable Active Policy.
Passive Policy	<i>Enabled</i> <i>Disabled</i>	Enable or Disable Passive Policy.
TRT Revision	<i>Traditional</i> <i>Priority</i>	Select the TRT influence.
Critical Policy	<i>Enabled</i> <i>Disabled</i>	Enable or Disable Critical Policy.
Cooling Mode Policy	<i>Enabled</i> <i>Disabled</i>	Enable or Disable Cooling Mode Policy.

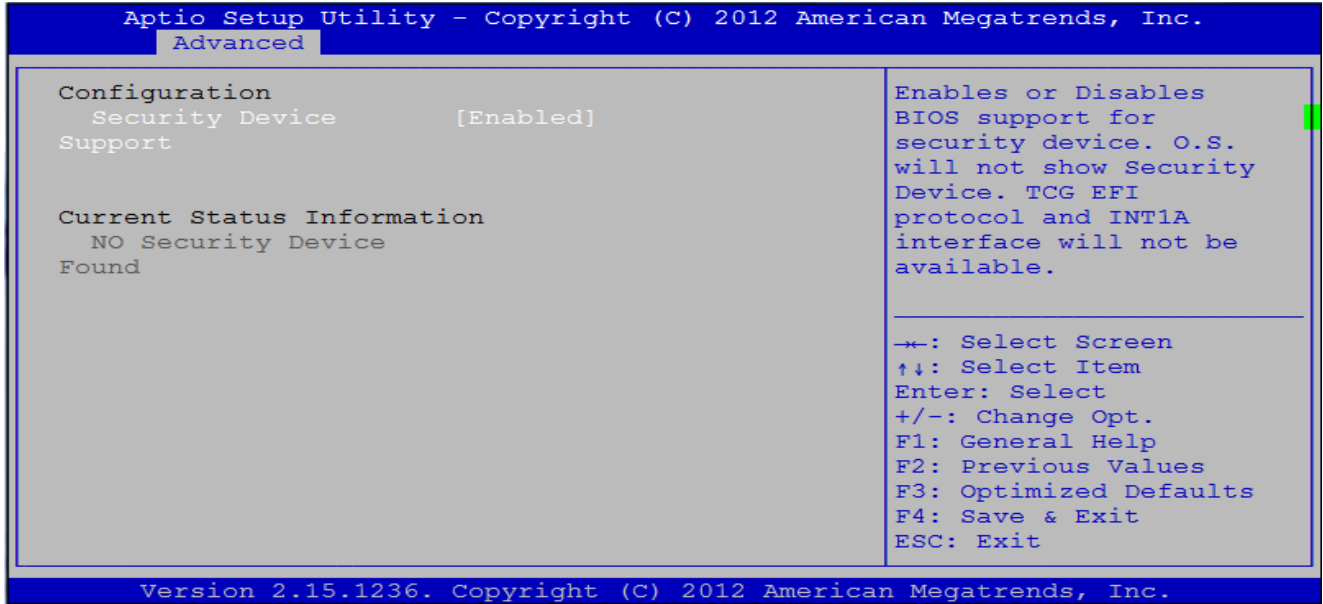
2.2.22 Switchable Graphics

Fig. 2.2.22.a Switchable Graphics



2.2.23 Trusted Computing

Fig. 2.2.23.a Trusted Computing



Feature	Options	Description
Security Device Support		Enables or Disables BIOS support for security device (ie TPM). Affects visibility of security device in OS, and whether TCG EFI protocol and INT1A interface will be available.

2.2.24 USB Configuration

Fig. 2.2.24.a USB Configuration



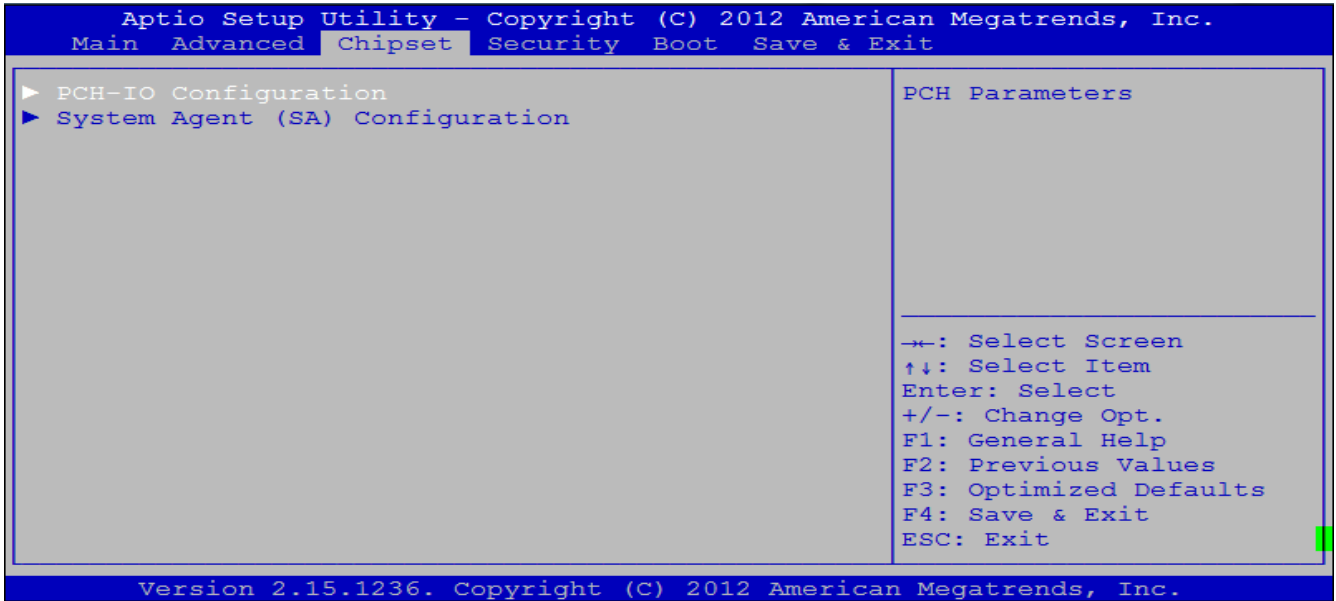
This option allows the user to view and change the USB Configuration.

Feature	Options	Description
Legacy USB Support	<i>Enabled</i> <i>Disabled</i> <i>Auto</i>	Allows selection of legacy support for USB devices. Enables Legacy USB support. Keep USB devices available only for EFI application. Disables legacy support if no USB devices are connected.
USB 3.0 Support	<i>Enabled</i> <i>Disabled</i>	Enables USB3,0 Extensible Host Controller Interface (xHCI) controller support.
XHCI Hand-off	<i>Enabled</i> <i>Disabled</i>	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
EHCI Hand-off	<i>Enabled</i> <i>Disabled</i>	This is a workaround for OSes without EHCI hand-off support. The XHCI ownership change should be claimed by EHCI driver.
USB Mass Storage Driver Support	<i>Enabled</i> <i>Disabled</i>	Enables or Disables USB Mass storage Driver Support.
USB transfer time-out	<i>1 sec</i> <i>5 sec</i> <i>10 sec</i> <i>20 sec</i>	The time-out value for control, bulk, and interrupt transfers.
Device reset time-out	<i>10 sec</i> <i>20 sec</i> <i>30 sec</i> <i>40 sec</i>	Sets USB mass storage devices start unit command time-out.
Device power-up delay	<i>Auto</i> <i>Manual</i>	Maximum time the device will take before it reports itself to the Host controller. 'Auto' uses default values; for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

2.3 Chipset Menu, Configuration, and Settings

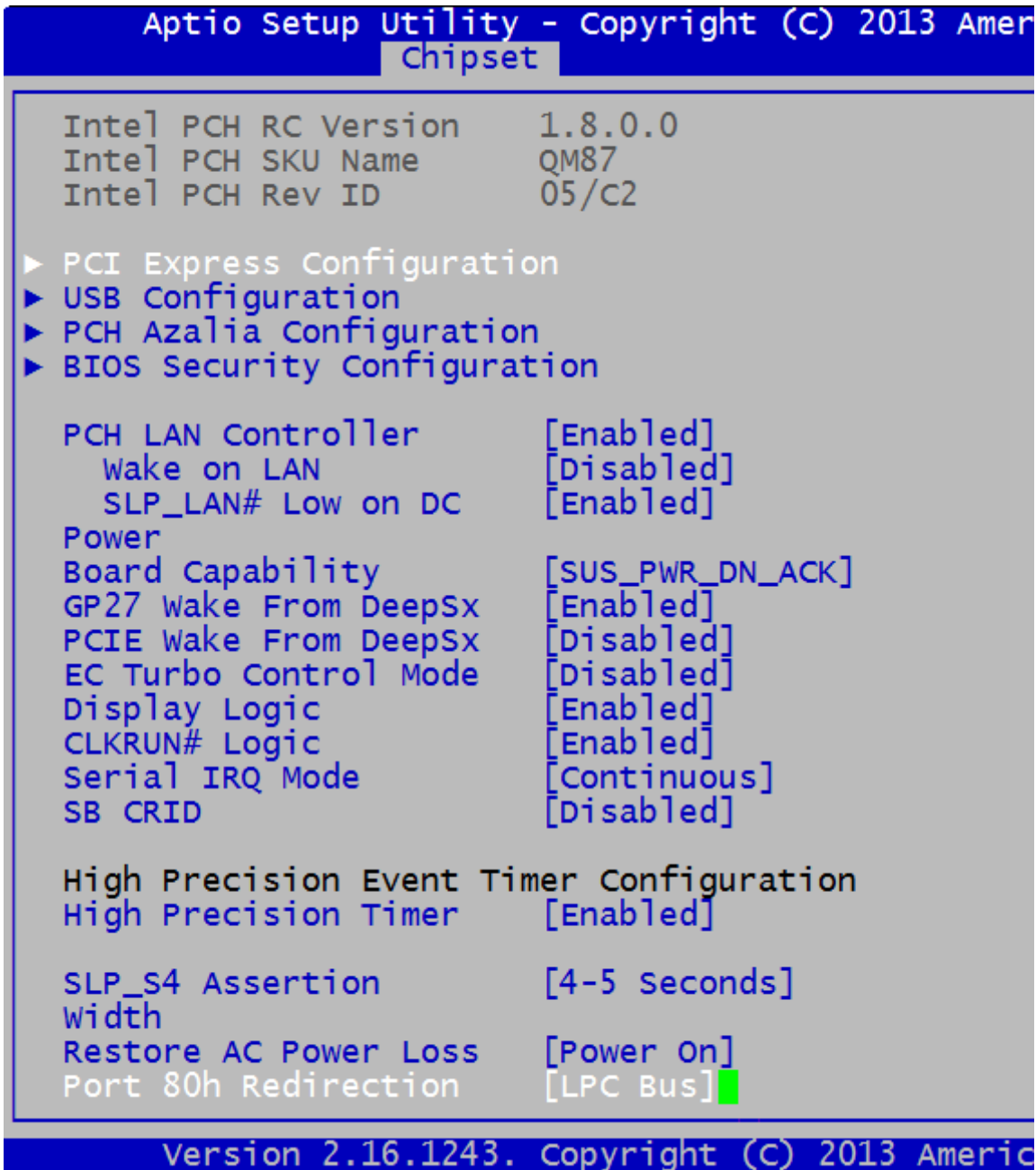
2.3 Chipset Menu

Fig. 2.3.a Chipset Menu



2.3.1 PCH I/O Configuration

Fig. 2.3.1.a PCH I/O Configuration

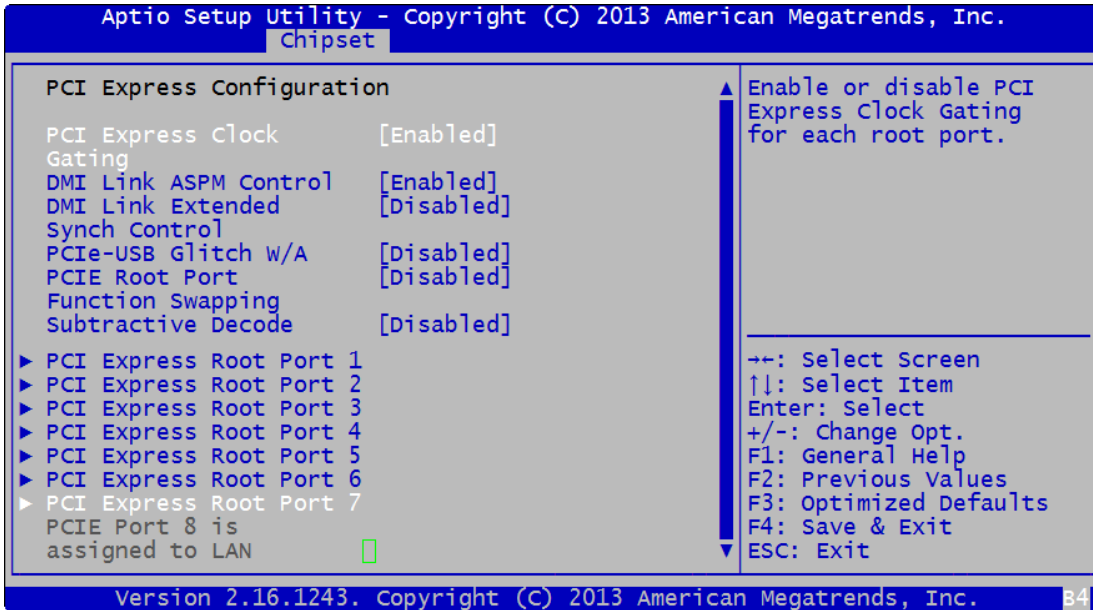


This option allows the user to view or edit the PCH I/O Configuration.

Feature	Options	Description
► PCI Express Configuration		PCI Express Configuration Menu Settings
► USB Configuration		USB Configuration Menu Settings
► PCH Azalia Configuration		PCH Azalia Configuration Menu Settings
► Bios Security Configuration		Bios Security Configuration Menu Settings
PCH Lan Controller	<i>Enabled</i> <i>Disabled</i>	Enables or Disables onboard NIC
Wake on LAN	<i>Disabled</i> <i>Enabled</i>	Enables or Disables integrated LAN to wake the system. The Wake on LAN cannot be disabled if ME is on at Sx state.
SLP_LAN# Low on DC Power	<i>Enabled</i> <i>Disabled</i>	Enables or Disables SLP_LAN# Low on DC Power.
Board Capability	<i>SUS_PWR_DN_ACK</i> <i>DeepSx</i>	Send Disabled to PCH Show DeepSx Policies Note: Our Boards currently do not support DeepSx.
GP27 Wake from DeepSx	<i>Enabled</i> <i>Disabled</i>	Enables or Disables Wake from DeepSx by the assertion of GP27 pin. Note: Our Boards currently do not support DeepSx.
PCIE Wake from DeepSx	<i>Disabled</i> <i>Enabled</i>	Enables or Disables Wake from DeepSx by the assertion of PCIE. Note: Our Boards currently do not support DeepSx.
EC Turbo Control Mode	<i>Disabled</i> <i>Enabled</i>	Enables or Disables Embedded Controller (EC) Turbo Control Mode.
Display Logic	<i>Enabled</i> <i>Disabled</i>	Enables or Disables the Platform Controller Hub (PCH) Display Logic.
CLKRUN# Logic	<i>Enabled</i> <i>Disabled</i>	Enables or Disables the CLKRUN# lgic to stop the PCI clocks
Serial IRQ Mode	<i>Quiet</i> <i>Continuous</i>	Configure Serial IRQ Mode
SB CRID	<i>Disabled</i> <i>Enabled</i>	When disabled, the Revision ID (RID) register reports Stepping Revision ID (SRID). When enabled, the RID register reports the Compatible Revision ID.
High Precision Event Timer Configuration		
High Precision Timer	<i>Enabled</i> <i>Disabled</i>	Enables or Disables the High Precision Event Timer.
SLP_S4 Assertion Width	<i>Disabled</i> <i>1-2 Seconds</i> <i>2-3 Seconds</i> <i>3-4 Seconds</i> <i>4-5 Seconds</i>	Select a minimum assertion width of the SLP_S4# signal.
Restore AC Power Loss	<i>Power Off</i> <i>Power On</i> <i>Last State</i>	Selects AC power state when power is re-applied after a power failure.
Port 80h Redirection	<i>LPC Bus</i> <i>PCIE Bus</i>	Controls where the Port 80h Cycles are sent.

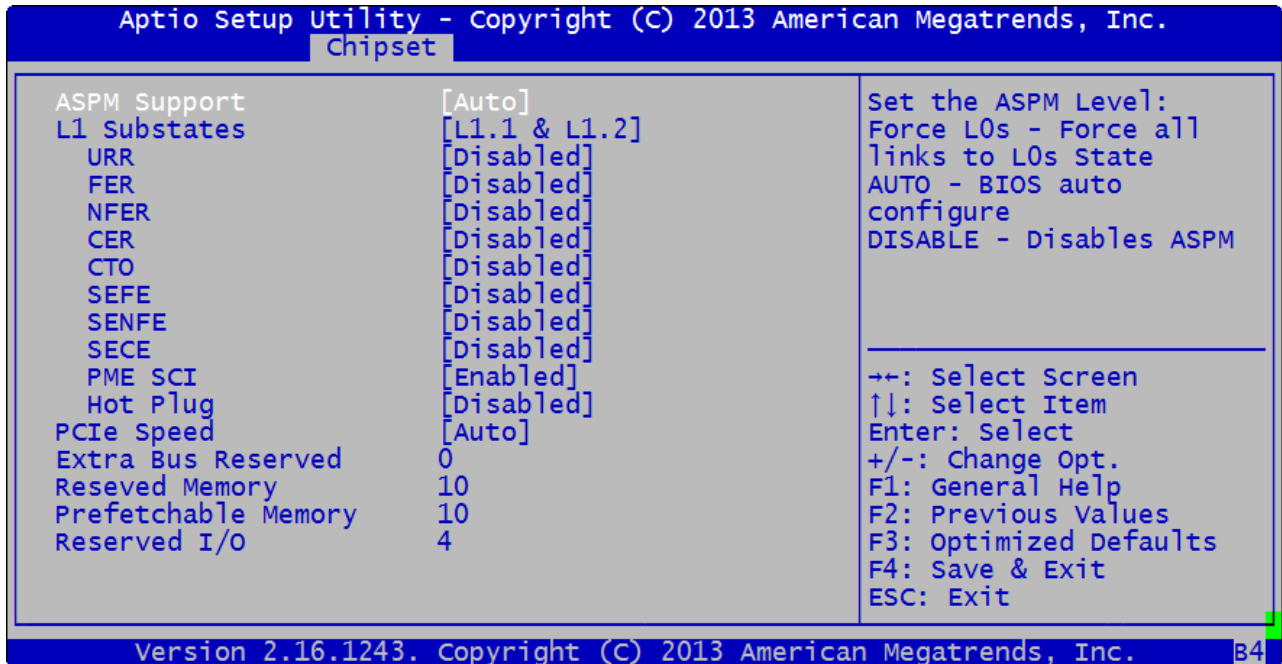
2.3.1.1 PCI Express Configuration

Fig. 2.3.1.1.a PCI Express Configuration



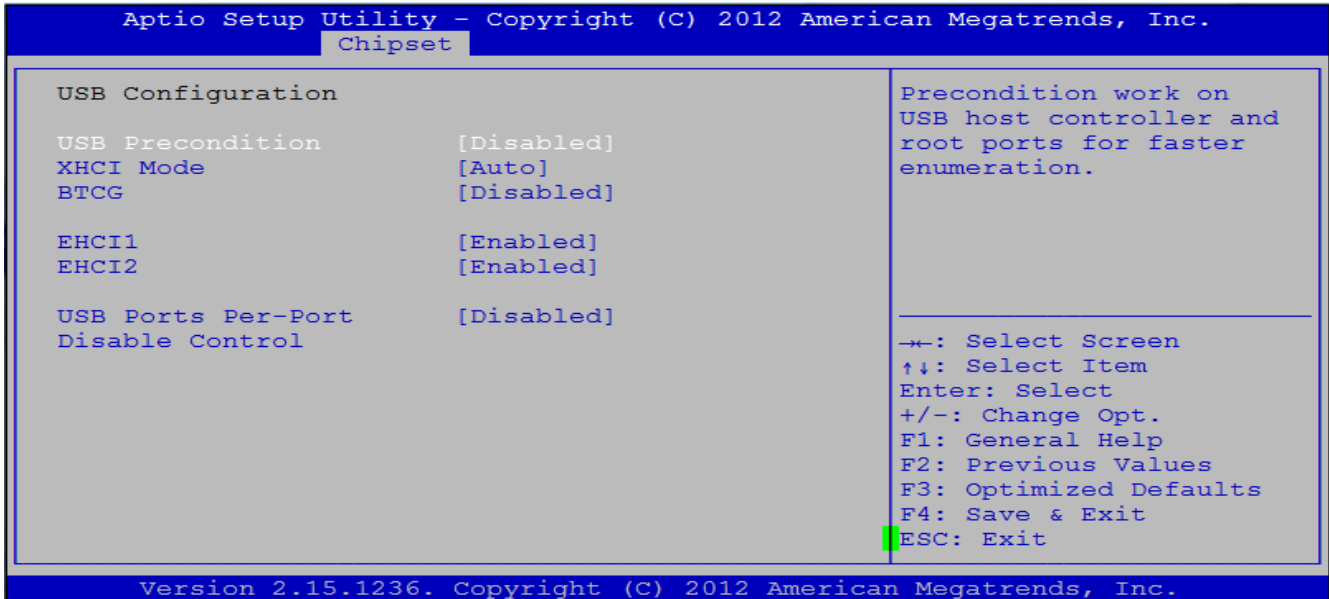
Feature	Options	Description
PCI Express Clock Gating		Controls Power Gating: reducing PCI Express power consumption to mobile levels.
PCI Express Root Port 1-7 All	Enabled Disabled	Master enable/disable of the individual PCI Express root port controllers within the chipset.

Fig. 2.3.1.1.b PCI Express Root Port (1 to 7)



2.3.1.2 USB Configuration

Fig. 2.3.1.2.a USB Configuration



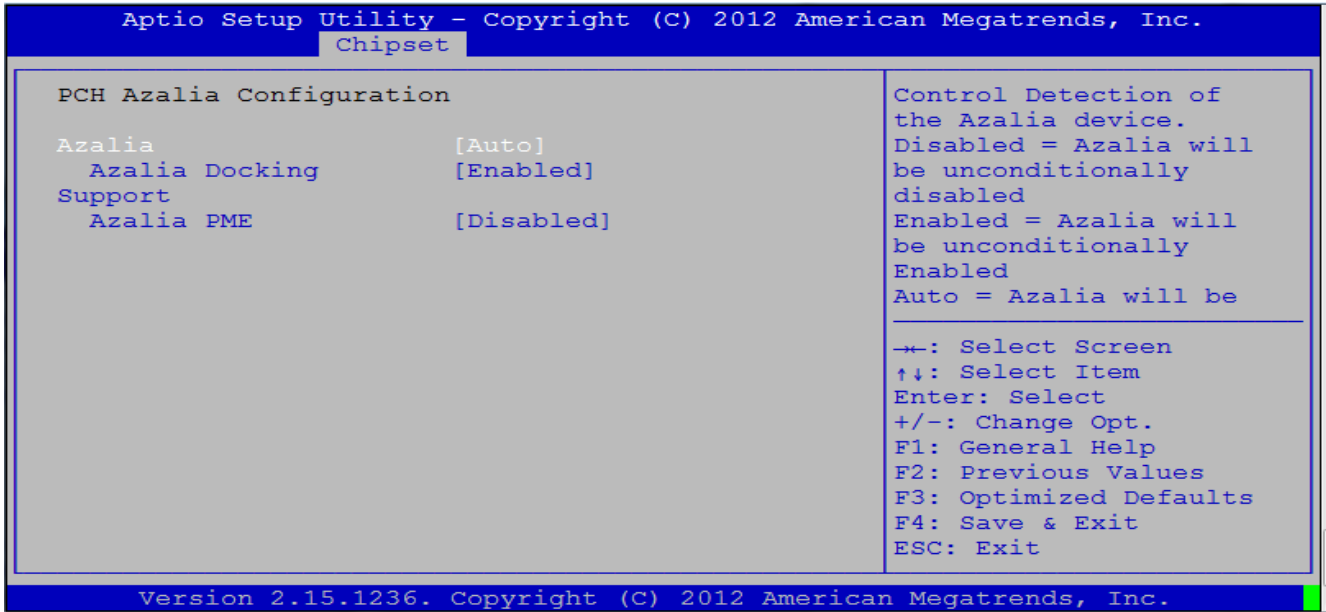
This option allows the user to view and change the USB Configuration.

Feature	Options	Description
USB Precondition	<i>Enabled</i> <i>Disabled</i>	Precondition work on USB host controller and root ports for faster enumeration.
XHCI Mode	<i>Auto</i> <i>Smart Auto</i> <i>Enabled</i>	<p>The Extensible Host Controller Interface (xHCI) is the USB 3.0 controller. The different modes of operation are:</p> <p><i>Auto</i> BIOS routes the sharable ports to EHCI controller. Then it uses ACPI protocols to provide an option to enable the xHCI controller and reroute the sharable ports. Note: This is the recommended mode when BIOS does NOT have xHCI pre-boot support.</p> <p><i>Smart Auto</i> This mode is available only when the BIOS supports the xHCI controller in the pre-boot environment. This mode is similar to Auto, but it adds the capability to route the ports to xHCI or EHCI according to setting used in previous boots (for non-G3 boot) in the pre-boot environment. This allows the use of USB 3.0 devices prior to OS boot. xHCI controller enabling and rerouting should follow the steps in Auto, when previous boot routes ports to EHCI. Note: This is the recommended mode when BIOS has xHCI pre-boot support.</p> <p><i>Enabled</i> All shared ports are eventually routed to the xHCI controller during the BIOS boot process. If BIOS does not have pre-boot support for the xHCI controller, it should initially route the sharable ports to the EHCI controller and then prior to OS boot it should route the ports to xHCI controller. Note: OS has to provide support for the xHCI controller in this mode. If the OS does not provide support, all sharable ports won't work.</p>

	<i>Disabled</i> <i>Manual</i>	The USB 3.0 ports are routed to the EHCI controller and the xHCI controller is turned off. All USB 3.0 devices function as High Speed devices regardless of xHCI software support or availability. Allows you to determine whether to rout the USB 3.0 ports to the xHCI or EHCI controller before booting to OS, and also provides you with options to manually rout each USB 3.0/2.0 port to xHCI or EHCI.
BTCG	<i>Enabled</i> <i>Disabled</i>	Allows you to enable or disable USB related trunk clock gating (BTCG).
EHCI1	<i>Enabled</i> <i>Disabled</i>	The USB Enhanced Controller Interface (EHCI) is the USB2.0 Controller. EHCI #1 controls Port 0 to 7.
EHC2	<i>Enabled</i> <i>Disabled</i>	The USB Enhanced Controller Interface (EHCI) is the USB2.0 Controller. EHCI #1 controls Port 8 to 13.
USB Ports Per-Port Disable Control	<i>Enabled</i> <i>Disabled</i>	This option allows enabling and disabling of the individual USB ports 0 to 14. Consult your specific hardware on what USB ports are available for your system.

2.3.1.3 PCH Azalia Configuration

Fig. 2.3.1.3.a PCH Azalia Configuration

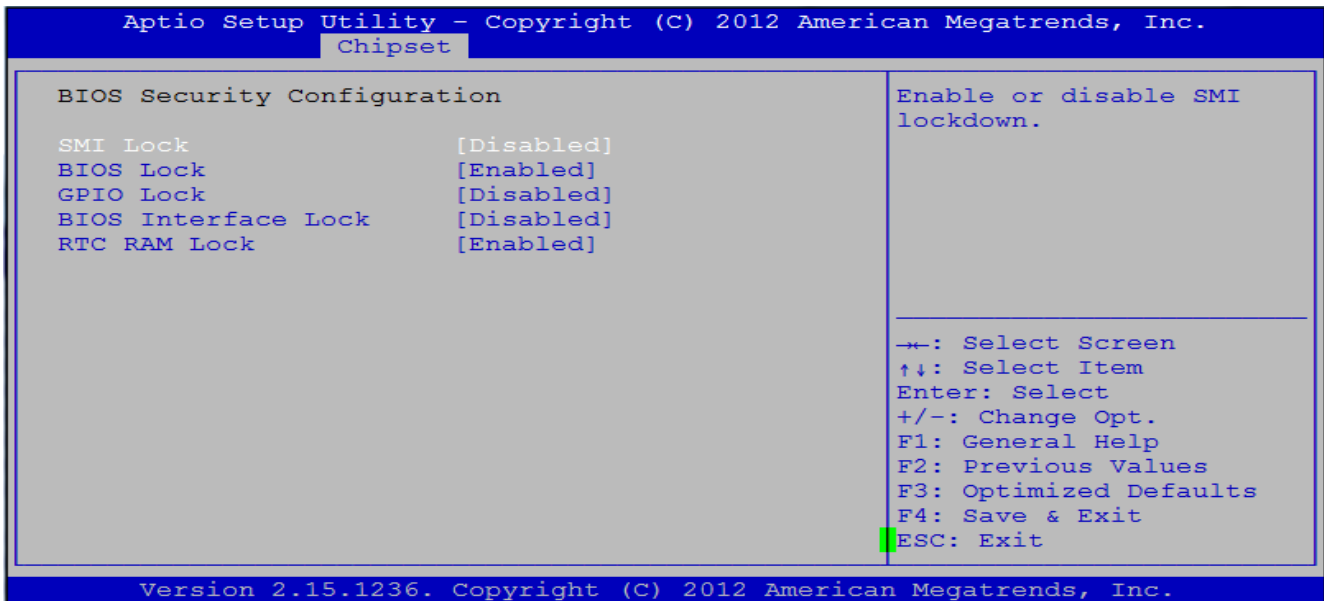


This option allows the user to view and change the Azalia Configuration. Azalia is the on-board audio controller.

Feature	Options	Description
Azalia	<i>Disabled</i> <i>Enabled</i> <i>Auto</i>	This item controls detection of the Azalia device. Azalia will be unconditionally disabled. Azalia will be unconditionally Enabled. Azalia will be enabled if present, disabled otherwise.
Azalia Docking Support	<i>Enabled</i> <i>Disabled</i>	Enable or disable Azalia Docking Support of Audio Controller.
Azalia PME	<i>Disabled</i> <i>Enabled</i>	Enable or disable Power Management Capability of Audio Controller.

2.3.1.4 BIOS Security Configuration

Fig. 2.3.1.4.a BIOS Security Configuration



The BIOS Security Configuration are the controls related to the security of the BIOS, including lockdown of SMI operation, GPIO settings, BIOS chip write access, and others.

Feature	Options	Description
SMI Lock	<i>Enabled</i> <i>Disabled</i>	Intel strongly recommends that SMI_LOCK be enabled in BIOS. This setting, when enabled, prevents writes to the Global SMI Enable bit. Enabling this bit mitigates malicious software attempts to gain system management mode privileges.
BIOS Lock	<i>Enabled</i> <i>Disabled</i>	When enabled, causes the chipset to block all access to the BIOS flash part unless they come through an SMI handler.
GPIO Lock	<i>Enabled</i> <i>Disabled</i>	When enabled, causes chipset to block attempts to change GPIO-related registers unless they come through an SMI handler.
BIOS Interface Lock	<i>Enabled</i> <i>Disabled</i>	When enabled, this bit mitigates malicious software attempts to replace the system BIOS option ROM with its own code.
RTC RAM Lock	<i>Enabled</i> <i>Disabled</i>	When enabled, this feature blocks writes to upper and lower CMOS RAM ranges, up until the next system reset.

2.3.2 System Agent Configuration

Fig. 2.3.2.a System Agent Configuration (Screen 1 of 2)

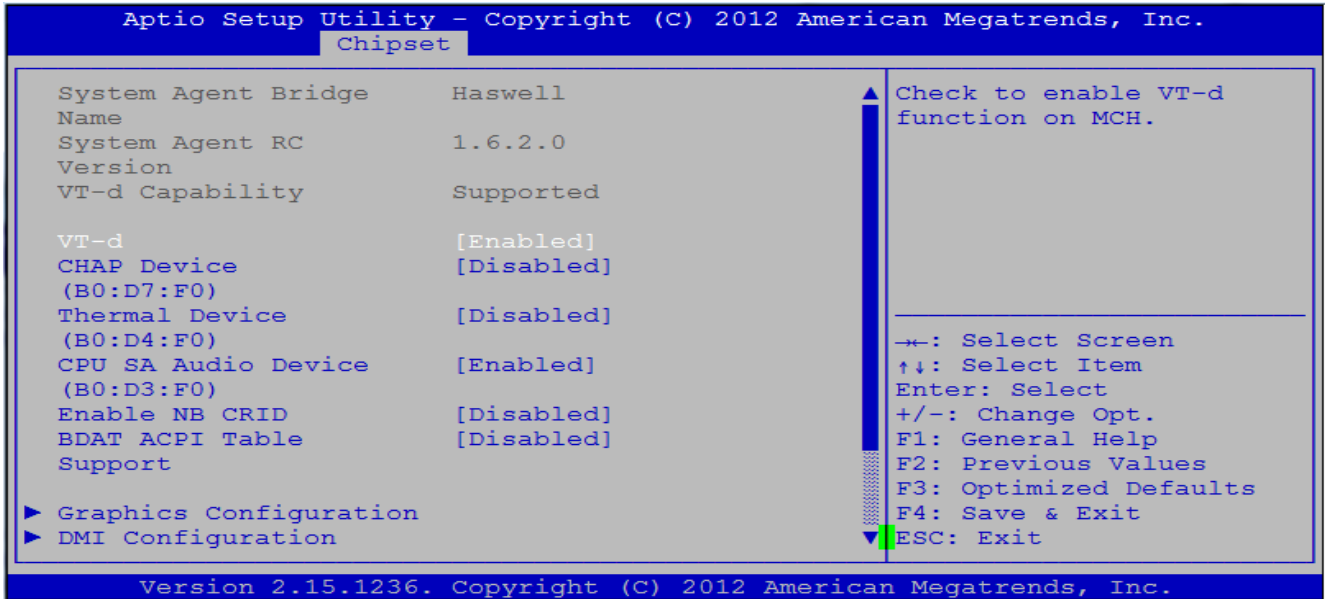
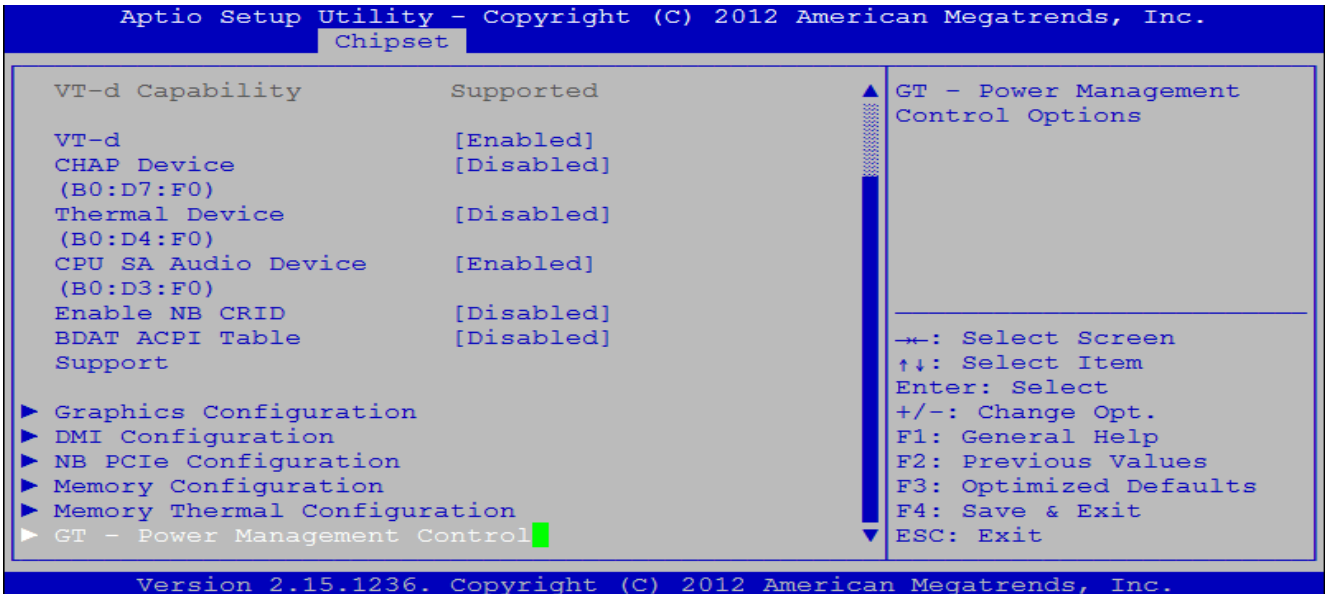


Fig. 2.3.2.b System Agent Configuration (Screen 2 of 2)

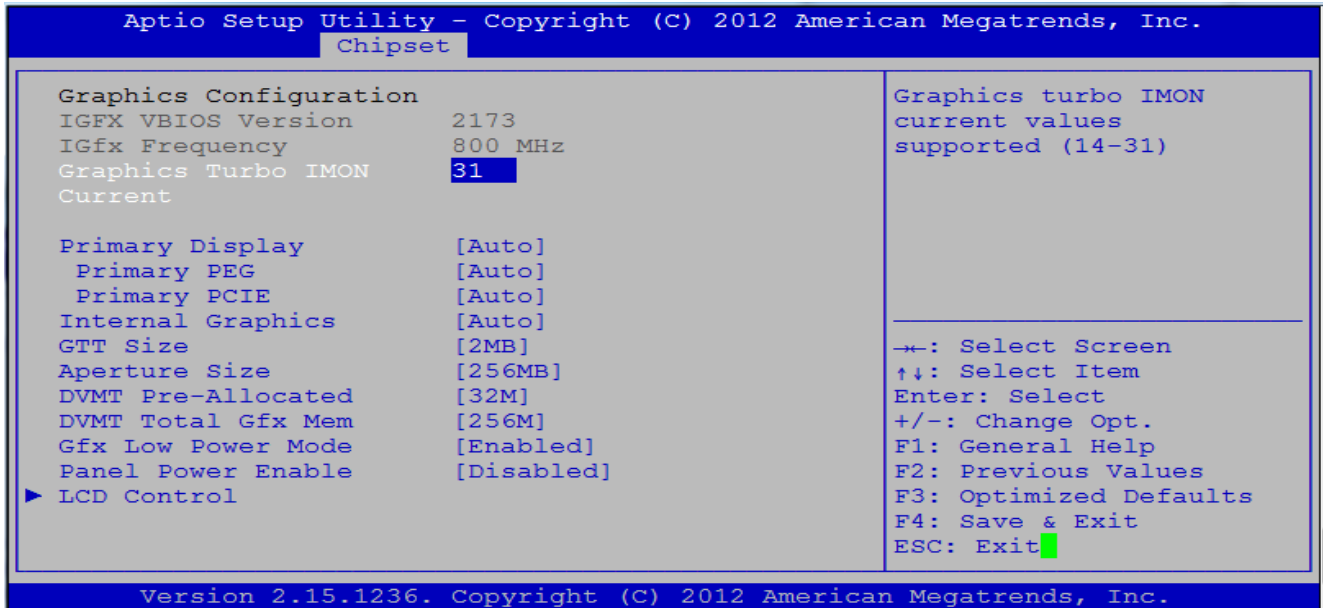


Feature	Options	Description
VT-d		Virtualization Technology for Directed I/O. Using this specific type of VT, users and/or administrators can: a) easily assign I/O devices to VMs, b) easily translate addresses in device DMA data transfers, and c) isolate the different VM's device interrupts from each other, and d) facilitate better I/O, DMA, and interrupt error reporting when using VT.

CHAP Device		Challenge Handshake Authentication Protocol. A CHAP device uses the CHAP protocol to validate the identity of servers and/or remote clients. Enabling this feature enables this device to authenticate or be authenticated using the CHAP protocol.
Thermal Device		Controls the chipset System Agent Thermal Device (Device 4).
CPU SA Audio Device		Enable or disable the System Agent audio device.
Enable NB CRID		Northbridge Compatible Revision ID (NB CRID), when enabled, makes it easy for the BIOS to load OS drivers that are optimized for a previous revision of the silicon instead of the current revision. This is enabled in order to minimize driver updates to the OS image for minor silicon optimizations.
BDAT ACPI Table Support		Disabled by default. This is a bios data table defined by Intel. Usually used for diagnostic purposes along with RMT support.

2.3.2.1 Graphics Configuration

Fig. 2.3.2.1.a Graphics Configuration

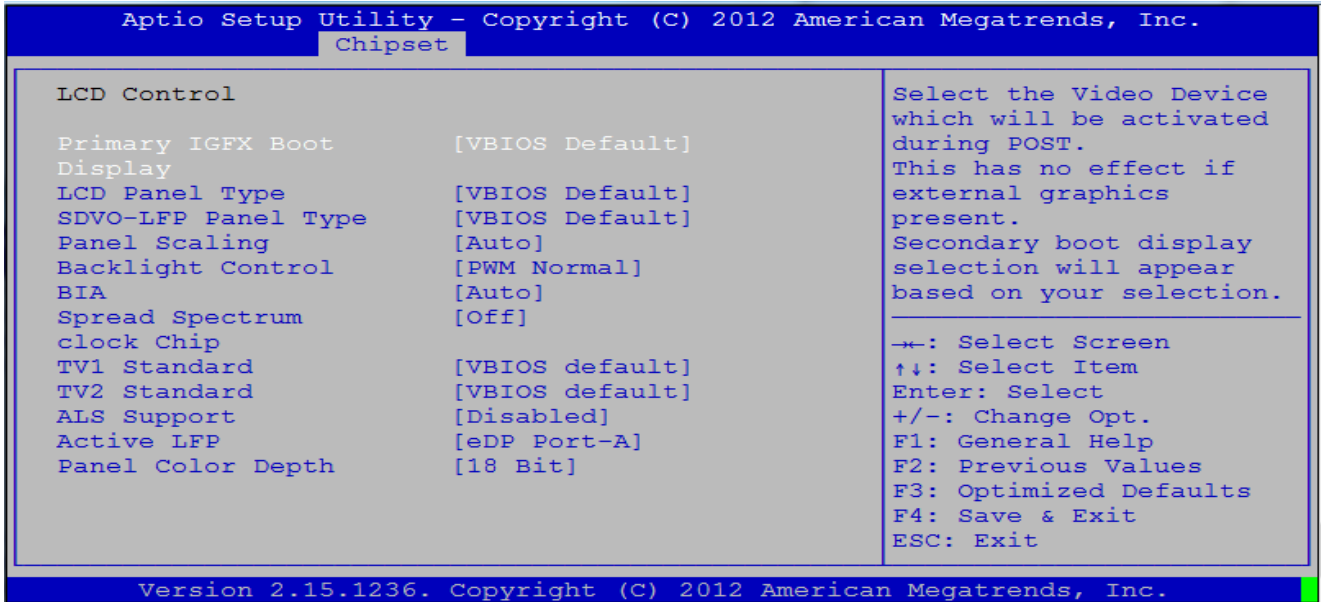


This option allows the user to view and configure the Graphics Configuration parameters

Feature	Options	Description
IGFX VBIOS Version		Displays the Intel Internal Graphics (IGFx) Video BIOS Version.
IGFX Frequency	<i>Enabled</i> <i>Disabled</i>	Displays the Internal Graphics (IGFx) card frequency in MHz.
Graphics Turbo IMON Current	<i>14-31</i>	Graphics turbo IMON current values supported (14-31)
Primary Display	<i>Auto</i> <i>IGFX</i> <i>PEG</i> <i>PCI</i> <i>SG</i>	Select which Graphics device should be the Primary Display. Auto Selection Internal Graphics Card PEG Port Graphics Card PCI Graphics Card Switchable Graphics (Gfx)
Primary PEG	<i>Auto</i> <i>PEG11</i> <i>PEG12</i>	Select which PEG Graphics should be the Primary graphics card.
Primary PCIE	<i>Auto</i> <i>PCIE1-7</i>	Select which PCIe Graphics should be the Primary graphics card.
Internal Graphics	<i>Auto</i> <i>Disabled</i> <i>Enabled</i>	Keep the Internal Graphics Display (IGD) enabled based on the setup options.
GTT Size	<i>1 MB</i> <i>2 MB</i>	Select the GTT Size. Options are 1MB or 2MB.
Aperture Size	<i>128 MB</i> <i>256 MB</i> <i>512 MB</i>	Select the Aperture Size.
DVMT Pre-Allocated	<i>0M</i> <i>32M</i> <i>64M</i> ... <i>512M</i>	Select Dynamic Video Memory Technology (DVMT) 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
DVMT Total Gfx Mem	<i>128M</i> <i>256M</i> <i>MAX</i>	Select Dynamic Video Memory Technology (DVMT) 5.0 Total Graphic Memory size used by the Internal Graphics Device.
Gfx Low Power Mode	<i>Enabled</i> <i>Disabled</i>	This option is applicable for SFF only.
Panel Power Enable	<i>Enabled</i> <i>Disabled</i>	This option allows enabling or disabling the forcing of the Panel Power in the BIOS.

2.3.2.1.1 LCD Control Configuration

Fig. 2.3.2.1.1.a LCD Control Configuration



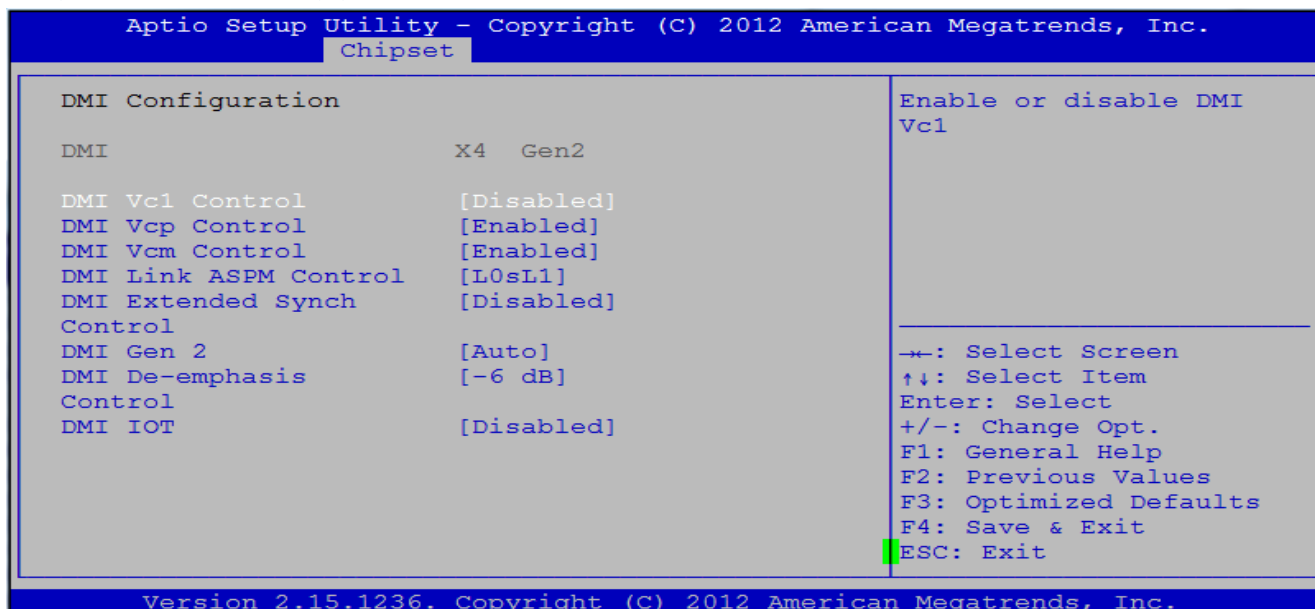
This option allows the user to view and configure the LCD Control parameters.

Features	Options	Description
Primacy IGFX Boot Display	<i>VBIOS Default</i> <i>CRT</i> <i>EFP</i> <i>LFP</i> <i>EFP3</i> <i>EFP2</i> <i>LFP2</i>	Select the video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display.
LCD Panel Type	<i>VBIOS Default</i> <i>640x480</i> ... <i>2048x1536</i>	Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.
SDVO-LFP Panel Type	<i>VBIOS Default</i> <i>1024x768</i> <i>1280x1024</i> <i>1400x1050</i> <i>1600x1200</i>	Select the Serial Digital Video Out (SDVO) panel used by Internal Graphics Device by selecting the appropriate setup item.
Panel Scaling	<i>Auto</i> <i>Off</i> <i>Force Scaling</i>	Select the LCD panel scaling option used by the Internal Graphics Device.
Backlight Control	<i>PWM Inverted</i> <i>PWM Normal</i> <i>GMBus Inverted</i> <i>GMBus Normal</i>	Back Light Control Setting.

BIA	<i>Auto</i> <i>Disabled</i> <i>Level 1 to 5</i>	The Graphics and Memory Control Hub (GMCH) uses VBT Default. Disable Enable with Selected Aggressiveness Level.
Spread Spectrum Clock Chip	<i>Off</i> <i>Hardware</i> <i>Software</i>	Spread is disabled. Spread is controlled by chip. Spread is controlled by BIOS.
TV1 Standard	<i>VBIOS default</i> NTSC_ ... PAL_ ... SECAM_ ... HDTV_ ...	Select the ability to configure a TV Format.
TV2 Standard	<i>VBIOS default</i> NTSC_ ... PAL_ ... SECAM_ ... HDTV_ ...	Select the ability to configure a TV Minor Format.
ALS Support	<i>Enabled</i> <i>Disabled</i>	Ambient Light Sensor (ALS) Support is valid only for ACPI. Legacy = ALS Support through the IGD INT10 function, ACPI = ALS support through an ACPI ALS driver.
Active LFP	No LVDS Int-LVDS SDVO LVD <i>eDP Port-A</i> eDP Port-D	Select the Active LFP Configuration. VBIOS does not enable LVDS. VBIOS enables LVDS driver by Integrated encoder. VBIOS enables LVDS driver by SDVO encoder. LFP Driven by Int-DisplayPort encoder from Port-A. LFP Driven by Int-DisplayPort encoder from Port-D.
Panel Color Depth	<i>18 Bit</i> <i>24 Bit</i>	Select the LFP Panel Color Depth.

2.3.2.2 DMI Configuration

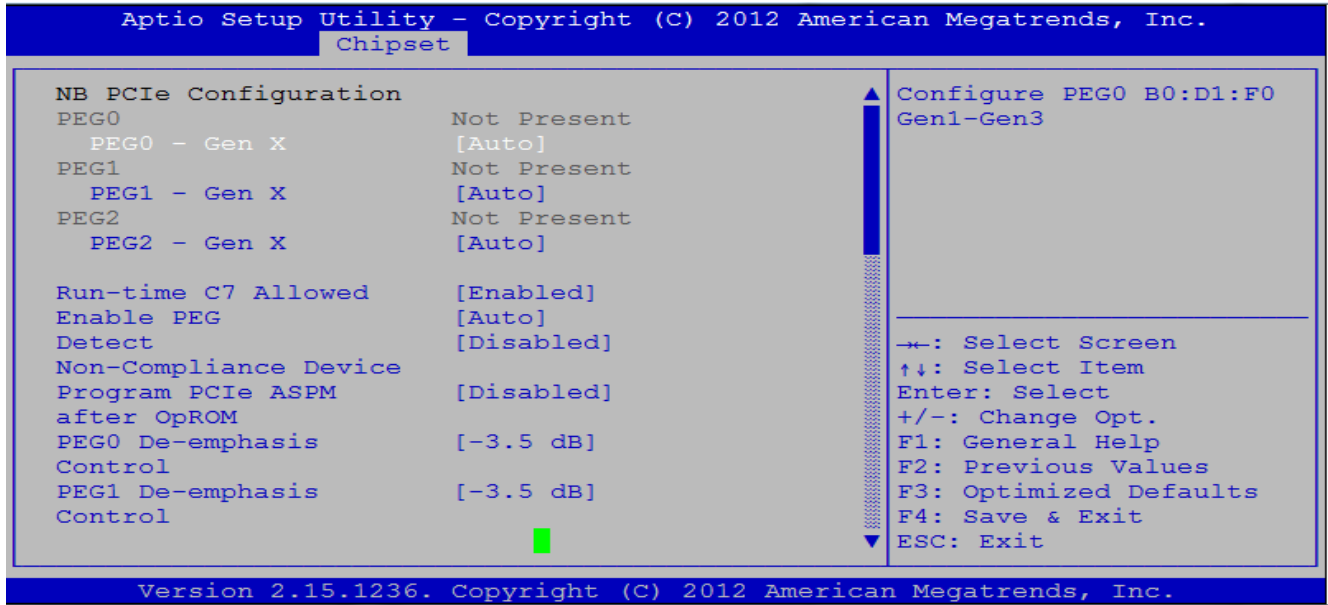
Fig. 2.3.2.2.a DMI Configuration



Feature	Options	Description
DMI Vc1 Control		Enables or disables DMI Virtual Channel 1. Controls the resources associated with PCI Express Virtual Channel 1 on PCH.
DMI Vcp Control		Virtual Channel (Private). This feature assigns a private ID to a given VC, and once assigned to a VC it cannot be altered.
DMI Vcm Control		Enables or disables DMI Virtual Channel Memory (the bus technology between the CPU and RAM).
DMI Link ASPM Control		DMI Active State Power Management (ASPM), when enabled, allows the DMI connection to the PCH chipset to enter a low-power state in order to reduce power consumption.
DMI Extended Sync Control		Disabled by default. DMI Extended sync is only to be used in a debug or testing environment and can cause lockups when Enabled with L0s.
DMI Gen 2		Auto by default, so actual default is a function of hardware. Serves as a chip to chip interface between the CPU and the PCH. The setting determines whether the interface is allowed to operate at faster Gen 2 speeds.
DMI De-emphasis Control		6DB by default. Allows user to alter the de-emphasis setting of the chipset for the DMI electrical interface.
DMI IOT		Disabled by default. Appears to alter chipset in some way beneficial to IoT usage. Check with Intel for details.

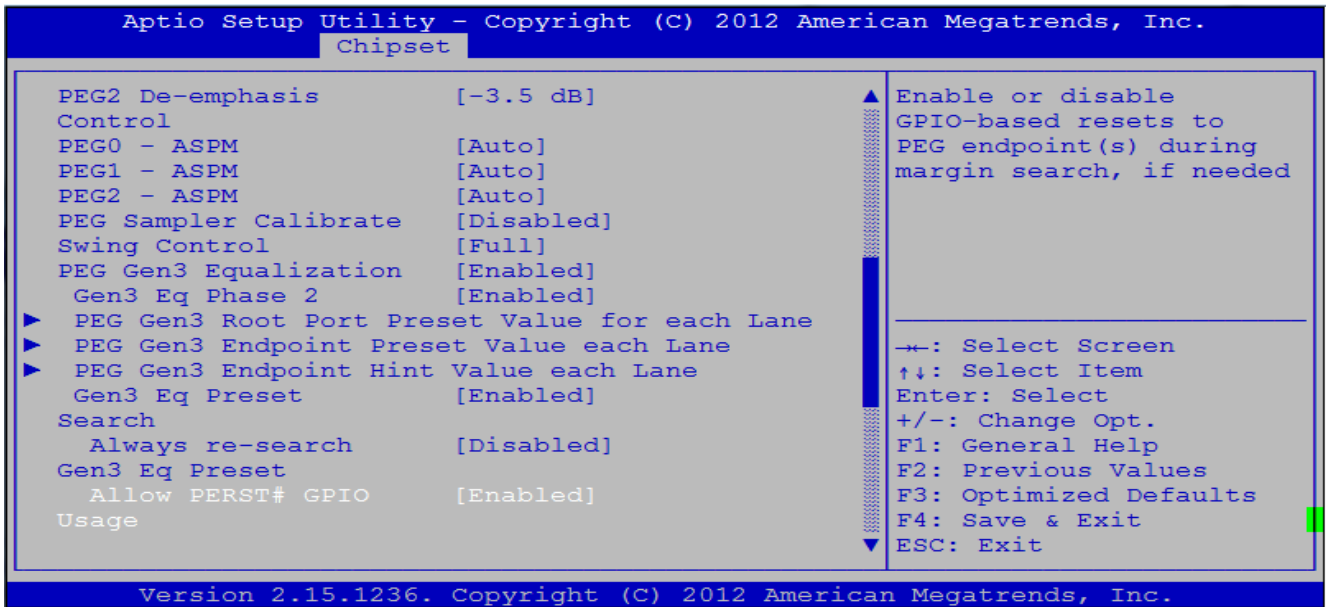
2.3.2.3 NB PCIe Configuration

Fig. 2.3.2.3.a NB PCIe Configuration (Screen 1 of 3)



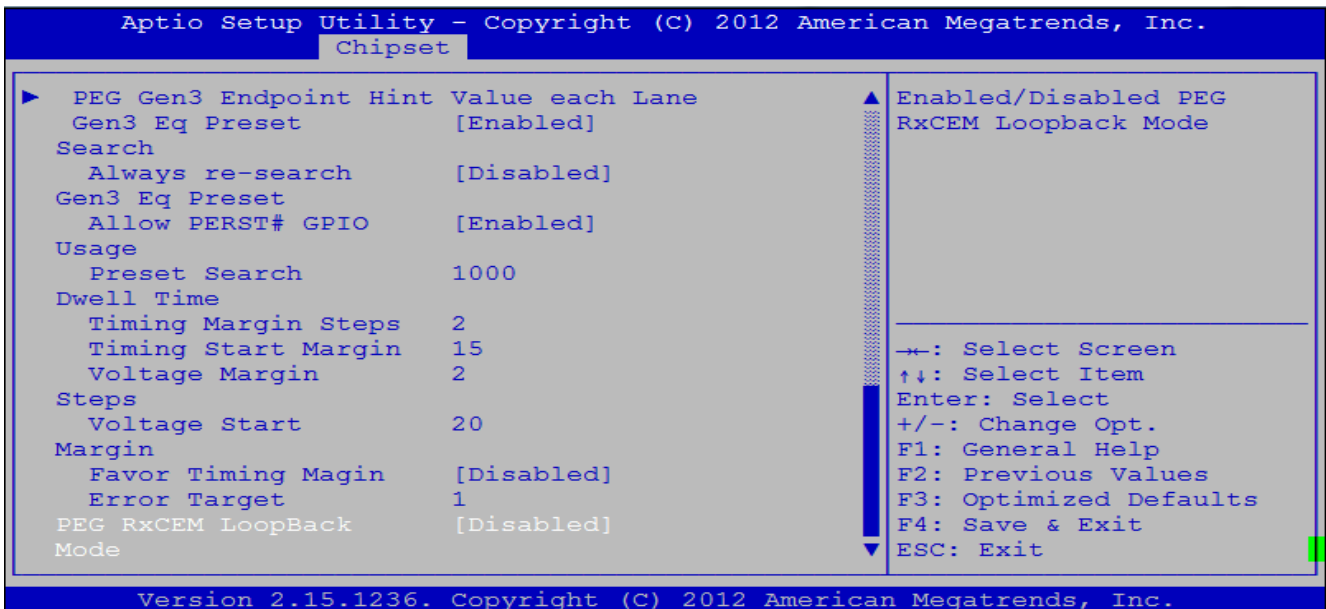
Feature	Options	Description
PEG0 thru PEG2 – Gen X		Auto for default, meaning actual default driven by hardware capabilities. This option determines the PCIe Generation speed that the slot should operate at.
Runtime C7 Allowed		Enabled by default. Determines whether information needed for the OS to be aware of and use the C7 state is made visible to the OS.
Enable PEG		Auto by default. Determines whether the PEG slot is active or not.
Detect Non-Compliance Device		Disabled by default. Detects whether the device installed in the slot is compliant or not.
Program PCIe ASPM after OpROM		Disabled by default. User control to allow selecting whether ASPM would be enabled before or after the OpROMs have been executed.
PEG De-emphasis Control		Chipset feature to allow user to control the electrical characteristics of the PEG port.

Fig. 2.3.2.3.b NB PCIe Configuration (Screen 2 of 3)



Feature	Options	Description
PEG ASPM		Active State Power Management control for user to disable if needed.
PEG Sampler Calibrate		Default is disabled. Additional calibration action for the PEG slot PCIe lanes.
Swing Control		Default is full. Control allows user to setup the MCH for either half or full swing control.
PEG Gen3 Equalization		Default is enabled. Control over the equalization process to ensure PCIe Gen3 links are working at the optimal speed.

Fig. 2.3.2.3.c NB PCIe Configuration (Screen 3 of 3)



Feature	Options	Description
PEG RxCeM LoopBack Mode		Disabled by default. Check with Intel about hardware implications.

2.3.2.3.1 PEG Gen3 Root Port Preset Value

Fig. 2.3.2.3.1.a PEG Gen3 Root Port Preset Value (Screen 1 of 2)

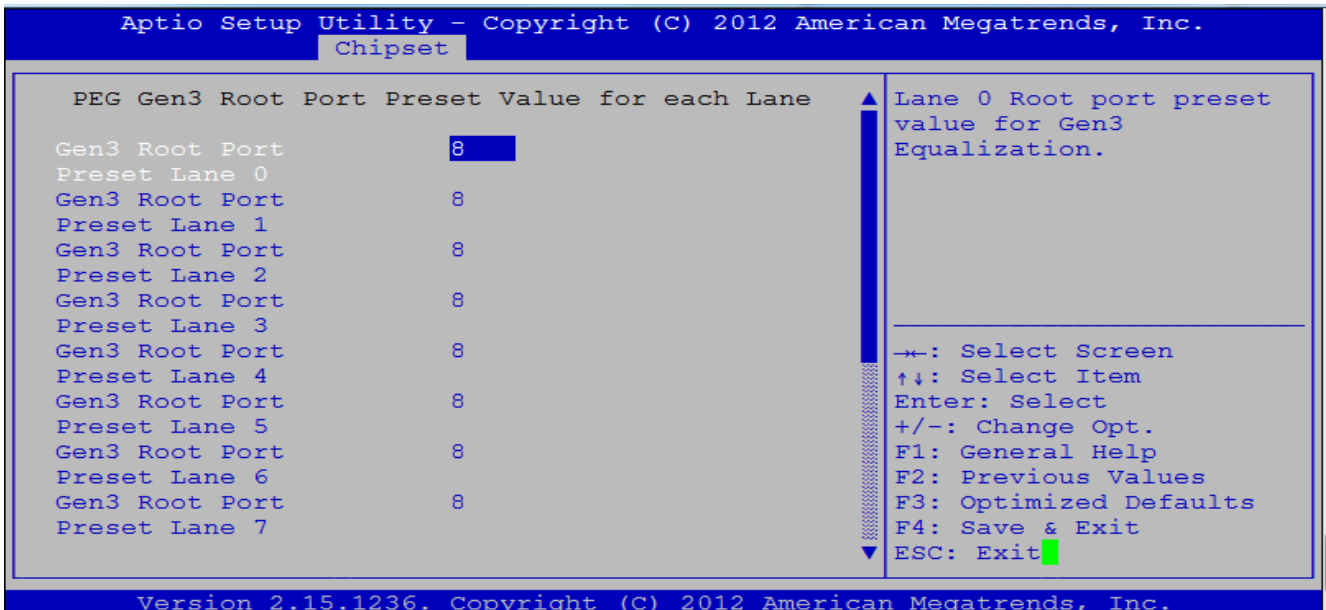
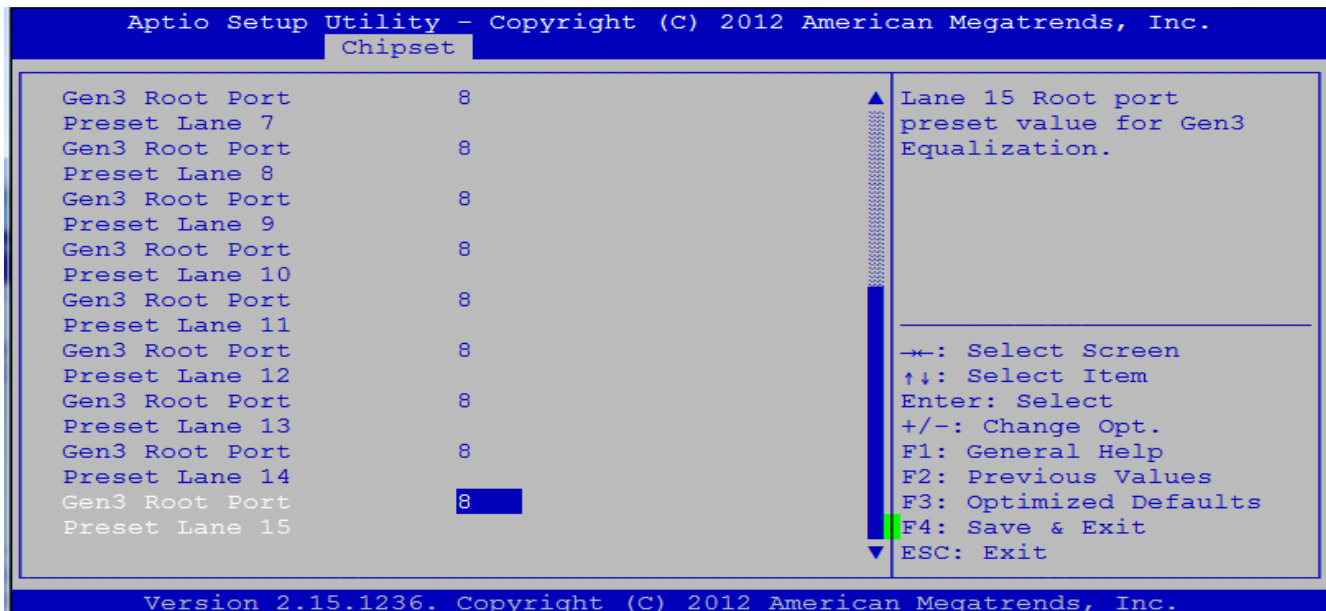
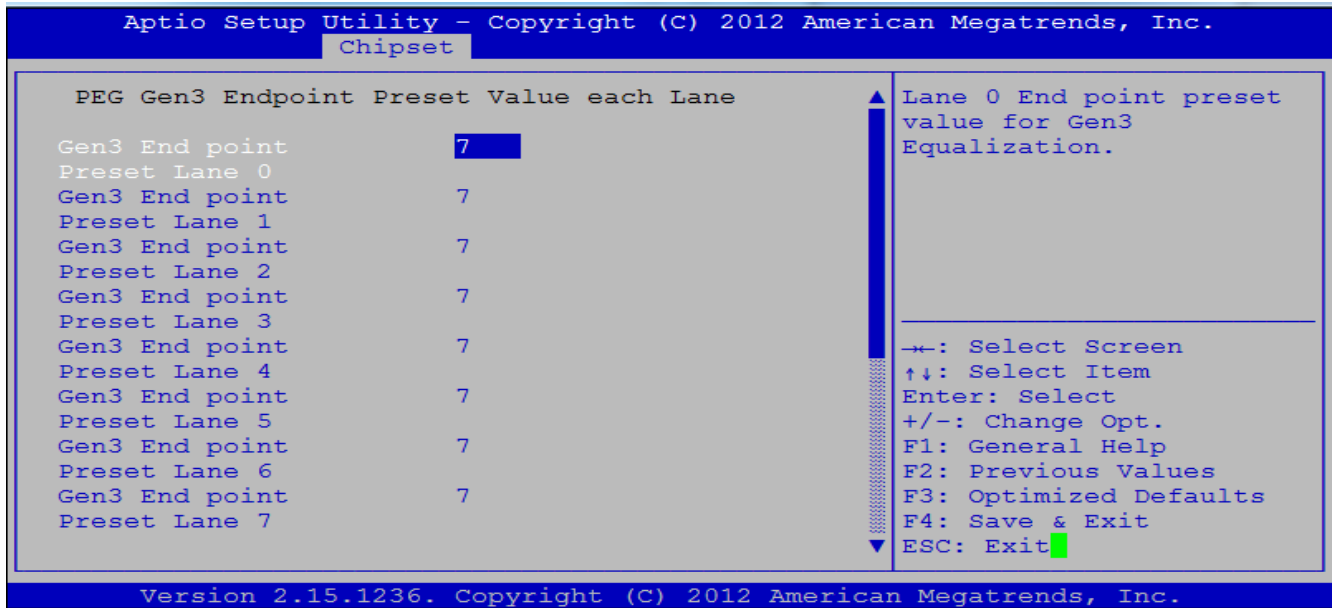


Fig. 2.3.2.3.1.b PEG Gen3 Root Port Preset Value (Screen 2 of 2)



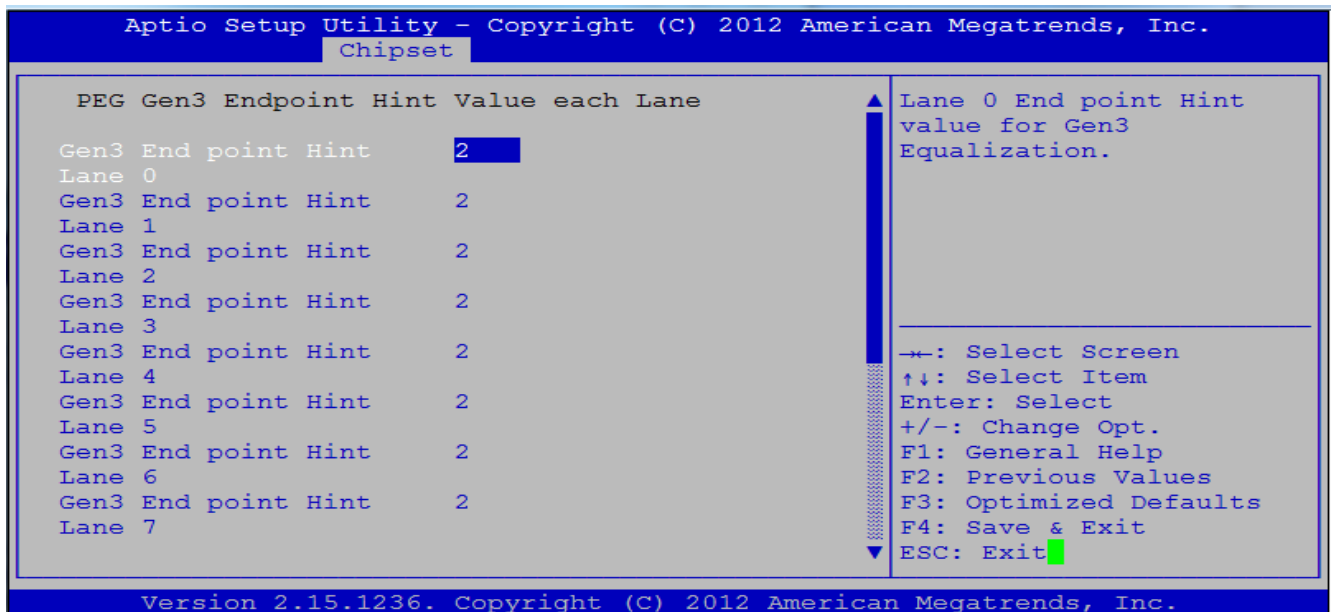
2.3.2.3.2 PEG Gen3 Endpoint Preset Value

Fig. 2.3.2.3.2.a PEG Gen3 Endpoint Preset Value



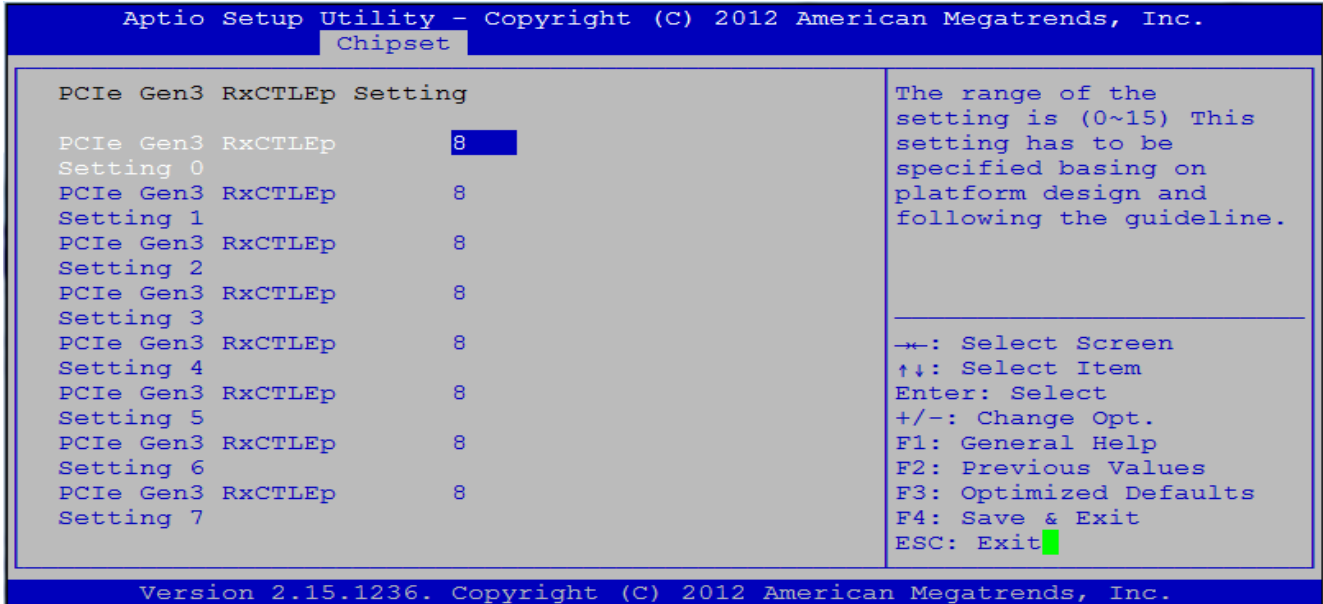
2.3.2.3.3 PEG Gen3 Endpoint Hint Value

Fig. 2.3.2.3.3.a PEG Gen3 Endpoint Hint Value



2.3.2.3.4 PCIe Gen3 RxCTLEp Setting

Fig. 2.3.2.3.4.a PCIe Gen3 RxCTLEp Setting



Feature	Options	Description
PCIe Gen3 RxCTLEp Setting		Default is CRB value. This is a tuning parameter related to trace lengths of the particular board. Should be set based on board design and Intel guidelines.

2.3.2.4 Memory Configuration

Fig. 2.3.2.4.a Memory Configuration (Screen 1 of 3)

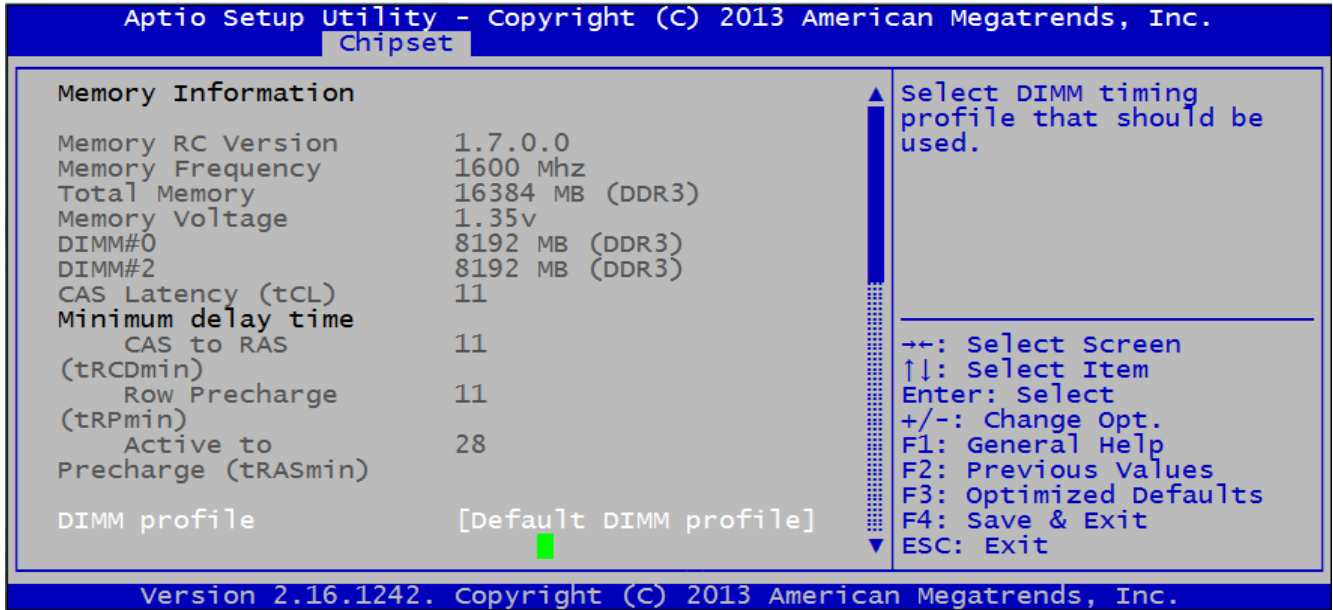
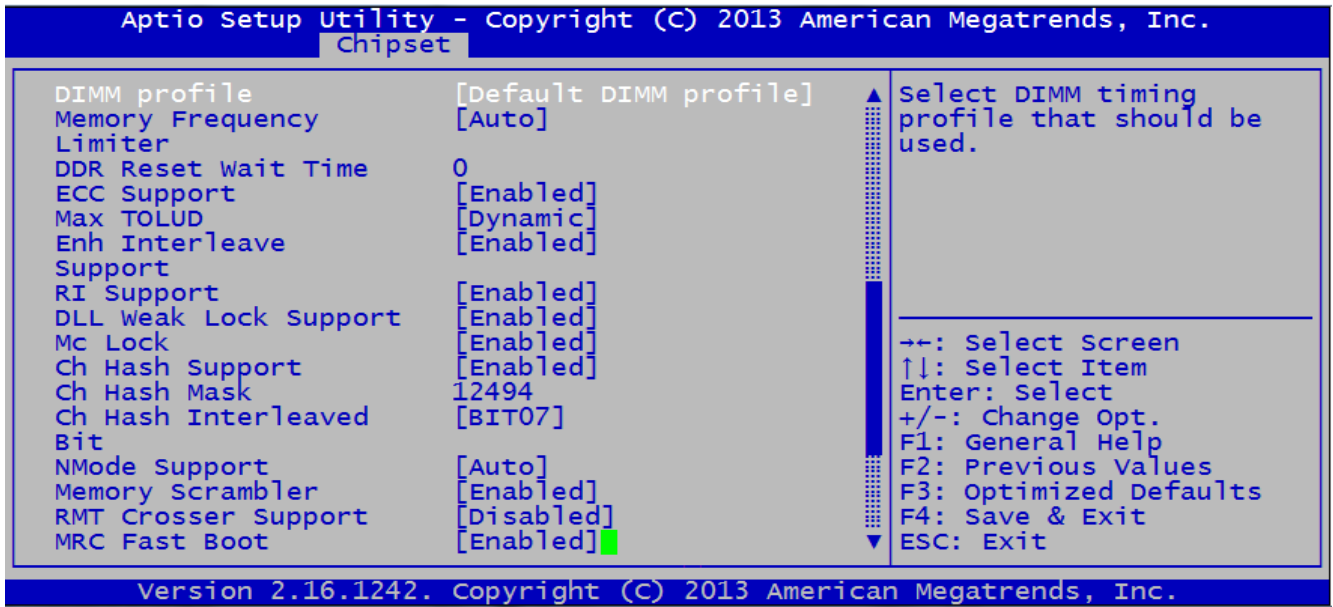


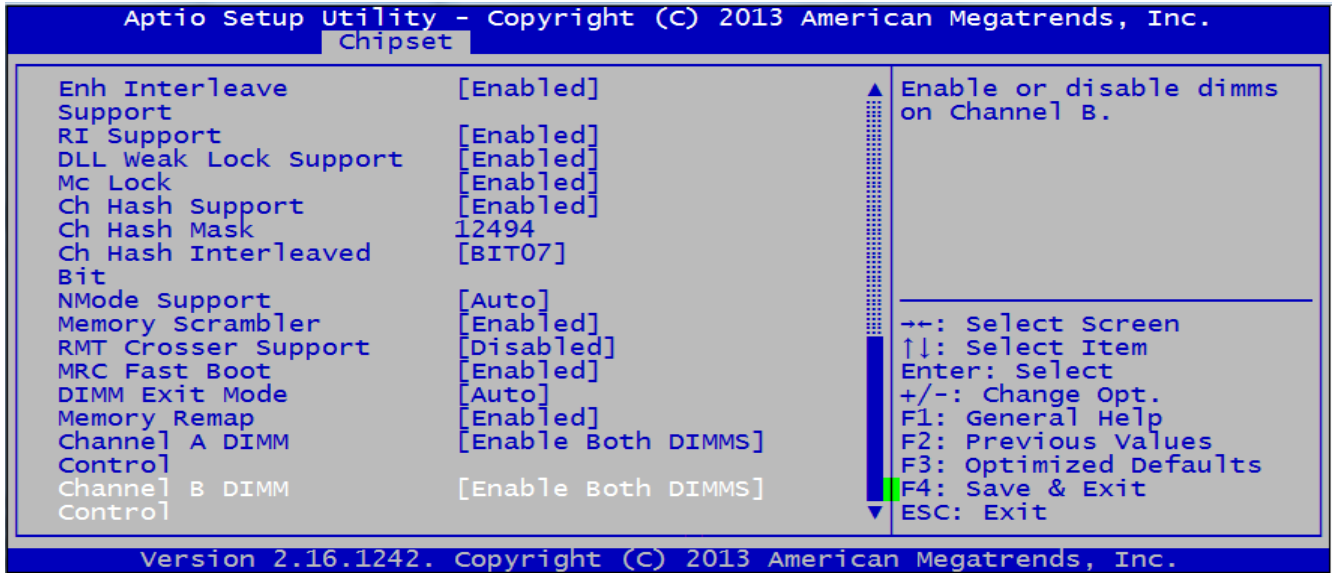
Fig. 2.3.2.4.b Memory Configuration (Screen 2 of 3)



Feature	Options	Description
DIMM Profile		Default is the DIMM SPD profile. A mechanism to allow the user to change the memory timing parameter profiles to XMP (if supported by DIMM) or even a custom profile.
Memory Frequency Limiter		Auto is default. A control to allow the user to limit the frequency memory runs at. Auto should result in published memory frequency – if the MRC supports that frequency on that DIMM.

DDR Reset Wait Time		Default is 2,000,000 nS. A wait time for DDR voltage changes after a reset.
ECC Support		Enabled by default. Allows user to disable ECC operation when ECC DRAMs are installed if desired.
Max TOLUD		Set for Dynamic by default. Feature to specify the Top Of Low User Dram. This is the point where DRAM ends and PCI MMIO begins below 4GB in the memory map. Dynamic means the bios figures out what PCI resources are needed in the current configuration then sets the top of DRAM accordingly. If re-mapping is enabled the DRAM between this point and 4GB will be moved to available space above 4GB in the address map.
Enh Interleave Support		Enabled by default. Control for the Enhanced Interleaving feature of the memory controller.
RI Support		Enabled by default. Control for the Rank Interleaving feature of the memory controller.
DLL Weak Lock Support		Enabled by default. Control over delay locked loop feature of the memory signal timings.
Mc Lock		Default is enabled. Enables chipset feature to lock registers related to memory configuration so that they cannot be changed at runtime.
Ch Hash Support		Enabled by default . Checksum and data validity/integrity checks.
Ch Hash Mask		Set to 0x30CE by default. Checksum and data validity/integrity checks.
Ch Hash Interleaved Bit		Set to Bit7 by default. Checksum and data validity/integrity checks.
NMode Support		Auto by default. Can be 1N, 2N or Auto. Check with Intel about hardware implications.
Memory Scrambler		Enabled by default. Chipset feature to randomize memory usage somewhat to avoid potentially inducing unintended bit changes in adjacent cells. See also Row Hammer.
RMT Crosser Support		Disabled by default. Control of the Rank Margining Tool that can be used by hardware folks to ensure the memory trainings are optimum during development.
MRC Fast Boot		Enabled by default. Allows MRC to use ‘remembered’ training data to speed up MRC execution if nothing has changed related to memory.

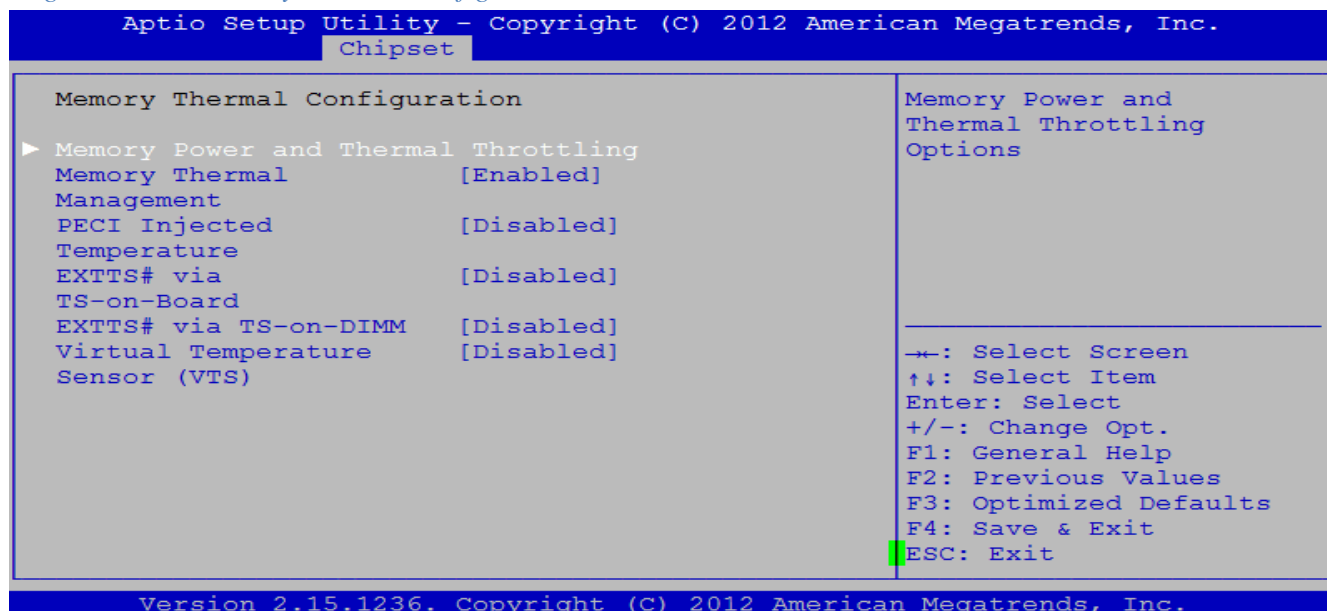
Fig. 2.3.2.4.c Memory Configuration (Screen 3 of 3)



Feature	Options	Description
DIMM Exit Mode		Auto by default. Slow exit mode saves more power than fast exit mode.
Memory Remap		Enabled by default. Control to determine whether DRAM memory displaced by the PCI/PCIe/MMIO region below 4GB in the address map should be remapped to appear above 4GB (e.g. a 1GB region for 32-bit PCI devices in a system with 8GB installed DRAM would result in the loss of 1GB of DRAM unless remapped to appear between 8GB and 9GB in the address map).
Channel A DIMM Control		Both DIMMs enabled by default. Allows either or both DIMMs on Channel A to be disabled.
Channel B DIMM Control		Both DIMMs enabled by default. Allows either or both DIMMs on Channel B to be disabled.
GDXC Support		Control for chipset feature Generic Debug eXternal Connection which allows for monitoring of traffic between IA cores and other signals with appropriate equipment.

2.3.2.5 Memory Thermal Configuration

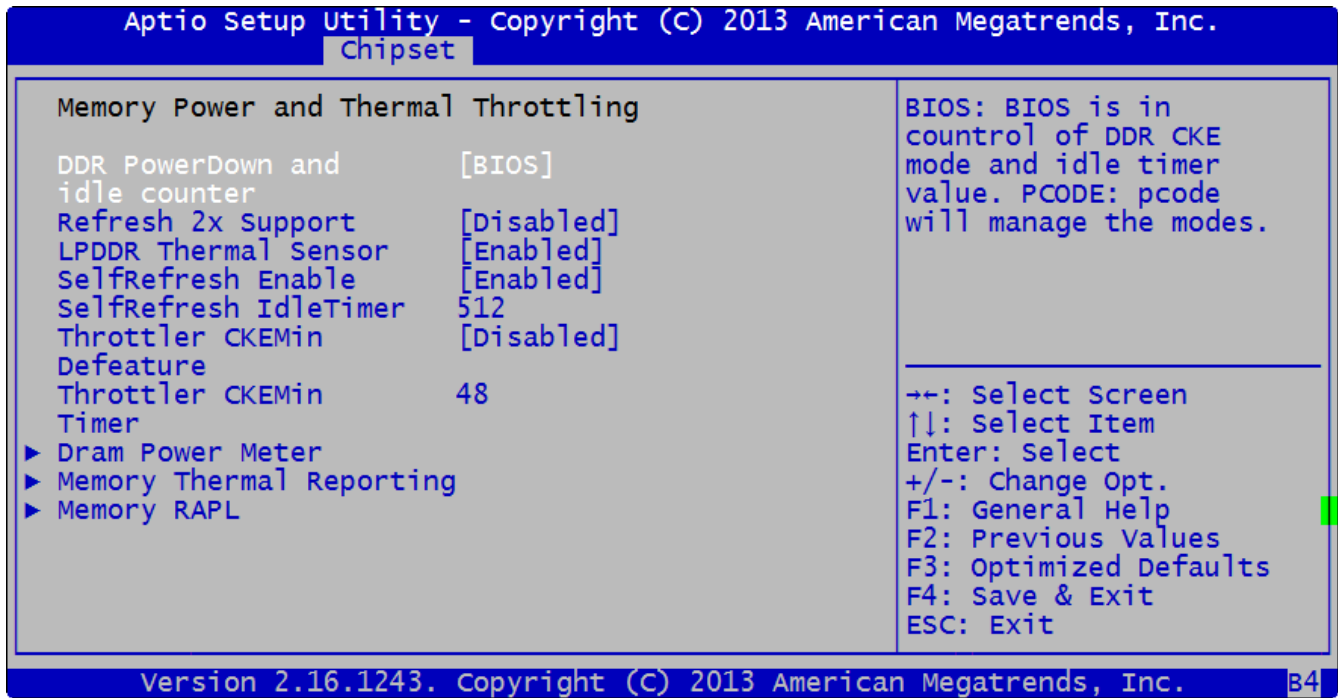
Fig. 2.3.2.5.a Memory Thermal Configuration



This option allows the user to view and change the Memory Thermal Configuration.

Feature	Options	Description
▶ Memory Power and Thermal Throttling		Memory Power and Thermal Throttling Options Menu
Memory Thermal	<i>Enabled</i> <i>Disabled</i>	Enable or disable Memory Thermal Management.
PECI Injected Temperature	<i>Disabled</i> <i>Enabled</i>	Enable or disable memory temperatures to be injected to the processor via the Platform Environment Control Interface (PECI).
EXTTS# via TS-on-Board	<i>Disabled</i> <i>Enabled</i>	Enable or disable routing Thermal Sensor-on-Board's ALERT# and THERM# to External Thermal Sensor (EXTTS#) pins on the Platform Control Hub (PCH).
EXTTS# via TS-on-DIMM	<i>Disabled</i> <i>Enabled</i>	Enable or disable routing Thermal Sensor-on-DIMM's ALERT# to External Thermal Sensor (EXTTS#) pins on the Platform Control Hub (PCH).
Virtual Temperature Sensor (VTS)	<i>Disabled</i> <i>Enabled</i>	Enable or disable Virtual Thermal Sensor (VTS).

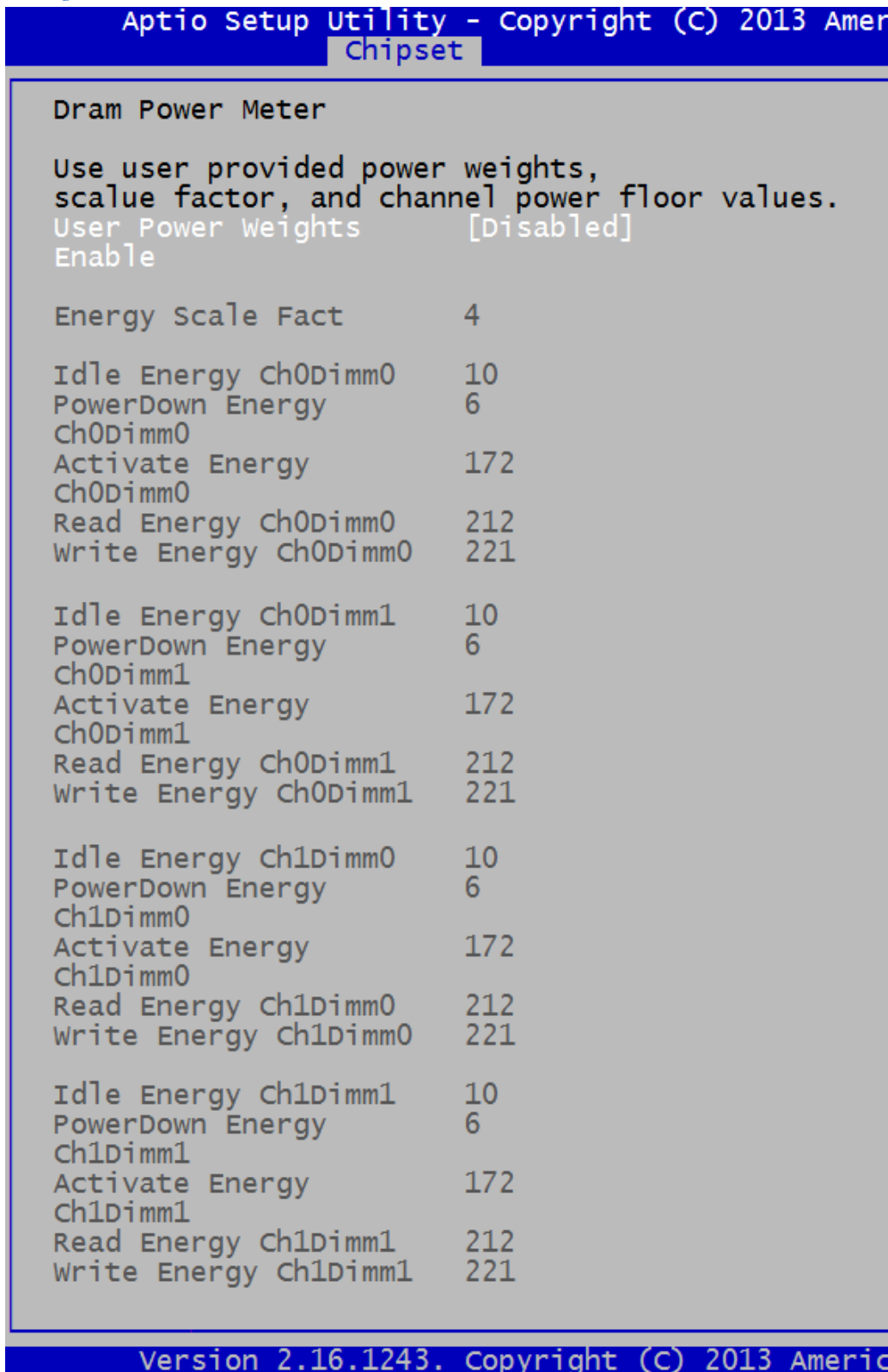
Fig. 2.3.2.5.1.a Memory Power and Thermal Throttling



This option allows the user to view and change the Memory Power and Thermal Throttling.

Feature	Options	Description
DDR PowerDown and Idle counter	<i>BIOS</i> <i>PCODE</i>	· BIOS is in control of Double Data Rate (DDR) Clock Enable (CKE) mode and idle timer value. · PCODE will manage the modes.
Refresh 2x Support	<i>Disabled</i> <i>Enabled</i>	Enable or disable Refresh 2x support.
LPDDR Thermal Sensor	<i>Enabled</i> <i>Disabled</i>	When enabled, MC uses MR4 to read LPDDR (Low Power Double Data Rate) thermal sensors.
SelfRefresh Enable	<i>Enabled</i> <i>Disabled</i>	Enable or disable SelfRefresh.
SelfRefresh IdleTimer	<i>512</i>	Range [64K-1;512] in DLCK800s.
Throttler CKEMin Defeature	<i>Disabled</i> <i>Enabled</i>	Enable or disable Throttler CKEMin Defeature.
Throttler CKEMin Timer	<i>512</i>	Range [64K-1;512] in DLCK800s.
▶ Dram Power Meter		Dram Power Meter Options Menu
▶ Memory Thermal Reporting		Memory Thermal Reporting Options Menu
▶ Memory RAPL		Memory RAPL Options Menu

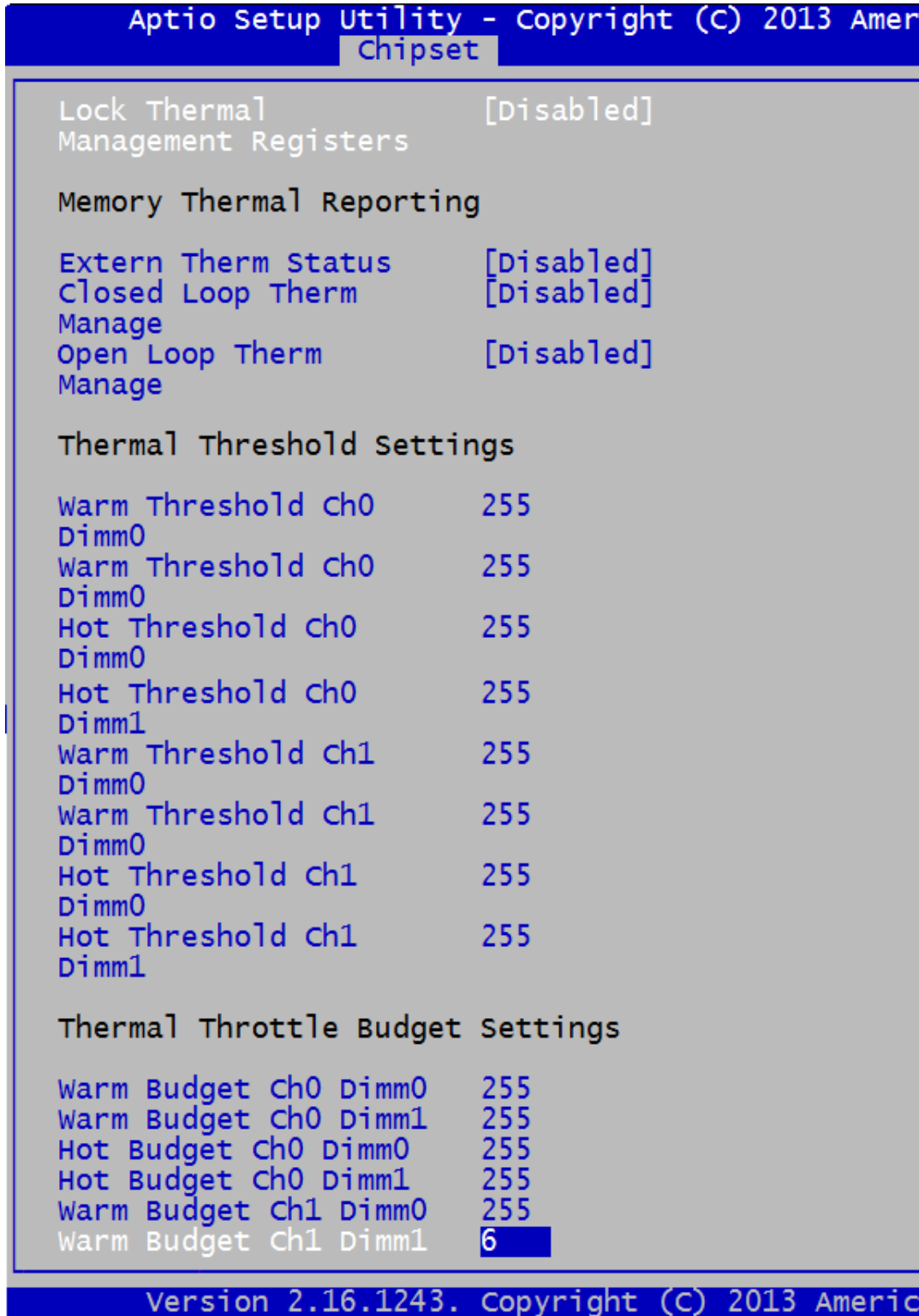
Fig. 2.3.2.5.1.1.a Dram Power Meter



This option allows the user to view and change the Dram Power Meter Configuration.

Feature	Options	Description
User Power Weights Enable	<i>Enabled</i> <i>Disabled</i>	· User provides power weights, scale factor, and channel power floor values are used. · BIOS sets power weights, scale factor, and channel power floor values based on DIMMs present in system.
Energy Scale Fact	<i>4</i>	Range [7;0] = [7.3;931.3] in pJ.
Idle Energy Ch0Dimm0	<i>10</i>	Idle Energy Consumed for 1 clk w/ dim idle/cke on, range[63;0].
PowerDown Energy Ch0Dimm0	<i>6</i>	PowerDown Energy Consumed for 1 clk w/ dim idle/cke off, range[63;0].
Activate Energy Ch0Dimm0	<i>172</i>	Activate Energy Contribution, range [255;0].
Read Energy Ch0Dimm0	<i>212</i>	Read Energy Contribution, range [255;0].
Write Energy Ch0Dimm0	<i>221</i>	Write Energy Contribution, range [255;0].
Idle Energy Ch0Dimm1	<i>10</i>	Idle Energy Consumed for 1 clk w/ dim idle/cke on, range[63;0].
PowerDown Energy Ch0Dimm1	<i>6</i>	PowerDown Energy Consumed for 1 clk w/ dim idle/cke off, range[63;0].
Activate Energy Ch0Dimm1	<i>172</i>	Activate Energy Contribution, range [255;0].
Read Energy Ch0Dimm1	<i>212</i>	Read Energy Contribution, range [255;0].
Write Energy Ch0Dimm1	<i>221</i>	Write Energy Contribution, range [255;0].
Idle Energy Ch1Dimm0	<i>10</i>	Idle Energy Consumed for 1 clk w/ dim idle/cke on, range[63;0].
PowerDown Energy Ch1Dimm0	<i>6</i>	PowerDown Energy Consumed for 1 clk w/ dim idle/cke off, range[63;0].
Activate Energy Ch1Dimm0	<i>172</i>	Activate Energy Contribution, range [255;0].
Read Energy Ch1Dimm0	<i>212</i>	Read Energy Contribution, range [255;0].
Write Energy Ch1Dimm0	<i>221</i>	Write Energy Contribution, range [255;0].
Idle Energy Ch1Dimm1	<i>10</i>	Idle Energy Consumed for 1 clk w/ dim idle/cke on, range[63;0].
PowerDown Energy Ch1Dimm1	<i>6</i>	PowerDown Energy Consumed for 1 clk w/ dim idle/cke off, range[63;0].
Activate Energy Ch1Dimm1	<i>172</i>	Activate Energy Contribution, range [255;0].
Read Energy Ch1Dimm1	<i>212</i>	Read Energy Contribution, range [255;0].
Write Energy Ch1Dimm1	<i>221</i>	Write Energy Contribution, range [255;0].

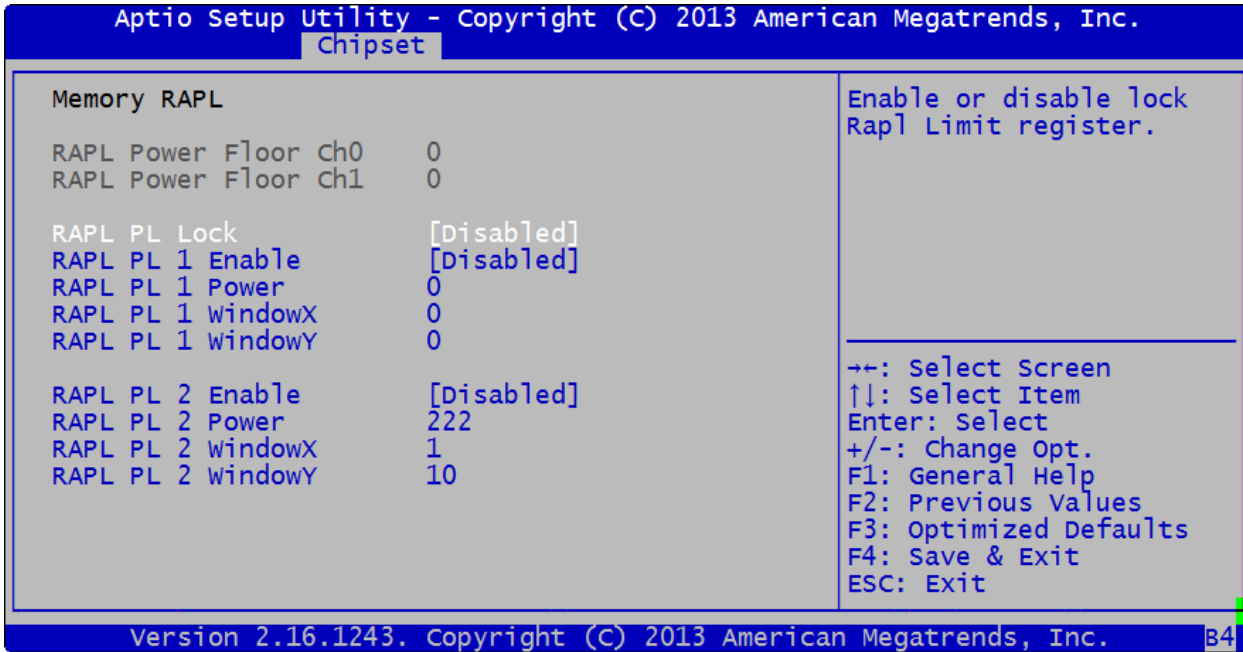
Fig. 2.3.2.5.1.2.a Memory Thermal Reporting



This option allows the user to view and change the Memory Thermal Reporting Configuration.

Feature	Options	Description
Lock Thermal Management Registers	<i>Enabled</i> <i>Disabled</i>	Enable or disable Lock several PCU registers related to DDR power Thermal Management.
Memory Thermal Reporting		
Extern Therm Status	<i>Enabled</i> <i>Disabled</i>	<ul style="list-style-type: none"> · The value from External thermal Sensors (EXTTS) are used. · Pcode ignores the EXTTS.
Closed Loop Therm Manage	<i>Enabled</i> <i>Disabled</i>	<ul style="list-style-type: none"> · CLTM pcode algorithm will be used. · CLTM pcode algorithm will be disabled. Note: CLTM will precede OLTM.
Open Loop Therm Manage	<i>Enabled</i> <i>Disabled</i>	<ul style="list-style-type: none"> · OLTM pcode algorithm will be used. · OLTM pcode algorithm will be disabled. Note: CLTM will precede OLTM.
Thermal Threshold Settings		
Warm Threshold Ch0 Dimm0	<i>255</i>	Range [255;0] = [0;31.875] in W, (255= 31.875W=Def)
Warm Threshold Ch0 Dimm0	<i>255</i>	Range [255;0] = [0;31.875] in W, (255= 31.875W=Def)
Warm Threshold Ch0 Dimm0	<i>255</i>	Range [255;0] = [0;31.875] in W, (255= 31.875W=Def)
Warm Threshold Ch0 Dimm1	<i>255</i>	Range [255;0] = [0;31.875] in W, (255= 31.875W=Def)
Warm Threshold Ch1 Dimm0	<i>255</i>	Range [255;0] = [0;31.875] in W, (255= 31.875W=Def)
Warm Threshold Ch1 Dimm0	<i>255</i>	Range [255;0] = [0;31.875] in W, (255= 31.875W=Def)
Warm Threshold Ch1 Dimm0	<i>255</i>	Range [255;0] = [0;31.875] in W, (255= 31.875W=Def)
Warm Threshold Ch1 Dimm1	<i>255</i>	Range [255;0] = [0;31.875] in W, (255= 31.875W=Def)
Thermal Throttle Budget Settings		
Warm Budget Ch0 Dimm0	<i>255</i>	Range [255;0] = [0;31.875] in W, (255= 31.875W=Def)
Warm Budget Ch0 Dimm1	<i>255</i>	Range [255;0] = [0;31.875] in W, (255= 31.875W=Def)
Hot Budget Ch0 Dimm0	<i>255</i>	Range [255;0] = [0;31.875] in W, (255= 31.875W=Def)
Hot Budget Ch0 Dimm1	<i>255</i>	Range [255;0] = [0;31.875] in W, (255= 31.875W=Def)
Warm Budget Ch1 Dimm0	<i>255</i>	Range [255;0] = [0;31.875] in W, (255= 31.875W=Def)
Warm Budget Ch1 Dimm1	<i>255</i>	Range [255;0] = [0;31.875] in W, (255= 31.875W=Def)
Hot Budget Ch1 Dimm0	<i>255</i>	Range [255;0] = [0;31.875] in W, (255= 31.875W=Def)
Hot Budget Ch1 Dimm1	<i>255</i>	Range [255;0] = [0;31.875] in W, (255= 31.875W=Def)

Fig. 2.3.2.5.1.3.a Memory RAPL

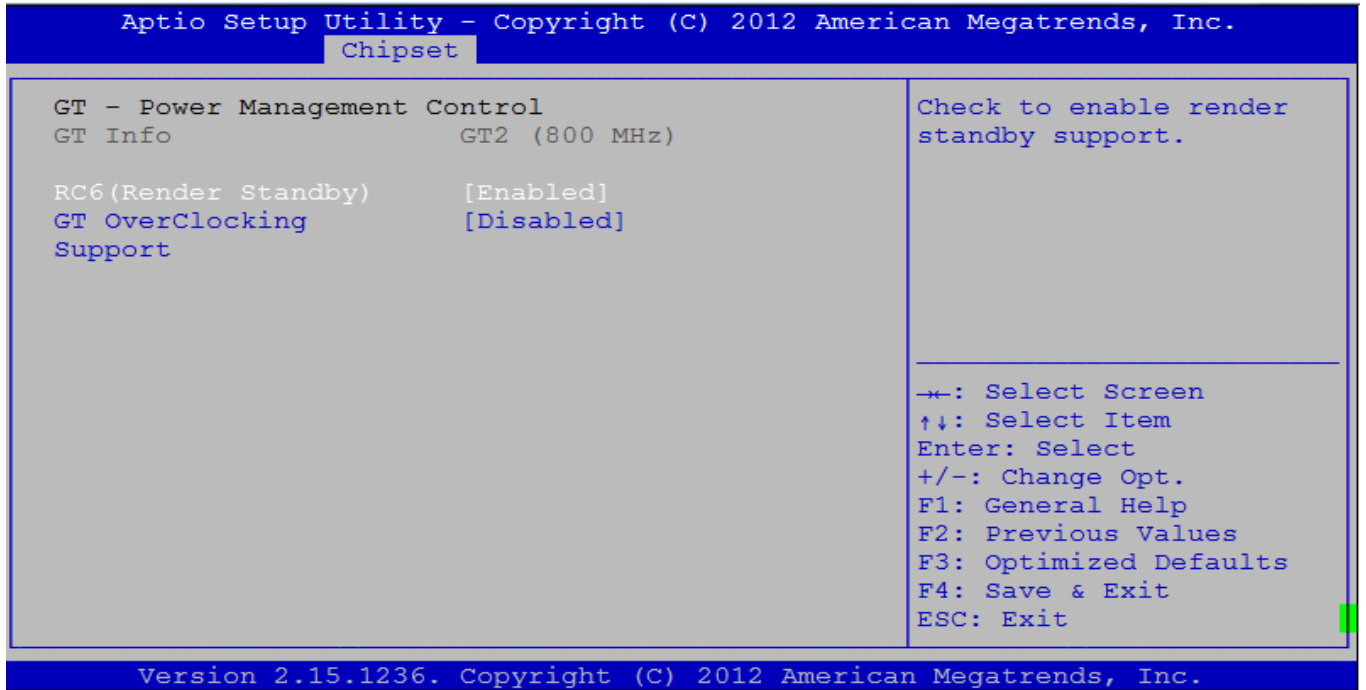


This option allows the user to view and change the Memory Running Average Power Limit (RAPL) Configuration.

Feature	Options	Description
RAPL Power Floor Ch0	0	
RAPL Power Floor Ch1	0	
RAPL PL Lock	Disabled Enabled	Enable or disable lock RAPL Limit register.
RAPL PL 1 Enable	Disabled Enabled	Enable or disable RAPL PL 1.
RAPL PL 1 Power	0	Range $[0;2^{14}-1]=[2047.875;0]$ in W.
RAPL PL 1 WindowsX	0	Power PL 1 time window, X value, $(1/1024)*(1+(x/4))*(2^y)$
RAPL PL 1 WindowsY	0	Power PL 1 time window, Y value, $(1/1024)*(1+(x/4))*(2^y)$
RAPL PL 2 Enable	Disabled Enabled	Enable or disable RAPL PL 2.
RAPL PL 2 Power	0	Range $[0;2^{14}-1]=[2047.875;0]$ in W.
RAPL PL 2 WindowsX	0	Power PL 2 time window, X value, $(1/1024)*(1+(x/4))*(2^y)$
RAPL PL 2 WindowsY	0	Power PL 2 time window, Y value, $(1/1024)*(1+(x/4))*(2^y)$

2.3.2.6 GT Power Management Control

Fig. 2.3.2.6.a GT Power Management Control



Feature	Options	Description
RC6 (Render Standby)		Enabled by default. Control of Intel graphics controller feature to reduce power consumption when asleep.
GT OverClocking Support		Disabled by default. Gateway control to graphics related frequency and voltage settings used for overclocking purposes.

2.4 Security, Boot, and Save and Exit

2.4.1 Security Screens

2.4.1.1 Passwords

Fig. 2.4.1.1.a Passwords (Screen 1 of 2)

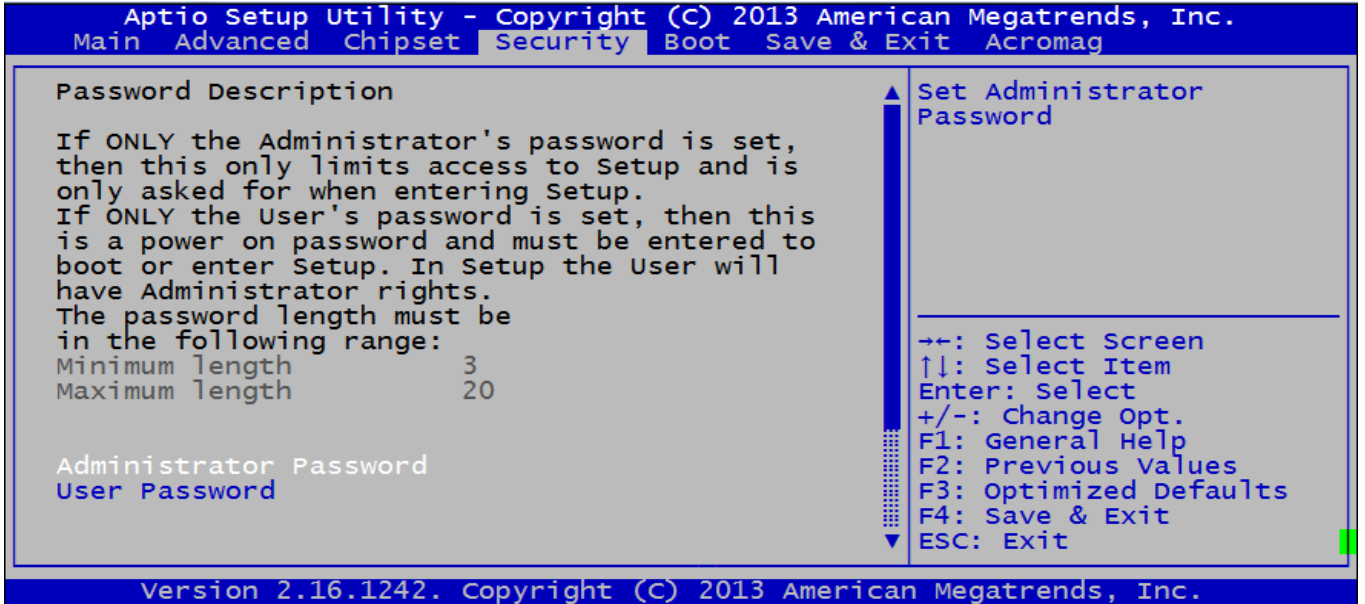
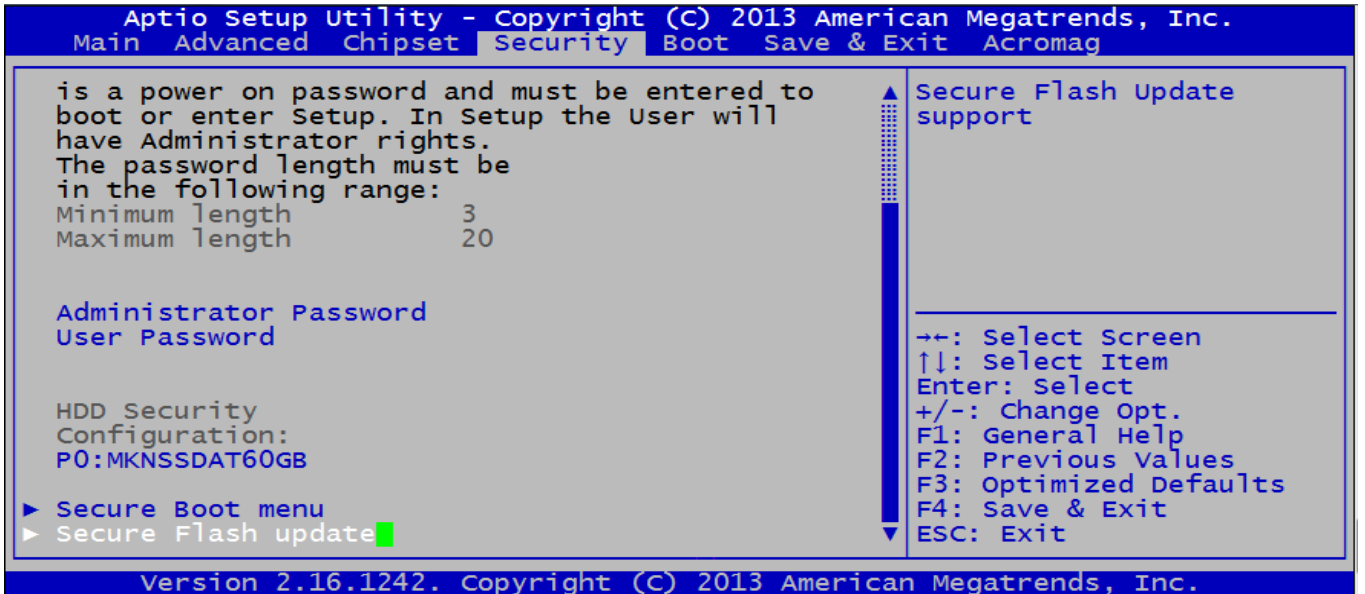


Fig. 2.4.1.1.b Passwords (Screen 2 of 2)



Two Levels of Password Protection

Security Setup provides both Administrator and User password. If you use both passwords, the Administrator password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when Setup is executed, using either the Administrator password or User password.

The Administrator and User passwords activate two different levels of password security as described in the table below.

If you select password support, you are prompted for a three to twenty character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must drain NVRAM and reconfigure.

This option allows the user to view and configure the Security setup parameters.

Feature	Description
User Password	This option allows the user to set a user level password for the BIOS. There is no Default password. If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup, the User will have Administrator rights.
Administrator Password	This option allows the user to set an administrative level password for the BIOS. There is no Default password. If ONLY the Administrator's password is set, this this only limits access to Setup and is only asked for when entering Setup.

Remember the Password

Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in NVRAM.

2.4.1.2 Key Management

Fig. 2.4.1.2.a Key Management (Screen 1 of 2)

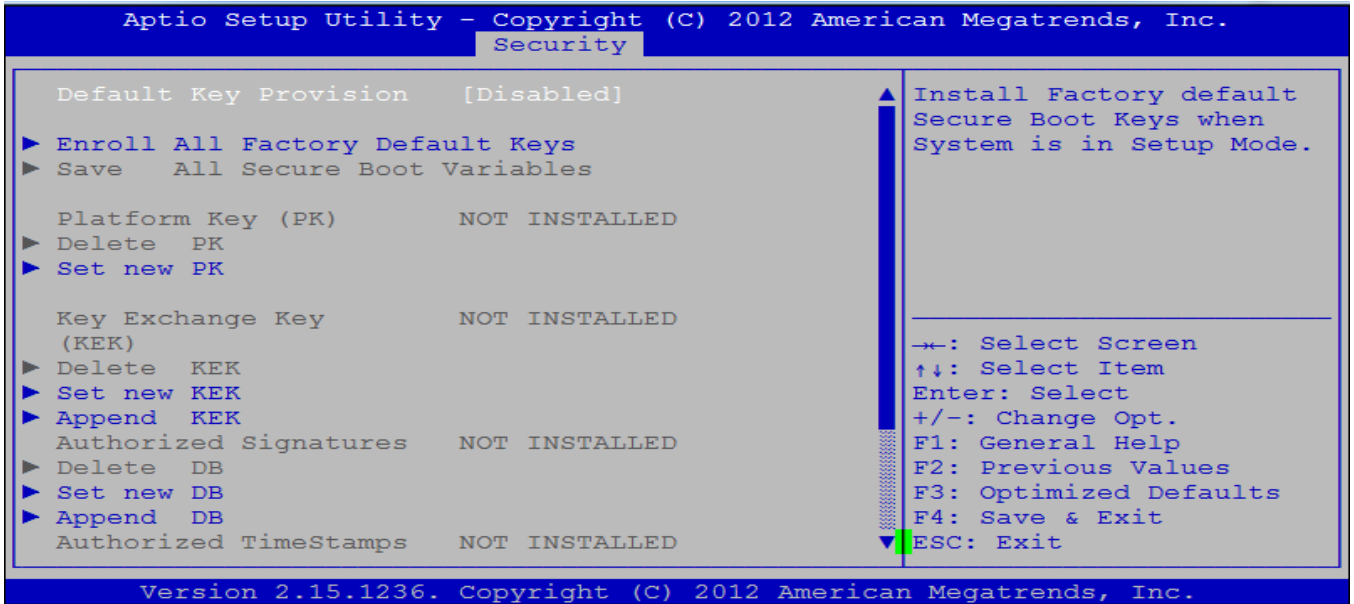
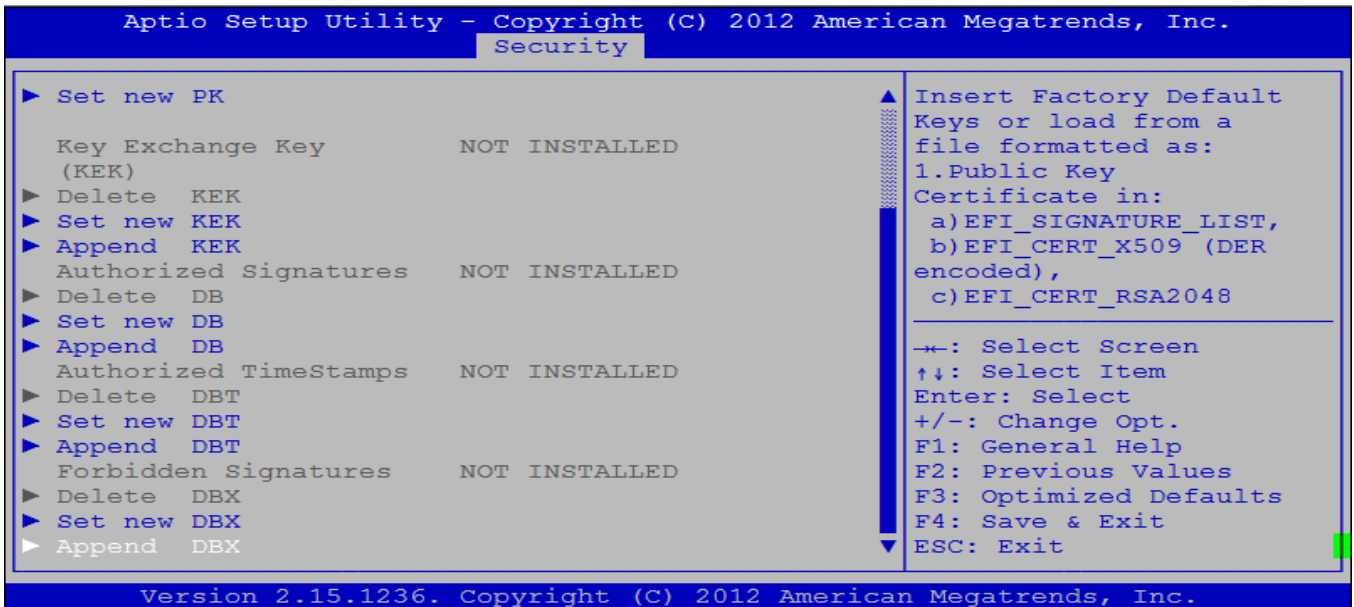
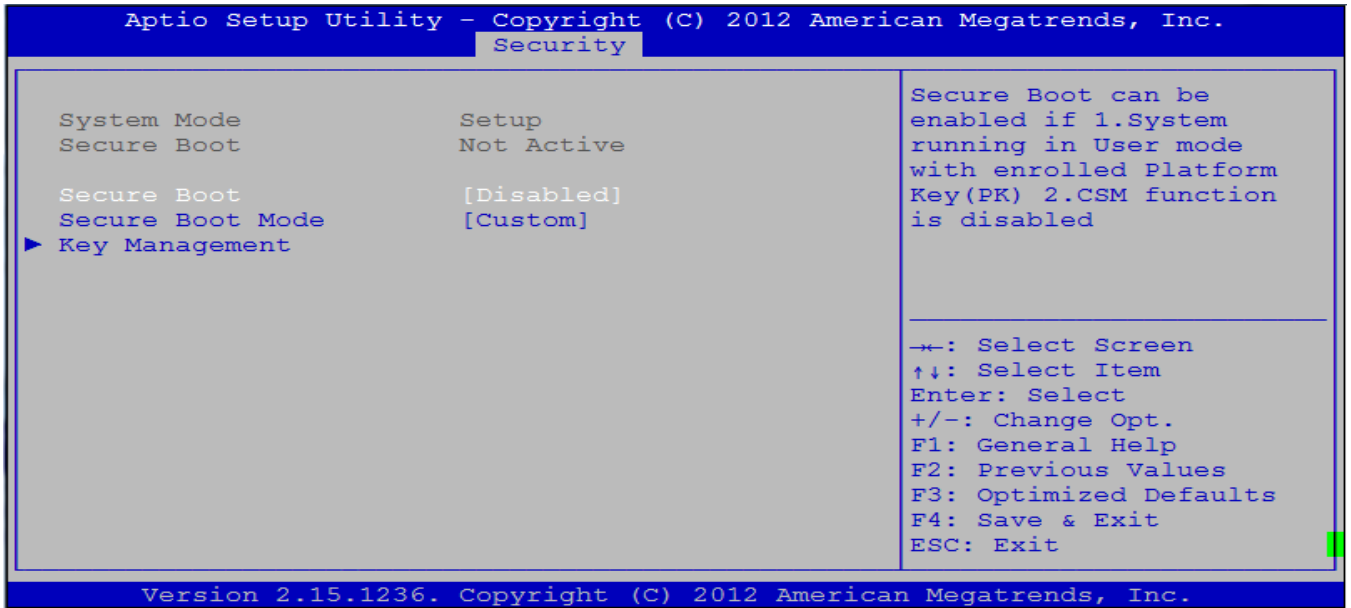


Fig. 2.4.1.2.b Key Management (Screen 2 of 2)



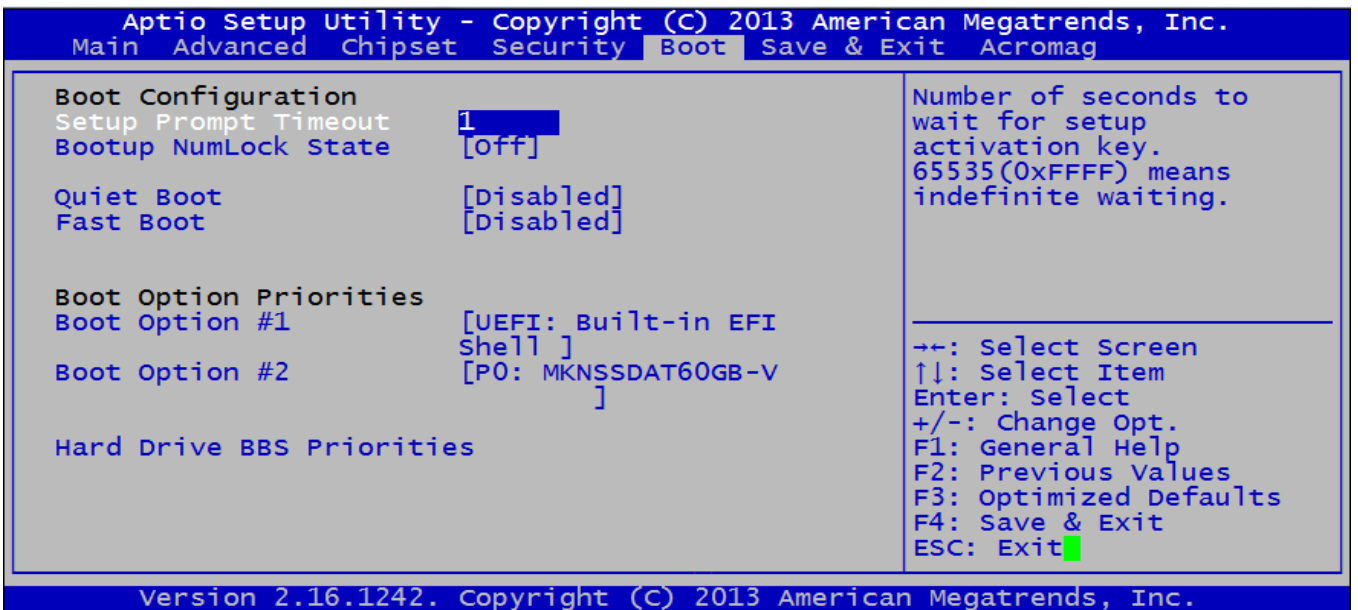
2.4.1.3 Secure Boot Menu

Fig. 2.4.1.3.a Secure Boot Menu



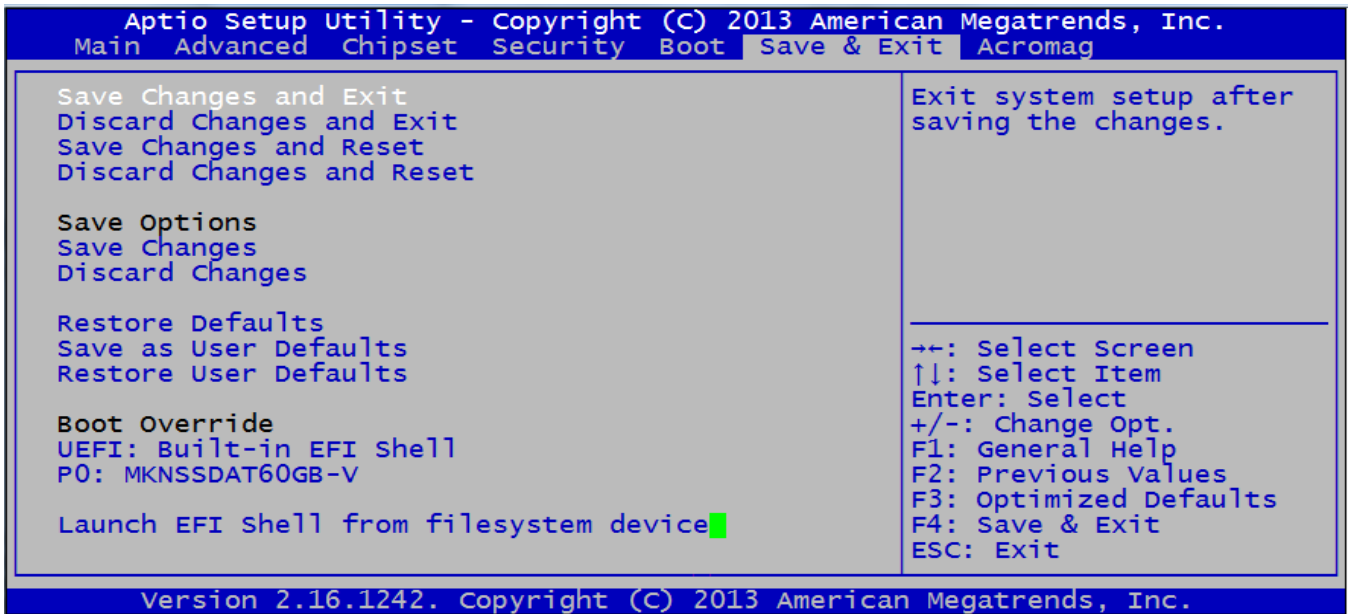
2.4.2 Boot Menu

Fig. 2.4.2.a Boot Menu



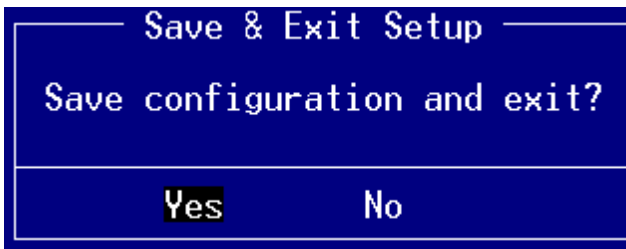
2.4.3 Save and Exit

Fig. 2.4.3.a Save and Exit



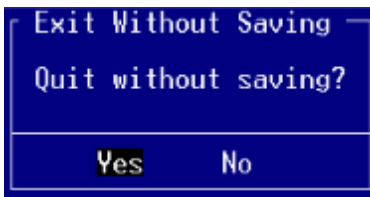
Save Changes and Exit

When you have completed the system configuration changes, select this option to save the changes and Exit from BIOS Setup, so the new system configuration parameters can take effect. The following window will appear after selecting the 'Save Changes and Exit' option selected. Select *YES* to Save Changes and Exit Setup.



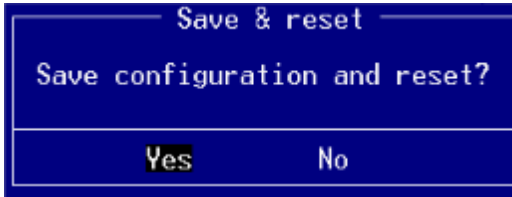
Discard Changes and Exit

Select this option to quit Setup without saving any modifications to the system configuration. The following window will appear after selecting the 'Discard Changes and Exit' option selected. Select *YES* to Discard changes and Exit Setup.



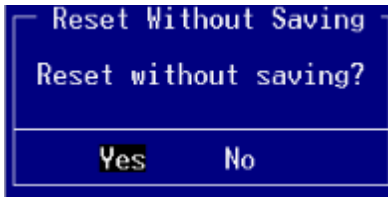
Save Changes and Reset

When you have completed the system configuration changes, select this option to save the changes and reboot the system, so the new system configuration parameters can take effect. The following window will appear after selecting the 'Save Changes and Reset' option selected. Select *YES* to Save Changes and Reset.



Discard Changes and Reset

Select this option to reboot the system without saving the changes done in the setup configuration. The following window will appear after selecting the 'Discard Changes and Reset' option selected. Select *YES* to Reset without saving.

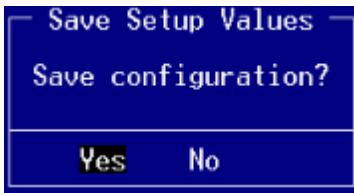


Save Options

Save Changes done so far to any of the setup options.

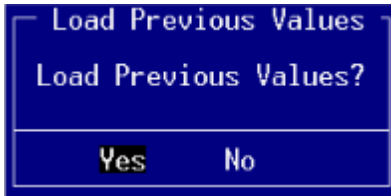
Save Changes

When you have completed the system configuration changes, select this option to save your system configuration and continue. For some of the options it required to reset the system to take effect. Select *YES* to Save Changes and continue.



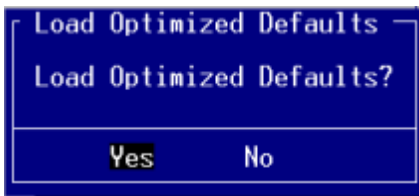
Discard Changes

When you have completed the system configuration changes, select this option to undo the previous changes. Select *YES* to load previous value and continue.



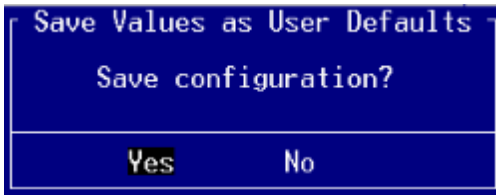
Restore Defaults

Restore default values for all setup options. Select *YES* to load Optimized defaults.



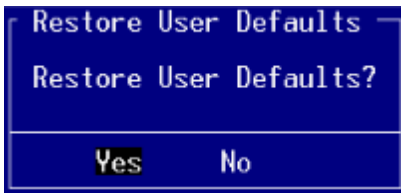
Save as User Defaults

Save changes done so far as User defaults. Select *YES* to save changes and continue.



Restore User Defaults

Restore the User defaults to all the setup options. Select *YES* to restore changes to user defaults and continue.



3.0 Revision History

The following table shows the revision history for this document:

Release Date	Version	EGR/DOC	Description of Revision
16 DEC 2013	A	BLD/TG	Preliminary release
18 DEC 2013	A1	BLD	Edits
08 JUL 2014	B	BLD	Add details for menu items that are referenced in the XCOM-6400 User's Manual
21 DEC 2016	C	BLD/ARP	Change the Manual title to: "APTIO HASWELL CORE BIOS MANUAL For Acromag Products using the Haswell Processor".
26 Nov 2018	D	JBO/RRP/ARP	Updated to include more BIOS menu items.