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What does the PMC-LX-EDK Engineering Design Kit contain?

The Engineering Design kit contains three directories, one for each model type. For example the LX40 directory contains the following files:

• LX_SX_UserManual.pdf	PMC LX/SX User's Manual
• AXM_User Manual.pdf	Mezzanine Modules User's Manual
• LX_SX_Schematic.pdf	Schematic and Part Location Drawing
• XC4VLX40.vhd	Main VHDL File for Example Design
• DP_SRAM.vhd	SRAM Component VHDL File for Example Design
• DIG_IO_8.vhd	8-bit Digital interrupt VHDL File for Example Design
• AXM_D.vhd	Front I/O Mezzanine VHDL File for Example Design
• RearLVDS.vhd	Rear I/O VHDL File for Example Design
• DDR_User_interface.vhd	DDR User Interface VHDL File for Example Design
• mem_interface_top*.vhd	27 DDR_SDRAM Controller VHDL Files for Example Design
• Constraints.Ucf	Xilinx Virtex-4 Constraints File
• LX40.mcs	Hex Configuration File Used to Program Virtex-4 FPGA
• README_LX40.txt	Getting Started Document
• AXM-EDK (qty. 1)	Development use AXM module with access to FPGA front I/O and JTAG

Overview

The LX_SX_Schematic.pdf file contains the part location and schematic. The first page contains the part location drawings. The remaining pages contain the schematics.

The vhd files are the source files for the example design provided by Acromag Inc. These files require the use of the Xilinx ISE software. The example design implements a PLX PCI9656 local bus interface to the FPGA, control of the dual port SRAM, control of the DDR_SDRAM, front I/O interface, and rear I/O interface. The DP_SRAM.vhd controls interface to a 256Kx36 dual port SRAM. The 27 mem_interface_top*.vhd files and file DDR_User_interface.vhd implement the DDR_SDRAM controller interface. The details of the memory map and register functions implemented in this example design are described in the user's manual.

The Constraints.Ucf file contains information about connected pin device assignments for the Xilinx project.

The mcs file is a hexadecimal configuration file which is used to configure the Xilinx FPGA over the PCI bus. The PMC board already has this file loaded into flash by Acromag. Thus, the FPGA will automatically be configuration with the example design upon power-up. This hex file is generated by the Xilinx iMPACT software and is an ASCII file in the Intel Hex format.