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Known Differences Between VPX4821A and Retired VPX4821

The VPX4821A is designed as a drop-in replacement for the VPX4821. The main difference between the two boards is the PCIe switch. The end-of-life PEX8632 switch was replaced with the PEX8734. The new switch component is quite different and requires different jumper settings than the original. The known differences between the existing VPX4821 and its replacement, the VPX4821A, are listed below. Our testing indicates that the new VPX4821A should work in all current customers' applications.

VPX4821

Jumpers

There are three jumper blocks located on the board. The jumper blocks are labeled J1, J2, and J3. Within each jumper block are five jumpers. Refer to Figure 2 below. Descriptions for each jumper are described in the tables below. The jumper position is OPEN if no jumper is present. The jumper position is SET if a jumper is present across the two pins.

For rugged designs all jumpers can be replaced with 0 ohm resistors. Please contact the factory for details.

Figure 2: Jumper and LED Locations

VPX4821A

Jumpers

There are six jumper blocks located on the board. The jumper blocks are labeled J1, J2, J3, J4, J5, and J6. Within each jumper block there are multiple jumper settings. A jumper can be used to shout post horizontally and vertically. The jumper position is OPEN if no jumper is present. The jumper position is SET if a jumper is present across the two pins. The description for each jumper is described in the tables that follow. Bold Selections are the factory default setting.

For rugged designs all jumpers can be replaced with 0 ohm resistors. Please contact the factory for details.

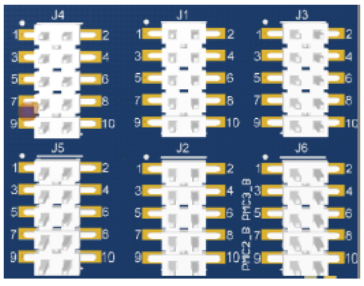

Figure 2 Jumper Diagram

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VPX4821

PCIe Lane Configuration

The VPX P1 PCIe lane configuration is selectable via the first and second jumper of J1. Please note that these strapping settings can be overwritten via a I²C write to the PEX8632.

Table 2-1 PCIe Lane Jumper Configuration

PCIe Lane Configuration	J1-1	J1-2
16x	**OPEN**	**OPEN**
8x-8x	SET	SET
4x-4x-4x-4x	OPEN	SET
8x-4x-4x	SET	OPEN

The PCIe lane configuration determined the PCIe switch port naming convention. Use Table 2-2 as a reference when selecting the upstream and downstream port.22.

Table 2-2 PCIe Port Naming Convention

PCIe Lane Configuration	Port Naming			
	L0-L3	L4-L7	L8-L11	L12-L15
16x	Port 0			
8x-8x	Port 0		Port 1	
4x-4x-4x-4x	Port 0	Port 1	Port 2	Port 3
8x-4x-4x	Port 0		Port 1	Port 2

PCIe Upstream Port Select

The PCIe Upstream port is selected by the third and forth jumpers of J1. Please note that these strapping settings can be overwritten via a I²C write to the PEX8632.

Table 2-3 PCIe Upstream Port Jumper Selection

PCIe Upsteam Port	J1-3	J1-4
0	**OPEN**	**OPEN**
1	SET	OPEN
2	OPEN	SET
3	SET	SET

VPX4821A

PCIe Lane Configuration

The VPX P1 PCIe lane configuration is selectable via the J1 jumper. Please note that these strapping settings can be overwritten via a I²C write to the PEX8734.

Table 2-1 PCIe Lane Jumper Configuration

PCIe Lane Configuration	J1 Jumper Configuration					
	5-6	5-7	6-8	1-2	1-3	2-4
8x-8x	O	S	O	S	O	O
4x-4x-4x-4x	**O**	**O**	**S**	**O**	**O**	**S**
8x-4x-4x	O	O	S	O	S	O

Default setting is 4x-4x-4x-4x with vertical jumbers J1 2-4 and 6-8 set.

The PCIe lane configuration determined the PCIe switch port naming convention. Use Table 2-2 as a reference when selecting the upstream and downstream port.

Table 2-2 PCIe Port Naming Convention

PCIe Lane Configuration	Port Naming			
	L0-L3	L4-L7	L8-L11	L12-L15
8x-8x	Port 0		Port 1	
4x-4x-4x-4x	Port 0	Port 1	Port 2	Port 3
8x-4x-4x	Port 0		Port 1	Port 2

PCIe Upstream Port Select

The PCIe Upstream port is selectable via the J3 jumper. Please note that these strapping settings can be overwritten via a I²C write to the PEX8734.

Table 2-3 PCIe Upstream Port Jumper Selection

PCIe Lane Configuration	J3 Jumper Configuration					
	5-6	5-7	6-8	1-2	1-3	2-4
Port 0	**O**	**S**	**O**	**O**	**S**	**O**
Port 1	O	S	O	O	O	S
Port 2	O	S	O	S	O	O
Port 3	O	O	S	O	S	O

Default setting is Port 0 with vertical J3 jumbers 1-3 and 5-7 set.

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VPX4821

PCIe Gen 1 Force

To Force all lanes of the PEX8632 to run at Gen 1 speeds set the fifth jumper of J2. Note only use this setting if the auto-negotiate process fails. Normally this only needs to be used for PCIe devices are were released prior to the finalization of the PCIe 1.0 specification. This will affect all PCIe connections on the board including to the processor and XMC modules.

Table 2-4 PCIe Force Gen 1 Jumper Setting

PCIe Speed	J2-5
Gen 1	SET
Gen 2	OPEN

Fan-Out Enable

N/A

PCIe NT Port Enable

To Enable the NT Port of the PCIe switch, SET the first jumper of J3. The PCIe NT port is selected by the second and third jumpers of J3. Please note that these strapping settings can be overwritten via a I^2C write to the PEX8632.

Table 2-5 NT Enabled Jumper Settings

NT Port	J3-1
Disabled	OPEN
Enabled	Set

PCIe NT Port Select

The PCIe NT port is selected by the second and third jumpers of J3. The NT Port must be enabled via jumpers J3-1 for these jumpers to operate properly. Please note that these strapping settings can be overwritten via a I^2C write to the PEX8632.

Table 2-6 PCIe NT Port Jumper Selection

PCIe NT Port	J3-2	J3-3
0	OPEN	OPEN
1	SET	OPEN
2	OPEN	SET
3	SET	SET

VPX4821A

PCIe Gen 1 Force

N/A

Fan-Out Enable

Enable peer-to-peer (Downstream endpoint-to-Downstream endpoint) traffic with jumper J5 9-10 set. If peer-to-peer (Downstream endpoint-to-Downstream endpoint) traffic is not needed, this jumper can be left open.

Table 2-4 Fan-Out Enable Jumper Setting

Fan-Out Enable	J5 9-10
Enable	SET
Disable	OPEN

Default Fan-Out Enabled setting horizontal J5 jumber 9-10 set.

PCIe NT Port Enable/Select

To Enable the Non-Transparent (NT) Port of the PCIe switch, SET J5 and J2 jumpers as listed in table 2-5. Please note that these strapping settings can be overwritten via a I^2C write to the PEX8734. Non-Transparent selected presents a processor as an endpoint rather than another memory system.

Table 2-5 NT Enabled Jumper Settings

Select NT Upstream Port	Jumper Configuration								
	J5						J2		
	1-2	1-3	2-4	5-6	5-7	6-8	1-2	1-3	2-4
Port 0	O	S	O	O	S	O	O	S	O
Port 1	O	S	O	O	S	O	O	O	S
Port 2	O	S	O	O	S	O	S	O	O
Port 3	O	S	O	O	O	S	O	S	O
NT Disable	**S**	**O**	**O**	**S**	**O**	**O**	**S**	**O**	**O**

Default setting is NT Disable with horizontal J5 jumber 1-2 set, 5-6 set, and J2 jumper 1-2 set.

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VPX4821

+3.3_AUX Power

The 3.3V_AUX power is required for proper operation of this board. For users without this power supply available on the VPX backplane you can alternatively use the onboard generated 3.3V.

Table 2-7 +3.3V_AUX Power Select Jumper Settings

Source of +3.3V-AUX	J3-4	J3-5
Backplane	**OPEN**	**SET**
Onboard	SET	OPEN

WARNING! The J3-4 and 5 jumpers should both never be set. This could cause damage to either the board or chassis power supply.

JTAG Reference Power

The pull-up voltage on the JTAG pins to XMC P15 and P25 can be selected as either +2.5V or +3.3V. Refer to the XMC User's Manual for proper voltage selection. The forth jumper in J2 is for slot A and the fifth jumper in J1 is for slot B.

Table 2-8 JTAG Power Select Jumper Settings

JTAG Ref Voltage		
Slot	LOC	Setting
Slot A	J2-4	**SET +3.3V** OPEN +2.5V
Slot B	J1-5	**SET +3.3V** OPEN +2.5V

VPX4821A

+3.3_AUX Power

The 3.3V_AUX power is required for proper operation of this board. For users without this power supply available on the VPX backplane you can alternatively use the onboard generated 3.3V.

Table 2-6 +3.3V_AUX Power Select Jumper Settings

Source of +3.3V-AUX	J6 7-8	J6 9-10
Onboard +3.3V	OPEN	SET
Backplane	**SET**	**OPEN**

WARNING! The J6 7-8 and J6 9-10 jumpers should both never be set. This could cause damage to either the board or chassis power supply.

Default setting is +3.3V_AUX from Backplane with horizontal J6 7-8 jumber set.

JTAG Reference Power

The pull-up voltage on the JTAG pins to XMC P15 and P25 can be selected as either +2.5V or +3.3V. Refer to the XMC User's Manual for proper voltage selection. The jumper J3 9-10 is for slot A and the jumper J1 9-10 is for slot B.

Table 2-7 JTAG Power Select Jumper Settings

JTAG Ref Voltage		
Slot	LOC	Setting
Slot A	J3 9-10	**OPEN +3.3V** SET +2.5V
Slot B	J1 9-10	**OPEN +3.3V** SET +2.5V

Default setting is +3.3V JTAG Ref with J3 9-10 jumber OPEN and J1 9-10 jumper OPEN.

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VPX4821

Clock Settings

There are several clock options available for the user. These options are set on the first, second, and third jumpers of J2. The default selection is to use the on-board crystal to generate the 100MHz PCIe clock. This frequency is propagated to all parts and XMC modules. Users also have the option to use a clock from the VPX backplane. Note that this must be a 100MHz clock for proper operation. Refer to the table below for jumper settings.

Table 2-9 Clock Jumper Settings

Global Clock Source	J2-1	J2-2	J2-3
On Board Crystal	OPEN	OPEN	OPEN
VPX SYSCLK	SET	OPEN	OPEN
Disable all CLK's	OPEN	OPEN	SET

Reset

N/A

I²C Programming

The PEX8632 PCI switch can alternately be programmed via a simple I²C bus. The I²C is accessed via the System Bus pins on the VPX backplane.

Furthermore, the I²C bus is connected to both XMC modules. For further information on programming using the I²C bus contact the factory.

VPX4821A

Clock Settings

There are several clock options available for the user. These options are set on J4 1-2, J4 3-4, and J4 5-6 jumpers. The default selection is to use the on-board crystal to generate the 100MHz PCIe clock. This frequency is propagated to all parts and XMC/PMC modules. Users also have the option to use a clock from the VPX backplane. Note that this must be a 100MHz clock for proper operation. Refer to the table below for jumper settings. Spread spectrum clocking is enabled when J4 3-4 is Set. Spread spectrum clocking should always be disabled.

Table 2-8 Clock Jumper Settings

Global Clock Source	J4 1-2	J4 3-4	J4 5-6
On Board Crystal	OPEN	OPEN	OPEN
VPX SYSCLK	SET	OPEN	OPEN
Disable all CLK's	OPEN	OPEN	SET

Default setting is On Board Crystal with J4 1-2, J4 3-4, and J4 5-6 jumbers OPEN.

Reset

This system reset is propagated to all parts XMC/PMC modules and backplane. Refer to the table below for jumper settings.

Table 2-9 Reset Output Generator Jumper Settings

Reset Output Generator	J6 1-2	J6 3-4
System Reset	OPEN	SET

I²C Programming

The PEX8734 PCI switch can alternately be programmed via a simple I²C bus. The I²C is accessed via the System Bus pins on the VPX backplane.

Furthermore, the I²C bus is connected to both XMC modules. For further information on programming using the I²C bus contact the factory.

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VPX4821

NVROM

The NVROM signal from the VPX Backplane is routed to the PCIe Switch EEPROM as well as both XMC modules.

LEDs

The VPX4821 has several status LEDS. These LED's are primarily used for initial power-up status. Refer to Figure 2 for the location of the LED's. The table below describes the functionality.

Table 2-10 LED

LED	Color	Description
DS1	Green	All power supplies are good.
DS2	Green	PMC A Only – PCIe Lane 1 has connected.
DS3	Green	PMC A Only – PCIe Lane 2 has connected.
DS4	Green	PMC A Only – PCIe Lane 3 has connected.
DS5	Green	PMC A Only – PCIe Lane 4 has connected.
DS6	Green	PMC B Only – PCIe Lane 1 has connected.
DS7	Green	PMC B Only – PCIe Lane 2 has connected.
DS8	Green	PMC B Only – PCIe Lane 3 has connected.
DS9	Green	PMC B Only – PCIe Lane 4 has connected.
DS10	Green	VPX PCIe Port 0 has successfully connected
DS11	Green	VPX PCIe Port 1 has successfully connected
DS12	Green	VPX PCIe Port 2 has successfully connected
DS13	Green	VPX PCIe Port 3 has successfully connected
DS14	Green	A Connection has been made to XMC/PMC Slot A.
DS15	Green	A Connection has been made to XMC/PMC Slot B.
DS16	Red	Fatal Error (non-recoverable)
DS17	Green	PCI INTA

Backplane Key

The VPX4821 is not keyed and will plug into any VPX backplane. Prior to powerup, verify that VS1 is +12V. Any other voltage on VS1 may damage the board.

VPX4821A

NVROM

The NVROM signal from the VPX Backplane is routed to the PCIe Switch EEPROM as well as both XMC modules.

LEDs

The VPX4821A has several status LEDS. These LED's are primarily used for initial power-up status. The LEDs are located on the front of the card near the J1 to J6 jumpers. The table below describes the functionality.

Table 2-10 LED

LED	Color	Description
DS1	Green	All power supplies are good.
DS2	Red	PMC A Only – PCIe Lane 1 has connected.
DS3	Red	PMC A Only – PCIe Lane 2 has connected.
DS4	Red	PMC A Only – PCIe Lane 3 has connected.
DS5	Red	PMC A Only – PCIe Lane 4 has connected.
DS6	Red	PMC B Only – PCIe Lane 1 has connected.
DS7	Red	PMC B Only – PCIe Lane 2 has connected.
DS8	Red	PMC B Only – PCIe Lane 3 has connected.
DS9	Red	PMC B Only – PCIe Lane 4 has connected.
DS10	Green	VPX PCIe Port 0 has successfully connected
DS11	Green	VPX PCIe Port 1 has successfully connected
DS12	Green	VPX PCIe Port 2 has successfully connected
DS13	Green	VPX PCIe Port 3 has successfully connected
DS14	Green	A Connection has been made to XMC/PMC Slot A.
DS15	Green	A Connection has been made to XMC/PMC Slot B.
DS16	Red	Fatal Error (non-recoverable)
DS17	Green	PCI INTA

Backplane Key

The VPX4821A is not keyed and will plug into any VPX backplane. Prior to powerup, verify that VS1 is +12V. Any other voltage on VS1 may damage the board.

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VPX4821

Power

Board power requirements are a function of the installed XMC module and of the carrier card. The carrier board supports up to four power supplies from the VPX Backplane +12V, +3.3V_AUX, +12V_AUX, -12V_AUX. The +5V and +3.3V supplies for the XMC/PMC modules are generated by on-board DC/DC converters from the +12V backplane supply.

Currents specified are for the carrier board only for Model VPX4821, add the XMC module currents for the total current required from each supply. The major power components are listed below to assist with power calculations.

Table 5-1 VPX4821 Internal Power usage typical.

Voltage	PCIe Switch[2]	PCIe-PCI Bridge[3]	Watts	Power from +12V[1]
+1.0V	2.8A		2.8W	3.36W
+2.5V	0.05A		0.125	0.15W
+1.2V		0.61A	1.81W	2.17W
+3.3V		0.17A	0.56W	0.672W

1. Assume 80% from on board DC/DC
2. Assume 16 lane operation. Typical.
3. Per PMC Slot Used. Typical

+12 Volts (±5%)	900 mA typ, 2A maximum.
+12V_AUX, -12V_AUX	Not used. Supplied to PMC/XMC modules only.
+3.3V_AUX	25mA typical, 50mA maximum.
Sequencing	All power supplies will ramp up with 400us of bus power. Onboard supplies will ramp up together once VS1 (+12V) has exceeded 2.5V. Note that there is no onboard detection to determine if +12V is within specification.

VPX4821A

Power

Board power requirements are a function of the installed XMC module and of the carrier card. The carrier board supports up to four power supplies from the VPX Backplane +12V, +3.3V_AUX, +12V_AUX, -12V_AUX. The +5V and +3.3V supplies for the XMC/PMC modules are generated by on-board DC/DC converters from the +12V backplane supply.

Currents specified are for the carrier board only for Model VPX4821A, add the XMC module currents for the total current required from each supply. The major power components are listed below to assist with power calculations.

Table 5-1 VPX4821A Internal Power usage typical.

Voltage	PCIe Switch[2]	PCIe-PCI Bridge[3]	Watts	Power from +12V[1]
+0.9V	3.264A		2.938W	3.53W
+1.8V	0.383A		0.69W	0.83W
+1.2V		0.61A	1.81W	2.17W
+3.3V		0.17A	0.56W	0.672W

1. Assume 83% from on board DC/DC
2. Assume 8 lane operation,Gen 2. Typical.
3. Per PMC Slot Used. Typical

+12 Volts (±5%)	900 mA typ, 2A maximum.
+12V_AUX, -12V_AUX	Not used. Supplied to PMC/XMC modules only.
+3.3V_AUX	25mA typical, 50mA maximum.
Sequencing	All power supplies will ramp up with 400us of bus power. Onboard supplies will ramp up together once VS1 (+12V) has exceeded 2.5V. Note that there is no onboard detection to determine if +12V is within specification.