

Embedded Computing & I/O Solutions

# XMC Products Brochure

FPGAs

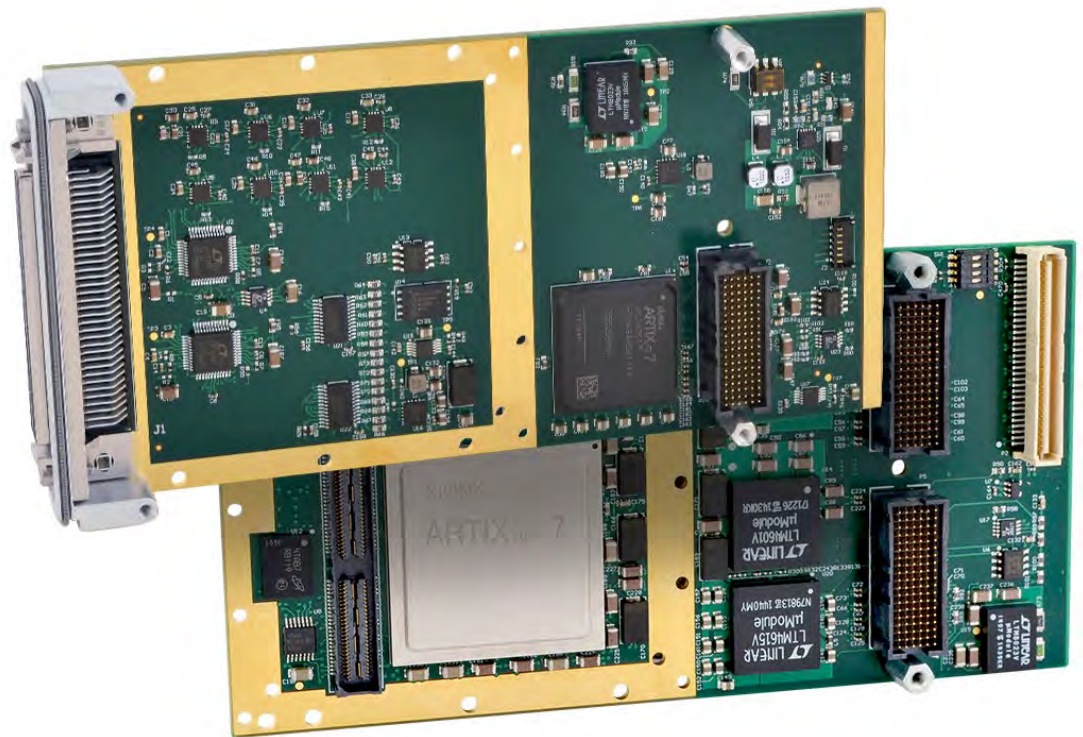
Extension I/O Modules

1/10Gb Ethernet

Multi-Function I/O

Carrier Cards

Software Support



High-Performance XMC FPGAs,  
XMC 1/10Gb Ethernet, and  
XMC Carrier Cards.

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Acromag is focused on developing embedded computing solutions that provide the best long term value in the industry. Compare and you will find that Acromag offers an unmatched balance of price, performance, and features.

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With over 60 years of industrial I/O design experience, Acromag stands alone in the high-performance bus-board market. Developing VMEbus I/O boards since 1984, we combine our process control expertise with extensive experience in embedded computing. This background gives us unrivaled insight to many unique concerns when interfacing computer systems to various sensors and controllers in a wide range of applications.

Acromag processor, FPGA, and I/O products are commonly used in these industries:

- military/defense
- aerospace
- transportation
- manufacturing
- semiconductors
- scientific
- communication
- research labs

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We take every measure to guarantee dependable operation with ISO9001 and AS9100 certified quality management. State-of-the-art manufacturing with industrial-grade components adds extra ruggedness. Advanced inspection and testing further ensure that Acromag I/O performs at or beyond their rated specs.

## Technical Support

Drawing on a wealth of embedded I/O experience, our sales engineers are well qualified to support you in the use of our products in your end-applications. We take pride in our highly experienced staff that excels at after-sale technical support.

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Great care has been put into building a team of highly skilled representatives and distributors. They are located around the world to service your needs.

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AS9100



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Reliability  
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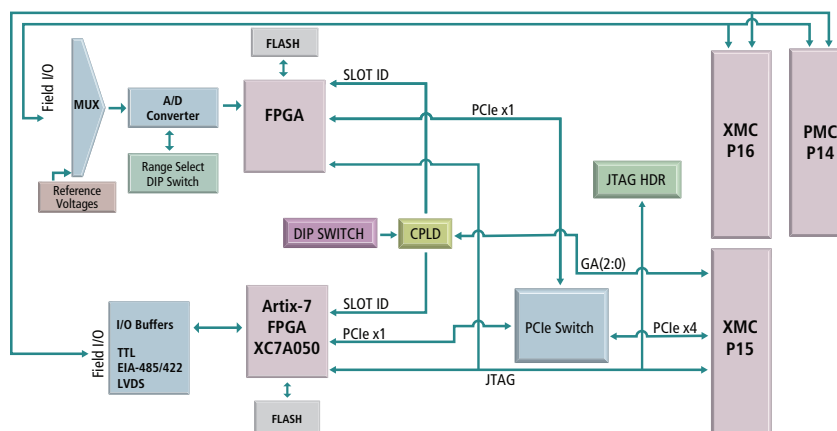
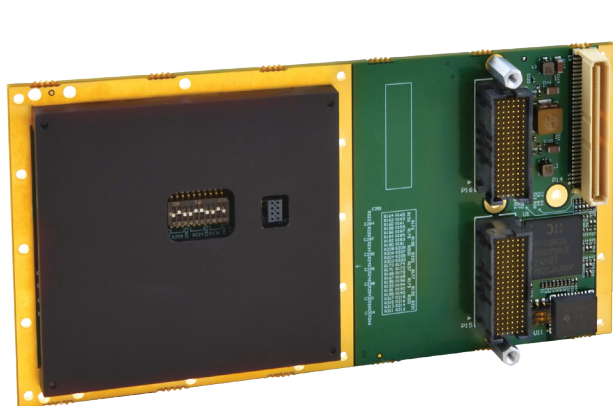


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Acromag, Incorporated ■ 30765 South Wixom Road ■ Wixom, Michigan 48393 ■ USA

# XMC Modules

## XMC-7A50-AP323 XMC Module with Artix®-7 FPGA and High-Density I/O



Reconfigurable Xilinx® Artix®-7 FPGA ◆ 48 Digital I/O ◆ 20 Diff or 40 SE Analog Inputs ◆ 16-bit ADC

### Description

XMC-7A51-AP323: 48 TTL channels

**Custom Requirements:** Other I/O combinations are possible, contact Acromag for more information.

Build Option A: 24 EIA-485/422 channels

Build Option B: 24 TTL and 12 EIA-485/422 channels

Build Option C: 24 LVDS channels

Designed for COTS applications, these XMC modules combine a user-customizable FPGA with digital I/O and high-performance analog inputs for high-density signal processing.

The XMC-7A50-AP323 series provides a FPGA based user-configurable bridge between a host processor and a custom digital interface via PCI Express. These XMC boards feature a best-in-class Artix®-7 interface to deliver the industry's lowest power and high performance.

The analog inputs monitor 20 differential or 40 single-ended channels. Software or an external hardware input can trigger A/D conversions for synchronization to external events. On-board, precision voltage references enable accurate software calibration of the module without external instruments.

The Engineering Design Kit provides users with basic info. required to develop custom FPGA firmware for download to the Xilinx® FPGA. Example FPGA design code is provided as a Vivado IP Integrator project for functions such as a one-lane PCI Express interface, DMA, digital I/O control register, and more. Users should be fluent using Xilinx Vivado® design tools.

### Key Features & Benefits

#### FPGA Digital I/O

- Reconfigurable Xilinx FPGA
- High channel count digital interface: TTL, RS485, and LVDS interface options
- 32Mb quad serial flash memory
- 52,160 logic cells
- 65,200 Flip flops
- 2,700 kb block RAM
- 120 DSP slices
- External LVTTTL clock input
- Long distance data transmission
- Example design
- Power up and system reset is failsafe

#### Analog Input

- 20 differential or 40 single-ended inputs
- Flexible scan control
- 16-bit A/D resolution
- 8µs conversion time
- FIFO buffer with 16K sample memory
- Interrupt upon FIFO threshold condition
- FIFO full, empty and threshold reached flags
- Programmable channel conversion control
- Programmable conversion timer
- Several scanning modes
- External trigger

#### General

- Wide temperature range
- Conduction cooling options
- Software development tools for VxWorks®, Linux®, and Windows® environments



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## Performance Specifications

### ■ XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-width module.

### ■ PCI Express Base Specification

Conforms to revision 2.0

#### Lanes

1 lane in each direction.

#### Bus Speed

2.5 Gbps (Generation 1).

#### Memory

128k space required.

1 base address register.

### ■ FPGA

#### FPGA device

Xilinx Artix-7 FPGA Model XC7A50T.

#### FPGA configuration

Download via flash memory.

#### Example FPGA program

IP integrator block diagram provided for PCIe bus 1 lane Gen 1 interface, DMA controller, on chip block RAM, flash memory and control of field I/O. See EDK kit.

### ■ I/O Processing

#### Field I/O Interface

PCIe bus 1 lane Gen 1 interface.

#### I/O Connector

100 pin field I/O connector.

### ■ Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7A50-AP323 series module (see [www.acromag.com](http://www.acromag.com) for more information).

### ■ Digital I/O

#### TTL Channels

48 input/output channels. Direction is controlled in groups of eight channels. 5V tolerant.

#### TTL Electrical Characteristics

$V_{IH}$ : 2.0V minimum.

$V_{IL}$ : 0.8V maximum.

$I_{OH}$ : -32.0mA.

$I_{OL}$ : 64.0mA.

$V_{OH}$ : 2.0V minimum.

$V_{OL}$ : 0.55V maximum at 64mA.

### ■ Analog Input

#### Input configuration

20 differential or 40 single-ended.

#### A/D Resolution

16 bits.

#### Input range (dip switch-selectable)

Bipolar  $\pm 5V$  or  $\pm 10V$ .

Unipolar 0 to +5V or 0 to +10V.

#### Data sample memory

16K sample FIFO buffer.

#### Maximum throughput rate

200KHz (5 $\mu$ S/conversion).

#### A/D triggers

External, and software.

#### System accuracy

2.4 LSB (0.014%).

Maximum overall calibrated error at 25°C.

| Input Range (Volts) | ADC Range (Volts) | Maximum Error $\pm$ LSB (%span) | Typical Error $\pm$ LSB (%span) |
|---------------------|-------------------|---------------------------------|---------------------------------|
| $\pm 5$             | $\pm 5$           | $\pm 8.6$ LSB (0.013%)          | $\pm 8.6$ LSB (0.013%)          |
| $\pm 10$            | $\pm 10$          | $\pm 9.4$ LSB (0.014%)          | $\pm 3$ LSB (0.005%)            |

#### Data format

Binary two's compliment and straight binary.

#### Input overvoltage protection

Power on: -20V to +40V.

Power off: -35V to +55V

#### Common mode rejection ratio (60Hz)

96dB typical.

#### Channel-to-channel rejection ratio (60Hz)

96dB typical.

### ■ Environmental

#### Operating temperature

-40 to 70°C.

#### Storage temperature

-55 to 100°C.

#### Relative humidity

5 to 95% non-condensing.

#### Power

| Power Supply | Typical | Maximum |
|--------------|---------|---------|
| +3.3V        | 455mA   | 550mA   |
| VPWR (+5V)   | 20mA    | 30mA    |
| VPWR (+12V)  | 0.7mA   | 1.4mA   |
| +12V         | <100mA  | 100mA   |
| -12V         | 0.7mA   | 1.4mA   |

### ■ Physical

#### Length

5.866 inches (143.75mm.)

#### Width

2.9134 inches (74mm.)

#### Weight

3.392 oz (96.162g).

## Ordering Information

### XMC Modules

[Go to on-line ordering page >](#)

XMC-7A51-AP323

48 TTL channels

**Custom Requirements:** Other I/O combinations are possible, contact Acromag for more information.

Build Option A: 24 EIA-485/422 channels.

Build Option B: 24 TTL and 12 EIA-485/422 channels.

Build Option C: 24 LVDS channels.

### Accessories

#### APA7-EDK

Engineering design kit. (One kit required).

#### 5028-564

JTAG adapter cable.

### Carrier Cards

See [Acromag.com](http://Acromag.com) for a full list of XMC carrier cards.

### Software

(see software documentation for details)

#### APSW-API-VXW

VxWorks® software support package.

#### APSW-API-WIN

Windows® DLL driver software support package.

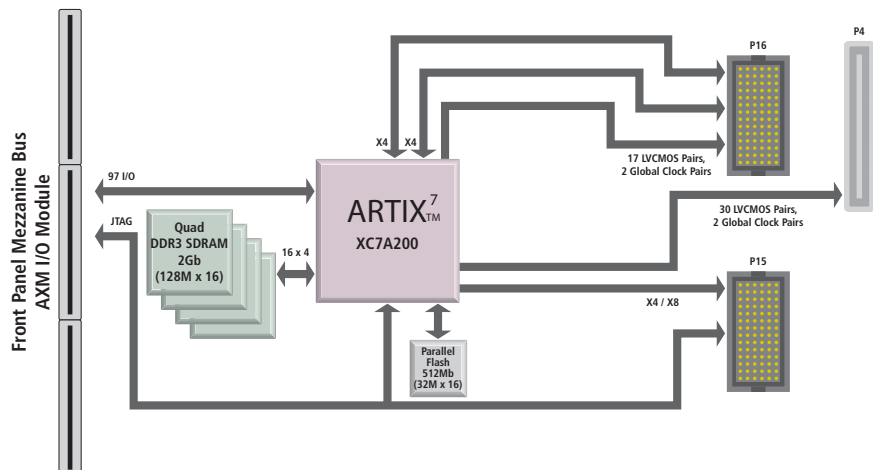
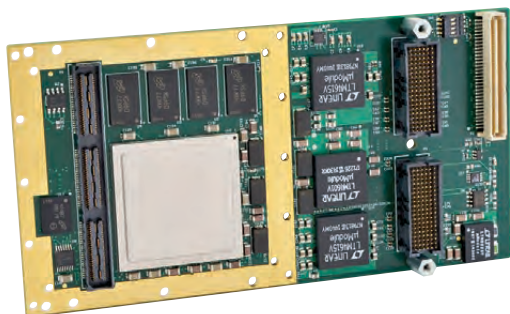
#### APSW-API-LNX

Linux® support (website download only).



# XMC Modules

**XMC-7A200** User-Configurable Artix®-7 FPGA Modules with Plug-In I/O   



**XMC module with PCIe interface ♦ Logic-optimized Artix-7 FPGA ♦ I/O Extension Mezzanine Modules**

## Description

Acromag's [XMC-7A](#) modules feature a high-performance user-configurable Xilinx® Artix®-7 FPGA enhanced with high-speed memory and a high-throughput serial bus interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

Both front and rear I/O is supported. Front I/O processing is supported with plug-in AXM mezzanine cards. A variety of AXM I/O cards are available to add the flexibility of a wide range of analog and digital I/O to your design.

The rear I/O provides an 8-lane high-speed serial interface on the P16 XMC port for customer-installed soft cores. P16 also supports 34 SelectIO and global clock lines. SelectIO signals are Artix-7 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL)

With Acromag's Artix-7 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with Vivado® or ISE® Design Suite. And with ChipScope™ Pro tools, you can rapidly debug logic and serial interfaces



## Key Features & Benefits

- Reconfigurable Xilinx Artix-7 FPGA with 200k logic cells
- 128M x 64-bit DDR3 SDRAM
- 32M x 16-bit parallel flash memory for MicroBlaze FPGA program code storage
- 4-lane high-speed serial interface on rear P15 connector for PCIe Gen 1/2 (standard), Serial RapidIO, 10Gb Ethernet, Xilinx Aurora
- 8-lane high-speed interfaces on rear P16 connector for customer-installed soft cores
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- DMA support provides data transfer between system memory and the on-board memory
- Support for Xilinx ChipScope™ Pro interface

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## XMC-7A200 User-Configurable Artix-7 FPGA Modules w Plug-In I/O

### Performance Specifications

#### ■ FPGA

FPGA device

Xilinx® Artix®-7 FPGA.

Model XC7A200T FPGA with 215,360 logic cells and 740 DSP48E1 slices.

FPGA configuration

Download via JTAG or flash memory.

Example FPGA program

IP integrator block diagram provided for bus interface, front & rear I/O control, and SDRAM memory interface controller. See EDK kit.

#### ■ I/O Processing

Acromag AXM I/O Modules:

AXM modules plug into the XMC module's front mezzanine for additional I/O lines. Analog and digital I/O AXM modules are sold separately.

Rear high-speed I/O

12 high-speed serial lanes.

x8 lanes via P15 and x8 lanes via P16.

Rear user I/O

P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.

P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

#### ■ Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7A module (see [www.acromag.com](http://www.acromag.com) for more information).

#### ■ XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### ■ Electrical

XMC PCIe bus interface (P15 and P16)

One 114-pin male connector (Samtec ASP-103614-05 or equivalent).

P15 primary XMC connector

8 differential pairs (PCIe x4 standard, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.

System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin, powers volatile memory to store the bitstream encryption key.

Variable power (5V or 12V): 8 pins at 1A per pin.

P16 XMC connector

8 differential pairs (PCIe, Serial RapidIO, or Xilinx Aurora).

17 LVDS pairs or 34 SelectIO signals (differential pairs grouped per VITA 46.0 X38s).

2 global clock pairs.

Vcco pins are powered by 2.5V and support the 2.5V I/O standards.

P4 PMC rear I/O connector

64-pin female receptacle header (AMP 120527-1 or equivalent).

64 I/O connections (30 LVDS pairs plus two global clocks).

Vcco pins powered by 2.5V and support the 2.5V I/O standards.

#### ■ Environmental

Operating temperature

XMC-7A200-LF: -40 to 55°C.

Storage temperature

-55 to 125°C.

Relative humidity

5 to 95% non-condensing.

Power

+3.3 Volts

2.1 A typical

+3.3 Aux Volts

17 uA typical

+12/5 Volts (VPWR)

150 mA @ +12V typical

+12 Volts

0.1 mA typical

MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-7KA-EDK is required to configure FPGA.

#### ■ XMC Modules

[XMC-7A200-LF](#)

User-configurable Artix-7 FPGA, 200k logic cells with AXM support

#### ■ Accessories

[AXM-A75](#)

16 analog inputs, 8 analog outputs, and 16 digital I/O

[AXM-A30](#)

2 analog input 100MHz 16-bit A/D channels.

[AXM-D02](#)

30 RS485 differential I/O channels.

[AXM-D03](#)

16 CMOS and 22 RS485 differential I/O channels.

[AXM-D04](#)

30 LVDS I/O channels.

AXM-??

Custom I/O configurations available, call factory

#### ■ Software

For more information, see [www.acromag.com](http://www.acromag.com).

[XMC-7KA-EDK](#)

Engineering Design Kit (one kit required)

[PMCSW-API-VXW](#)

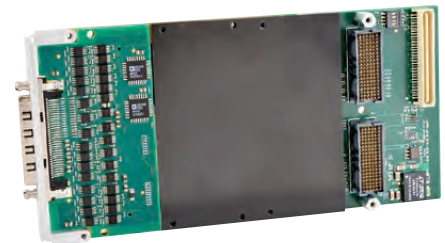
VxWorks® 32-bit software support package

[PCISW-API-WIN](#)

Windows® DLL software support package

[PCISW-API-LNX](#)

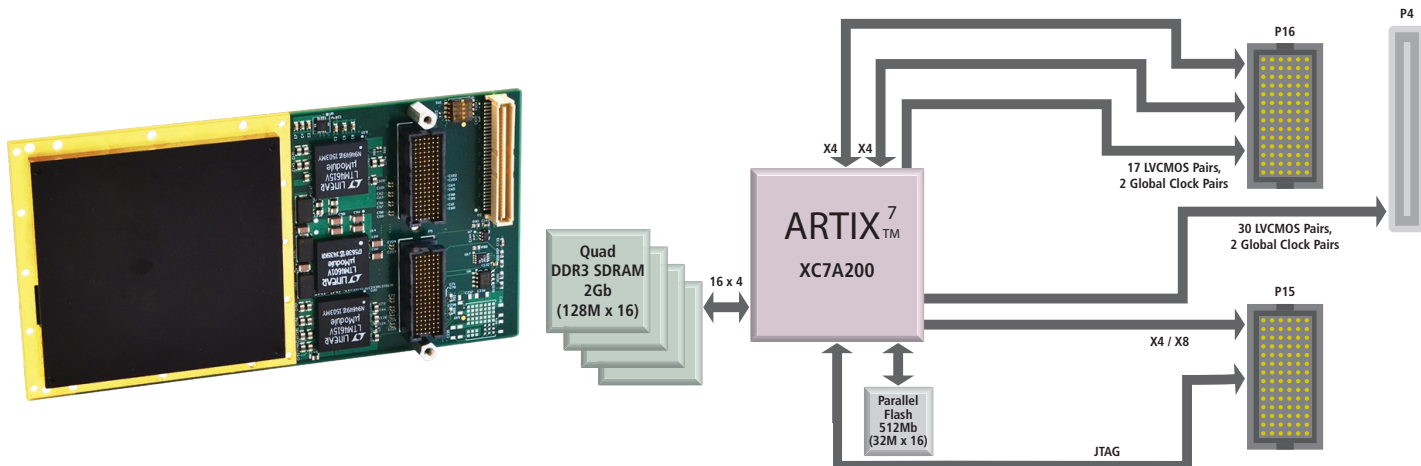
Linux® support (website download only)



XMC-7A200-LF with AXM-A75 and heat sink.



## XMC-7A200CC User-Configurable Conduction-Cooled Artix®-7 FPGA Modules



XMC module with PCIe interface ♦ Logic-optimized Artix-7 FPGA ♦ Conduction-Cooled

### Description

Acromag's **XMC-7A200CC** modules feature a high-performance user-configurable Xilinx® Artix®-7 FPGA enhanced with high-speed memory and a high-throughput serial bus interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

The rear I/O provides an 8-lane high-speed serial interface on the P16 XMC port for customer-installed soft cores. P16 also supports 34 SelectIO channels. The P4 port adds another 60 SelectIO and global clock lines. SelectIO signals are Artix-7 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL)

With Acromag's Artix-7 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with Vivado® or ISE® Design Suite. And with ChipScope™ Pro tools, you can rapidly debug logic and serial interfaces

### Key Features & Benefits

- Reconfigurable Xilinx Artix-7 FPGA with 215K logic cells
- 128M x 64-bit DDR3 SDRAM
- 32M x 16-bit parallel flash memory for MicroBlaze FPGA program code storage
- 4-lane high-speed serial interface on rear P15 connector for PCIe Gen 1/2 (standard), Serial RapidIO, 10Gb Ethernet, Xilinx Aurora
- 8-lane high-speed interfaces on rear P16 connector for customer-installed soft cores
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- DMA support provides data transfer between system memory and the on-board memory
- Support for Xilinx ChipScope™ Pro interface
- Extended temperature conduction-cooled

## XMC-7A200CC User-Configurable Conduction-Cooled Artix-7 FPGA Modules

### Performance Specifications

#### ■ FPGA

FPGA device

Xilinx Artix-7 FPGA.

Model XC7A200T FPGA with 215,360 logic cells and 740 DSP48E1 slices.

FPGA configuration

Download via JTAG or flash memory.

Example FPGA program

IP integrator block diagram provided for bus interface, front & rear I/O control, and SDRAM memory interface controller. See EDK kit.

#### ■ I/O Processing

Rear high-speed I/O

12 high-speed serial lanes.

x4 lanes via P15 and x8 lanes via P16.

Rear user I/O

P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.

P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

#### ■ Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7 series module (see [www.acromag.com](http://www.acromag.com) for more information).

#### ■ XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### ■ Electrical

XMC PCIe bus interface (P15 and P16)

One 114-pin male connector

(Samtec ASP-103614-05 or equivalent).

P15 primary XMC connector

4 differential pairs (PCIe standard, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.

System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin, powers volatile memory to store the bitstream encryption key.

Variable power (5V or 12V): 8 pins at 1A per pin.

P16 XMC connector

8 differential pairs (PCIe, Serial RapidIO, or Xilinx Aurora).

17 LVDS pairs or 34 SelectIO signals (differential pairs grouped per VITA 46.0 X38s).

2 global clock pairs.

Vcco pins are powered by 2.5V and support the 2.5V I/O standards.

P4 PMC rear I/O connector

64-pin female receptacle header

(AMP 120527-1 or equivalent).

64 I/O connections (30 LVDS pairs plus two global clocks).

Vcco pins powered by 2.5V and support the 2.5V I/O standards.

#### ■ Environmental

Operating temperature

XMC-7A200CC-LF: Conduction-cooled, -40 to 75°C.

Storage temperature

-55 to 125°C.

Relative humidity

5 to 95% non-condensing.

Power

3.3V (±5%): 7W typical.

12V (±5%): 2W typical.

3.3V AUX (±5%): 57µW

MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-7KA-EDK is required to configure FPGA.

#### ■ XMC Modules

[Go to on-line ordering page >](#)

XMC-7A200CC-LF

User-configurable Artix-7 FPGA, 215k logic cells, conduction-cooled

#### ■ Software

For more information, see [www.acromag.com](http://www.acromag.com).

XMC-7KA-EDK

Engineering Design Kit (one kit required)

PMCSW-API-VXW

VxWorks® 32-bit software support package

PCISW-API-WIN

Windows® DLL software support package

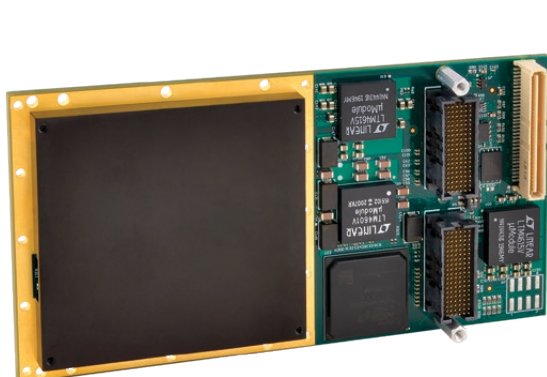
PCISW-API-LNX

Linux® support (website download only)

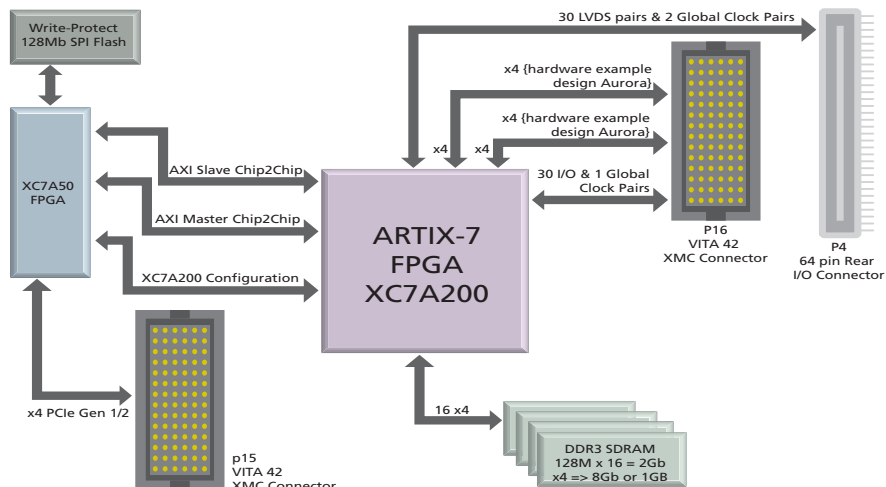


# XMC Modules

## XMC-7AWP User-Configurable Artix®-7 FPGA Modules



ARTIX<sup>7</sup>



XMC module with PCIe interface ♦ Logic-optimized Artix-7 FPGA ♦ Write-protected flash

### Description

Acromag's XMC-7AWP modules feature a high-performance user-configurable Xilinx® Artix®-7 FPGA enhanced with high-speed memory and a high-throughput serial bus interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

For security, the FPGA's configuration flash is write-protected. The XC7A200 is only configurable via PCIe bus or JTAG. There is no configuration memory.

The rear I/O provides an 8-lane high-speed serial interface on the P16 XMC port for customer-installed soft cores. P16 also supports 34 SelectIO channels. The P4 port adds another 60 SelectIO and global clock lines. SelectIO signals are Artix-7 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL)

With Acromag's Artix-7 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with Vivado® or ISE® Design Suite. And with Integrated Logic Analyzer, you can rapidly debug logic and serial interfaces.

### Key Features & Benefits

- Reconfigurable Xilinx Artix-7 FPGA with 200k logic cells
- 128M x 64-bit DDR3 SDRAM
- XC7A50 FPGA bitstream storage flash is write protected via DIP switch selection.
- 4-lane high-speed serial interface on rear P15 connector for PCIe Gen 1/2 (standard), Serial RapidIO, 10Gb Ethernet, Xilinx Aurora
- 8-lane high-speed interfaces on rear P16 connector for customer-installed soft cores
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- DMA support provides data transfer between system memory and the on-board memory

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## XMC-7AWP User-Configurable Artix-7 FPGA Modules

### Performance Specifications

#### ■ FPGA

##### FPGA device

Xilinx® Artix®-7 FPGA.

Model XC7A200T FPGA with 215,360 logic cells and 740 DSP48E1 slices.

##### FPGA configuration

XC7A200 is configurable via PCIe bus or JTAG.

XC7A50 is configured from flash memory or JTAG.

Flash is write protected by default.

##### Example FPGA program

IP integrator block diagram provided for bus interface, front & rear I/O control, and SDRAM memory interface controller. See EDK kit.

#### ■ I/O Processing

##### Rear high-speed I/O

12 high-speed serial lanes.

x8 lanes via P15 and x8 lanes via P16.

##### Rear user I/O

P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.

P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

#### ■ Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7AWP module (see [www.acromag.com](http://www.acromag.com) for more information).

#### ■ XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### ■ Electrical

##### XMC PCIe bus interface (P15 and P16)

One 114-pin male connector

(Samtec ASP-103614-05 or equivalent).

##### P15 primary XMC connector

8 differential pairs (PCIe x4 standard, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.

System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin, powers volatile memory to store the bitstream encryption key.

Variable power (5V or 12V): 8 pins at 1A per pin.

##### P16 XMC connector

8 differential pairs (PCIe, Serial RapidIO, or Xilinx Aurora).

17 LVDS pairs or 34 SelectIO signals (differential pairs grouped per VITA 46.0 X38s).

2 global clock pairs.

Vcco pins are powered by 2.5V and support the 2.5V I/O standards.

##### P4 PMC rear I/O connector

64-pin female receptacle header

(AMP 120527-1 or equivalent).

64 I/O connections (30 LVDS pairs plus two global clocks).

FPGA Vcco pins powered by 2.5V and support 2.5V I/O standards. Optionally can be powered by 3.3V to support 3.3V I/O standards.

#### ■ Environmental

##### Operating temperature

XMC-7AWP: -40 to 75°C cold-plate.

##### Storage temperature

-55 to 125°C.

##### Relative humidity

5 to 95% non-condensing.

##### Power

|                    |                       |
|--------------------|-----------------------|
| +3.3 Volts         | 2.1 A typical         |
| +3.3 Aux Volts     | 17 uA typical         |
| +12/5 Volts (VPWR) | 150 mA @ +12V typical |
| +12 Volts          | 0.1 mA typical        |

##### MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-7AWP-EDK is required to configure FPGA.

#### ■ XMC Modules

[Go to on-line ordering page >](#)

##### XMC-7AWP

User-configurable Artix-7 FPGA, 200k logic cells

#### ■ Software

##### XMC-7AWP-EDK

Engineering Design Kit (one kit required)

##### PMCSW-API-VXW

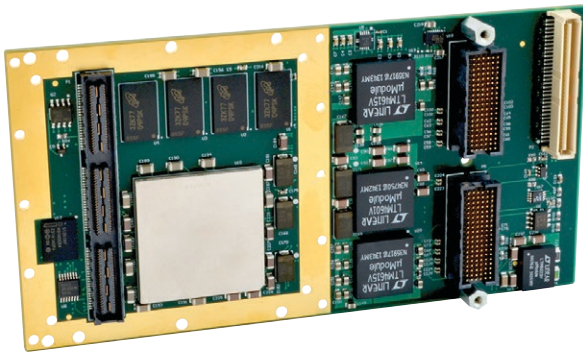
VxWorks® 32-bit software support package

##### PCISW-API-WIN

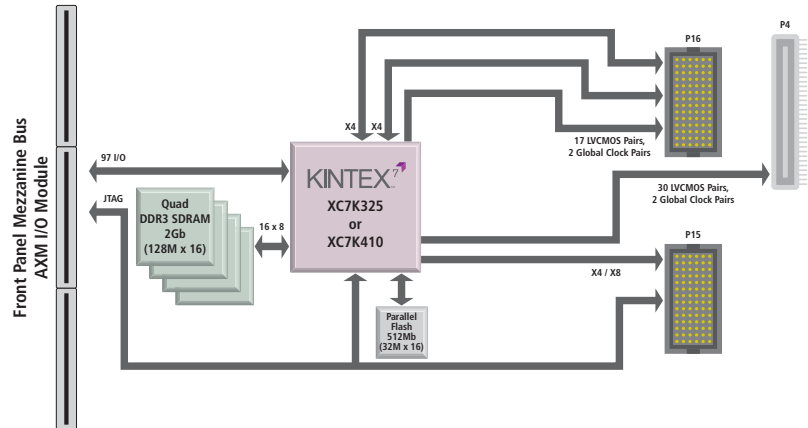
Windows® DLL software support package

##### PCISW-API-LNX

Linux® support (website download only)



KINTEX<sup>7</sup>



XMC module with PCIe interface ♦ Logic-optimized Kintex-7 FPGA ♦ I/O Extension Mezzanine Modules

### Description

Acromag's **XMC-7K** modules feature a high-performance user-configurable Xilinx® Kintex®-7 FPGA enhanced with high-speed memory and a high-throughput serial bus interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

Both front and rear I/O is supported. Front I/O processing is supported with plug-in AXM mezzanine cards. A variety of AXM I/O cards are available to add the flexibility of a wide range of analog and digital I/O to your design.

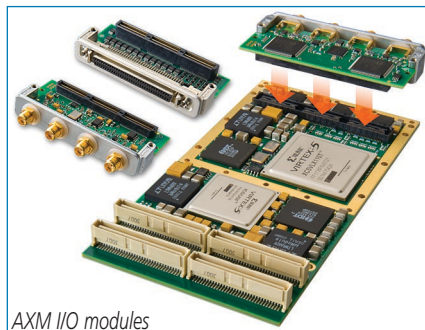
The rear I/O provides an 8-lane high-speed serial interface on the P16 XMC port for customer-installed soft cores. P16 also supports 34 SelectIO channels. The P4 port adds another 60 SelectIO and global clock lines. SelectIO signals are Kintex-7 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL)

Two versions of the Kintex-7 are available, offering a choice of an FPGA device with 325k or 410k logic cells.

With Acromag's Kintex-7 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with Vivado® or ISE® Design Suite. And with ChipScope™ Pro tools, you can rapidly debug logic and serial interfaces



AXM I/O modules

### Key Features & Benefits

- Reconfigurable Xilinx Kintex-7 FPGA with 325k or 410k logic cells
- 128M x 128-bit DDR3 SDRAM
- 32M x 16-bit parallel flash memory for MicroBlaze FPGA program code storage
- 8-lane high-speed serial interface on rear P15 connector for PCIe Gen 1/2 (standard), Serial RapidIO, 10Gb Ethernet, Xilinx Aurora
- 8-lane high-speed interfaces on rear P16 connector for customer-installed soft cores
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- DMA support provides data transfer between system memory and the on-board memory
- Support for Xilinx ChipScope™ Pro interface

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## XMC-7K AX User-Configurable Kintex-7 FPGA Modules w Plug-In I/O

### Performance Specifications

#### ■ FPGA

FPGA device

Xilinx Kintex-7 FPGA.

Model XC7K325T FPGA with 326,080 logic cells and 840 DSP48E1 slices or Model XC7K410T with 406,720 logic cells and 1540 DSP48E1 slices.

FPGA configuration

Download via JTAG or flash memory.

Example FPGA program

IP integrator block diagram provided for bus interface, front & rear I/O control, and SDRAM memory interface controller. See EDK kit.

#### ■ I/O Processing

Acromag AXM I/O Modules:

AXM modules plug into the XMC module's front mezzanine for additional I/O lines. Analog and digital I/O AXM modules are sold separately.

Rear high-speed I/O

12 high-speed serial lanes.

x8 lanes via P15 and x4 lanes via P16.

Rear user I/O

P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.

P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

#### ■ Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7K module (see [www.acromag.com](http://www.acromag.com) for more information).

#### ■ XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### ■ Electrical

XMC PCIe bus interface (P15 and P16)

One 114-pin male connector (Samtec ASP-103614-05 or equivalent).

P15 primary XMC connector

8 differential pairs (PCIe standard, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.

System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin, powers volatile memory to store the bitstream encryption key.

Variable power (5V or 12V): 8 pins at 1A per pin.

P16 XMC connector

4 differential pairs (PCIe, Serial RapidIO, or Xilinx Aurora).

17 LVDS pairs or 34 SelectIO signals (differential pairs grouped per VITA 46.0 X38s).

2 global clock pairs.

Vcco pins are powered by 2.5V and support the 2.5V I/O standards.

P4 PMC rear I/O connector

64-pin female receptacle header

(AMP 120527-1 or equivalent).

64 I/O connections (30 LVDS pairs plus two global clocks).

Vcco pins powered by 2.5V and support the 2.5V I/O standards.

#### ■ Environmental

Operating temperature

XMC-7K325AX-LF: -40 to 45°C.

XMC-7K410AX-LF: -40 to 40°C

Storage temperature

-55 to 125°C.

Relative humidity

5 to 95% non-condensing.

Power

3.3V (±5%): 7.8W typical.

12V (±5%): 2.7W typical

3.3V AUX (±5%): 57μW

MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-7K-EDK is required to configure FPGA.

#### ■ XMC Modules

[XMC-7K325AX-LF](#)

User-configurable Kintex-7 FPGA, 325k logic cells with AXM support

[XMC-7K410AX-LF](#)

User-configurable Kintex-7 FPGA, 410k logic cells with AXM support

#### ■ Accessories

[AXM-A75](#)

16 analog inputs, 8 analog outputs, and 16 digital I/O

[AXM-A30](#)

2 analog input 100MHz 16-bit A/D channels.

[AXM-D02](#)

30 RS485 differential I/O channels.

[AXM-D03](#)

16 CMOS and 22 RS485 differential I/O channels.

[AXM-D04](#)

30 LVDS I/O channels.

AXM-??

Custom I/O configurations available, call factory.

#### ■ Software

[XMC-7KA-EDK](#)

Engineering Design Kit (one kit required)

[PMCSW-API-VXW](#)

VxWorks® 32-bit software support package

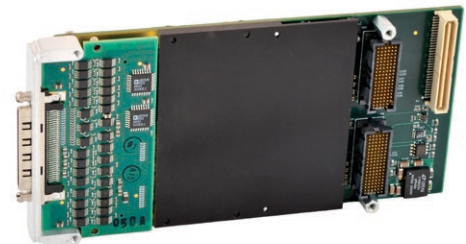
[PCISW-API-WIN](#)

Windows® DLL software support package

[PCISW-API-LNX](#)




Linux™ support (website download only)

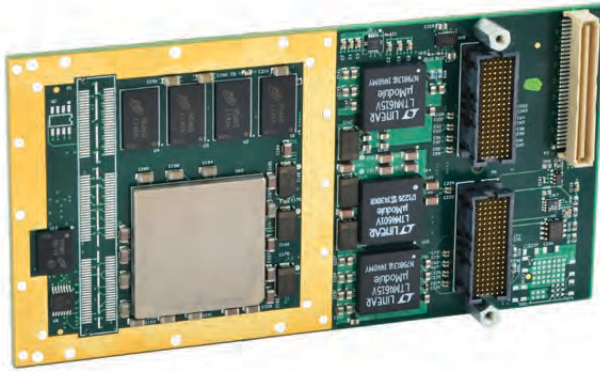
XMC-7K325AX-LF shown with optional AXM-A75



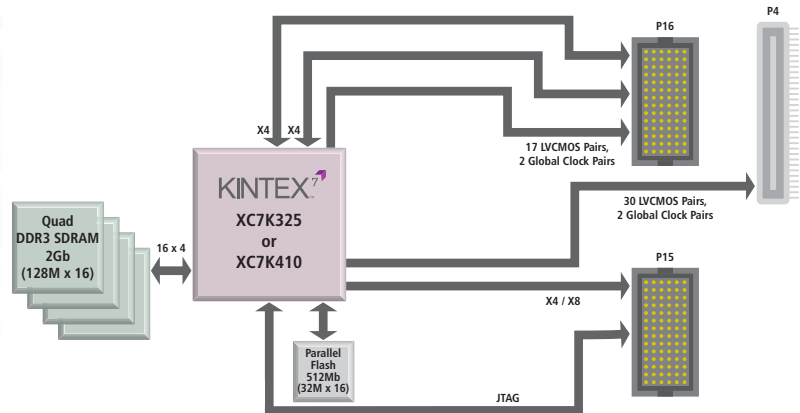


# XMC Modules

**XMC-7K CC** User-Configurable Conduction-Cooled Kintex-7 FPGA Modules   



**KINTEX<sup>7</sup>**



**XMC module with PCIe interface ♦ Logic-optimized Kintex-7 FPGA ♦ Conduction-Cooled**

## Description

Acromag's **XMC-7K** modules feature a high-performance user-configurable Xilinx® Kintex®-7 FPGA enhanced with high-speed memory and a high-throughput serial bus interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

The rear I/O provides an 8-lane high-speed serial interface on the P16 XMC port for customer-installed soft cores. P16 also supports 34 SelectIO channels. The P4 port adds another 60 SelectIO and global clock lines. SelectIO signals are Kintex-7 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL)

Two versions of the Kintex-7 are available, offering a choice of an FPGA device with 325k or 410k logic cells.

With Acromag's Kintex-7 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with Vivado® or ISE® Design Suite. And with ChipScope™ Pro tools, you can rapidly debug logic and serial interfaces

## Key Features & Benefits

- Reconfigurable Xilinx Kintex-7 FPGA with 325k or 410k logic cells
- 128M x 64-bit DDR3 SDRAM
- 32M x 16-bit parallel flash memory for MicroBlaze FPGA program code storage
- 8-lane high-speed serial interface on rear P15 connector for PCIe Gen 1/2 (standard), Serial RapidIO, 10Gb Ethernet, Xilinx Aurora
- 8-lane high-speed interfaces on rear P16 connector for customer-installed soft cores
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- DMA support provides data transfer between system memory and the on-board memory
- Support for Xilinx ChipScope™ Pro interface
- Extended temperature conduction-cooled

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## XMC-7K CC User-Configurable Conduction-Cooled Kintex-7 FPGA Modules

### Performance Specifications

#### FPGA

FPGA device

Xilinx Kintex-7 FPGA.

Model XC7K325T FPGA with 326,080 logic cells and 840 DSP48E1 slices or Model XC7K410T with 406,720 logic cells and 1540 DSP48E1 slices.

FPGA configuration

Download via JTAG or flash memory.

Example FPGA program

IP integrator block diagram provided for bus interface, front & rear I/O control, and SDRAM memory interface controller. See EDK kit.

#### I/O Processing

Rear high-speed I/O

16 high-speed serial lanes.

x8 lanes via P15 and x8 lanes via P16.

Rear user I/O

P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.

P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

#### Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7K module (see [www.acromag.com](http://www.acromag.com) for more information).

#### XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### Electrical

XMC PCIe bus interface (P15 and P16)

One 114-pin male connector (Samtec ASP-103614-05 or equivalent).

P15 primary XMC connector

8 differential pairs (PCIe standard, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.

System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin, powers volatile memory to store the bitstream encryption key.

Variable power (5V or 12V): 8 pins at 1A per pin.

P16 XMC connector

4 differential pairs (PCIe, Serial RapidIO, or Xilinx Aurora).

17 LVDS pairs or 34 SelectIO signals (differential pairs grouped per VITA 46.0 X38s).

2 global clock pairs.

Vcco pins are powered by 2.5V and support the 2.5V I/O standards.

P4 PMC rear I/O connector

64-pin female receptacle header (AMP 120527-1 or equivalent).

64 I/O connections (30 LVDS pairs plus two global clocks).

Vcco pins powered by 2.5V and support the 2.5V I/O standards.

#### Environmental

Operating temperature

XMC-7K325AX-LF: Conduction-cooled, -40 to 70°C.

XMC-7K410AX-LF: Conduction-cooled, -40 to 70°C

Storage temperature

-55 to 125°C.

Relative humidity

5 to 95% non-condensing.

Power

3.3V (±5%): 7.8W typical.

12V (±5%): 2.7W typical.

3.3V AUX (±5%): 57µW

MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-7K-EDK is required to configure FPGA.

#### XMC Modules

[XMC-7K325CC-LF](#)

User-configurable Kintex-7 FPGA, 325k logic cells, conduction-cooled

[XMC-7K410CC-LF](#)

User-configurable Kintex-7 FPGA, 410k logic cells, conduction-cooled

#### Software

[XMC-7KA-EDK](#)

Engineering Design Kit (one kit required)

[PMCSW-API-VXW](#)

VxWorks® 32-bit software support package

[PCISW-API-WIN](#)

Windows® DLL software support package

[PCISW-API-LNX](#)

Linux™ support (website download only)

XMC-7K325CC-LF shown with heatsink



ISO9001  
AS9100

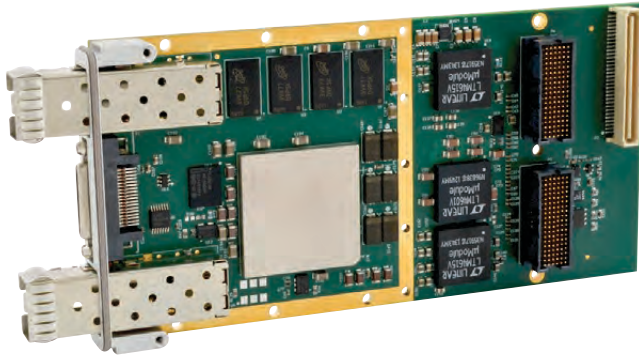


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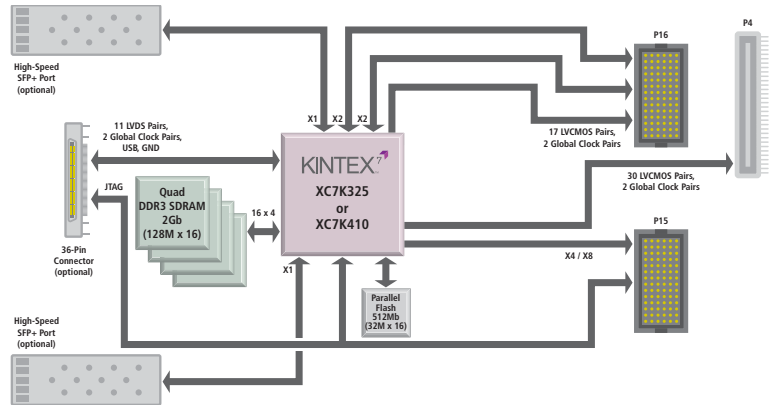
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# XMC Modules

## XMC-7K F User-Configurable Kintex-7 FPGA Modules with Dual SFP+ Ports



KINTEX<sup>7</sup>



### XMC module with PCIe and SFP+/Aurora interface ♦ Logic-optimized Kintex-7 FPGA ♦ 10-Gigabit Ethernet

#### Description

Acromag's **XMC-7K** modules feature a high-performance user-configurable Xilinx® Kintex®-7 FPGA enhanced with high-speed memory and a high-throughput serial interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

Two versions of this module are available, offering a choice of an FPGA device with 325k or 410k logic cells.

Front I/O adds dual SFP+ ports and a VHDCR connector. The two SFP+ ports each provide a copper or fibre interface of up to 10.3125Gbps. They also support a Gigabit Ethernet interface. The VHDCR connector interfaces JTAG, USB, and 22 SelectIO.

The rear I/O provides an 4-lane high-speed serial interface on the P16 XMC port for customer-installed soft cores. P16 also supports 34 SelectIO channels. The P4 port adds another 60 SelectIO and global clock lines. SelectIO signals are Kintex-7 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL).

With Acromag's Kintex-7 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with Vivado® or ISE® Design Suite. And with ChipScope™ Pro tools, you can rapidly debug logic and serial interfaces

#### Key Features & Benefits

- Reconfigurable Xilinx Kintex-7 FPGA with 325k or 410k logic cells
- 128M x 64-bit DDR3 SDRAM
- 32M x 16-bit parallel flash memory for MicroBlaze FPGA program code storage
- 8-lane high-speed serial interface on rear P15 connector for PCIe Gen 1/2 (standard), Serial RapidIO, 10Gb Ethernet, Xilinx Aurora
- 4-lane high-speed interfaces on rear P16 connector for customer-installed soft cores
- Dual SFP+ ports for Fibre Channel or 10GbE
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- 22 SelectIO, 2 global clock pairs, JTAG, USB, and ground signals via front 36-pin connector
- DMA support provides data transfer between system memory and the on-board memory
- Support for Xilinx ChipScope™ Pro interface

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## XMC-7K F User-Configurable Kintex-7 FPGA Modules w Dual SFP+ Ports

### Performance Specifications

#### ■ FPGA

##### FPGA device

Xilinx Kintex-7 FPGA.

Model XC7K325T FPGA with 326,080 logic cells and 840 DSP48E1 slices or Model XC7K410T with 406,720 logic cells and 1540 DSP48E1 slices.

##### FPGA configuration

Download via JTAG or flash memory.

##### Example FPGA program

IP integrator block diagram provided for bus interface, front & rear I/O control, and SDRAM memory interface controller. See EDK kit.

#### ■ I/O Processing

##### Front high-speed I/O

Two x1 lanes via SFP+ connectors for Gigabit Ethernet and Fibre Channel interface

##### Front user I/O

36-pin connector provides JTAG connection, USB signals, 2 global differential clock pairs, 11 LVDS signal pairs, and 2 ground signals.

##### Rear high-speed I/O

12 high-speed serial lanes.

x8 lanes via P15 and x4 lanes via P16.

##### Rear user I/O

P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.

P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

#### ■ Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7K module (see [www.acromag.com](http://www.acromag.com) for more information).

#### ■ XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### ■ Electrical

##### XMC PCIe bus interface (P15 and P16)

One 114-pin male connector (Samtec ASP-103614-05 or equivalent).

##### P15 primary XMC connector

8 differential pairs (PCIe standard, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.

System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin for system management.

Variable power (5V or 12V): 8 pins at 1A per pin.

##### P16 XMC connector

4 differential pairs (PCIe, Serial RapidIO, or Xilinx Aurora).

17 LVDS pairs or 34 SelectIO signals (differential pairs grouped per VITA 46.0 X38s).

2 global clock pairs.

Vcco pins are powered by 2.5V and support the 2.5V I/O standards.

##### P4 PMC rear I/O connector

64-pin female receptacle header (AMP 120527-1 or equivalent).

64 I/O connections (30 LVDS pairs plus two global clocks).

Vcco pins powered by 2.5V and support the 2.5V I/O standards.

##### VHDCR connector

36-position connector (Samtec VHDCR-36-01-M-RA) mates with industry-standard VHDCI cable assemblies.

##### SFP+ host connector

SFP transceiver signals route directly to Kintex-7 FPGA. 10.3125Gb/s maximum data rate.

SFP+ copper (Gigabit Ethernet) or fibre optic modules available from Acromag.

#### ■ Environmental

##### Operating temperature

XMC-7K325F-LF: -40 to 55°C.

XMC-7K410F-LF: -40 to 55°C.

##### Storage temperature

-55 to 125°C.

##### Relative humidity

5 to 95% non-condensing.

##### Power

3.3V (±5%): 7.8W typical.

12V (±5%): 2.7W typical.

3.3V AUX (±5%): 57μW typical.

##### MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-7K-EDK is required to configure FPGA.

#### ■ XMC Modules

##### [XMC-7K325F-LF](#)

User-configurable Kintex-7 FPGA, 325k logic cells plus SFP front I/O

##### [XMC-7K410F-LF](#)

User-configurable Kintex-7 FPGA, 410k logic cells plus SFP front I/O

#### ■ Accessories

##### [5025-921](#)

Cable, VHDCI 36-pin to SCSI-2, 6 feet long.

##### [5028-449](#)

Cable, copper twin-ax, SFP to SFP, 1 meter long.

##### [5028-455](#)

Transceiver, 10/100/1000BASE-T copper SFP, up to 1.25Gb/s bi-directional data links.

##### [5028-452](#)

Transceiver, short-wavelength SFP, up to 2.125Gb/s bi-directional data links.

#### ■ Software

##### [XMC-7KA-EDK](#)

Engineering Design Kit (one kit required)

##### [PMCSW-API-VXW](#)

VxWorks® 32-bit software support package

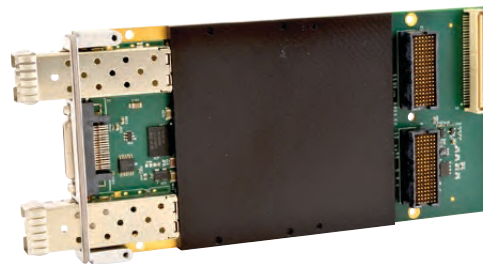
##### [PCISW-API-WIN](#)

Windows® DLL software support package

##### [PCISW-API-LNX](#)

Linux® support (website download only)

XMC-7K325F-LF shown with heatsink



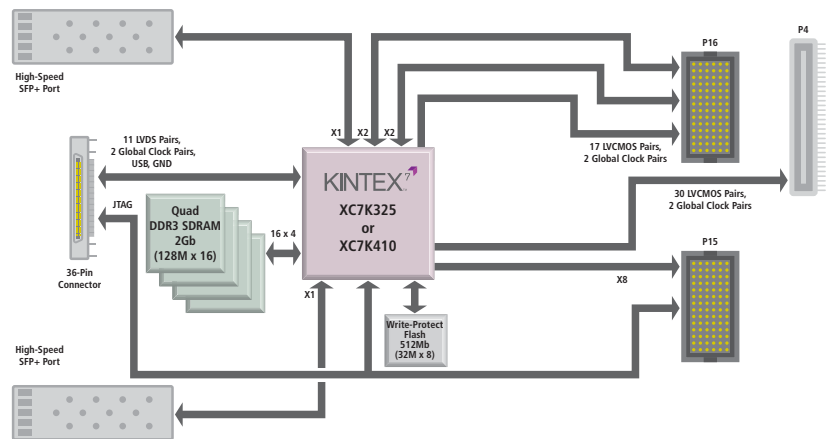


# XMC Modules

## XMC-7KWP User-Configurable Kintex-7 FPGA Modules with Dual SFP+ Ports



KINTEX<sup>7</sup>



XMC module ♦ Kintex-7 FPGA ♦ 10-Gigabit Ethernet ♦ Write-protected flash

### Description

Acromag's XMC-7KWP modules feature a high-performance user-configurable Xilinx® Kintex®-7 FPGA enhanced with high-speed memory and a high-throughput serial interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing. For security, the FPGA's configuration flash is write-protected.

Two versions of this module are available, offering a choice of an FPGA device with 325k or 410k logic cells.

Front I/O adds dual SFP+ ports and a VHDCR connector. The two SFP+ ports each provide a copper or fibre interface of up to 10.3125Gbps. They also support a Gigabit Ethernet interface. The VHDCR connector interfaces JTAG, USB, and 22 SelectIO.

The rear I/O provides 4-lane high-speed serial interface on the P16 XMC port for customer-installed soft cores. P16 also supports 34 SelectIO channels. The P4 port adds another 60 SelectIO and global clock lines. SelectIO signals are Kintex-7 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL).

With Acromag's Kintex-7 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with Vivado® or ISE® Design Suite. And with ChipScope™ Pro tools, you can rapidly debug logic and serial interfaces.

### Key Features & Benefits

- Reconfigurable Xilinx Kintex-7 FPGA with 325k or 410k logic cells
- 128M x 64-bit DDR3 SDRAM
- 32M x 16-bit parallel flash memory for MicroBlaze FPGA program code storage
- FPGA bitstream storage flash write-protected unless access jumper installed
- 8-lane high-speed serial interface on rear P15 connector for PCIe Gen 1/2 (standard), Serial RapidIO, 10Gb Ethernet, Xilinx Aurora
- 4-lane high-speed interfaces on rear P16 connector for customer-installed soft cores
- Dual SFP+ ports for Fibre Channel or 10GbE
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- 22 SelectIO, 2 global clock pairs, JTAG, USB, and ground signals via front 36-pin connector
- DMA support provides data transfer between system memory and the on-board memory
- Support for Xilinx ChipScope™ Pro interface

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## XMC-7KWP User-Configurable Kintex-7 FPGA Modules w Dual SFP+ Ports

### Performance Specifications

#### FPGA

FPGA device

Xilinx Kintex-7 FPGA.

Model XC7K325T FPGA with 326,080 logic cells and 840 DSP48E1 slices or Model XC7K410T with 406,720 logic cells and 1540 DSP48E1 slices.

#### FPGA configuration

Download via JTAG or flash memory. Installation of 2mm pitch jumper shunt required for writing to flash memory.

#### Example FPGA program

IP integrator block diagram provided for bus interface, front & rear I/O control, and SDRAM memory interface controller. See EDK Kit.

#### I/O Processing

##### Front high-speed I/O

Two x1 lanes via SFP+ connectors for Gigabit Ethernet and Fibre Channel interface.

##### Front user I/O

36-pin connector provides JTAG connection, USB signals, 2 global differential clock pairs, 11 LVDS signal pairs, and 2 ground signals.

##### Rear high-speed I/O

12 high-speed serial lanes.

x8 lanes via P15 and x4 lanes via P16.

##### Rear user I/O

P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.

P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

#### Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7K module (see [www.acromag.com](http://www.acromag.com) for more information).

#### XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### Electrical

XMC PCIe bus interface (P15 and P16)

One 114-pin male connector

(Samtec ASP-103614-05 or equivalent).

##### P15 primary XMC connector

8 differential pairs (PCIe standard, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.

System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin for system management.

Variable power (5V or 12V): 8 pins at 1A per pin.

##### P16 XMC connector

4 differential pairs (PCIe, Serial RapidIO, or Xilinx Aurora).

17 LVDS pairs or 34 SelectIO signals (differential pairs grouped per VITA 46.0 X38s).

2 global clock pairs.

Vcco pins are powered by 2.5V and support the 2.5V I/O standards.

##### P4 PMC rear I/O connector

64-pin female receptacle header

(AMP 120527-1 or equivalent).

64 I/O connections (30 LVDS pairs plus two global clocks).

Vcco pins powered by 2.5V and support the 2.5V I/O standards.

##### VHDCR connector

36-position connector (Samtec VHDCR-36-01-M-RA) mates with industry-standard VHDCI cable assemblies.

##### SFP+ host connector

SFP transceiver signals route directly to Kintex-7 FPGA.

10.3125Gb/s maximum data rate.

SFP+ copper (Gigabit Ethernet) or fibre optic modules available from Acromag.

##### JTAG voltage level

2.5V default.

Resistor stuff option for 3.3V (consult factory).

#### Environmental

##### Operating temperature

XMC-7KWP-325F: -40 to 55°C.

XMC-7KWP-410F: -40 to 55°C.

##### Storage temperature

-55 to 125°C.

##### Relative humidity

5 to 95% non-condensing.

##### Power

3.3V (±5%): 7.8W typical.

12V (±5%): 2.7W typical.

3.3V AUX (±5%): 57μW typical.

##### MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-7KA-EDK is required to configure FPGA.

#### XMC Modules

[Go to on-line ordering page >](#)

##### XMC-7KWP-325F

User-configurable Kintex-7 FPGA, 325k logic cells plus SFP front I/O, write protected flash

##### XMC-7KWP-410F

User-configurable Kintex-7 FPGA, 410k logic cells plus SFP front I/O, write protected flash

#### Accessories

##### 5025-921

Cable, VHDCI 36-pin to SCSI-2, 6 feet long.

##### 5028-449

Cable, copper twin-ax, SFP to SFP, 1 meter long.

##### 5028-455

Transceiver, 10/100/1000BASE-T copper SFP, up to 1.25Gb/s bi-directional data links.

##### 5028-452

Transceiver, short-wavelength SFP, up to 2.125Gb/s bi-directional data links.

#### Software

##### XMC-7KA-EDK

Engineering Design Kit (one kit required)

##### PMCSW-API-VXW

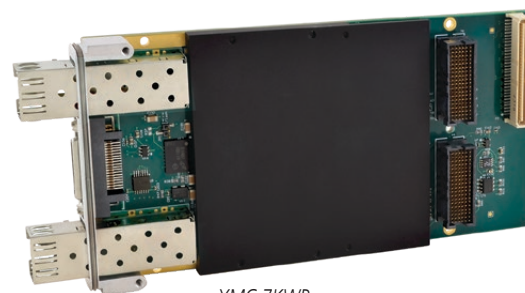
VxWorks® 32-bit software support package

##### PCISW-API-WIN

Windows® DLL software support package

##### PCISW-API-LNX

Linux® support (website download only)



XMC-7KWP

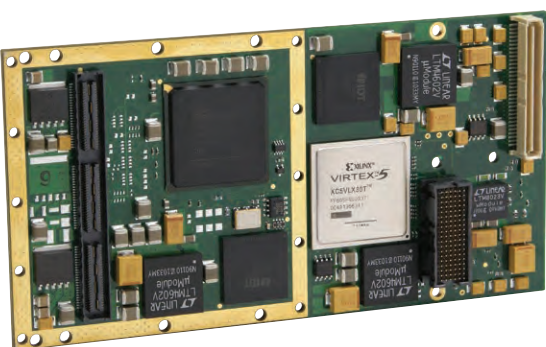
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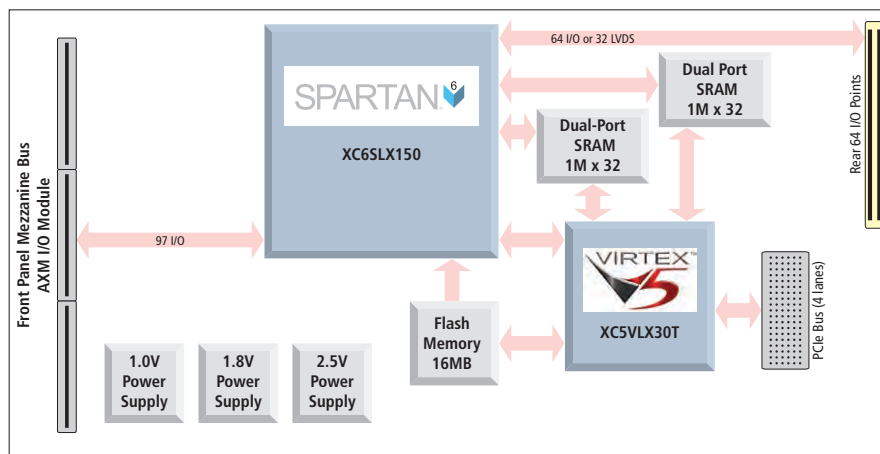
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## XMC-SLX User-Configurable Spartan-6 FPGA Modules with Plug-In I/O



SPARTAN<sup>6</sup>



### XMC module with PCIe interface ♦ Logic-optimized Spartan-6 FPGA ♦ I/O extension mezzanine modules

#### Description

Acromag's cost-effective [XMC-SLX](#) modules feature a user-configurable Xilinx® Spartan®-6 FPGA enhanced with high-speed memory and a high-throughput PCIe interface. Field I/O interfaces to the FPGA via the rear J4/P4 connector and/or with optional front mezzanine plug-in I/O modules. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

Large, high-speed memory banks enable efficient data handling. The dual-port SRAM facilitates high-speed DMA transfers to the bus or CPU. A high-bandwidth PCIe interface ensures fast data throughput.

64 I/O lines are accessible through the rear (J4) connector. Additional I/O processing is supported on a separate mezzanine card that plugs into the FPGA base board. A variety of these external AXM I/O cards are available to interface your analog and digital I/O signals.

Take advantage of the conduction-cooled design for use in hostile environments. Conduction efficiently dissipates heat if there is inadequate cooling air flow. Optional extended temperature models operate reliably from -40 to 85°C.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board VHDL debugging.



Plug in an AXM analog or digital I/O module for additional I/O signal processing capabilities.



VPX air-cooled and REDI versions are available

#### Key Features & Benefits

- Reconfigurable Xilinx Spartan-6 FPGA with 147,433 logic cells
- PCIe bus 4-lane Gen 1 interface
- 256k x 64-bit dual-ported SRAM provides direct links from the PCIe bus and to the FPGA (optional 1M x 64-bit)
- Supports both front and rear I/O connections
- 64 I/O or 32 LVDS lines direct to FPGA via rear (J4) connector
- Plug-in I/O extension modules are available for the front mezzanine
- FPGA code loads from the PCIe bus or from flash memory
- Other memory options available (call factory)
- Supports dual DMA channel data transfer to the CPU/bus
- Support for Xilinx ChipScope™ Pro interface
- Designed for conduction-cooled host card or -40 to 85°C operation in air-cooled systems

**Acromag**   
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## XMC-SLX User-Configurable Spartan-6 FPGA Modules with Plug-In I/O

### Performance Specifications

#### FPGA

##### FPGA Device

Xilinx Spartan-6 FPGA.

Model XC6SLX150-3FG676 FPGA with 147,433 logic cells and 180 DSP48A1 slices.

##### FPGA configuration

Download via PCIe bus or flash memory.

##### Example FPGA program

VHDL provided for bus interface, front & rear I/O control, SRAM read/write interface logic, and SDRAM memory interface controller. See EDK kit.

#### I/O Processing

Acromag AXM I/O modules:

AXM modules plug into the XMC module's front mezzanine for additional I/O lines. Analog and digital I/O AXM modules are sold separately.

##### Rear I/O

64 I/O (32 LVDS) lines supported with a direct connection between the FPGA and the rear I/O connector (J4).

#### Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-SLX module (see [www.acromag.com](http://www.acromag.com) for more information).

#### XMC Compliance

Conforms to PCI Express 1.1a electrical and protocol standards. 2.5Gbps data rate per lane per direction.

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### Environmental

##### Operating temperature

-0 to 70°C or -40 to 85°C (E versions).

##### Storage temperature

-55 to 125°C.

##### Relative humidity

5 to 95% non-condensing.

##### Power

3.3V (±5%): 700mA typical, 840mA maximum.

12V (±5%): 640mA typical, 804mA maximum.

##### MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-SLX-EDK is required to configure FPGA.

#### XMC Modules

##### XMC-SLX150

User-configurable Spartan-6 FPGA, 150k logic cells, 256 x 64-bit dual-port SRAM

##### XMC-SLX150E

Same as XMC-SLX150 with extended temp. range

##### XMC-SLX150-1M

User-configurable Spartan-6 FPGA, 150k logic cells, 1M x 64-bit dual-port SRAM

##### XMC-SLX150E-1M

Same as XMC-SLX150-1M with extended temp. range

#### AXM Plug-In I/O Extension Modules

For more information, see [www.acromag.com](http://www.acromag.com).

##### AXM-A30

2 analog input 100MHz 16-bit A/D channels

##### AXM-D02

30 RS485 differential I/O channels

##### AXM-D03

16 CMOS and 22 RS485 differential I/O channels

##### AXM-D04

30 LVDS I/O channels

##### AXM-??

Custom I/O configurations available, call factory.

#### Software

For more information, see [www.acromag.com](http://www.acromag.com).

##### XMC-SLX-EDK

Engineering Design Kit (one kit required)

##### PMCSW-API-VXW

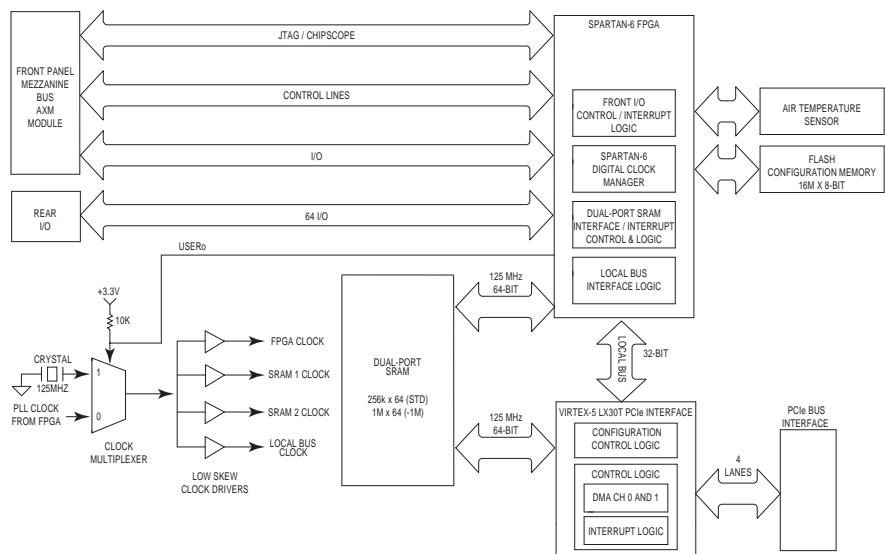
VxWorks® software support package

##### PCISW-API-WIN

Windows® DLL software support package

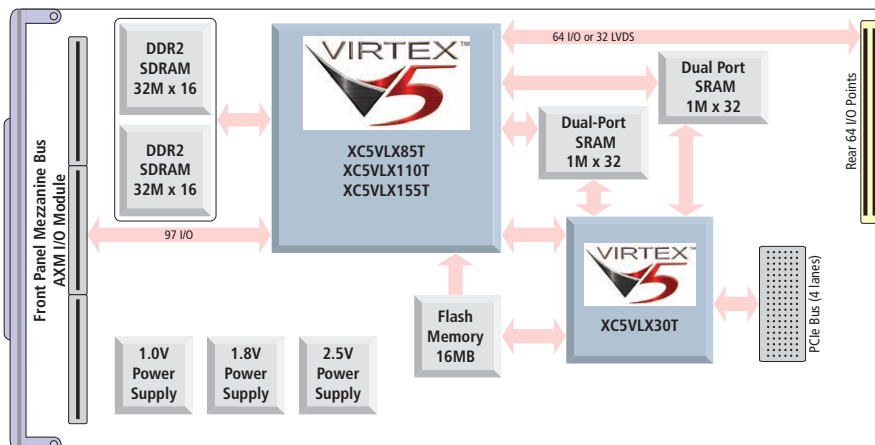
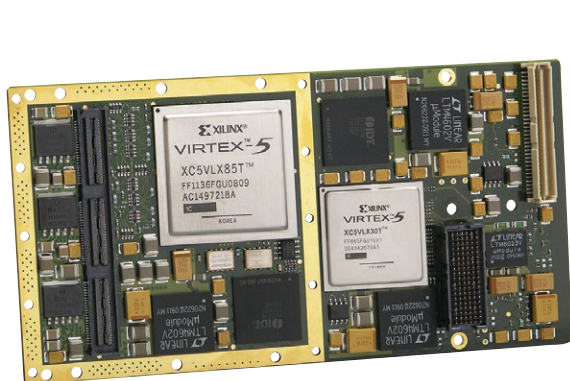
##### PCISW-API-LNX

Linux® support (website download only)





## XMC-VLX User-Configurable Virtex-5 FPGA Modules with Plug-In I/O



### XMC module with PCIe interface ♦ Logic-optimized Virtex-5 FPGA ♦ I/O extension mezzanine modules

#### Description

##### Models

XMC-VLX85: 85k logic cells  
XMC-VLX110: 110k logic cells  
XMC-VLX155: 155k logic cells

Acromag's XMC-VLX mezzanine modules feature a configurable Xilinx® Virtex™-5 FPGA enhanced with multiple high-speed memory buffers and a high-throughput PCIe interface. Field I/O interfaces to the FPGA via the rear J4/P4 connector and/or with optional front mezzanine plug-in I/O modules. The result is a powerful and flexible I/O processor module that is capable of executing your custom instruction sets and algorithms.

Three models provide a choice of logic-optimized FPGAs to match your performance requirements. Although there is no limit to the uses for these boards, several applications are ideal. Typical uses include hardware simulation, military servers, communications, in-circuit diagnostics, signal intelligence, and image processing.

64 I/O lines are accessible through the rear (J4) connector. Additional I/O processing is supported on a separate mezzanine card that plugs into the FPGA base board. A variety of these external I/O cards are available to interface for your analog and digital I/O signals.

Large, high-speed memory banks provide efficient data handling. Generous DDR2 SDRAM buffers store captured data prior to FPGA processing. Afterward, data is moved to dual-port SRAM for high-speed DMA transfer to the bus or CPU. Our high-bandwidth PCIe interface ensures fast data throughput.

Take advantage of the conduction-cooled design for use in hostile environments. Conduction efficiently dissipates heat if there is inadequate cooling air flow. Optional extended temperature models operate reliably from -40 to 85°C.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board VHDL debugging.



Plug in an AXM analog or digital I/O module for additional I/O signal processing capabilities.

#### Key Features & Benefits

- Reconfigurable Xilinx Virtex-5 FPGA
- PCIe bus 4-lane Gen 1 interface
- Supports both front and rear I/O connections
- 64 I/O or 32 LVDS lines direct to FPGA via rear (J4) connector
- Plug-in I/O extension modules are available for the front mezzanine
- FPGA code loads from the PCIe bus or from flash memory
- 1M x 64-bit dual-ported SRAM provides direct links from the PCIe bus and to the FPGA
- 32M x 32-bit DDR2 SDRAM is directly accessed through the FPGA
- Other memory options available (call factory)
- Supports dual DMA channel data transfer to the CPU/bus
- Support for Xilinx ChipScope™ Pro interface
- Designed for conduction-cooled host card or -40 to 85°C operation in air-cooled systems

## XMC-VLX User-Configurable Virtex-5 FPGA Modules with Plug-In I/O

### Performance Specifications

#### FPGA

##### FPGA Device

Xilinx Virtex-5 FPGA.

##### Model XMC-VLX85:

XC5VLX85T-1FF1136 FPGA with 82,944 logic cells and 48 DSP48E slices.

##### Model XMC-LX110:

XC5VLX110T-1FF1136 FPGA with 110,592 logic cells and 64 DSP48E slices.

##### Model XMC-LX155:

XC5VLX155T-1FF1136 FPGA with 155,648 logic cells and 128 DSP48E slices.

##### FPGA configuration

Download via PCIe bus or flash memory.

##### Example FPGA program

VHDL provided for bus interface, front & rear I/O control, SRAM read/write interface logic, and SDRAM memory interface controller. See EDK kit.

#### I/O Processing

##### Acromag AXM I/O modules:

AXM modules plug into the XMC module's front mezzanine for additional I/O lines. Analog and digital I/O AXM modules are sold separately.

##### Rear I/O

64 I/O (32 LVDS) lines supported with a direct connection between the FPGA and the rear I/O connector (J4).

#### Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-VLX module (see [www.acromag.com](http://www.acromag.com) for more information).

#### XMC Compliance

Conforms to PCI Express 1.1a electrical and protocol standards. 2.5Gbps data rate per lane per direction.

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### Environmental

##### Operating temperature

-0 to 70°C or -40 to 85°C (E versions).

##### Storage temperature

-55 to 125°C.

##### Relative humidity

5 to 95% non-condensing.

##### Power

3.3V (±5%): 700mA typical, 840mA maximum  
+12V (±5%): 820mA typical, 984mA maximum

##### MTBF

Contact the factory.

### Ordering Information

#### XMC Modules

[Go to on-line order page >](#)

##### XMC-VLX85

User-configurable Virtex-5 FPGA, 85k logic cells

##### XMC-VLX85E\*

Same as XMC-VLX85 with extended temp. range

##### XMC-VLX110\*

User-configurable Virtex-5 FPGA, 110k logic cells

##### XMC-VLX110E

Same as XMC-VLX110 with extended temp. range

##### XMC-VLX155

User-configurable Virtex-5 FPGA, 155k logic cells

##### XMC-VLX155E

Same as XMC-VLX155 with extended temp. range

##### XMC-VLX-EDK

Engineering Design Kit (one kit required)

\* Consult factory for long-term availability.

#### AXM Plug-In I/O Extension Modules

For more information, see [www.acromag.com](http://www.acromag.com).

##### AXM-A30

2 analog input 100MHz 16-bit A/D channels

##### AXM-D02

30 RS485 differential I/O channels

##### AXM-D03

16 CMOS and 22 RS485 differential I/O channels

##### AXM-D04

30 LVDS I/O channels

##### AXM-??

Custom I/O configurations available, call factory.

#### Software

For more information, see [www.acromag.com](http://www.acromag.com).

##### PMCSW-API-VXW

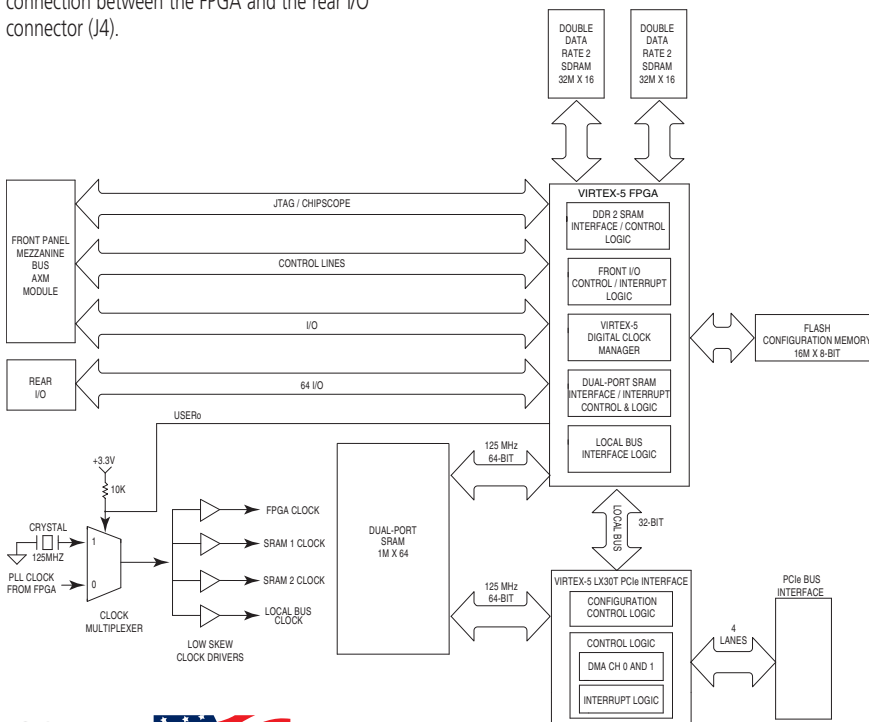
VxWorks® software support package

##### PCISW-API-WIN

Windows® DLL software support package

##### PCISW-API-LNX

Linux™ support (website download only)



ISO9001  
AS9100

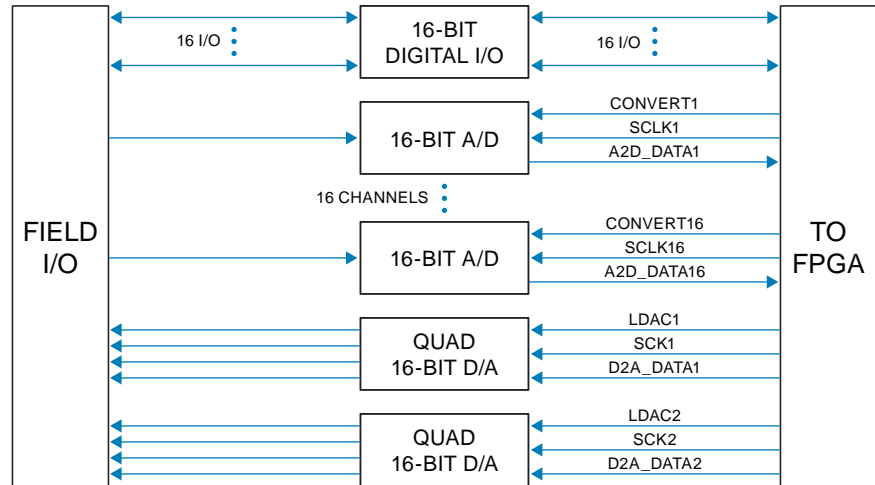
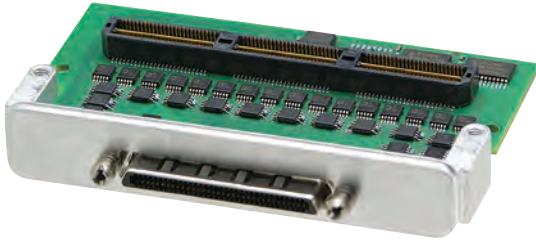


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# Extension I/O Modules

## AXM-A75 Multi-function I/O extension module for Acromag FPGA cards



16 analog inputs, simultaneous A/D ♦ 8 analog outputs, simultaneous D/A ♦ 16 digital I/O channels

### Description

The AXM-75 is a multi-function I/O module that adds A/D, D/A, and digital I/O signal processing functions to an FPGA board. These extension I/O modules plug directly onto many Acromag reconfigurable FPGA cards equipped with an AXM mezzanine connector.

### Analog Input

There are sixteen differential analog input channels on the AXM-A75. Each input has its own high-speed 16-bit A/D converter offering the ability to simultaneously sample all channels.

At the beginning of the analog signal chain is a low-pass filter to remove any unwanted EMI. A programmable gain instrumentation amplifier scales the input and provides giga-ohm input impedance. Serial FLASH memory is included to store factory calibration constants.

### Analog Output

Two quad serial input DAC devices drive eight analog output channels. Each channel has its own high-speed 16-bit D/A converter allowing simultaneous updates to all outputs.

### Digital I/O

Sixteen bi-directional digital I/O channels provide the ability to monitor and control discrete devices. Each I/O channel is individually configurable as an input or output for great flexibility to match your requirements

### Key Features & Benefits

- 16 channels of analog input capable of simultaneous sampling
- 16-bit 500kHz A/D converter on each channel
- Analog input range of  $\pm 10.24$  volts
- Programmable gain of 1x, 2x, 4x, or 8x
- 8 channels of analog output capable of simultaneous updates
- Each A/D channel includes a 2K sample FIFO
- FIFO status interrupts configurable for half-full or overflow conditions
- Dual quad 16-bit serial input D/A converters with 10 $\mu$ s settling time
- Analog output range of  $\pm 10$  volts
- 16 channels of general-purpose digital I/O
- Front panel 68-pin VHDCI receptacle for field I/O connections
- Example VHDL code provided in the base board's Engineering Design Kit to control sample rate and gain selection



AXM extension I/O modules plug into a mezzanine connector on many Acromag FPGA boards to provide additional I/O signal processing capabilities.

# Extension I/O Modules



## AXM-A75 Multi-function I/O extension module for Acromag FPGA cards

### Performance Specifications

#### ■ Analog Input

##### Input configuration

16 differential channels with a separate A/D converter on each channel.

##### A/D resolution

16 bits.

##### Input range

±10.24 volts.

##### Programmable gain

1x, 2x, 4x, or 8x.

##### Input impedance

1 giga-ohm.

##### Maximum throughput rate

2 $\mu$ S A/D (500kHz).

##### A/D trigger

FPGA controlled.

##### Signal-to-noise ratio

69dB (25°C) typical.

##### Signal-to-noise and distortion

67dB (25°C) typical.

#### ■ Analog Output

##### Output configuration

8 channels with a separate D/A converter for each channel provided by two quad serial input DACs. Double buffering allows the simultaneous updating of all channels.

##### D/A resolution

16 bits.

##### Output range

±10 volts.

##### Settling time

10 $\mu$ S (100kHz).

#### ■ Digital I/O

##### I/O configuration

16 bi-directional I/O channels, individually configured.

##### I/O range

5V TTL.

##### Output type

Open collector type with open drain outputs.

##### Pull-up resistor

Digital I/O lines are pulled high via a 4.75k ohm resistor to +5 volts.

#### ■ Physical

Acromag AXM I/O modules plug into a PMC or XMC FPGA module's front mezzanine for additional I/O lines. Analog and digital I/O AXM modules are sold separately.

##### Size

12.7 mm high x 42.1 mm deep x 74.0 mm wide (0.500 inches x 1.659 inches x 2.913 inches).

**The AXM-A75 exceeds the allowable mezzanine envelope as defined in IEEE 1386-2001 and may not be compatible with all PMC/XMC carriers. See user manual for details.**

##### Stacking height

5.0 mm (0.315 in).

##### Weight

41.3 g (1.46 oz).

##### Connectors

I/O: 68-pin VHDCI receptacle.

Mezzanine: High-speed 150-pin header.

#### ■ Environmental

##### Operating temperature

-40 to 85°C.

##### Storage temperature

-55 to 125°C.

##### Relative humidity

5 to 95% non-condensing.

##### Power

+3.3V: 39mA typical, 50mA maximum.

+5V: 54mA typical, 65mA maximum.

+12V: 103mA typical, 115mA maximum.

-12V: 92mA typical, 115mA maximum.

##### MTBF

Contact the factory.

##### Electromagnetic Compatibility (EMC)

Minimum immunity per European Norm EN61000-6-2:2005.

##### Electrostatic Discharge (ESD) Immunity

4KV direct contact and 8KV air-discharge to the enclosure port per IEC61000-4-2.

##### Radiated Field Immunity (RFI)

10V/m, 80 to 1000MHz AM; 3V/m, 1.4 to 2.0GHz;

1V/m, 2.0 to 2.7GHz, per IEC61000 4 3.

##### Electrical Fast Transient Immunity (EFT)

2KV to power, and 1KV to signal I/O per IEC61000-4-4.

##### Conducted RF Immunity (CRFI)

10Vrms, 150KHz to 80MHz, per IEC61000-4-6.

##### Surge Immunity

0.5KV to power and 1KV to signal per IEC61000-4-5.

##### Emissions

Per European Norm EN61000-6-4:2007.

##### Radiated Frequency Emissions

30 to 1000MHz per CISPR16 Class A.

### Ordering Information

#### ■ AXM Plug-In I/O Extension Modules

For more information, see [www.acromag.com](http://www.acromag.com).

##### [AXM-A75](#)

16 analog inputs, 8 analog outputs, and 16 digital I/O

##### [AXM-??](#)

Custom I/O configurations available, call factory.

#### ■ Accessories

For more information, see [www.acromag.com](http://www.acromag.com).

##### [5025-288](#)

Termination Panel for 68-pin SCSI-3 cable to connect field I/O Signals to the board.

##### [5028-420](#)

Termination shielded cable, 34-wire pairs, ultra SCSI/VHDCI male and SCSI-3 male connectors. Recommended for all I/O connections to model 5025-288 termination panel. 2 meters long.

##### [XMC FPGA Modules](#)

##### [PMC FPGA Modules](#)

ISO9001  
AS9100



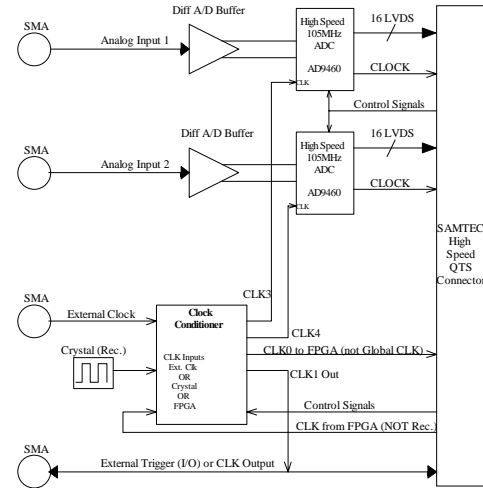
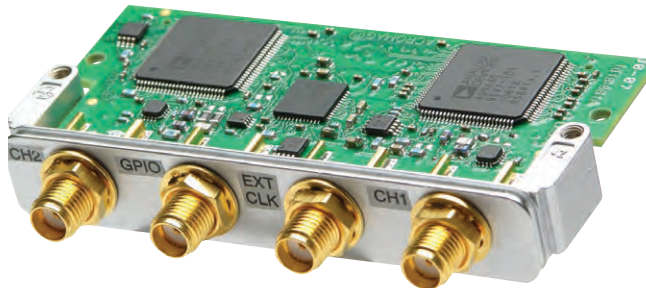
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# Extension I/O Modules

## AXM-A30 Analog I/O Extension Modules for PMC FPGA Boards



High Speed Analog Input ♦ 2 Differential Channels ♦ 2 16-bit A/D Channels

### Description

AXM Series extension modules offer numerous I/O options for Acromag's PMC modules with configurable FPGAs. These extension modules plug into the front mezzanine on Acromag's PMC-LX/SX (Virtex®-4 FPGA), and PMC-VLX/VSX/VFX (Virtex-5 FPGA) modules.

### AXM-A30 Analog Input

This module features two 105MHz 16-bit A/D channels. An external clock and trigger can be used to control sampling.

An internal precision clock conditioner provides the functions of jitter cleaning/reconditioning, multiplication, and distribution of a reference clock.

Each clock distribution block includes a programmable divider, a phase synchronization circuit, and a programmable delay. This allows multiple integer-related and phase-adjusted copies of the reference to be distributed to multiple system components.

### Key Features & Benefits

- Analog Input
- Input configuration: Two differential channels using two Analog Devices AD9460 A/D converter
- A/D resolution: 16 bits
- Input range: 3.4V peak-to-peak, centered at 0V, into a 50 ohm load
- External clock input: 3.3V peak-to-peak
- Input clock range: 1-105MHz
- Maximum throughput rate:  
1 channel (max.): 9.5nS (105MHz)  
2 channels (max.): 9.5nS (105MHz)  
A/D trigger: External source, FPGA controlled
- Input clock controller: Precision clock conditioner combines the functions of jitter cleaning/reconditioning, multiplication, and distribution of a reference clock
- Signal-to-noise ratio: 69dB (25°C) typical
- Signal-to noise and distortion: 67dB (25°C) typical
- General purpose I/O: Low voltage TTL



AXM modules attach to PMC Modules with user-configurable FPGAs.

# Extension I/O Modules



## AXM-A30 Analog I/O Extension Modules for PMC FPGA Boards

### Performance Specifications

#### ■ AXM-A30 Analog Input

##### Input configuration

Two differential channels using two Analog Devices AD9460 A/D converter.

##### A/D resolution

16 bits.

##### Input range

3.4V peak-to-peak, centered at 0V, into a 50 ohm load.

##### External clock input:

3.3V peak-to-peak.

##### Input clock range:

1-105MHz.

##### Maximum throughput rate

1 channel (max.): 9.5nS (105MHz).

2 channels (max.): 9.5nS (105MHz).

##### A/D trigger

External source, FPGA controlled.

##### Input clock controller:

Precision clock conditioner combines the functions of jitter cleaning/reconditioning, multiplication, and distribution of a reference clock.

##### Signal-to-noise ratio

69dB (25°C) typical.

##### Signal-to-noise and distortion

67dB (25°C) typical.

General purpose I/O: Low voltage TTL.

#### ■ Physical

Acromag's AXM Series extension modules offer numerous I/O options for Acromag's PMC modules with configurable FPGA. These extension modules plug into the front mezzanine on Acromag's PMC-LX/SX (Virtex@-4 FPGA), and PMC-VLX/VSX/VFX (Virtex-5 FPGA) modules. Analog and digital I/O AXM modules are sold separately.

##### Size

11.5 mm high x 31.0 mm deep x 74.0 mm wide  
(0.453 inches x 1.220 inches x 2.913 inches).

##### Stacking height

5.0 mm (0.197 inches).

##### Weight

41.3 g (1.46 oz).

##### Connectors

Front field I/O: Four SMA PCB jack female receptacle connectors.

*Complies with PMC Specification P1386.1 for a single-width PMC module when installed on a supported PMC module.*

#### ■ Environmental

##### Operating temperature

-0 to 70°C.

##### Storage temperature

-55 to 105°C.

##### Relative humidity

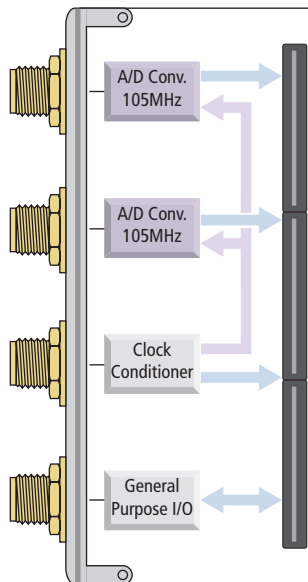
5 to 95% non-condensing.

##### Power

4.5 Watts typical.

##### MTBF

1,972,542 hrs. at 25°C, MIL-HDBK-217F, Notice 2.



### Ordering Information

#### ■ AXM Plug-In I/O Modules

For more information, see [www.acromag.com](http://www.acromag.com).

##### [AXM-A30](#)

2 analog input channels

AXM-??

Custom I/O configurations available, call factory.

#### ■ Accessories

For more information, see [www.acromag.com](http://www.acromag.com).

[XMC FPGA Modules](#)

[PMC FPGA Modules](#)

ISO9001  
AS9100   
MADE IN USA

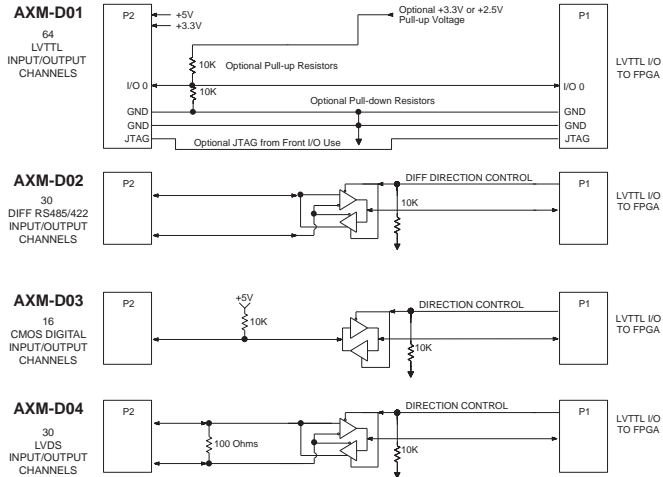
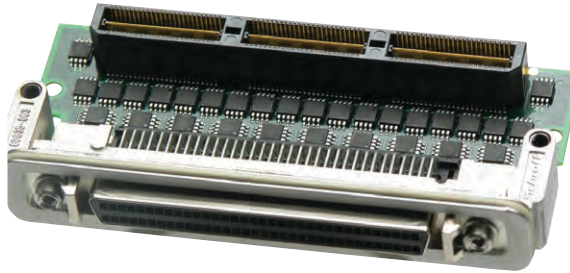
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# Extension I/O Modules



## AXM Series Digital I/O Extension Modules



Plug-In I/O Modules ♦ Choose from four I/O Options ♦ JTAG Support Option

### Description

AXM Series extension modules offer numerous I/O options for Acromag's PMC and XMC modules with configurable FPGAs. These extension modules plug into the front mezzanine on Acromag's I/O compatible FPGAs.

#### AXM-D01 LVTTTL I/O

This module provides 64 LVTTTL I/O channels for straight through I/O. custom modules are available for optional pull-ups, pull-downs, JTAG, and fusted power for front I/O use.

#### AXM-D02 RS-485 Differential I/O

This module provides 30 differential I/O channels. Data direction, either input or output, on each channel is independently controlled. Eight of the channels support programmable change-of-state interrupts. JTAG option.

#### ACR5264 LVDS and RS-485 Differential I/O

This module provides 30 differential I/O channels. Data direction, either input or output, on each channel is independently controlled. Eight of the channels support programmable change-of-state interrupts. 16 LVDS and 14 RS-485 differential I/O channels.

#### AXM-D03 CMOS and RS-485 Differential I/O

This module provides 16 CMOS and 22 RS-485 differential I/O channels. Data direction, either input or output, on each channel is independently controlled. Eight of the channels support programmable change-of-state interrupts.

#### AXM-DX03 CMOS and RS-485 Differential I/O

Same as AXM-D03 above except 16 CMOS and 24 RS-485 differential I/O channels. Provides a replacement for legacy PMC-DX503/2003 FPGA modules when used with PMC/XMC-SLX.

#### AXM-D04 LVDS

This module provides 30 channels of low voltage differential signaling with independently configured direction. Interrupts are programmable on eight of the channels for any bit change of state or level. JTAG option



AXM modules attach to PMC Modules with user-configurable FPGAs.

### Key Features & Benefits

- Various modules allows users to select the Front I/O required for their application.
- Differential RS485/RS422 can be configured for input or output with independent direction control.
- Interface with 5V compliant input/output CMOS channels which can be configured as input or output with independent direction control.
- Low voltage differential signaling can be configured for input or output with independent direction control.
- The EDK board provides the standard Xilinx JTAG interface to allow direct programming of the FPGA and an interface with ChipScope®.
- Example code provides interrupts that are software programmable for any bit Change-Of-State or level on 8 channels.
- Example Design – The example VHDL design, provided in the base board EDK, includes control of all I/O, and eight Change-Of-State interrupts.

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# Extension I/O Modules



## AXM Series Digital I/O Extension Modules

### Performance Specifications

#### AXM-D01

Channel configuration: 64 channel bi-directional LVTTTL signals are independently direction controlled. LVTTTL I/O characteristics: all I/O characteristics are determined by the FPGA.

#### AXM-D02

Channel configuration: 30 bi-directional differential signals with independently configured direction. Channels to the FPGA are buffered using EIA RS485/RS422 line transceivers. Optional JTAG access via front connector.

Differential driver output voltage:

1.5V minimum, 3.3V maximum with 54 ohm load.

#### ACR5364

Channel configuration: 16 channels of low voltage differential signaling with independently configured I/O direction and 14 bi-directional differential signals with independently configured direction.

RS485 channels: Same as AXM-D02

LVDS channels: Same as AXM-D04

#### AXM-D03

Channel configuration: 16 bi-directional CMOS transceivers (input/output direction controlled as pairs of channels) and 22 bi-directional differential signals with independently configured direction.

Differential channels: Same as AXM-D02.

CMOS I/O electrical characteristics:

VoH: 3.8V minimum    Vol: 0.55V maximum

IoH: -32.0mA    IoL: 32.0mA

ViH: 3.5V minimum    ViL: 1.5V maximum

#### AXM-DX03

Same as AXM-D03 above except 16 CMOS and 24 RS-485 differential I/O channels. Provides a replacement for legacy PMC-DX503/2003 FPGA modules when used with PMC/XMC-SLX.

#### AXM-D04

Channel configuration: 30 channels of low voltage differential signaling with independently configured I/O direction. Optional JTAG access via front connector.

LVDS I/O electrical characteristics:

LVDS driver output voltage: 247mV min., 454mV max.

Common mode output voltage: 1.37V max.

LVDS Input Threshold Voltage: -50mV min., 50mV max.

### Physical Dimensions

#### Size

11.5 mm high x 31.0 mm deep x 74.0 mm wide  
(0.453 inches x 1.220 inches x 2.913 inches)

#### Stacking height

8.0 mm (0.315 inches).

#### PMC Compliance

Complies with PMC Specification P1386.1 for a single-width PMC module when attached to the PMC front mezzanine.

#### Connectors

Front field I/O: 68-pin, SCSI-3, female receptacle header (AMP 5787394-7 or equivalent).

### Environmental

#### Operating temperature

-40 to 85°C

#### Storage temperature

-55 to 150°C

#### Relative humidity

5 to 95% non-condensing

#### Power:

1.5W typical (AXM-D02, AXM-D03)

0.6W typical (AXM-D04)

#### MTBF

Hours are at 25°C, MIL-HDBK-217F, Notice 2

AXM-D01: TBD

AXM-D02: 3,559,276 hours

AXM-D03: 3,921,522 hours

AXM-DX03: TBD

AXM-D04: 6,534,197 hours

### Ordering Information

#### AXM Plug-In I/O Modules

##### [AXM-D01](#)

64 bi-directional LVTTTL I/O channels

##### [AXM-D02](#)

30 RS-485 Differential I/O channels

##### [ACR5364](#)

Same as AXM-D02 except 16 LVDS and 14 RS485 I/O channels

##### [AXM-D02-JTAG](#)

Same as AXM-D02 plus JTAG support

##### [AXM-D03](#)

16 CMOS and 22 RS485 differential I/O channels

##### [AXM-DX03](#)

16 CMOS and 24 RS485 differential I/O channels

##### [AXM-D04](#)

30 LVDS I/O channels

##### [AXM-D04-JTAG](#)

Same as AXM-D04 plus JTAG support

##### [AXM-??](#)

Custom I/O configurations available, call factory.

#### Accessories

##### [5025-288](#)

Termination Panel for 68-pin SCSI-3 cable to connect field I/O Signals to the board.

##### [5028-432](#)

Round shielded cable, 34 twisted pairs, SCSI-3 male connector at both ends. Connects model 5025-288 termination panel to the board. 2 meters long.

##### [XMC FPGA Modules](#)

##### [PMC FPGA Modules](#)

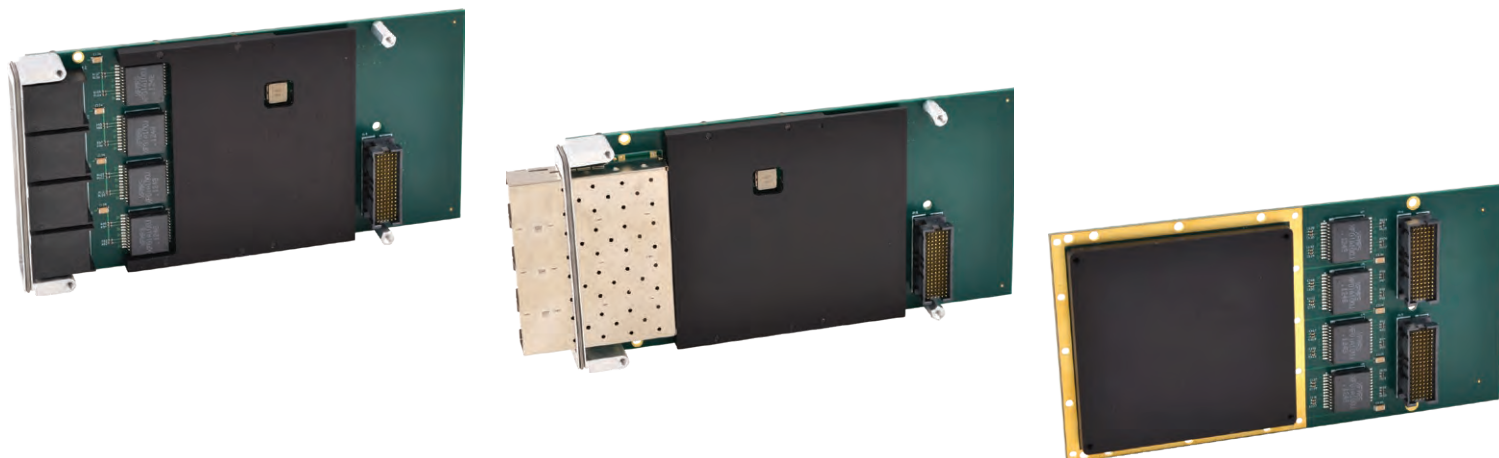
ISO9001  
AS9100  MADE IN USA

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## XMC610 Quad-port Gigabit Ethernet XMC NIC Card



Quad RJ45, SFP, or rear ports ♦ Intel® I350 Controller ♦ Conduction-cooled version available

### Description

#### Models

**XMC611:** RJ45 connectors

**XMC612:** SFP connectors

**XMC613:** Rear I/O connectors

Acromag's XMC610 series provides up to four independent gigabit Ethernet interface ports. Different models feature RJ45, SFP, or rear connectors with conduction cooling support. Intel's I350 quad gigabit Ethernet controller delivers high-performance and offers many powerful networking capabilities.

Designed for COTS applications, these rugged XMC mezzanine modules offer a high-density, high-performance solution for network interface applications over fiber or copper media. They are ideal for use in defense, aerospace, industrial, and scientific research computing systems.

### Key Features & Benefits

- Four independent 1-gigabit Ethernet interfaces
- Industry-leading Intel I350 Ethernet controller
- Front or rear I/O access (RJ45, SFP, or P16)
- XMC PCIe x4 Gen 2 interface
- Up to 5Gbps bus speed per lane
- Supports fiber optic or copper media
- 10/100/1000 Mbps data rates
- 3.3V low power design
- -40 to 85°C operation
- Linux®, Windows®, and VxWorks® support
- CE compliant.

### Intel I350 Features

**IEEE 802.3 Auto-negotiation** – Automatic link configuration for speed, duplex, & flow control.

**IEEE 1588 and 802.1AS Precision Timing** – Time-stamping and synchronization of time sensitive applications. Distribute common time to connected devices.

**IEEE 802.3az Energy Efficient Ethernet (EEE)** – Power consumption is reduced by approximately 50% during idle state.

**DMA Coalescing** – Reduces platform power consumption by coalescing, aligning, and synchronizing DMA transfers. Enables synchronizing port activity & power management of memory, CPU, and other internal circuitry.

**8 Tx and Rx Queue Pairs per Port** – Supports VMware NetQueue and Microsoft VMQ

**Flexible Port Partitioning (PCI-SIG SR-IOV)** – Up to 32 Virtual Functions (VFs) appear as Ethernet Controllers in Linux OSes that can be assigned to VMs, Kernel processes, or teamed using Linux Bonding Drivers

**TCP/UDP, IPv4/IPv6 Checksum Offloads** – Extended Tx descriptors provide increased offload capabilities

**Jumbo Frame Packet Support** – Improves system performance related to handling of network data on multiprocessor systems.

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## XMC610 Quad-port Gigabit Ethernet XMC NIC Card



### Performance Specifications

#### ■ Communication

##### Ethernet interface

Four 1-Gigabit Ethernet interfaces.  
XMC611: Front, four RJ45 ports.  
XMC612: Front, four SFP ports.  
XMC613: Rear, four 1000BASE-T via P16

##### Throughput

XMC611 and XMC613 supports 10/100/1000 Mb/s data rate auto-negotiation.

##### PCI Express

PCIe 4-lane (x4) Gen 2.0 interface operates at a bus speed of 5 Gbps per lane per direction.

#### ■ XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-width module.

#### ■ Software Support

Linux®, Windows®, and VxWorks® systems  
Drivers available with support for all NIC functions.  
See [www.acromag.com](http://www.acromag.com) for more information.

#### ■ Electrical

PCIe Interface x4  
Complies with VITA 42.3 XMC PCIe Standard.

##### JTAG Interface

Complies with IEEE 1149.1.

##### RJ45 Interface (XMC611)

Four 1000BASE-T ports complying with IEEE 802.3.

##### SFP Interface (XMC612)

Four ports complying with INF-8074i SFP Specification.

##### P16 XMC Rear I/O (XMC613)

Four 1000BASE-T ports complying with IEEE 802.3.

##### SFP connectors

Four SFP module front I/O ports.

#### ■ Environmental

##### Operating temperature

-40 to 85°C.

##### Storage temperature

-55 to 125°C.

##### Relative humidity

5 to 95% non-condensing.

##### Power requirements

XMC611 and XMC613: 3.3V (±5%): 3.7W typical.

XMC612: 3.3V (±5%): 2.3W typical.

All ports active.

5V, 12V: not used on all models.

##### Weight

XMC611: 83.2 g

XMC612: 98.5 g

XMC613: 78.5 g

##### Certifications

CE Compliant

### Ordering Information

#### ■ XMC Modules

##### XMC611

Gigabit Ethernet interface module with RJ45 connectors, lead-free.

##### XMC612

Gigabit Ethernet interface module with SFP optical connectors, lead-free.

##### XMC613

Gigabit Ethernet interface module with rear I/O connectors, conduction-cooled, lead-free.

#### ■ Carrier Cards

##### PCIe Carriers

##### VPX Carriers

#### ■ Accessories

##### 5028-449

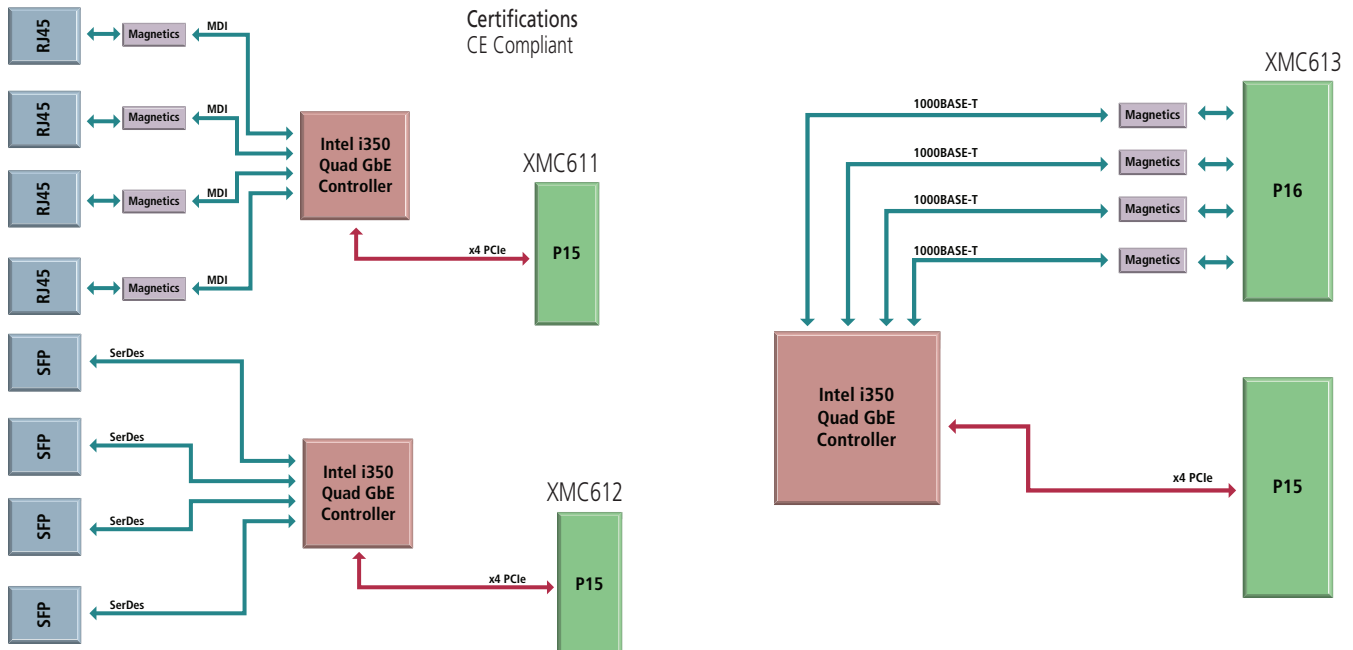
SFP cable, SFP-to-SFP (male-male) connectors, 1 meter.

##### 5028-452

SFP transceiver, MSA, 1000BASE-SX multi-mode Fiber.

##### 5028-455

SFP transceiver, MSA, 1000Base-T RJ45 copper.



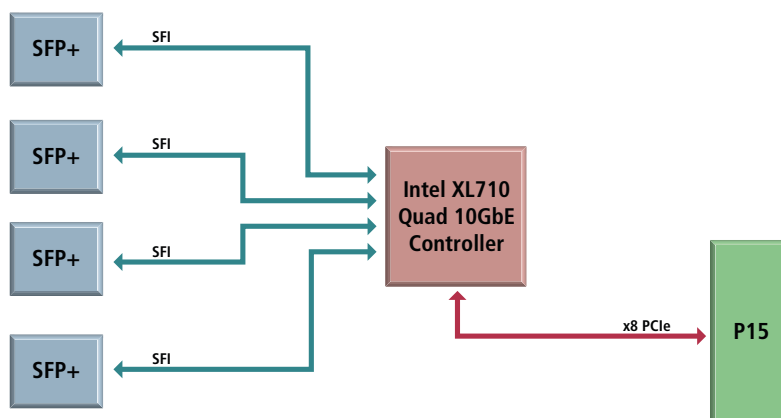
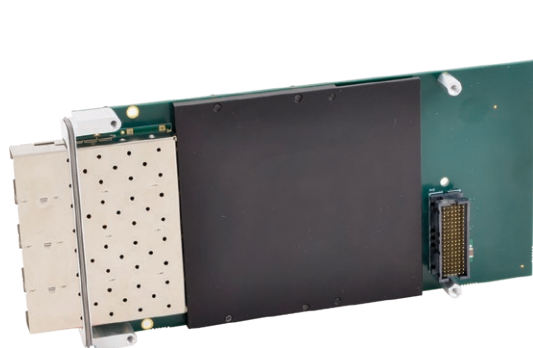
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# XMC Modules

## XMC631 10-Gigabit Ethernet Network Interface Card (NIC)



Quad SFP+ ports ♦ Intel® XL710 Controller ♦ PCIe Gen 3 x8 interface ♦ Extended temperature operation

### Description

Acromag's XMC631 module provides up to four 10-GbE interface ports. Different models are available for extended temperature operation and [VITA 42/61 connector](#) options to support a PCIe Gen 3 interface. Four SFP+ ports support optical or copper cabling.

[Intel's XL710 quad-port 10-gigabit Ethernet controller](#) delivers high-performance and offers many powerful networking capabilities. Advanced virtualization, intelligent offload and accelerator technologies optimize network performance.

Combining the intelligent off-loading features of the XL710 controller with the processing power of a Xeon-D processor can deliver outstanding performance levels. Together, the two Intel devices provide a balanced hybrid solution of compute and off-load to achieve optimal performance and efficiency in an embedded system.

Designed for COTS applications, these rugged XMC mezzanine modules offer a high-density, high-performance solution for network interface applications. They are ideal for use in defense, aerospace, industrial, and scientific research computing systems.

### Key Features & Benefits

- Industry-leading Intel XL710 controller with four independent 10-GbE interfaces
- Four SFP+ ports support 10GBASE-SR, 10GBASE-LR, 10GBASE-T and 10GSFP+Cu connections
- PCIe x8 Gen 3 interface
- IEEE 1588 and 802.1AS precision timing
- IEEE 802.3az Energy Efficient Ethernet (EEE)
- Advanced traffic steering capability increases transaction rates and reduces latency
- VMDq for emulated path
- Dynamic load balancing
- Flexible port partitioning (PCI-SIG SR-IOV)
- Tx/Rx IP, TCP/UDP/SCTP, IPv4/IPv6 checksum offloads lower processor usage
- Jumbo frame packet support up to 9.5KB
- Up to -40 to 85°C operation
- Linux® and Windows® support
- CE compliant.



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## XMC631 10-Gigabit Ethernet Network Interface Card (NIC)



### Performance Specifications

#### ■ Ethernet Interface

Ethernet Controller  
Intel® XL710

#### Network Interface

Four SFP+ 10-Gigabit Ethernet interfaces.

Complies with IEEE 802.3-2008 standard for Ethernet.

Complies with IEEE 802.3ae-2002 amendment for 10 Gb/s Ethernet.

#### Throughput

10,000 MB/s (10GB/s) per port, full-duplex.

Total aggregate rate limited by PCIe host interface.

#### ■ XMC Host Interface

##### XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

##### PCI Express

Conforms to PCI Express Base Specification, Rev. 3.1.

PCIe 8-lane (x8) Gen 3 interface operates at a bus speed of 8 Gbps per lane per direction.

Gen 3 PCIe interface requires VITA 61 connectors.

Gen 2 PCIe interface supported w/ VITA 42 connectors

#### ■ Electrical / Mechanical

##### SFP+ Connectors

Four front panel connector cages for insertion of SFP+ transceiver modules supporting optical or copper cables.

Complies with SFF-8431 specification.

##### XMC Connectors

P15 for PCIe bus via eight high-speed serial lanes.

Available as VITA 42 standard or VITA 61 upgrade for PCIe Gen 3 applications.

##### Power Requirement

3.3V: 250mA idle, 250mA active, 400mA max.

5.5V: 470mA idle, 565mA active, 1100mA max.

12V: 220mA idle, 260mA active, 485mA max.

Power: 3.0W idle, 3.5W active, 6.2W max.

##### Dimensions

Single-width XMC. 149 x 74 x 10 mm.

Unit weight: 104.2 g.

#### ■ Environmental

Operating Temperature Range

Operation - Industrial: 0 to 70°C.

Operation - Extended: -40 to 85°C  
(200 lfm airflow min.)

Storage: -55 to 125°C.

#### Relative Humidity

5 to 95% non-condensing.

#### Shock

Designed to comply with VITA 47 Class OS1.

#### Vibration

Designed to comply with VITA 47 Class V1.

#### Certifications

CE compliant.

#### ■ Software Support

Linux® and Windows® Systems

Intel XL710 Ethernet Controller drivers  
available at [www.intel.com](http://www.intel.com).

### Ordering Information

#### ■ XMC Modules

[Go to on-line ordering page >](#)

##### XMC631-42-20

10GbE NIC with quad SFP+ front I/O, VITA 42, industrial temperature ratings

##### XMC631-61-20

10GbE NIC with quad SFP+ front I/O, VITA 61, industrial temperature ratings

##### XMC631-42-30

10GbE NIC with quad SFP+ front I/O, VITA 42, extended temperature ratings

##### XMC631-61-30

10GbE NIC with quad SFP+ front I/O, VITA 61, extended temperature ratings

#### ■ Accessories

##### SM10G-LR

10-GbE long reach single-mode optical SFP+ module.

##### SM10G-SR

10-GbE short reach multi-mode optical SFP+ module.

##### TAPCABLE1M

SFP+ cable, SFP+-to-SFP+ (male-male) connectors, 1 meter.

#### ■ Carrier Cards

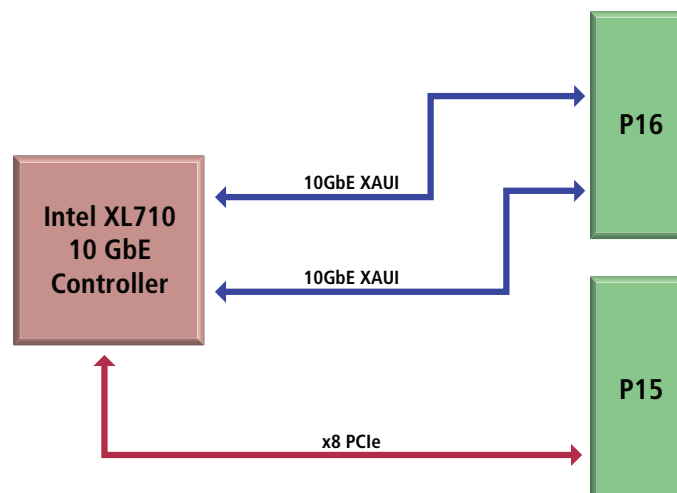
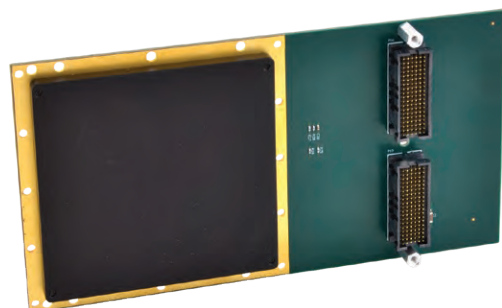
PCIe Carriers

VPX Carriers





## XMC632 10-Gigabit Ethernet Network Interface Card (NIC)



Dual XAUI ports ♦ Intel® XL710 Controller ♦ PCIe Gen 3 x8 interface ♦ Conduction-cooled

### Description

Acromag's [XMC632](#) module provides up to two 10-GbE XAUI interface ports. Different models are available for [VITA 42/61 connector](#) options to support a PCIe Gen 3 interface. The rugged, rear I/O design is ready for use in conduction-cooled systems for extreme temperature environments.

[Intel's XL710 quad-port 10-gigabit Ethernet controller](#) delivers high-performance and offers many powerful networking capabilities. Advanced virtualization, intelligent offload and accelerator technologies optimize network performance.

Combining the intelligent off-loading features of the XL710 controller with the processing power of a Xeon-D processor can deliver outstanding performance levels. Together, the two Intel devices provide a balanced hybrid solution of compute and off-load to achieve optimal performance and efficiency in an embedded system.

Designed for COTS applications, these rugged XMC mezzanine modules offer a high-density, high-performance solution for network interface applications. They are ideal for use in defense, aerospace, industrial, and scientific research computing systems.

### Key Features & Benefits

- Industry-leading Intel XL710 controller with four independent 10-GbE interfaces
- Two XAUI interfaces available as rear I/O via the P16 connector
- PCIe x8 Gen 3 interface
- IEEE 1588 and 802.1AS precision timing
- IEEE 802.3az Energy Efficient Ethernet (EEE)
- Advanced traffic steering capability increases transaction rates and reduces latency
- VMDq for emulated path
- Dynamic load balancing
- Flexible port partitioning (PCI-SIG SR-IOV)
- Tx/Rx IP, TCP/UDP/SCTP, IPv4/IPv6 checksum offloads lower processor usage
- Jumbo frame packet support up to 9.5KB
- Up to -40 to 85°C operation
- Linux® and Windows® support
- CE compliant.

## XMC632 10-Gigabit Ethernet Network Interface Card (NIC)



### Performance Specifications

#### ■ Communication

Ethernet Controller  
Intel® XL710

#### Network Interface

Four XAUI 10-Gigabit Ethernet interfaces.

Complies with IEEE 802.3-2008 standard for Ethernet.

Complies with IEEE 802.3ae-2002 amendment for 10 Gb/s Ethernet.

#### Throughput

10,000 MB/s (10GB/s) per port, full-duplex.

Total aggregate rate limited by PCIe host interface.

#### ■ XMC Host Interface

##### XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Complies with ANSI/VITA 42.6 specification for XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard.

##### PCI Express

Conforms to PCI Express Base Specification, Rev. 3.1.

PCIe 8-lane (x8) Gen 3 interface operates at a bus speed of 8 Gbps per lane per direction.

Gen 3 PCIe interface requires VITA 61 connectors.

Gen 2 PCIe interface supported w/ VITA 42 connectors

#### ■ Electrical / Mechanical

##### XMC Connectors

P15 for PCIe bus via eight high-speed serial lanes.

P16 for two 10GbE XAUI interfaces.

Available as VITA 42 standard or VITA 61 upgrade for PCIe Gen 3 applications.

##### Power Requirement

3.3V: 220mA idle, 220mA active, 330mA max.

5.5V: 450mA idle, 500mA active, 1025mA max.

12V: 215mA idle, 235mA active, 455mA max.

Power: 2.8W idle, 3.1W active, 5.7W max.

##### Dimensions

Single-width XMC. 149 x 74 x 10 mm.

Unit weight: 76.9 g.

#### ■ Environmental

##### Operating Temperature Range

Operation: -40 to 85°C (conduction-cooled).

Storage: -55 to 125°C.

##### Relative Humidity

5 to 95% non-condensing.

##### Shock

Designed to comply with VITA 47 Class OS1.

##### Vibration

Designed to comply with VITA 47 Class V1.

##### Certifications

CE compliant.

#### ■ Software Support

##### Linux® and Windows® Systems

Intel XL710 Ethernet Controller drivers available at [www.intel.com](http://www.intel.com).

### Ordering Information

#### ■ XMC Modules

##### [XMC632-42-50](#)

10GbE NIC with dual XAUI rear I/O, VITA 42

##### [XMC632-61-50](#)

10GbE NIC with dual XAUI rear I/O, VITA 61

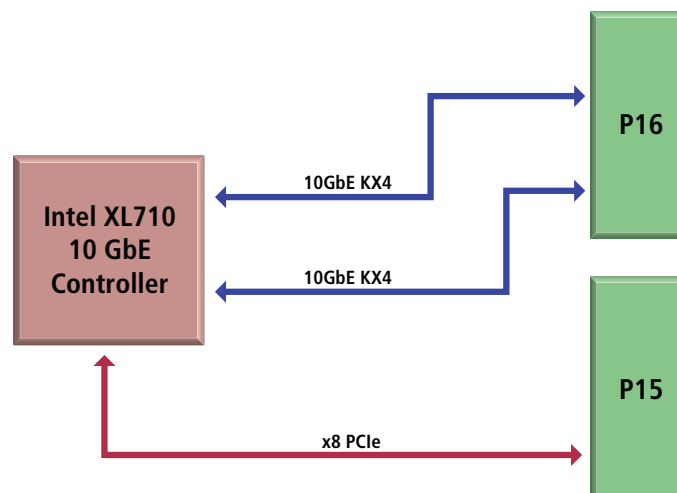
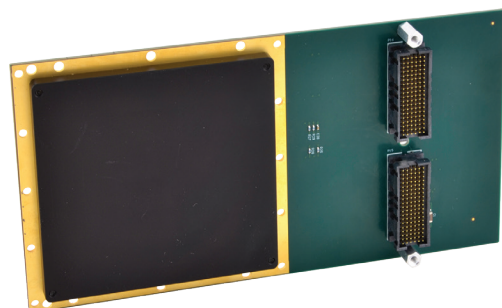
#### ■ Carrier Cards

##### [PCIe Carriers](#)

##### [VPX Carriers](#)



## XMC633 10-Gigabit Ethernet Network Interface Card (NIC)



Dual 10GBASE-KX4 ports ♦ Intel® XL710 Controller ♦ PCIe Gen 3 x8 interface ♦ Conduction-cooled

### Description

Acromag's XMC633 module provides up to two 10-GbE KX4 interface ports. Different models are available for VITA 42/61 connector options to support a PCIe Gen 3 interface. The rugged, rear I/O design is ready for use in conduction-cooled systems for extreme temperature environments.

Intel's XL710 quad-port 10-gigabit Ethernet controller delivers high-performance and offers many powerful networking capabilities. Advanced virtualization, intelligent offload and accelerator technologies optimize network performance.

Combining the intelligent off-loading features of the XL710 controller with the processing power of a Xeon-D processor can deliver outstanding performance levels. Together, the two Intel devices provide a balanced hybrid solution of compute and off-load to achieve optimal performance and efficiency in an embedded system.

Designed for COTS applications, these rugged XMC mezzanine modules offer a high-density, high-performance solution for network interface applications. They are ideal for use in defense, aerospace, industrial, and scientific research computing systems.

### Key Features & Benefits

- Industry-leading Intel XL710 controller with four independent 10-GbE interfaces
- Two 10GBASE-KX4 interfaces available as rear I/O via the P16 connector
- PCIe x8 Gen 3 interface
- IEEE 1588 and 802.1AS precision timing
- IEEE 802.3az Energy Efficient Ethernet (EEE)
- Advanced traffic steering capability increases transaction rates and reduces latency
- VMDq for emulated path
- Dynamic load balancing
- Flexible port partitioning (PCI-SIG SR-IOV)
- Tx/Rx IP, TCP/UDP/SCTP, IPv4/IPv6 checksum offloads lower processor usage
- Jumbo frame packet support up to 9.5KB
- Up to -40 to 85°C operation
- Linux® and Windows® support
- CE compliant.

## XMC633 10-Gigabit Ethernet Network Interface Card (NIC)



### Performance Specifications

#### ■ Communication

Ethernet Controller  
Intel® XL710

#### Network Interface

Two KX4 10-Gigabit Ethernet interfaces.

Complies with IEEE 802.3-2008 standard for Ethernet.

Complies with IEEE 802.3ae-2002 amendment for 10 Gb/s Ethernet.

#### Throughput

10,000 MB/s (10GB/s) per port, full-duplex.

Total aggregate rate limited by PCIe host interface.

#### ■ XMC Host Interface

##### XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Complies with ANSI/VITA 42.6 specification for XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard.

##### PCI Express

Conforms to PCI Express Base Specification, Rev. 3.1.

PCIe 8-lane (x8) Gen 3 interface operates at a bus speed of 8 Gbps per lane per direction.

Gen 3 PCIe interface requires VITA 61 connectors.

Gen 2 PCIe interface supported w/ VITA 42 connectors

#### ■ Electrical / Mechanical

##### XMC Connectors

P15 for PCIe bus via eight high-speed serial lanes.

P16 for two 10GbE KX4 interfaces.

Available as VITA 42 standard or VITA 61 upgrade for PCIe Gen 3 applications.

##### Power Requirement

3.3V: 220mA idle, 220mA active, 330mA max.

5.5V: 450mA idle, 500mA active, 1025mA max.

12V: 215mA idle, 235mA active, 455mA max.

Power: 2.8W idle, 3.1W active, 5.7W max.

##### Dimensions

Single-width XMC. 149 x 74 x 10 mm.

Unit weight: 76.9 g.

#### ■ Environmental

##### Operating Temperature Range

Operation: -40 to 85°C (conduction-cooled).

Storage: -55 to 125°C.

##### Relative Humidity

5 to 95% non-condensing.

##### Shock

Designed to comply with VITA 47 Class OS1.

##### Vibration

Designed to comply with VITA 47 Class V1.

##### Certifications

CE compliant.

#### ■ Software Support

Linux® and Windows® Systems

Intel XL710 Ethernet Controller drivers available at [www.intel.com](http://www.intel.com).

### Ordering Information

#### ■ XMC Modules

[Go to on-line ordering page >](#)

##### XMC633-42-50

10GbE NIC with dual KX4 rear I/O, VITA 42

##### XMC633-61-50

10GbE NIC with dual KX4 rear I/O, VITA 61

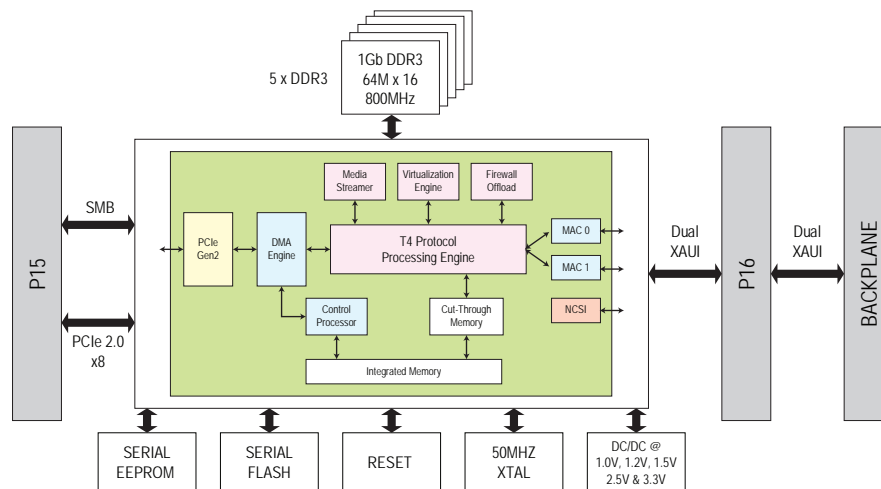
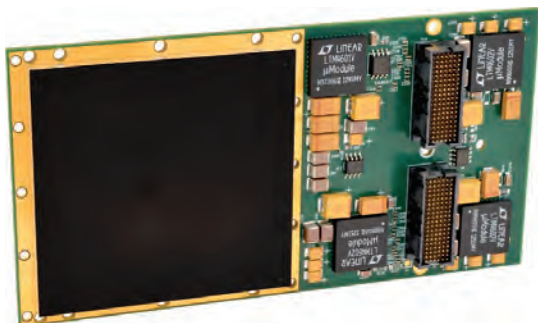
#### ■ Carrier Cards

[PCle Carriers - go to on-line ordering page >](#)

[VPX Carriers - go to on-line ordering page >](#)



## XMC-6260-CC 10-Gigabit Ethernet Interface Module with Dual XAUI Ports



XMC module with TCP/IP offload engine ASIC ♦ Dual XAUI 10GBASE-KX4 ports ♦ PCIe x8 Gen2

### Description

Acromag's [XMC-6260-CC](#) provides a 10-gigabit Ethernet (10GbE) interface solution for data-intensive real-time embedded computing systems. Ultra-high performance is achieved using an ASIC-based TCP/IP offload engine (TOE).

Typical applications include high-speed data storage, image collection/transfer, distributed control networks, and board-to-board interfaces.

### Fully Integrated Network Interface Card

With the adoption of 10GbE interfaces and rapidly increasing volumes of data, even the most powerful embedded processors can no longer manage data flow without a significant reduction in performance. To solve this problem, Acromag's XMC-6260-CC pairs a high-performance Chelsio T4 purpose-built multi-protocol processor with two channels of 10GbE connectivity. This combination maintains maximum 10GbE performance to meet the needs of data-intensive real-time applications.

### High Performance Protocol Offload Engine

A PCI Express v2.0 x8 host interface provides a high-speed connection to the system processor. With support for 5Gbps data rates, the PCIe interface delivers up to 32Gbps of bandwidth to the server. This connection accommodates stateless offloads, packet filtering (firewall offload), and traffic shaping (media streaming).

### Complete and Flexible TCP Offload

The XMC-6260-CC's TOE ASIC has hundreds of programmable registers for protocol configuration and offload control. As a result, the XMC-6260-CC can offload TCP processing per connection, per server, per interface. It can also globally and simultaneously tunnel traffic from non-offloaded connections to the host processor for the native TCP/IP stack to process. Additionally, the XMC-6260-CC provides a flexible zero-copy capability for regular TCP connections, requiring no changes to the sender, to deliver line rate performance with minimal CPU usage.

### Packet Switching and Routing

The XMC-6260-CC integrates a high-performance packet switch, which allows switching of traffic from any of the input ports to any of the output ports (wire-to-wire), and from any of the output ports to any of the input ports (host-to-host).

### Compatibility

Acromag's XMC-6260-CC provides guaranteed interoperability and compatibility with the full Ethernet standard.

### Extensive Software Support

The XMC-6260-CC offers a full suite of protocol software and drivers. Linux software tools support all offload (TOE) and network interface (NIC) operations. Windows software supports NIC operations.

### Key Features & Benefits

- Dual port 10 GbE via XAUI 10GBASE-KX4
- XMC PCI Express Gen2 x8
- Supports up to 1M connections
- Full offload support for:
  - TCP
  - UDP
  - iSCSI,
  - FCoE (Fiber Channel over Ethernet)
- Low processor overhead
- Very low Ethernet latency
- High-level determinism
- Zero-copy direct data placement
- Traffic filtering and management
- 5Gb DDR3 memory to enhance the number of virtual connections
- Designed for conduction-cooled host card or up to -40 to 85°C operation

# XMC Modules

## XMC-6260-CC 10-Gigabit Ethernet Interface Module with Dual XAUI Ports



### Performance Specifications

#### ■ Communication

Ethernet interface

Dual XAUI ports.

Throughput

2500Mbytes per second, per port, full-duplex.

Latency

2µs end-to-end.

PCI Express

PCIe 8-lane (x8) Gen 2.0 interface.

Determinism

±1µs.

#### ■ XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Complies with ANSI/VITA 42.6 specification for XMC modules with XAUI interface.

Electrical/Mechanical Interface: Single-Width Module.

#### ■ TCP/IP Offload Engine (TOE)

TOE processor

The ASIC incorporates two XGMAC (10GbE) interfaces. These interfaces are labeled MAC0 and MAC1. The ports support 10GBASE-KX4 and XAUI standards. They contain four lanes (four differential TX pairs and four differential RX pairs) of high speed SERDES. KX4 and XAUI operations will use all four lanes of MAC0 and MAC1. For MAC0 and MAC1, all 10GbE serial communication takes place on Lane 0 only.

#### ■ Software Support

Linux operating systems

Drivers available with support for all TOE and NIC functions. Please contact factory for details.

Windows operating systems

Drivers available with support for NIC functions. Please contact factory for details.

#### ■ Electrical

XMC PCIe bus interface (P15 and P16)

One 114-pin male connector (Samtec ASP-103614-05 or equivalent).

P15 primary XMC connector

8 differential TX pairs (PCIe) and

8 differential RX pairs (PCIe).

Optional JTAG: 6 JTAG signals

(TDI, TDO, TMS, TCK, 3.3V, and ground).

JTAG interface follows IEEE Standard 1149.1, which defines a test access port (TAP) and boundary-scan architecture.

System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin for system management.

Variable power (5V or 12V): 8 pins at 1A per pin.

P16 XMC connector

2 ports each with 4 differential TX pairs and 4 differential RX pairs (XAUI/KX4 operations).

1 global clock differential pair.

#### ■ Environmental

Operating temperature

-40 to 85°C.

Storage temperature

-55 to 125°C.

Relative humidity

5 to 95% non-condensing.

Power requirements

3.3V (±5%): Consult factory.

5V (±5%): Consult factory.

12V (±5%): Consult factory.

MTBF

Contact the factory.

### Ordering Information

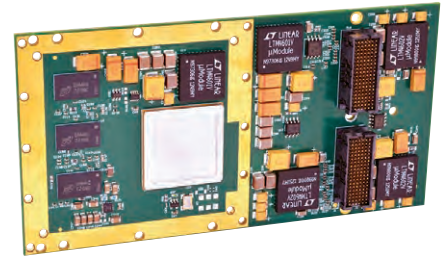
#### ■ XMC Modules

XMC-6260-CC-LF

10-gigabit Ethernet interface module, lead-free

#### ■ Accessories

For more information, see [www.acromag.com](http://www.acromag.com).



### Comparison of TCP/IP Offload Engines (TOE): ASIC vs. Software Stack

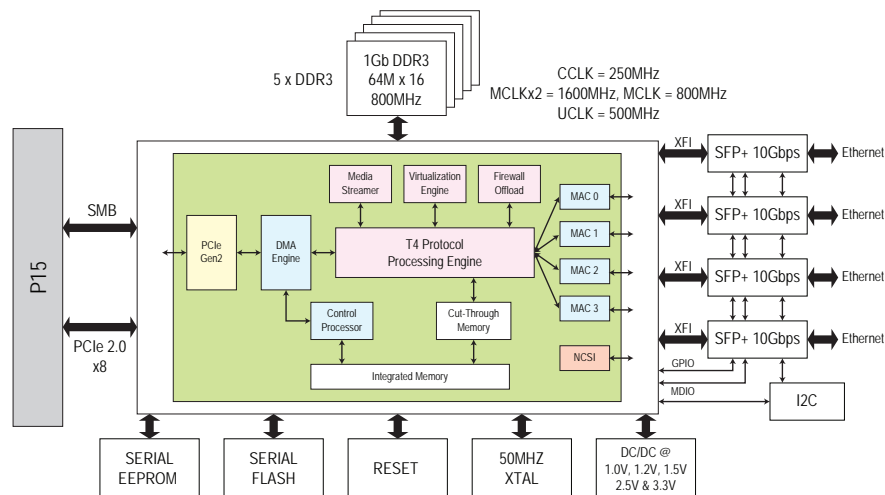
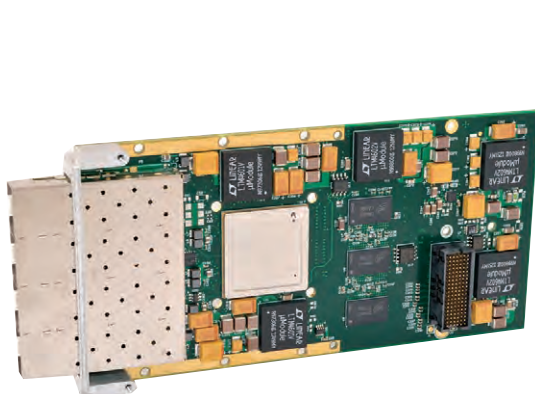
|                                  | Acromag ASIC TOE 10GbE Interface | Software Stack TOE 10GbE Interface |
|----------------------------------|----------------------------------|------------------------------------|
| Throughput per Port, Full-Duplex | 2500MBps (full-duplex)           | 40MBps (limited by CPU)            |
| Host Overhead                    | very low                         | very high                          |
| User-to-User Latency             | 2µs                              | 250µs                              |
| Determinism                      | ±1µs                             | ±200µs                             |
| Reliability Under Load           | Excellent (any load condition)   | Variable (dependent on load)       |

ISO9001  
AS9100



Tel 248-295-0310 ■ [solutions@acromag.com](mailto:solutions@acromag.com) ■ [www.acromag.com](http://www.acromag.com) ■ 30765 Wixom Rd, Wixom, MI 48393 USA

## XMC-6280 10-Gigabit Ethernet Interface Module with Quad SFP+ Ports



XMC module with TCP/IP offload engine ASIC ♦ Quad SFP+ fibre/copper ports ♦ PCIe x8 Gen2

### Description

Acromag's [XMC-6280](#) provides a 10-gigabit Ethernet (10GbE) interface solution for data-intensive real-time embedded computing systems. Ultra-high performance is achieved using an ASIC-based TCP/IP offload engine (TOE).

Typical applications include high-speed data storage, image collection/transfer, distributed control networks, and board-to-board interfaces.

### Fully Integrated Network Interface Card

With the adoption of 10GbE interfaces and rapidly increasing volumes of data, even the most powerful embedded processors can no longer manage data flow without a significant reduction in performance. To solve this problem, Acromag's XMC-6280 pairs a high-performance Chelsio T4 purpose-built multi-protocol processor with four channels of 10GbE connectivity. This combination maintains maximum 10GbE performance to meet the needs of data-intensive real-time applications.

### High Performance Protocol Offload Engine

A PCI Express v2.0 x8 host interface provides a high-speed connection to the system processor. With support for 5Gbps data rates, the PCIe interface delivers up to 32Gbps of bandwidth to the server. This connection accommodates stateless offloads, packet filtering (firewall offload), and traffic shaping (media streaming).

### Complete and Flexible TCP Offload

The XMC-6280's TOE ASIC has hundreds of programmable registers for protocol configuration and offload control. As a result, the XMC-6280 can offload TCP processing per connection, per server, per interface. It can also globally and simultaneously tunnel traffic from non-offloaded connections to the host processor for the native TCP/IP stack to process. Additionally, the XMC-6280 provides a flexible zero-copy capability for regular TCP connections, requiring no changes to the sender, to deliver line rate performance with minimal CPU usage.

### Packet Switching and Routing

The XMC-6280 integrates a high-performance packet switch, which allows switching of traffic from any of the input ports to any of the output ports (wire-to-wire), and from any of the output ports to any of the input ports (host-to-host).

### Compatibility

Acromag's XMC-6280 provides guaranteed interoperability and compatibility with the full Ethernet standard.

### Extensive Software Support

The XMC-6280 offers a full suite of protocol software and drivers. Linux software tools support all offload (TOE) and network interface (NIC) operations. Windows software supports NIC operations.

### Key Features & Benefits

- Quad port 10 GbE via SFP+
- XMC PCI Express Gen2 x8
- Supports up to 1M connections
- Full offload support for:
  - TCP
  - UDP
  - iSCSI,
  - FCoE (Fibre Channel over Ethernet)
- Low processor overhead
- Very low Ethernet latency
- High-level determinism
- Zero-copy direct data placement
- Traffic filtering and management
- 5Gb DDR3 memory to enhance the number of virtual connections

## XMC-6280 10-Gigabit Ethernet Interface Module with Front SFP+ Ports



### Performance Specifications

#### ■ Communication

Ethernet interface

Quad SFP+ ports.

Throughput

2500Mbytes per second, per port, full-duplex.

Latency

2μs end-to-end.

PCI Express

PCIe 8-lane (x8) Gen 2.0 interface.

Determinism

±1μs.

#### ■ XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### ■ TCP/IP Offload Engine (TOE)

TOE processor

The ASIC incorporates four XGMAC (10GbE) interfaces. These interfaces are labeled MAC0, MAC1, MAC2 and MAC3. These ports will support the 10GbE standard's SFP+ limited mode. They contain one lane (one differential TX pair and one differential RX pair) of high speed SERDES.

The SFP+ limited mode allows a maximum drive of 5m of twin ax cable and a maximum of 300m of fiber.

#### ■ Software Support

Linux operating systems

Drivers available with support for all TOE and NIC functions. Please contact factory for details.

Windows operating systems

Drivers available with support for NIC functions. Please contact factory for details.

### Comparison of TCP/IP Offload Engines (TOE): ASIC vs. Software Stack

|                                  | Acromag ASIC TOE<br>10GbE Interface | Software Stack TOE<br>10GbE Interface |
|----------------------------------|-------------------------------------|---------------------------------------|
| Throughput per Port, Full-Duplex | 2500Mbps (full-duplex)              | 40Mbps (limited by CPU)               |
| Host Overhead                    | very low                            | very high                             |
| User-to-User Latency             | 2μs                                 | 250μs                                 |
| Determinism                      | ±1μs                                | ±200μs                                |
| Reliability Under Load           | Excellent (any load condition)      | Variable (dependent on load)          |

#### ■ Electrical

XMC PCIe bus interface (P15)

One 114-pin male connector (Samtec ASP-103614-05 or equivalent).

P15 primary XMC connector

8 differential TX pairs (PCIe) and 8 differential RX pairs (PCIe).

Optional JTAG: 6 JTAG signals

(TDI, TDO, TMS, TCK, 3.3V, and ground).

JTAG interface follows IEEE Standard 1149.1, which defines a test access port (TAP) and boundary-scan architecture. System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin for system management.

Variable power (5V or 12V): 8 pins at 1A per pin.

SFP+ connectors

Four SFP+ module front I/O ports. SFP+ transceiver signals routed directly to the TOE device are capable of a maximum data rate of 10 Gb/sec

20 signals (transmit pair, receive pair, TX\_Fault, TX\_disable, MOD\_DEF(0), MOD\_DEF(1), MOD\_DEF(2), rate select, LOS, 3.3 Vdc, and ground)

#### ■ Environmental

Operating temperature

-40 to 70°C.

Storage temperature

-55 to 125°C.

Relative humidity

5 to 95% non-condensing.

Power requirements

3.3V (±5%): Consult factory.

5V (±5%): Consult factory.

12V (±5%): Consult factory.

MTBF

Contact the factory.

### Ordering Information

#### ■ XMC Modules

[XMC-6280-LF](#)

10-Gigabit Ethernet interface module, lead-free

#### ■ Accessories

For more information, see [www.acromag.com](http://www.acromag.com).

[5028-449](#)

SFP cable, SFP-to-SFP (male-male) connectors, 1 meter

[TAPCABLE1M](#)

SFP+ cable, SFP+to-SFP+ (male-male) connectors, 1 meter

[5028-452](#)

Optical module SFP transceiver, MSA, 1000Base-SX, Fiber

[5028-455](#)

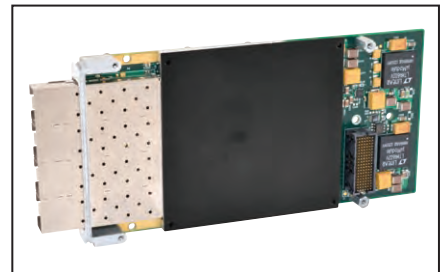
Optical module SFP transceiver, MSA, 1000Base-T RJ45 copper

[SM10G-LR](#)

10-Gigabit long reach single-mode optical module

[SM10G-SR](#)

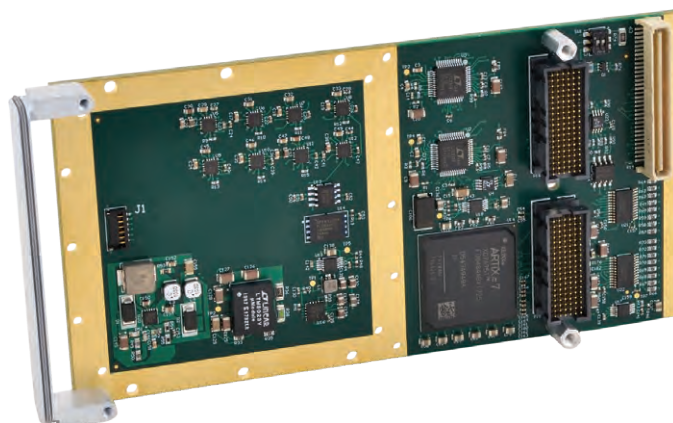
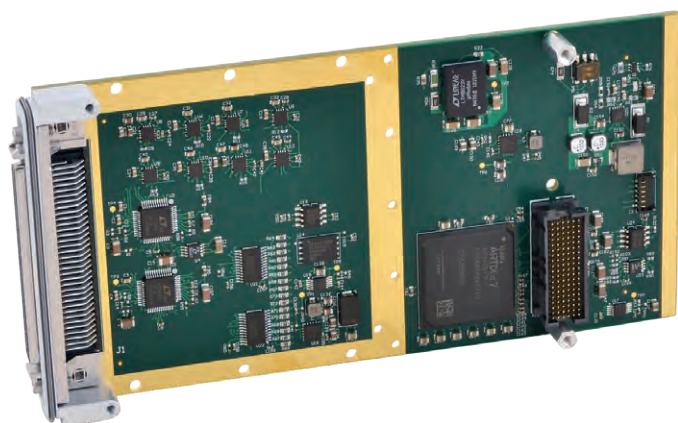
10-Gigabit short reach multi-mode optical module



Model XMC-6280 shown as it ships with pre-installed heat sink.



## XMC730 Multi-function I/O



Analog input ♦ Analog output ♦ Digital I/O ♦ Counter/timers ♦ Conduction-cooled option

### Models

**XMC730:** Front I/O

**XMC730E:** Front I/O, extended temperature

**XMC730CC:** Rear I/O, conduction-cooled

### Description

**XMC730** mezzanine modules provide a variety of I/O functions on a single plug-in card. These new high-density modules perform both high-speed and high resolution A/D and D/A conversion and also handle digital I/O and counter/timer functions.

Now you can conserve your precious XMC slots and still get all the I/O functionality you need. The XMC730 is designed for extreme versatility with many deluxe features to meet most applications. However, the XMC730 is still very budget-friendly. A conduction-cooled version is also available.

### Key Features & Benefits

#### Analog Inputs

- 16 differential ( $\pm 10.24V$ ,  $\pm 10.0V$ ,  $\pm 5.12V$ ,  $\pm 5.0V$ , 0 to 10.24V, 0 to 10.0V, 0 to 5.12V ranges)
- 16-bit ADC with integral sample-and-hold and reference
- 1.264 $\mu$ s conversion time (791KHz rate)
- 1026 sample FIFO buffer
- Programmable FIFO threshold conditions for interrupts, DMA transfers, and flags
- User-programmable channel conversion sequence and timing

- External trigger input or output
- Factory calibration constants stored in on-board flash memory for error correction

#### Analog Outputs

- Eight analog output channels ( $\pm 3V$ ,  $\pm 5V$ ,  $\pm 10V$ , -2.5 to +7.5V, 0-5V, and 0-10V ranges)
- Individual 16-bit DACs per channel with 7.5 $\mu$ s settling time
- Flexible operating mode, trigger, and memory allocation
- Configurable for direct access, single burst, continuous, or streaming (FIFO) output
- Reliable software calibration with coefficients stored on-board
- FIFO for waveform generation
- Interrupt on user-programmable FIFO threshold
- Shared 64K x 16-bit sample memory

#### Digital I/O

- 16 bidirectional input/output channels (direction configured in 8-channel groups)
- TTL-compatible thresholds
- Programmable change-of-state/level interrupts
- Failsafe power-up and system reset

#### Counter/Timers

- Multi-function 32-bit counter/timer
  - Quadrature Position measurement
  - Pulse Width modulation
  - Watchdog timer
  - Event counter
  - Frequency measurement
  - Pulse-width or period measurement
- One-shot and repetitive one-shot pulse waveform generation
- Programmable interface polarity
- Internal or external triggering
- CMOS compatible thresholds

#### General

- DMA transfer support to move data between module memory and PCIe bus
- Software development tools for VxWorks®, Linux®, and Windows® environments

## Performance Specifications

### Analog Input

Input channels:  
16 differential, voltage (non-isolated).  
Resolution: 16 bits.  
Conversion rate: 791,139.24Hz maximum.  
Settling time:  
Full-scale step 420 ns to 0.005% of FSR.  
Input ranges:  
Software-selectable on a per channel basis.  
Bipolar:  $\pm 10.24V$ ,  $\pm 10.0V \pm 5.12V$ ,  $\pm 5.0V$ .  
Unipolar: 0 to 10.24V, 0 to 10.0V, 0 to 5.12V.  
Calibrated error:  
 $\pm 3.125$  LSB max. (0 to 5.12V).  
 $\pm 2.125$  LSB max. (all other ranges).

### Analog Output

Output channels:  
8 single-ended voltage (non-isolated).  
Resolution: 16 bits.  
Settling Time:  
12.5  $\mu s$  20 V step to 1 LSB maximum.  
8.5  $\mu s$  10 V step to 1 LSB maximum.  
7.5  $\mu s$  typical.  
Output ranges (software-selectable):  
Bipolar:  $\pm 10V$ ,  $\pm 5V$ ,  $\pm 3V$ , -2.5 to +7.5V.  
Unipolar: 0 to 10V, 0 to 5V.  
Output current:  $\pm 10mA$  maximum (minimum load resistance of 1K $\Omega$  with a 10V output).  
Calibrated error:  $\pm 2.125$  LSB ( $\pm 0.0032\%$  FSR) max.

### Digital I/O

Input/output range: 0 to 5V.  
Signal thresholds:  
VIH: 2.0V minimum.  
VIL: 0.8V maximum.  
IOH: 24 mA maximum.  
IOL: 24mA maximum.  
VOH: 3.7V minimum VCCA.  
VOL: 0.55V maximum VCCA.  
Minimum pulse: 32nS.  
Debounce: Filters signals with duration <2.4  $\mu s$ .

### Counter/Timer

Configuration: 32-bit timer.  
Counter input: TTL input port.  
Counter output: MOSFET output port.  
Counter output pull-up voltage:  
+5V or 12V with 1K pull-up, set by DIP switch.  
Internal clock: 62.5MHz, 15.625MHz, 7.8125MHz, 3.90625MHz, 1.953125MHz.

### XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.  
Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.  
Electrical/mechanical interface:  
Single-Width Module.

### PCIe Compliance

Conforms to PCI Express Base Specification, Revision 2.1.  
Gen1 PCIe interface.  
BAR0 memory size: 1M Byte.

### Environmental

Operating temperature:  
XMC730: 0 to 70°C (200 LFM airflow).  
XMC730E: -40 to 85°C (200 LFM airflow).  
XMC730CC: -40 to 85°C (cold plate).  
Storage temperature: -55 to 100°C.  
Relative humidity: 5 to 95% non-condensing.  
Shock, operating:  
Designed to comply with VITA 47 Class OS1.  
Vibration, random operating:  
Designed to comply with VITA 47 Class V1.  
Power:  
3.3V  $\pm 5\%$ : 0.567A typical, 0.7A maximum.  
VPWR  $\pm 5\%$ : 0.10A typical, 0.11A maximum.  
+12V  $\pm 5\%$ : 0.03A typical, 0.0374 maximum.

## Ordering Information

### XMC Modules

**XMC730:** Multi-function I/O module with front I/O 68-pin SCSI-2 connector. Lead free.  
**XMC730E:** Multi-function I/O module with front I/O 68-pin SCSI-2 connector plus extended temperature. Lead free.  
**XMC730CC:** Multi-function I/O module with rear P16 and P4 connectors. Conduction-cooled and lead free.

### Software (see software documentation for details)

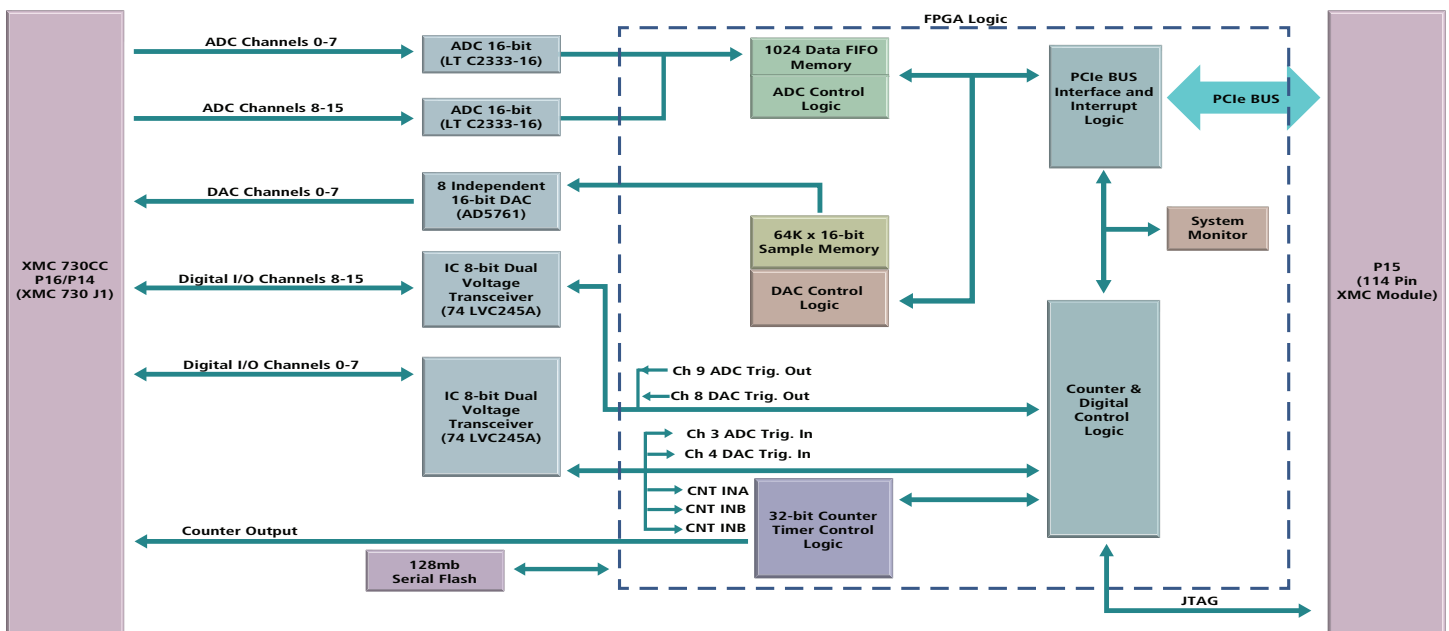
**PMCSW-API-VXW:** VxWorks® software support package  
**PCISW-API-WIN:** Windows® DLL Driver software package  
**PCISW-API-LNX:** Linux® support (website download only)

### Accessories

**5025-288:** Termination panel, SCSI-3 connector, 68 screw terminals.  
**5028-432:** Cable, shielded, SCSI-3 connector both ends.

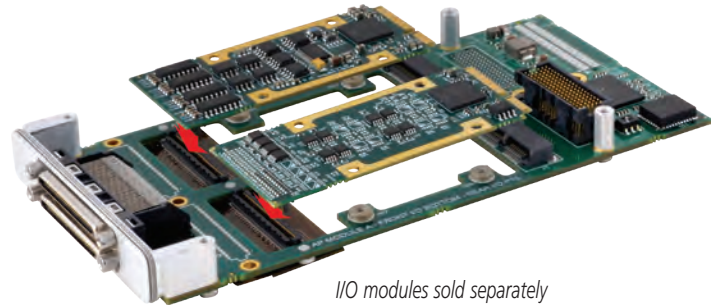
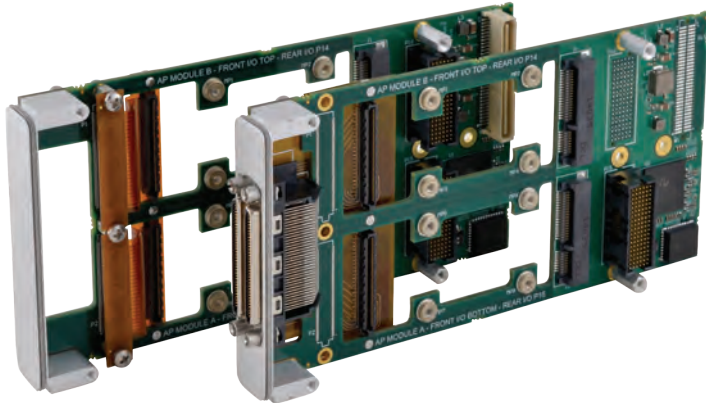
### Carrier Cards

[VPX Carrier Cards](#) | [PCIe Carrier Cards](#)



# AcroPack® Carriers

## XMCAP2000 Series XMC Carrier Cards for AcroPack® Modules



*I/O modules sold separately*

Two AcroPack or mini-PCIe mezzanine module slots ♦ Non-Intelligent carrier card ♦ PCIe x4 interface

### Description

#### Models:

XMCAP2020-LF: Front I/O

XMCAP2021-LF: Rear I/O

XMCAP2022-LF: For use with ARCX-4000 rugged computers

The AcroPack® product line updates our popular Industry Pack I/O modules with a PCIe interface format. This tech-refresh design offers a compact size, low-cost I/O, the same functionality and memory map of the existing Industry Pack modules.

This board interfaces two AcroPack mezzanine modules to a PCI Express bus on an air-cooled XMC carrier.

Two AcroPack module slots give you the freedom to mix a variety of I/O functions (A/D, D/A, digital in, digital out, serial I/O, etc.) on a single board. Or, combine modules of the same type for almost one hundred channels on a single card. Either way, the XMCAP2020/2021 saves your precious card slots and reduces your costs.

Select I/O modules from Acromag's offering or use most third-party mPCIe compliant modules.

### Key Features & Benefits

- Two AcroPack or mini-PCIe module slots support any combination of I/O functions
- PCI Express compliant
- Plug-and-play carrier configuration and interrupt support
- Front panel 68-pin CHAMP 0.8mm connectors for field I/O
- Rear P14 and P16 connectors for field I/O
- DIP switch and/or geographical addressing for card identification
- VITA 42.0, 42.3 compliant
- JTAG programming through XMC P15 connector or through onboard micro connector
- Software development tools for VxWorks®, Linux®, and Windows® environments.

**Acromag**   
THE LEADER IN INDUSTRIAL I/O

Tel: 844-878-2352 ■ solutions@acromag.com ■ www.acromag.com ■ 30765 Wixom Rd, Wixom, MI 48393 USA

## Performance Specifications

### ■ PCI Express Bus Compliance

This device meets or exceeds all written PCI Express specifications per revision 2.1.

Includes a PCIe Gen 2 switch to expand the single host PCIe port to two ports, one to each device (AcroPack or mini-PCIe).

The host port consists of four PCIe lanes, each of the mini-PCIe sites have one lane each.

### ■ Field I/O Connectors

Front I/O

XMCAP2020-LF: Two 68-pin 0.8mm Champ cable connection. Pin assignments are defined by the installed AcroPack or mini-PCIe module.

Rear I/O

XMCAP2021-LF: One AcroPack routed to rear P14 connector and one AcroPack routed to rear P16 connection.

XMCAP2022-LF: One AcroPack routed to P16 and the second to P14. Intended for ARCX-4000 applications only.

### ■ Ease of Use

A unique carrier and site number can be set for each AcroPack site by a DIP switch or geographical addressing. This provides the capability to distinguish a particular AcroPack module from others when multiple instances of the same module are used in a system.

JTAG signal are provided for programming and debugging the FPGA on some AcroPack modules. The JTAG ports of the two AcroPack modules are daisy-chained.

### ■ Physical

Physical Configuration

PCIe x4 lane

Length: 5.866 inches (149 mm)

Height: 2.9134 inches (74 mm)

Conforms to VITA 42 air-cooled XMC specification.

### ■ Environmental

Operating temperature

-40 to +70°C

Storage temperature

-55 to +125°C.

Relative humidity

5 to 95% non-condensing.

Power

+3.3 Volts (±5%): 140mA typical

VPWR: +5 Volts (± 5%): 200mA typical

VPWR: +12 Volts (± 8%): <100 mA typical

The XMCAP2020/2021 has four DC/DC converters to provide the power supply voltages to the AcroPack modules that are not present at the host interface. The +1.5 Volt supply is sourced from the VPWR host power. The +5 Volt and ±12 Volt supplies are sourced from +3.3 Volt host power.

## Ordering Information

### Carrier Card

XMCAP2020-LF: AcroPack carrier card for AcroPack or mPCIe modules, front I/O, air-cooled, two AcroPack slots.

XMCAP2021-LF: AcroPack carrier card for AcroPack or mPCIe modules, rear I/O, air-cooled, two AcroPack slots.

XMCAP2022-LF: AcroPack carrier card, rear I/O, two AcroPack slots, for ARCX-4000 applications (consult factory).

See [Acromag.com/AcroPacks](http://Acromag.com/AcroPacks) for a full list of I/O modules.

### Accessories

5025-288: Termination panel, SCSI-3 connector, 68 screw terminals.

5028-420: VHDCI 68-pin, round cable, shielded, SCSI-3 to CHAMP. 0.8mm, 2 meters long.

5028-615: Cable, 68-pin CHAMP to pigtail, 36 inches long

5028-616: Cable, 68-pin CHAMP to pigtail, 70 inches long

### Heatsinks for ARCX-4000 (consult factory)

AP-CC-02: Heat sink for two generic AP modules (left rail or single wide ARCX)

AP-CC-03: Heat sink for AP57x and generic AP modules (left rail or single wide ARCX)

AP-CC-05: Heat sink for two generic AP modules (right rail)

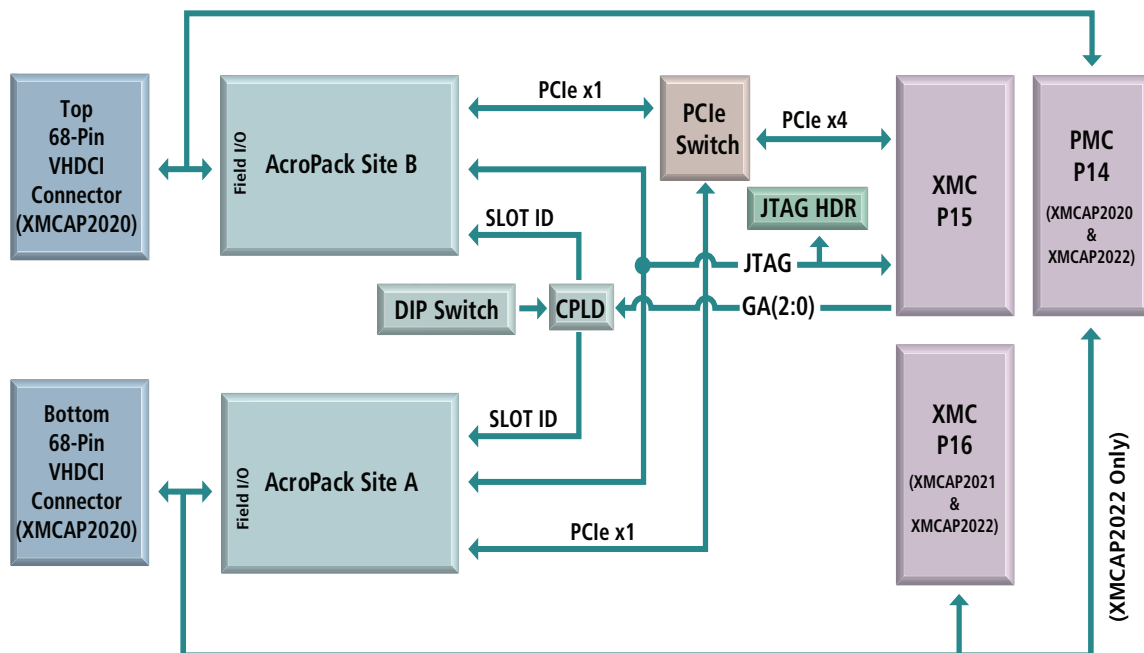
See User Manual for compatible AP modules.

### Software (see software documentation for details)

APSW-API-VXW: VxWorks® software support package

APSW-API-WIN: Windows® DLL driver software support pkg

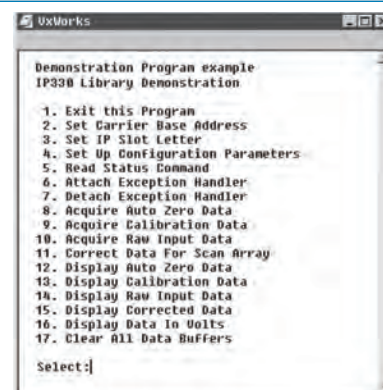
APSW-API-LNX: Linux® support (website download only)







## VxWorks® Libraries I/O Function Routines



The VxWorks software libraries provide a simple API to quickly integrate Acromag's I/O boards with your application program.

Supports any CPU target with quick modification ♦ API easily convertible for any operating system

### Description

#### Application Programming Interface (API)

Acromag's software development tools greatly simplify the interface between the I/O boards and your software application program. VxWorks libraries are supplied as "C" source code. These libraries provide easy-to-use function routines that quickly integrate with your application. Function routines are ready for use "as-is," but they are also easily customized for your unique application.

This powerful program lets you fully exercise the libraries and your hardware before running the actual application. These diagnostics will save you hours troubleshooting and debugging your applications. You can set addresses, set up registers, read real-world inputs, or drive outputs. The demonstration program steps you through the exact functions that are called in your application.

#### Target any CPU

Acromag provides direct support for VxWorks when using PowerPC, x86 and 68000 CPU boards. The VxWorks C Library includes support for x86 PCI, MV167 and MV2700 CPU boards. Each library contains detailed information on integrating with the CPU's Board Support Package (BSP). The libraries also include instructions for implementing this software with other manufacturer's CPU board BSPs. Use with Industry Pack carriers from third-party board vendors is also supported.

The IPSW-API-VXW library package offers support for Acromag carriers. Other carriers are compatible, but require some minor modifications. Acromag uses a very innovative modular programming technique. This allows new carrier files to be created without affecting any of the complex IP module files or interrupt service routines.

#### User-Friendly Licensing

Acromag's VxWorks software libraries are provided with a full site license. This allows anyone at your location to use this software without any additional charges. Additionally, no run-time license is required either.

The VxWorks software libraries include support for the full family of boards or modules, not just certain models unless otherwise noted.

### Key Features & Benefits

- Easy installation procedure
- Readme files with step-by-step instructions
- Quickly creates libraries
- Targeted support for Power PC, x86, and 68000 series CPUs
- Supports any CPU target with quick modification
- API easily convertible for any operating system
- Source code provided to ensure maximum flexibility in implementing your application
- Ability to verify operation of your modules and carriers with a demonstration program to ensure proper hardware operation before attaching your application

### Ordering Information

#### APSW-API-VXW

VxWorks software support package for AcroPack modules and carriers.

#### IPSW-A7VME-VXW

VxWorks software support package for Acromag VME SBC Series XVME6500 and XVME6700 when used with Industry Pack modules.

#### IPSW-API-VXW

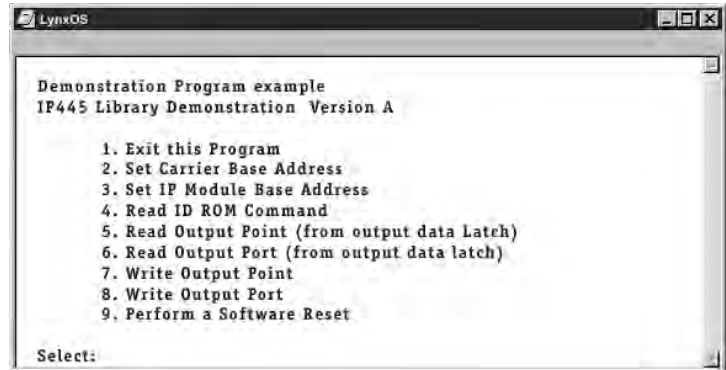
VxWorks software support package for Industry Pack modules and carriers.

#### PMCSW-API-VXW

VxWorks software support package for XMC, PMC, PCI, and CompactPCI products (supports all Acromag PMC modules and PCI or cPCI boards except IP carriers).



## Linux® Libraries I/O Function Routines



*This free software utility is available for download from Acromag's website.*

## Simplify interfacing between Acromag I/O boards and your software ♦ Demonstration Program

### Description

#### IPSW-API-LNX

Support for Industry Pack modules and carriers

#### PCISW-API-LNX

Support for PCI/CompactPCI boards and PMC modules

#### APSW-API-LNX

Support for AcroPack® modules and carriers

### Application Programming Interface (API)

Acromag's software development tools greatly simplify the interface between the I/O boards and your software application program. The Linux libraries are supplied as "C" source code. These libraries provide easy-to-use function routines that quickly integrate with your application. Function routines are ready for use "as-is," but they are also easily customized for your unique application.

### Demonstration Program

This powerful program lets you fully exercise the libraries and your hardware before running the actual application. These diagnostics will save you hours troubleshooting and debugging your applications. You can set addresses, set up registers, read real-world inputs, or drive outputs. The demonstration program steps you through the exact functions that are called in your application.

### Key Features & Benefits

- Easy installation procedure
- Readme files with step-by-step instructions
- Programming tools for most Acromag I/O boards (excludes serial I/O and VME products)
- Demonstration program
- Downloadable at no charge from the Acromag website
- Source code provided to ensure maximum flexibility in implementing your driver
- Verify operation of your I/O modules and carrier cards with a demonstration program to ensure proper hardware operation before attaching your application

### Ordering Information

*NOTE: This unsupported software is available ONLY by download from Acromag's website.*

#### [IPSW-API-LNX](#)

Linux example libraries for Industry Pack modules and PCI/CompactPCI carrier cards

#### [PCISW-API-LNX](#)

Linux example libraries for PCI, CompactPCI, and PMC modules.

#### [APSW-API-LNX](#)

Linux example libraries for AcroPack® modules and carriers.

#### [IPSW-VME-LNX](#)

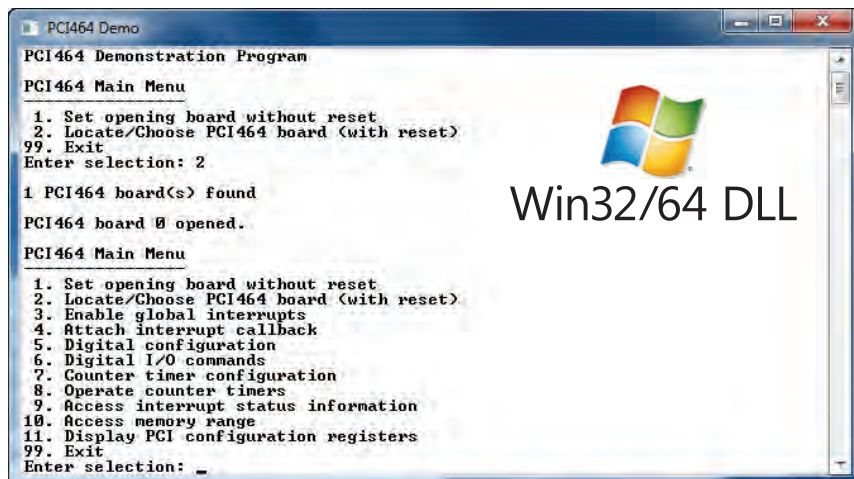
Linux example libraries, works with TSI148 chipset for models XVME-6300, XVME-6400, Industry Pack modules, and VME carriers.

#### [IPSW-A7VME-LNX](#)

VxWorks® 7.0 64-bit, software support package for Acromag Series XVME6500 and XVME6700 SBC when used with Industry Pack modules and VME carriers. Supplied on CD-ROM.

# Software Support

## PCISW-API-WIN PCI Driver Software for Windows® Operating Systems



For Windows 10 / 8 / 7 / Vista ♦ Supports Acromag XMC, PMC, PCI, CompactPCI cards ♦ Includes DLLs

### Description

#### Application Programming Interface

Acromag's software development tools greatly simplify the interface between the I/O boards and your Windows-based application program. This package provides DLL driver level support for Acromag's complete line of PMC, XMC, PCI and cPCI products. In addition, "C" source demonstration programs provide easy-to-use tools to test the operation of the module.

#### Demonstration Programs

Powerful programs let you fully exercise your hardware before developing the actual application. These diagnostics will save you hours troubleshooting and debugging your applications. You can set addresses, set up registers, read real-world inputs, or drive outputs. The demonstration programs step you through the exact functions that are called in your application.

### Key Features & Benefits

- Easy installation procedure
- Documentation with step-by-step instructions
- Support for all active Acromag I/O PMC, XMC, PCI and CompactPCI boards and all Acromag FPGA PMC, XMC, PCI and CompactPCI boards except PMC CX family Virtex-II boards.
- Support for 32-bit and 64-bit systems
- Demonstration Programs
- Driver level support for desktop and embedded Windows level programming environments
- Compatible with Windows Embedded Standard applications
- Verifies operation of your I/O boards with a demonstration program to ensure proper hardware performance before attaching your application



### Ordering Information

#### ■ Software

For more information, see [www.acromag.com](http://www.acromag.com).

#### PCISW-API-WIN

32 or 64-bit Windows driver software package with DLLs and demonstration programs for PMC, XMC, PCI, and cPCI products. Supplied on CD-ROM.

*NOTE: For Industry Pack module and carrier card support software, please refer to IPSW-API-WIN.*

#### User-Friendly Licensing

Acromag's PCI Windows driver software is provided with a full site license. This allows anyone at your location to use this software without any additional charges. No run-time license is required.

Each package supports all active PCI-based (PMC, XMC, PCI, CompactPCI) products. You do not need to order additional software for different models within the family. (does not support PMC CX family Virtex-II boards)

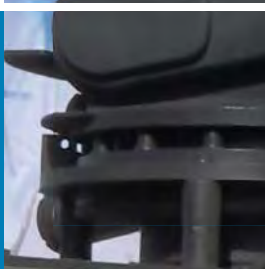


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