

Embedded Computing & I/O Solutions

# Reconfigurable FPGA Modules

mPCIe-based, XMC, PMC  
or Industry Pack Formats

Faster & Easier  
Development

Engineering  
Design Kit



# Depend on Acromag



*Experience counts – especially when engineering the right embedded solution. And with more than 60 years experience, Acromag can help you reduce your costs and increase your productivity.*



## Acromag: The I/O Leader

Acromag is focused on developing embedded computing solutions that provide the best long term value in the industry. Compare and you will find that Acromag offers an unmatched balance of price, performance, and features.

### 60+ Years of I/O Experience

With over 60 years of industrial I/O design experience, Acromag stands alone in the high-performance bus-board market. Developing VMEbus I/O boards since 1984, we combine our process control expertise with extensive experience in embedded computing. This background gives us unrivaled insight to many unique concerns when interfacing computer systems to various sensors and controllers in a wide range of applications.

Acromag processor, FPGA, and I/O products are commonly used in these industries:

- military/defense
- aerospace
- transportation
- manufacturing
- semiconductors
- scientific
- communication
- research labs

## Quality You Can Count On

We take every measure to guarantee dependable operation with ISO9001 and AS9100 certified quality management. State-of-the-art manufacturing with industrial-grade components adds extra ruggedness. Advanced inspection and testing further ensure that Acromag I/O performs at or beyond their rated specs.

## Technical Support

Drawing on a wealth of embedded I/O experience, our sales engineers are well qualified to support you in the use of our products in your end-applications. We take pride in our highly experienced staff that excels at after-sale technical support.

## Global Representation

Great care has been put into building a team of highly skilled representatives and distributors. They are located around the world to service your needs.

## Online Ordering

Find full documentation and pricing information online. You can get quotes and even order directly on our website.



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Extended Temperature  
Extended Life Cycle

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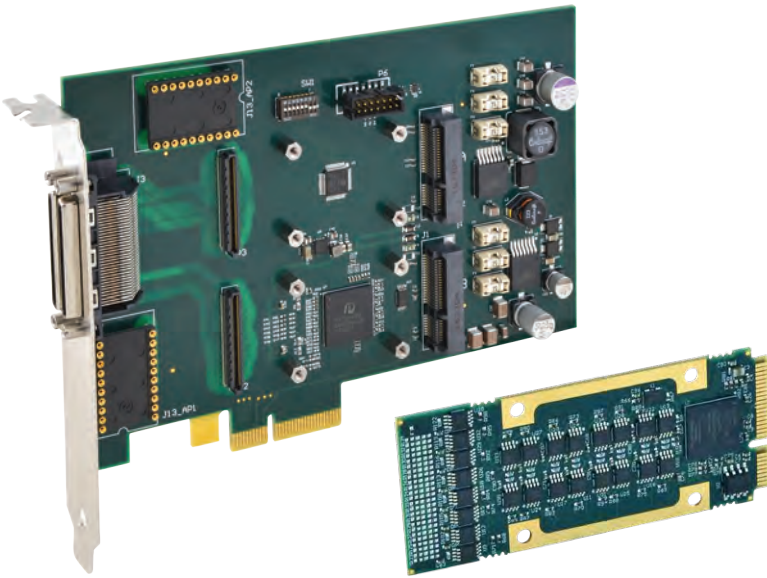
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# FPGAs Made Easy



Above: APCe7022 PCIe carrier card shown with the APA7-500

Do you want to learn how to implement FPGAs? Think the only way is with a high start-up price tag and complicated setup? Think again.

Acromag offers you an easy, cost-effective package to start your FPGA development today.

## Custom Embedded Computing with Re-Configurable FPGAs on Off-the-Shelf Mezzanine Modules

Acromag's line of user-configurable FPGA I/O modules offer the ability to create custom I/O boards. Just download your own instruction sets into the I/O module's FPGA. You can use your own application program to control the module's analog or digital I/O channels for simulation, communication, diagnostics, image processing and other applications.

## Faster and Easier Development

To help you develop custom programs, Acromag offers an Engineering Design Kit. This kit provides utilities to help you load VHDL into the FPGA and to establish DMA transfers between the FPGA and the CPU. Kits include a compiled FPGA file and example VHDL code for the local bus interface, read/writes, and change-of-state interrupts to the bus.

## What You Will Need:

### 1 Choose your FPGA module

**XMC-SLX Series** Spartan®-6 FPGA Modules

**XMC-7A Series** Artix®-7 FPGA Modules

**XMC-7K Series** Kintex®-7 FPGA Modules

**APA7 Series** Artix-7 FPGA Modules

**APZU Series** Zynq® UltraScale+™ MPSoC FPGA Modules

### 2 Select your carrier card

**APCe8675** PCI Express Carrier Card

**APCe7000** AcroPack® mPCIe-based Carrier Cards

- XMC or AcroPack module slots
- Up to 8-lanes of PCIe-based support depending on carrier
- Support high-speed serial interface between neighboring cards using protocols such as XAUI or Aurora
- JTAG support for FPGA programming

### 3 Add your EDK

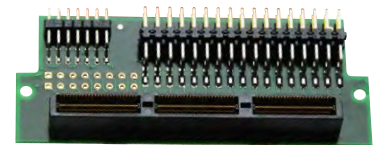
**EDK Engineering Design Kit**

- Includes AXM-EDK extension module providing standard JTAG header and LVTTTL I/O
- Includes parts list and location, schematics, compiled FPGA file and example VHDL code
- Loads VHDL code and establishes DMA transfers to CPU

### 4 Pick your OS

**Software Support Package**

- For XMC: [PCISW-API-WIN](#) Windows® DLL | [PCISW-API-LNX](#) Linux® | [PMCSW-API-VXW](#) VxWorks®
- For AcroPack: [APSW-API-VXW](#) VxWorks | [APSW-API-WIN](#) Windows DLL | [APSW-API-LNX](#) Linux



The AXM-EDK front I/O extension module includes a JTAG interface and LVTTTL I/O for application interface or debugging purposes.

 Visit [Acromag.com/FPGAS](https://www.acromag.com/FPGAS)  
**TO LEARN MORE**

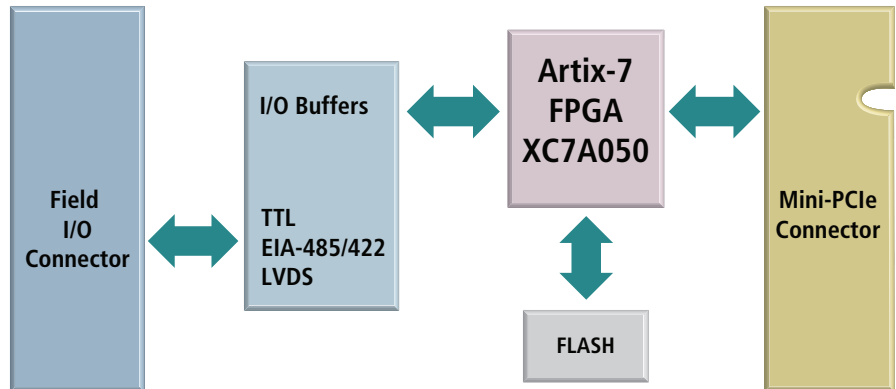
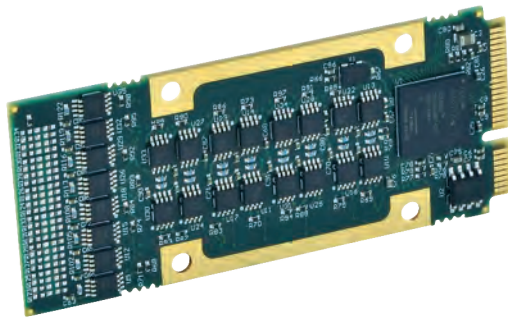
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# AcroPack® Modules

## APA7 Series User-Configurable Artix®-7 FPGA I/O Modules



Reconfigurable Xilinx® Artix®-7 FPGA ♦ Conduction or Air Cooled ♦ PCIe Bus Interface

### Description

#### Models

- APA7-501E-LF: 48 TTL channels
- APA7-502E-LF: 24 EIA-485/422 channels
- APA7-503E-LF: 24 TTL and  
12 EIA-485/422 channels
- APA7-504E-LF: 24 LVDS channels

The AcroPack® product line updates our popular Industry Pack I/O modules with a PCIe interface format. This tech-refresh design offers a compact size, low-cost I/O, the same functionality as the existing Industry Pack modules and a rugged form factor.

The APA7-500 series provides a FPGA based user-configurable bridge between a host processor and a custom digital interface via PCI Express. These boards feature a best in class Artix®-7 interface to deliver the industry's lowest power and high performance.

Designed for COTS applications these FPGA based digital I/O modules deliver user-customizable I/O, high-density, high-reliability, and high-performance at a low cost.

The APA7-500 series modules are 70mm long. This is 19.05mm longer than the full length mini PCIe card at 50.95mm. The boards width is the same as mPCIe board of 30mm and they use the same mPCIe standard board hold down standoff and screw keep out areas.

A down facing 100 pin Samtec connector mates with the carrier card. Fifty of these pins are available for field I/O signals.

The Engineering Design Kit provides users with basic information required to develop custom FPGA firmware for download to the Xilinx FPGA. Example FPGA design code is provided as a Vivado IP Integrator project for functions such as a one-lane PCI Express interface, DMA, digital I/O control register, and more. Users should be fluent in the use of Xilinx Vivado design tools.

### Key Features & Benefits

- PCI Express Generation 1 interface
- Reconfigurable Xilinx® FPGA
- High channel count digital interface: RS485, LVDS and TTL interface options.
- 32Mb quad serial Flash memory
- 52,160 logic cells
- 65,200 Flip flops
- 2,700 kb block RAM
- 120 DSP slices
- External LVTTTL clock input
- Long distance data transmission
- Example design
- Power up and system reset is failsafe
- Conduction-cooled options



## Performance Specifications

### ■ FPGA

FPGA device

Xilinx Artix-7 FPGA Model XC7A50T.

FPGA configuration

Download via flash memory.

Example FPGA program

IP integrator block diagram provided for PCIe bus 1 lane Gen 1 interface, DMA controller, on chip block RAM, flash memory and control of field I/O.

See EDK kit.

### ■ I/O Processing

Field I/O Interface

PCIe bus 1 lane Gen 1 interface .

I/O Connector

100 pin field I/O connector.

### ■ Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a APA7-500 series module (see [www.acromag.com](http://www.acromag.com) for more information).

### ■ PCI Express Base Specification

Conforms to revision 2.0

Lanes

1 lane in each direction.

Bus Speed

2.5 Gbps (Generation 1).

Memory

128k space required.

1 base address register.

### ■ Environmental

Operating temperature

Air Cooled with heat sink

-40 to 80°C.

Air Cooled without heat sink

-40 to 70°C.

Conduction Cooled

-40 to 85°C.

*A conduction cooled application with an AcroPack requires heatsink model AP-CC-01.*

Storage temperature

-55 to 125°C .

Relative humidity

5 to 95% non-condensing.

Power

+3.3V (±5%) 500mA typical.

### ■ Physical

Length

70mm.

Width

30mm.

## Ordering Information

### AcroPack<sup>®</sup> Modules

[APA7-501E-LF](#)

48 TTL channels.

[APA7-502E-LF](#)

24 EIA-485/422 channels.

[APA7-503E-LF](#)

24 TTL & 12 EIA-485/422 channels.

[APA7-504E-LF](#)

24 LVDS channels.

*(Note: AcroPack modules are compatible only with the carriers listed below)*

### Accessories

[AP-CC-01](#)

Conduction-cool kit.

[APA7-EDK](#)

Engineering design kit. *(One kit required)*

### Carrier Cards

See [Acromag.com/AcroPack-Carriers](http://Acromag.com/AcroPack-Carriers) for a full list of AcroPack carrier cards.

**Software** *(see software documentation for details)*

[APSW-API-VXW](#)

VxWorks<sup>®</sup> software support package.

[APSW-API-WIN](#)

Windows<sup>®</sup> DLL driver software support package.

[APSW-API-LNX](#)

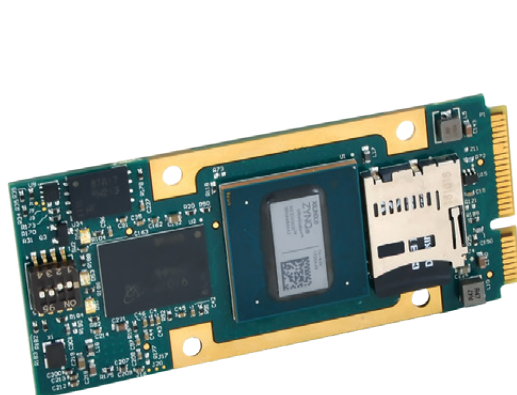
Linux<sup>®</sup> support (website download only).



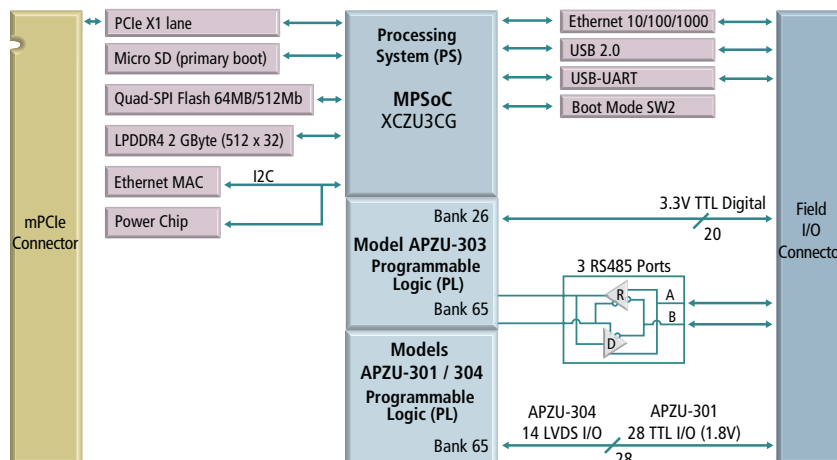
AP-CC-01 Conduction-Cool Kit

# AcroPack® Modules

## APZU Series User-Configurable Zynq® UltraScale+™ MPSoC I/O Modules



ZYNQ®



Xilinx® Zynq UltraScale+™ MPSoC ♦ ARM Cortex™ A53 & R5 CPUs ♦ Programmable logic ♦ PCIe Bus Interface

### Models

APZU-301: 28 TTL I/O  
APZU-303: 20 TTL and 3 RS485/422  
APZU-304: 14 LVDS I/O

### Description

AcroPack® modules are a ruggedized version of a mini PCIe card. AcroPacks add a down-facing 100-pin connector to internally route I/O signals through the carrier card to secure field connectors, thus eliminating loose cables and increasing reliability.

APZU series modules provide a programmable Xilinx Zynq UltraScale+ multiprocessor system on a chip (MPSoC). This MPSoC combines a feature-rich ARM-based processing system and programmable logic in a single device. Two dual-core ARM Cortex CPUs (A53 application processor and R5 real-time processor) deliver high-performance computation capability. Additional resources include on-chip memory, external memory interfaces, and a rich set of peripheral connectivity interfaces. The integrated ASIC-class programmable logic is ideal for compute-intensive tasks and offloading critical applications.

The real value of the Zynq UltraScale+ MPSoC architecture lies in the tight integration of its programmable logic with the processing system. Its high throughput interface eliminates bottlenecks that plague two-chip ASSP-FPGA solutions and allows designers to easily extend the processing system capabilities. Now developers can build custom designs by adding peripherals in the programmable logic and increase overall system performance by partitioning hardware and software functions with custom accelerators.

Designed for COTS applications these FPGA-based digital I/O modules deliver user-customizable I/O in a high-density and very rugged form factor. Typical applications involve adaptive filtering, sensor fusion, motor control, and image processing.

Acromag's Engineering Design Kit (EDK) provides an FPGA generated firmware example design that provides host access to the hardware digital I/O on the APZU module. The example is implemented using the Xilinx Vivado® development environment and offers a starting point from which customers can develop their customized applications.

### Key Features & Benefits

#### Zynq MPSoC

- Dual-core ARM Cortex A53-based application processor unit (APU)
- Dual-core ARM Cortex R5-based real-time processor unit (RPU)
- NEON™ media-processing engine
- UltraScale+ 154k programmable logic cells
- Extensive on-chip memory

#### I/O and Peripherals

- TTL, LVDS, or RS422/485 I/O interface
- Gigabit Ethernet interface
- USB 2.0 transceiver
- USB-UART debug terminal port

#### General

- PCI Express interface
- MicroSD or NOR flash boot
- Quad-SPI flash memory
- LPDDR4 storage memory
- DMA transfers
- BSP and FPGA design kit software
- VxWorks®, Linux®, and Windows® support

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## Performance Specifications

### ■ Multiprocessor SoC

#### MPSoC device

Xilinx Zynq XCZU3CG-2SBVA484I.

Application processor: Dual-core ARM Cortex-A53, 1.3GHz. Single/double precision floating point unit.

Real-time processor: Dual-core ARM Cortex-R5, 533MHz. Single/double precision floating point unit.

NEON Advanced SIMD media-processing engine.

Programmable logic resources:

154,350 logic cells; 70,560 LUTs; 360 DSP slices.

#### Configuration

Primary boot from SD card or NOR flash alternate.

### ■ I/O and Peripheral Interfaces

#### I/O connector

68 pin field I/O (to carrier card).

#### Digital I/O

APZU-301: 28 TTL I/O channels (1.8V).

APZU-303: 20 TTL and 3 RS485/422 channels (3.3V).

APZU-304: 14 LVDS I/O channels.

#### Interrupts

20 channels of interrupts configurable for high-to-low, low-to-high, and change-of-state event types.

#### LPDDR Memory

2 Gbyte (512Mbit x 32).

#### Quad-SPI flash

512 Mbit (64 Mbyte) Nor flash device.

#### SD card interface

16 GB industrial MLC microSD card pre-programmed with boot.bin file.

#### Gigabit Ethernet interface

Supports 1000BASE-T, 100BASE-TX, and 10BASE-T. Zynq gigabit Ethernet controller uses a media independent interface (RGMII). External magnetics and RJ45 are provided on the breakout panel.

#### USB 2.0 interface

Microchip USB3320C.

#### UART to USB interface

Silicon Labs CP2103GM.

#### Breakout panel

Model 5028-626 panel mates directly to all 68-pin AcroPack carriers. Brings RJ45 ethernet port, USB 2.0 port, UART to USB port, digital I/O at jumper blocks, and power and reset buttons out to the field.

### ■ PCI Express

#### Compatibility

Conforms to PCI Express Base Specification, Rev.2.1.

#### PCIe interface

PCIe bus 1-lane (x1) Gen 1 interface.

2.5 Gbps signaling rate.

#### Memory space

1M Byte: BAR0 to Zynq DMA registers.

32K Byte: BAR1 to programmable logic register space.

64K Byte: BAR2 to DDR memory space.

### ■ Environmental

#### Operating temperature

Air-cooled (with heat spreader): -40 to 70°C (minimum airflow of 400LFM is recommended).

Conduction-cooled: -40 to 80°C.

#### Storage temperature

-55 to 125°C.

#### Relative humidity

5 to 95% non-condensing.

#### Power

3.3V DC (±5%): 57 mA typical, 100 mA max.

5.0V DC (±5%): 183 mA typical, 230 mA max.

+12V DC (±5%): 165 mA typical, 200 mA max.

1.5V, -12V DC: not used.

#### Vibration, sinusoidal operating

Designed to comply with IEC 60068-2-6.

10-500Hz, 5G, 2 hours/axis.

#### Vibration, random operating

Designed to comply with IEC 60068-2-64.

10-500Hz, 5G-rms, 2 hours/axis.

#### Shock, operating

Designed to comply with IEC 60068-2-27.

30G, 11ms half sine; 50G, 3ms half sine;

18 shocks at 6 orientations for both test levels.

#### Mean time between failure (MTBF)

MIL-HDBK-217F, FN2. Ground benign, controlled.

25°C: 1,459,102 MTBF hours; 167 MTBF years;

685.4 failure rate (FIT).

40°C: 923,762 MTBF hours; 105.5 MTBF years;

1,082.5 failure rate (FIT).

FIT is failures in 10<sup>9</sup> hours.

### ■ Physical

#### Dimensions

Length, width, height: 70 x 30 x 12.5 mm.

Board thickness: 1.0 mm.

Weight: 35.18 g (including heat spreader).

### ■ Engineering Design Kit

Board support package and FPGA design kit for Xilinx Vivado®. Example of IP Block design, block RAM, system monitor, AXI interface to digital I/O.

Kit must be ordered with the first purchase of an APZU module (see [www.acromag.com](http://www.acromag.com) for more information).

## Ordering Information

### AcroPack® Modules

[Go to website product page for more information.](#)

#### APZU-301

28 TTL channels (1.8V).

#### APZU-301-QSP

Quick Start Package includes APZU-301 module, APCe7012 carrier, 5028-626 I/O panel, APZU-EDK software.

#### APZU-303

20 TTL & 3 EIA-485/422 channels (3.3V).

#### APZU-303-QSP

Quick Start Package includes APZU-303 module, APCe7012 carrier, 5028-626 I/O panel, APZU-EDK software.

#### APZU-304

14 LVDS channels.

#### APZU-304-QSP

Quick Start Package includes APZU-304 module, APCe7012 carrier, 5028-626 I/O panel, APZU-EDK software.

### Accessories

#### APZU-EDK

Engineering design kit. (One kit required)

#### 5028-626

I/O breakout panel with cables for Ethernet, USB, UART, JTAG, and 68-pin carrier card connections.

### Carrier Cards

See [Acromag.com/AcroPack-Carriers](http://Acromag.com/AcroPack-Carriers) for a full list of AcroPack carrier cards.

### Software

(see software documentation for details)

#### APSW-API-VXW

VxWorks® software support package.

#### APSW-API-WIN

Windows® DLL driver software support package.

#### APSW-API-LNX

Linux® support (website download only).

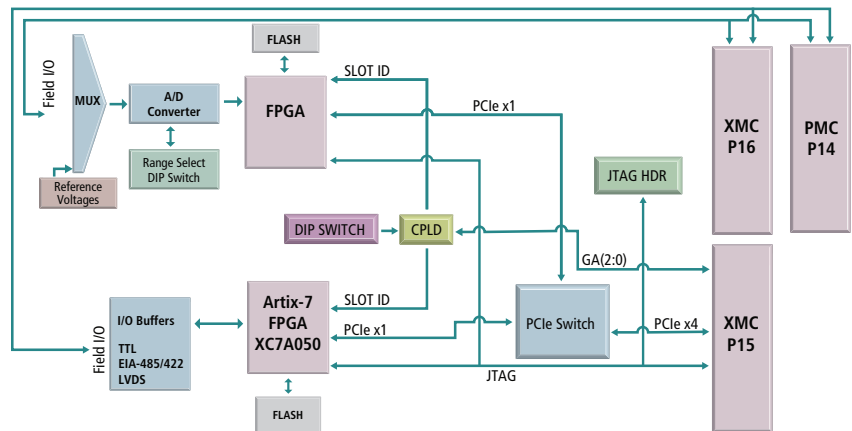
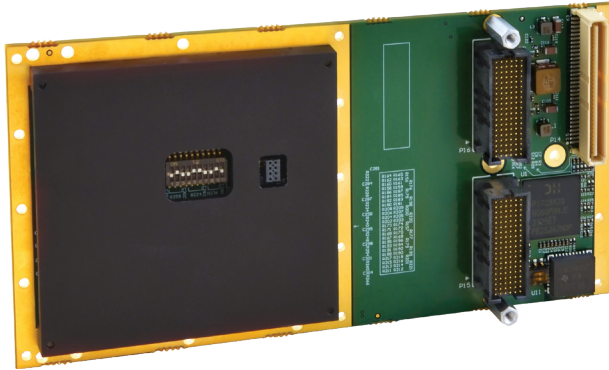


APZU-30x with included heat spreader attached



# XMC Modules

## XMC-7A50-AP323 XMC Module with Artix®-7 FPGA and High-Density I/O



Reconfigurable Xilinx® Artix®-7 FPGA ◆ 48 Digital I/O ◆ 20 Diff or 40 SE Analog Inputs ◆ 16-bit ADC

### Description

XMC-7A51-AP323: 48 TTL channels

**Custom Requirements:** Other I/O combinations are possible, contact Acromag for more information.  
Build Option A: 24 EIA-485/422 channels  
Build Option B: 24 TTL and 12 EIA-485/422 channels  
Build Option C: 24 LVDS channels

Designed for COTS applications, these XMC modules combine a user-customizable FPGA with digital I/O and high-performance analog inputs for high-density signal processing.

The XMC-7A50-AP323 series provides a FPGA based user-configurable bridge between a host processor and a custom digital interface via PCI Express. These XMC boards feature a best-in-class Artix®-7 interface to deliver the industry's lowest power and high performance.

The analog inputs monitor 20 differential or 40 single-ended channels. Software or an external hardware input can trigger A/D conversions for synchronization to external events. On-board, precision voltage references enable accurate software calibration of the module without external instruments.

The Engineering Design Kit provides users with basic info. required to develop custom FPGA firmware for download to the Xilinx® FPGA. Example FPGA design code is provided as a Vivado IP Integrator project for functions such as a one-lane PCI Express interface, DMA, digital I/O control register, and more. Users should be fluent using Xilinx Vivado® design tools.

### Key Features & Benefits

#### FPGA Digital I/O

- Reconfigurable Xilinx FPGA
- High channel count digital interface: TTL, RS485, and LVDS interface options
- 32Mb quad serial flash memory
- 52,160 logic cells
- 65,200 Flip flops
- 2,700 kb block RAM
- 120 DSP slices
- External LVTTTL clock input
- Long distance data transmission
- Example design
- Power up and system reset is failsafe

#### Analog Input

- 20 differential or 40 single-ended inputs
- Flexible scan control
- 16-bit A/D resolution
- 8µs conversion time
- FIFO buffer with 16K sample memory
- Interrupt upon FIFO threshold condition
- FIFO full, empty and threshold reached flags
- Programmable channel conversion control
- Programmable conversion timer
- Several scanning modes
- External trigger

#### General

- Wide temperature range
- Conduction cooling options
- Software development tools for VxWorks®, Linux®, and Windows® environments

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## Performance Specifications

### ■ XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-width module.

### ■ PCI Express Base Specification

Conforms to revision 2.0

#### Lanes

1 lane in each direction.

#### Bus Speed

2.5 Gbps (Generation 1).

#### Memory

128k space required.

1 base address register.

### ■ FPGA

#### FPGA device

Xilinx Artix-7 FPGA Model XC7A50T.

#### FPGA configuration

Download via flash memory.

#### Example FPGA program

IP integrator block diagram provided for PCIe bus 1 lane Gen 1 interface, DMA controller, on chip block RAM, flash memory and control of field I/O. See EDK kit.

### ■ I/O Processing

#### Field I/O Interface

PCIe bus 1 lane Gen 1 interface.

#### I/O Connector

100 pin field I/O connector.

### ■ Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7A50-AP323 series module (see [www.acromag.com](http://www.acromag.com) for more information).

### ■ Digital I/O

#### TTL Channels

48 input/output channels. Direction is controlled in groups of eight channels. 5V tolerant.

#### TTL Electrical Characteristics

$V_{IH}$ : 2.0V minimum.

$V_{IL}$ : 0.8V maximum.

$I_{OH}$ : -32.0mA.

$I_{OL}$ : 64.0mA.

$V_{OH}$ : 2.0V minimum.

$V_{OL}$ : 0.55V maximum at 64mA.

### ■ Analog Input

#### Input configuration

20 differential or 40 single-ended.

#### A/D Resolution

16 bits.

#### Input range (dip switch-selectable)

Bipolar  $\pm 5V$  or  $\pm 10V$ .

Unipolar 0 to +5V or 0 to +10V.

#### Data sample memory

16K sample FIFO buffer.

#### Maximum throughput rate

200KHz (5 $\mu$ S/conversion).

#### A/D triggers

External, and software.

#### System accuracy

2.4 LSB (0.014%).

Maximum overall calibrated error at 25°C.

Input Range (Volts)	ADC Range (Volts)	Maximum Error $\pm$ LSB (%span)	Typical Error $\pm$ LSB (%span)
$\pm 5$	$\pm 5$	$\pm 8.6$ LSB (0.013%)	$\pm 8.6$ LSB (0.013%)
$\pm 10$	$\pm 10$	$\pm 9.4$ LSB (0.014%)	$\pm 3$ LSB (0.005%)

#### Data format

Binary two's compliment and straight binary.

#### Input overvoltage protection

Power on: -20V to +40V.

Power off: -35V to +55V

#### Common mode rejection ratio (60Hz)

96dB typical.

#### Channel-to-channel rejection ratio (60Hz)

96dB typical.

### ■ Environmental

#### Operating temperature

-40 to 70°C.

#### Storage temperature

-55 to 100°C.

#### Relative humidity

5 to 95% non-condensing.

#### Power

Power Supply	Typical	Maximum
+3.3V	455mA	550mA
VPWR (+5V)	20mA	30mA
VPWR (+12V)	0.7mA	1.4mA
+12V	<100mA	100mA
-12V	0.7mA	1.4mA

### ■ Physical

#### Length

5.866 inches (143.75mm.)

#### Width

2.9134 inches (74mm.)

#### Weight

3.392 oz (96.162g).

## Ordering Information

### XMC Modules

[Go to on-line ordering page >](#)

XMC-7A51-AP323

48 TTL channels

**Custom Requirements:** Other I/O combinations are possible, contact Acromag for more information.

Build Option A: 24 EIA-485/422 channels.

Build Option B: 24 TTL and 12 EIA-485/422 channels.

Build Option C: 24 LVDS channels.

### Accessories

#### APA7-EDK

Engineering design kit. (One kit required).

#### 5028-564

JTAG adapter cable.

### Carrier Cards

See [Acromag.com](http://Acromag.com) for a full list of XMC carrier cards.

### Software

(see software documentation for details)

#### APSW-API-VXW

VxWorks® software support package.

#### APSW-API-WIN

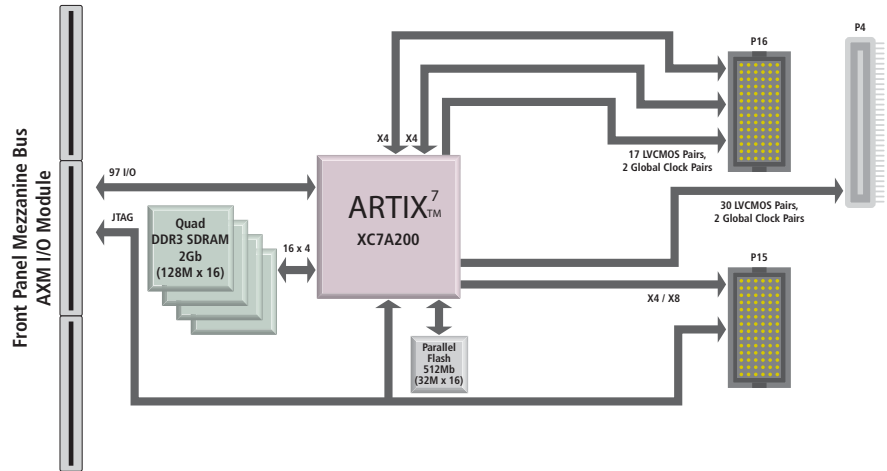
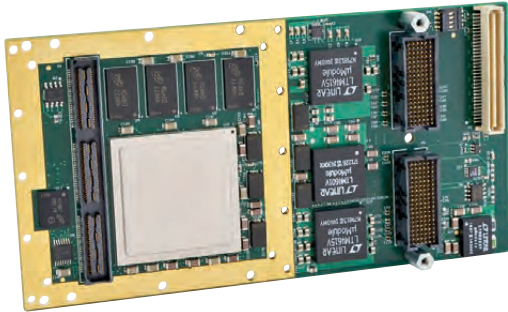
Windows® DLL driver software support package.

#### APSW-API-LNX

Linux® support (website download only).

# XMC Modules

**XMC-7A200** User-Configurable Artix<sup>®</sup>-7 FPGA Modules with Plug-In I/O   



**XMC module with PCIe interface ♦ Logic-optimized Artix-7 FPGA ♦ I/O Extension Mezzanine Modules**

## Description

Acromag's [XMC-7A](#) modules feature a high-performance user-configurable Xilinx<sup>®</sup> Artix<sup>®</sup>-7 FPGA enhanced with high-speed memory and a high-throughput serial bus interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

Both front and rear I/O is supported. Front I/O processing is supported with plug-in AXM mezzanine cards. A variety of AXM I/O cards are available to add the flexibility of a wide range of analog and digital I/O to your design.

The rear I/O provides an 8-lane high-speed serial interface on the P16 XMC port for customer-installed soft cores. P16 also supports 34 SelectIO channels. The P4 port adds another 60 SelectIO and global clock lines. SelectIO signals are Artix-7 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL)

With Acromag's Artix-7 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze<sup>™</sup> soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with Vivado<sup>®</sup> or ISE<sup>®</sup> Design Suite. And with ChipScope<sup>™</sup> Pro tools, you can rapidly debug logic and serial interfaces



## Key Features & Benefits

- Reconfigurable Xilinx Artix-7 FPGA with 200k logic cells
- 128M x 64-bit DDR3 SDRAM
- 32M x 16-bit parallel flash memory for MicroBlaze FPGA program code storage
- 4-lane high-speed serial interface on rear P15 connector for PCIe Gen 1/2 (standard), Serial RapidIO, 10Gb Ethernet, Xilinx Aurora
- 8-lane high-speed interfaces on rear P16 connector for customer-installed soft cores
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- DMA support provides data transfer between system memory and the on-board memory
- Support for Xilinx ChipScope<sup>™</sup> Pro interface

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## XMC-7A200 User-Configurable Artix-7 FPGA Modules w Plug-In I/O

### Performance Specifications

#### ■ FPGA

FPGA device

Xilinx® Artix®-7 FPGA.

Model XC7A200T FPGA with 215,360 logic cells and 740 DSP48E1 slices.

FPGA configuration

Download via JTAG or flash memory.

Example FPGA program

IP integrator block diagram provided for bus interface, front & rear I/O control, and SDRAM memory interface controller. See EDK kit.

#### ■ I/O Processing

Acromag AXM I/O Modules:

AXM modules plug into the XMC module's front mezzanine for additional I/O lines. Analog and digital I/O AXM modules are sold separately.

Rear high-speed I/O

12 high-speed serial lanes.

x8 lanes via P15 and x8 lanes via P16.

Rear user I/O

P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.

P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

#### ■ Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7A module (see [www.acromag.com](http://www.acromag.com) for more information).

#### ■ XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### ■ Electrical

XMC PCIe bus interface (P15 and P16)

One 114-pin male connector (Samtec ASP-103614-05 or equivalent).

P15 primary XMC connector

8 differential pairs (PCIe x4 standard, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.

System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin, powers volatile memory to store the bitstream encryption key.

Variable power (5V or 12V): 8 pins at 1A per pin.

P16 XMC connector

8 differential pairs (PCIe, Serial RapidIO, or Xilinx Aurora).

17 LVDS pairs or 34 SelectIO signals (differential pairs grouped per VITA 46.0 X38s).

2 global clock pairs.

Vcco pins are powered by 2.5V and support the 2.5V I/O standards.

P4 PMC rear I/O connector

64-pin female receptacle header (AMP 120527-1 or equivalent).

64 I/O connections (30 LVDS pairs plus two global clocks).

Vcco pins powered by 2.5V and support the 2.5V I/O standards.

#### ■ Environmental

Operating temperature

XMC-7A200-LF: -40 to 55°C.

Storage temperature

-55 to 125°C.

Relative humidity

5 to 95% non-condensing.

Power

+3.3 Volts

2.1 A typical

+3.3 Aux Volts

17 uA typical

+12/5 Volts (VPWR)

150 mA @ +12V typical

+12 Volts

0.1 mA typical

MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-7KA-EDK is required to configure FPGA.

#### ■ XMC Modules

[XMC-7A200-LF](#)

User-configurable Artix-7 FPGA, 200k logic cells with AXM support

#### ■ Accessories

[AXM-A75](#)

16 analog inputs, 8 analog outputs, and 16 digital I/O

[AXM-A30](#)

2 analog input 100MHz 16-bit A/D channels.

[AXM-D02](#)

30 RS485 differential I/O channels.

[AXM-D03](#)

16 CMOS and 22 RS485 differential I/O channels.

[AXM-D04](#)

30 LVDS I/O channels.

AXM-??

Custom I/O configurations available, call factory

#### ■ Software

For more information, see [www.acromag.com](http://www.acromag.com).

[XMC-7KA-EDK](#)

Engineering Design Kit (one kit required)

[PMCSW-API-VXW](#)

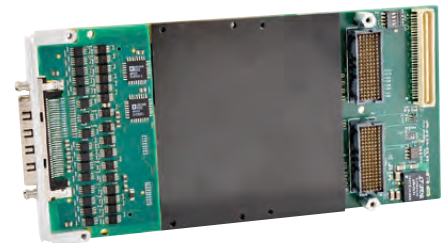
VxWorks® 32-bit software support package

[PCISW-API-WIN](#)

Windows® DLL software support package

[PCISW-API-LNX](#)

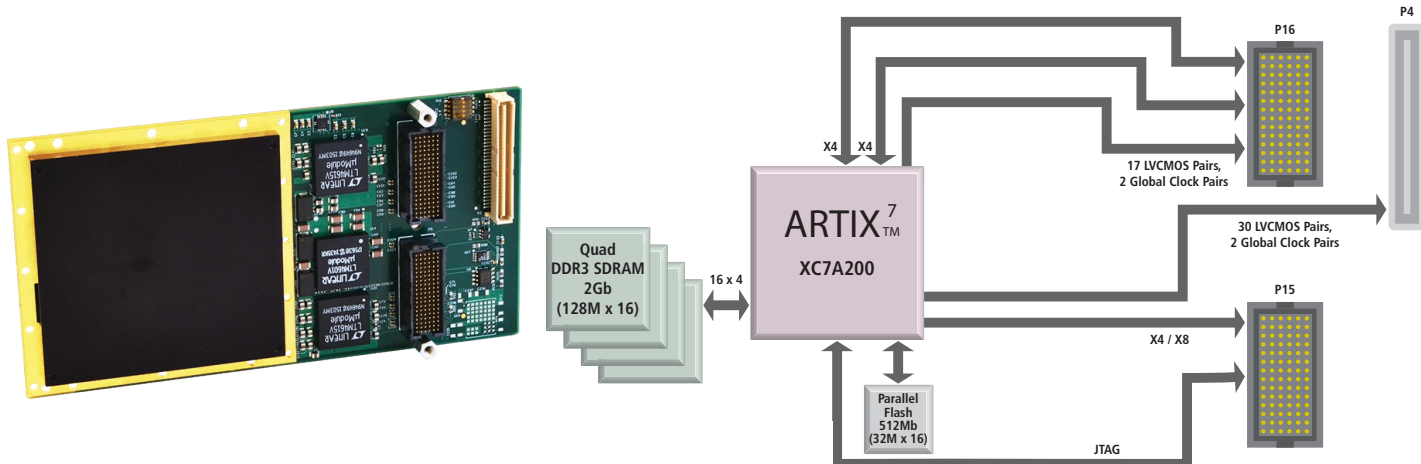
Linux® support (website download only)



XMC-7A200-LF with AXM-A75 and heat sink.



## XMC-7A200 CC User-Configurable Conduction-Cooled Artix®-7 FPGA Modules C€



XMC module with PCIe interface ♦ Logic-optimized Artix-7 FPGA ♦ Conduction-Cooled

### Description

Acromag's **XMC-7A200CC** modules feature a high-performance user-configurable Xilinx® Artix®-7 FPGA enhanced with high-speed memory and a high-throughput serial bus interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

The rear I/O provides an 8-lane high-speed serial interface on the P16 XMC port for customer-installed soft cores. P16 also supports 34 SelectIO channels. The P4 port adds another 60 SelectIO and global clock lines. SelectIO signals are Artix-7 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL)

With Acromag's Artix-7 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with Vivado® or ISE® Design Suite. And with ChipScope™ Pro tools, you can rapidly debug logic and serial interfaces

### Key Features & Benefits

- Reconfigurable Xilinx Artix-7 FPGA with 215K logic cells
- 128M x 64-bit DDR3 SDRAM
- 32M x 16-bit parallel flash memory for MicroBlaze FPGA program code storage
- 4-lane high-speed serial interface on rear P15 connector for PCIe Gen 1/2 (standard), Serial RapidIO, 10Gb Ethernet, Xilinx Aurora
- 8-lane high-speed interfaces on rear P16 connector for customer-installed soft cores
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- DMA support provides data transfer between system memory and the on-board memory
- Support for Xilinx ChipScope™ Pro interface
- Extended temperature conduction-cooled

## XMC-7A200 CC User-Configurable Conduction-Cooled Artix-7 FPGA Modules

### Performance Specifications

#### ■ FPGA

FPGA device

Xilinx Artix-7 FPGA.

Model XC7A200T FPGA with 215,360 logic cells and 740 DSP48E1 slices.

FPGA configuration

Download via JTAG or flash memory.

Example FPGA program

IP integrator block diagram provided for bus interface, front & rear I/O control, and SDRAM memory interface controller. See EDK kit.

#### ■ I/O Processing

Rear high-speed I/O

12 high-speed serial lanes.

x4 lanes via P15 and x8 lanes via P16.

Rear user I/O

P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.

P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

#### ■ Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7 series module (see [www.acromag.com](http://www.acromag.com) for more information).

#### ■ XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### ■ Electrical

XMC PCIe bus interface (P15 and P16)

One 114-pin male connector

(Samtec ASP-103614-05 or equivalent).

P15 primary XMC connector

4 differential pairs (PCIe standard, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.

System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin, powers volatile memory to store the bitstream encryption key.

Variable power (5V or 12V): 8 pins at 1A per pin.

P16 XMC connector

8 differential pairs (PCIe, Serial RapidIO, or Xilinx Aurora).

17 LVDS pairs or 34 SelectIO signals (differential pairs grouped per VITA 46.0 X38s).

2 global clock pairs.

Vcco pins are powered by 2.5V and support the 2.5V I/O standards.

P4 PMC rear I/O connector

64-pin female receptacle header

(AMP 120527-1 or equivalent).

64 I/O connections (30 LVDS pairs plus two global clocks).

Vcco pins powered by 2.5V and support the 2.5V I/O standards.

#### ■ Environmental

Operating temperature

XMC-7A200CC-LF: Conduction-cooled, -40 to 75°C.

Storage temperature

-55 to 125°C.

Relative humidity

5 to 95% non-condensing.

Power

3.3V (±5%): 7W typical.

12V (±5%): 2W typical.

3.3V AUX (±5%): 57µW

MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-7KA-EDK is required to configure FPGA.

#### ■ XMC Modules

[Go to on-line ordering page >](#)

XMC-7A200CC-LF

User-configurable Artix-7 FPGA, 215k logic cells, conduction-cooled

#### ■ Software

For more information, see [www.acromag.com](http://www.acromag.com).

XMC-7KA-EDK

Engineering Design Kit (one kit required)

PMCSW-API-VXW

VxWorks® 32-bit software support package

PCISW-API-WIN

Windows® DLL software support package

PCISW-API-LNX

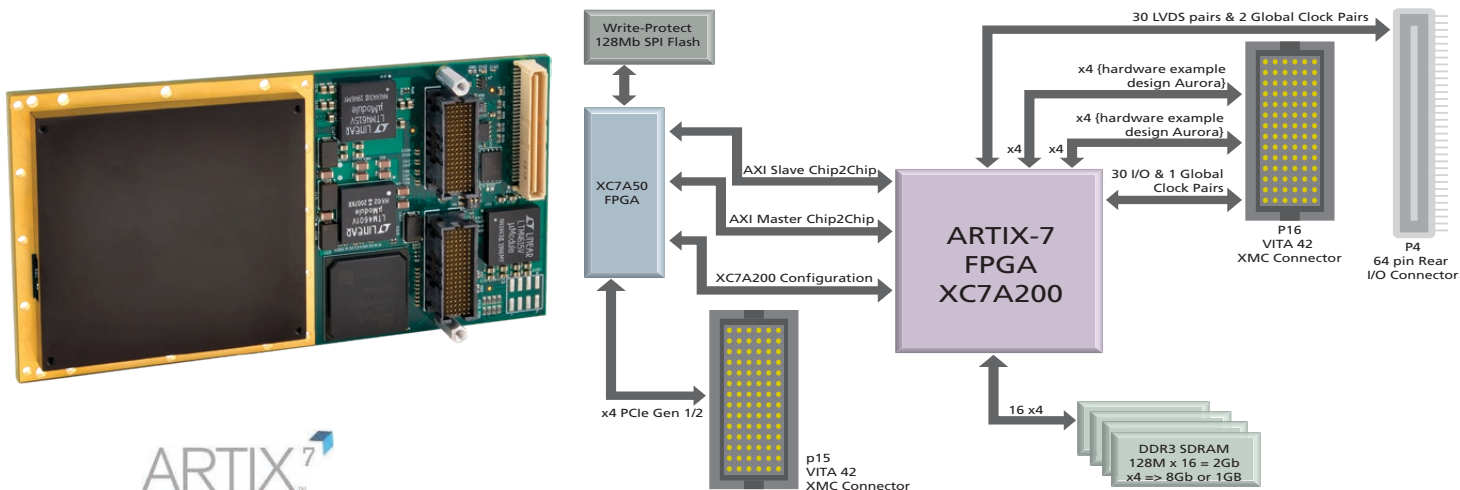
Linux® support (website download only)





# XMC Modules

## XMC-7AWP User-Configurable Artix®-7 FPGA Modules



XMC module with PCIe interface ♦ Logic-optimized Artix-7 FPGA ♦ Write-protected flash

### Description

Acromag's XMC-7AWP modules feature a high-performance user-configurable Xilinx® Artix®-7 FPGA enhanced with high-speed memory and a high-throughput serial bus interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

For security, the FPGA's configuration flash is write-protected. The XC7A200 is only configurable via PCIe bus or JTAG. There is no configuration memory.

The rear I/O provides an 8-lane high-speed serial interface on the P16 XMC port for customer-installed soft cores. P16 also supports 34 SelectIO channels. The P4 port adds another 60 SelectIO and global clock lines. SelectIO signals are Artix-7 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL)

With Acromag's Artix-7 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with Vivado® or ISE® Design Suite. And with Integrated Logic Analyzer, you can rapidly debug logic and serial interfaces.

### Key Features & Benefits

- Reconfigurable Xilinx Artix-7 FPGA with 200k logic cells
- 128M x 64-bit DDR3 SDRAM
- XC7A50 FPGA bitstream storage flash is write protected via DIP switch selection.
- 4-lane high-speed serial interface on rear P15 connector for PCIe Gen 1/2 (standard), Serial RapidIO, 10Gb Ethernet, Xilinx Aurora
- 8-lane high-speed interfaces on rear P16 connector for customer-installed soft cores
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- DMA support provides data transfer between system memory and the on-board memory



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## XMC-7AWP User-Configurable Artix-7 FPGA Modules

### Performance Specifications

#### FPGA

FPGA device

Xilinx® Artix®-7 FPGA.

Model XC7A200T FPGA with 215,360 logic cells and 740 DSP48E1 slices.

FPGA configuration

XC7A200 is configurable via PCIe bus or JTAG.

XC7A50 is configured from flash memory or JTAG.

Flash is write protected by default.

Example FPGA program

IP integrator block diagram provided for bus interface, front & rear I/O control, and SDRAM memory interface controller. See EDK kit.

#### I/O Processing

Rear high-speed I/O

12 high-speed serial lanes.

x8 lanes via P15 and x8 lanes via P16.

Rear user I/O

P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.

P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

#### Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7AWP module (see [www.acromag.com](http://www.acromag.com) for more information).

#### XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### Electrical

XMC PCIe bus interface (P15 and P16)

One 114-pin male connector

(Samtec ASP-103614-05 or equivalent).

P15 primary XMC connector

8 differential pairs (PCIe x4 standard, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.

System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin, powers volatile memory to store the bitstream encryption key.

Variable power (5V or 12V): 8 pins at 1A per pin.

P16 XMC connector

8 differential pairs (PCIe, Serial RapidIO, or Xilinx Aurora).

17 LVDS pairs or 34 SelectIO signals (differential pairs grouped per VITA 46.0 X38s).

2 global clock pairs.

Vcco pins are powered by 2.5V and support the 2.5V I/O standards.

P4 PMC rear I/O connector

64-pin female receptacle header

(AMP 120527-1 or equivalent).

64 I/O connections (30 LVDS pairs plus two global clocks).

FPGA Vcco pins powered by 2.5V and support 2.5V I/O standards. Optionally can be powered by 3.3V to support 3.3V I/O standards.

#### Environmental

Operating temperature

XMC-7AWP: -40 to 75°C cold-plate.

Storage temperature

-55 to 125°C.

Relative humidity

5 to 95% non-condensing.

Power

+3.3 Volts 2.1 A typical

+3.3 Aux Volts 17 uA typical

+12/5 Volts (VPWR) 150 mA @ +12V typical

+12 Volts 0.1 mA typical

MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-7AWP-EDK is required to configure FPGA.

#### XMC Modules

[Go to on-line ordering page >](#)

XMC-7AWP

User-configurable Artix-7 FPGA, 200k logic cells

#### Software

XMC-7AWP-EDK

Engineering Design Kit (one kit required)

PMCSW-API-VXW

VxWorks® 32-bit software support package

PCISW-API-WIN

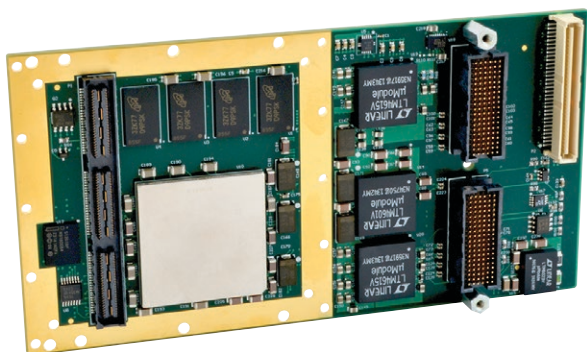
Windows® DLL software support package

PCISW-API-LNX

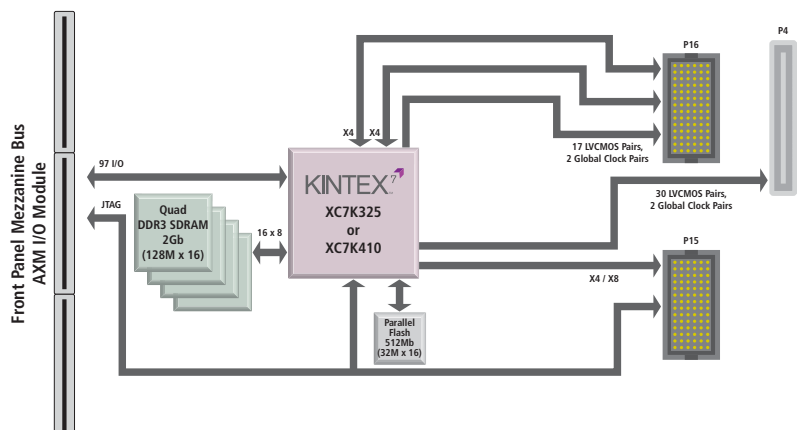
Linux® support (website download only)

ISO9001  
AS9100





KINTEX<sup>7</sup>



XMC module with PCIe interface ♦ Logic-optimized Kintex-7 FPGA ♦ I/O Extension Mezzanine Modules

### Description

Acromag's **XMC-7K** modules feature a high-performance user-configurable Xilinx® Kintex®-7 FPGA enhanced with high-speed memory and a high-throughput serial bus interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

Both front and rear I/O is supported. Front I/O processing is supported with plug-in AXM mezzanine cards. A variety of AXM I/O cards are available to add the flexibility of a wide range of analog and digital I/O to your design.

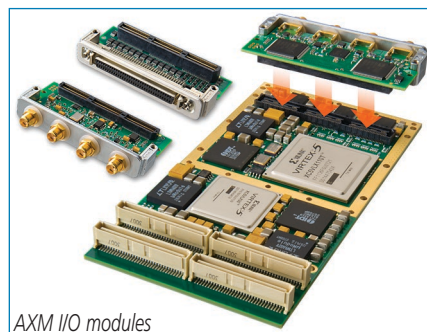
The rear I/O provides an 8-lane high-speed serial interface on the P16 XMC port for customer-installed soft cores. P16 also supports 34 SelectIO channels. The P4 port adds another 60 SelectIO and global clock lines. SelectIO signals are Kintex-7 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL)

Two versions of the Kintex-7 are available, offering a choice of an FPGA device with 325k or 410k logic cells.

With Acromag's Kintex-7 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with Vivado® or ISE® Design Suite. And with ChipScope™ Pro tools, you can rapidly debug logic and serial interfaces



AXM I/O modules

### Key Features & Benefits

- Reconfigurable Xilinx Kintex-7 FPGA with 325k or 410k logic cells
- 128M x 128-bit DDR3 SDRAM
- 32M x 16-bit parallel flash memory for MicroBlaze FPGA program code storage
- 8-lane high-speed serial interface on rear P16 connector for PCIe Gen 1/2 (standard), Serial RapidIO, 10Gb Ethernet, Xilinx Aurora
- 8-lane high-speed interfaces on rear P16 connector for customer-installed soft cores
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- DMA support provides data transfer between system memory and the on-board memory
- Support for Xilinx ChipScope™ Pro interface

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## XMC-7K AX User-Configurable Kintex-7 FPGA Modules w Plug-In I/O

### Performance Specifications

#### ■ FPGA

FPGA device

Xilinx Kintex-7 FPGA.

Model XC7K325T FPGA with 326,080 logic cells and 840 DSP48E1 slices or Model XC7K410T with 406,720 logic cells and 1540 DSP48E1 slices.

FPGA configuration

Download via JTAG or flash memory.

Example FPGA program

IP integrator block diagram provided for bus interface, front & rear I/O control, and SDRAM memory interface controller. See EDK kit.

#### ■ I/O Processing

Acromag AXM I/O Modules:

AXM modules plug into the XMC module's front mezzanine for additional I/O lines. Analog and digital I/O AXM modules are sold separately.

Rear high-speed I/O

12 high-speed serial lanes.

x8 lanes via P15 and x4 lanes via P16.

Rear user I/O

P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.

P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

#### ■ Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7K module (see [www.acromag.com](http://www.acromag.com) for more information).

#### ■ XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### ■ Electrical

XMC PCIe bus interface (P15 and P16)

One 114-pin male connector

(Samtec ASP-103614-05 or equivalent).

P15 primary XMC connector

8 differential pairs (PCIe standard, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.

System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin, powers volatile memory to store the bitstream encryption key.

Variable power (5V or 12V): 8 pins at 1A per pin.

P16 XMC connector

4 differential pairs (PCIe, Serial RapidIO, or Xilinx Aurora).

17 LVDS pairs or 34 SelectIO signals (differential pairs grouped per VITA 46.0 X38s).

2 global clock pairs.

Vcco pins are powered by 2.5V and support the 2.5V I/O standards.

P4 PMC rear I/O connector

64-pin female receptacle header

(AMP 120527-1 or equivalent).

64 I/O connections (30 LVDS pairs plus two global clocks).

Vcco pins powered by 2.5V and support the 2.5V I/O standards.

#### ■ Environmental

Operating temperature

XMC-7K325AX-LF: -40 to 45°C.

XMC-7K410AX-LF: -40 to 40°C

Storage temperature

-55 to 125°C.

Relative humidity

5 to 95% non-condensing.

Power

3.3V (±5%): 7.8W typical.

12V (±5%): 2.7W typical

3.3V AUX (±5%): 57μW

MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-7K-EDK is required to configure FPGA.

#### ■ XMC Modules

[XMC-7K325AX-LF](#)

User-configurable Kintex-7 FPGA, 325k logic cells with AXM support

[XMC-7K410AX-LF](#)

User-configurable Kintex-7 FPGA, 410k logic cells with AXM support

#### ■ Accessories

[AXM-A75](#)

16 analog inputs, 8 analog outputs, and 16 digital I/O

[AXM-A30](#)

2 analog input 100MHz 16-bit A/D channels.

[AXM-D02](#)

30 RS485 differential I/O channels.

[AXM-D03](#)

16 CMOS and 22 RS485 differential I/O channels.

[AXM-D04](#)

30 LVDS I/O channels.

AXM-??

Custom I/O configurations available, call factory.

#### ■ Software

[XMC-7KA-EDK](#)

Engineering Design Kit (one kit required)

[PMCSW-API-VXW](#)

VxWorks® 32-bit software support package

[PCISW-API-WIN](#)

Windows® DLL software support package

[PCISW-API-LNX](#)

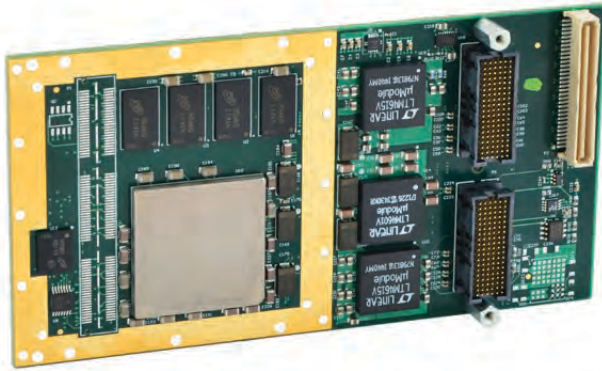
Linux™ support (website download only)

XMC-7K325AX-LF shown with optional AXM-A75

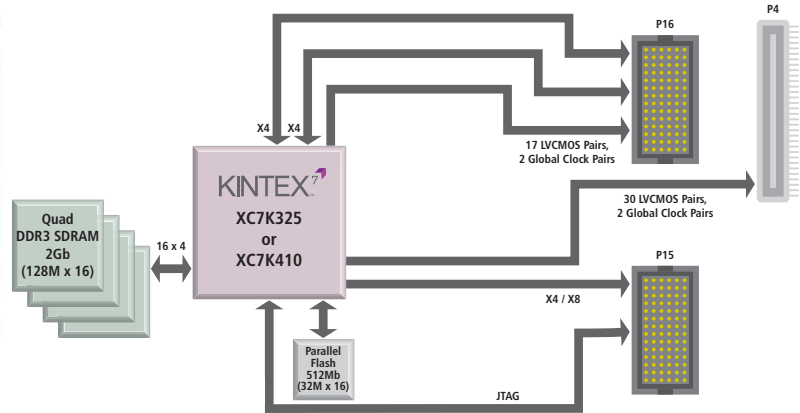


# XMC Modules

## XMC-7K CC User-Configurable Conduction-Cooled Kintex-7 FPGA Modules



KINTEX<sup>7</sup>



XMC module with PCIe interface ♦ Logic-optimized Kintex-7 FPGA ♦ Conduction-Cooled

### Description

Acromag's **XMC-7K** modules feature a high-performance user-configurable Xilinx® Kintex®-7 FPGA enhanced with high-speed memory and a high-throughput serial bus interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

The rear I/O provides an 8-lane high-speed serial interface on the P16 XMC port for customer-installed soft cores. P16 also supports 34 SelectIO channels. The P4 port adds another 60 SelectIO and global clock lines. SelectIO signals are Kintex-7 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL)

Two versions of the Kintex-7 are available, offering a choice of an FPGA device with 325k or 410k logic cells.

With Acromag's Kintex-7 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with Vivado® or ISE® Design Suite. And with ChipScope™ Pro tools, you can rapidly debug logic and serial interfaces

### Key Features & Benefits

- Reconfigurable Xilinx Kintex-7 FPGA with 325k or 410k logic cells
- 128M x 64-bit DDR3 SDRAM
- 32M x 16-bit parallel flash memory for MicroBlaze FPGA program code storage
- 8-lane high-speed serial interface on rear P15 connector for PCIe Gen 1/2 (standard), Serial RapidIO, 10Gb Ethernet, Xilinx Aurora
- 8-lane high-speed interfaces on rear P16 connector for customer-installed soft cores
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- DMA support provides data transfer between system memory and the on-board memory
- Support for Xilinx ChipScope™ Pro interface
- Extended temperature conduction-cooled

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## XMC-7K CC User-Configurable Conduction-Cooled Kintex-7 FPGA Modules

### Performance Specifications

#### FPGA

FPGA device

Xilinx Kintex-7 FPGA.

Model XC7K325T FPGA with 326,080 logic cells and 840 DSP48E1 slices or Model XC7K410T with 406,720 logic cells and 1540 DSP48E1 slices.

FPGA configuration

Download via JTAG or flash memory.

Example FPGA program

IP integrator block diagram provided for bus interface, front & rear I/O control, and SDRAM memory interface controller. See EDK kit.

#### I/O Processing

Rear high-speed I/O

16 high-speed serial lanes.

x8 lanes via P15 and x8 lanes via P16.

Rear user I/O

P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.

P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

#### Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7K module (see [www.acromag.com](http://www.acromag.com) for more information).

#### XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### Electrical

XMC PCIe bus interface (P15 and P16)

One 114-pin male connector (Samtec ASP-103614-05 or equivalent).

P15 primary XMC connector

8 differential pairs (PCIe standard, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.

System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin, powers volatile memory to store the bitstream encryption key.

Variable power (5V or 12V): 8 pins at 1A per pin.

P16 XMC connector

4 differential pairs (PCIe, Serial RapidIO, or Xilinx Aurora).

17 LVDS pairs or 34 SelectIO signals (differential pairs grouped per VITA 46.0 X38s).

2 global clock pairs.

Vcco pins are powered by 2.5V and support the 2.5V I/O standards.

P4 PMC rear I/O connector

64-pin female receptacle header (AMP 120527-1 or equivalent).

64 I/O connections (30 LVDS pairs plus two global clocks).

Vcco pins powered by 2.5V and support the 2.5V I/O standards.

#### Environmental

Operating temperature

XMC-7K325AX-LF: Conduction-cooled, -40 to 70°C.

XMC-7K410AX-LF: Conduction-cooled, -40 to 70°C

Storage temperature

-55 to 125°C.

Relative humidity

5 to 95% non-condensing.

Power

3.3V (±5%): 7.8W typical.

12V (±5%): 2.7W typical.

3.3V AUX (±5%): 57µW

MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-7K-EDK is required to configure FPGA.

#### XMC Modules

[XMC-7K325CC-LF](#)

User-configurable Kintex-7 FPGA, 325k logic cells, conduction-cooled

[XMC-7K410CC-LF](#)

User-configurable Kintex-7 FPGA, 410k logic cells, conduction-cooled

#### Software

[XMC-7KA-EDK](#)

Engineering Design Kit (one kit required)

[PMCSW-API-VXW](#)

VxWorks® 32-bit software support package

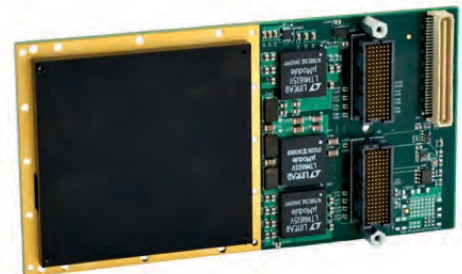
[PCISW-API-WIN](#)

Windows® DLL software support package

[PCISW-API-LNX](#)

Linux™ support (website download only)

XMC-7K325CC-LF shown with heatsink



ISO9001  
AS9100

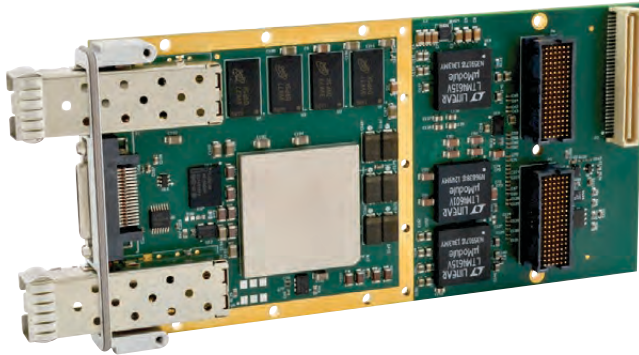


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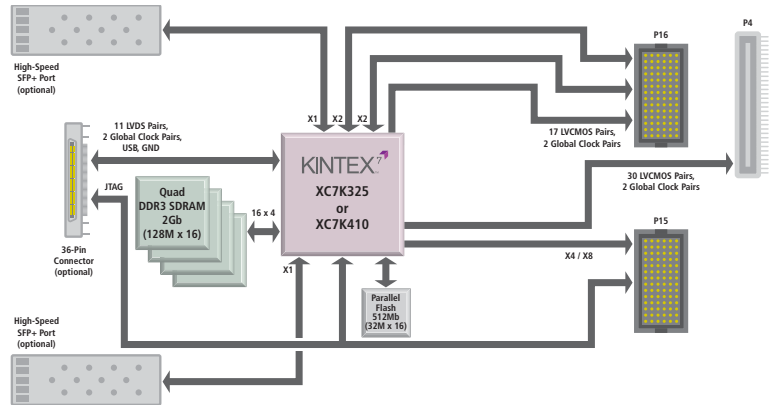
Tel 248-295-0310 ■ [solutions@acromag.com](mailto:solutions@acromag.com) ■ [www.acromag.com](http://www.acromag.com) ■ 30765 Wixom Rd, Wixom, MI 48393 USA

# XMC Modules

## XMC-7K F User-Configurable Kintex-7 FPGA Modules with Dual SFP+ Ports



KINTEX<sup>7</sup>



### XMC module with PCIe and SFP+/Aurora interface ♦ Logic-optimized Kintex-7 FPGA ♦ 10-Gigabit Ethernet

#### Description

Acromag's [XMC-7K](#) modules feature a high-performance user-configurable Xilinx® Kintex®-7 FPGA enhanced with high-speed memory and a high-throughput serial interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

Two versions of this module are available, offering a choice of an FPGA device with 325k or 410k logic cells.

Front I/O adds dual SFP+ ports and a VHDCR connector. The two SFP+ ports each provide a copper or fibre interface of up to 10.3125Gbps. They also support a Gigabit Ethernet interface. The VHDCR connector interfaces JTAG, USB, and 22 SelectIO.

The rear I/O provides an 4-lane high-speed serial interface on the P16 XMC port for customer-installed soft cores. P16 also supports 34 SelectIO channels. The P4 port adds another 60 SelectIO and global clock lines. SelectIO signals are Kintex-7 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL).

With Acromag's Kintex-7 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with Vivado® or ISE® Design Suite. And with ChipScope™ Pro tools, you can rapidly debug logic and serial interfaces

#### Key Features & Benefits

- Reconfigurable Xilinx Kintex-7 FPGA with 325k or 410k logic cells
- 128M x 64-bit DDR3 SDRAM
- 32M x 16-bit parallel flash memory for MicroBlaze FPGA program code storage
- 8-lane high-speed serial interface on rear P15 connector for PCIe Gen 1/2 (standard), Serial RapidIO, 10Gb Ethernet, Xilinx Aurora
- 4-lane high-speed interfaces on rear P16 connector for customer-installed soft cores
- Dual SFP+ ports for Fibre Channel or 10GbE
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- 22 SelectIO, 2 global clock pairs, JTAG, USB, and ground signals via front 36-pin connector
- DMA support provides data transfer between system memory and the on-board memory
- Support for Xilinx ChipScope™ Pro interface

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## XMC-7K F User-Configurable Kintex-7 FPGA Modules w Dual SFP+ Ports

### Performance Specifications

#### FPGA

FPGA device

Xilinx Kintex-7 FPGA.

Model XC7K325T FPGA with 326,080 logic cells and 840 DSP48E1 slices or Model XC7K410T with 406,720 logic cells and 1540 DSP48E1 slices.

FPGA configuration

Download via JTAG or flash memory.

Example FPGA program

IP integrator block diagram provided for bus interface, front & rear I/O control, and SDRAM memory interface controller. See EDK kit.

#### I/O Processing

Front high-speed I/O

Two x1 lanes via SFP+ connectors for Gigabit Ethernet and Fibre Channel interface

Front user I/O

36-pin connector provides JTAG connection, USB signals, 2 global differential clock pairs, 11 LVDS signal pairs, and 2 ground signals.

Rear high-speed I/O

12 high-speed serial lanes.

x8 lanes via P15 and x4 lanes via P16.

Rear user I/O

P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.

P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

#### Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7K module (see [www.acromag.com](http://www.acromag.com) for more information).

#### XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### Electrical

XMC PCIe bus interface (P15 and P16)

One 114-pin male connector (Samtec ASP-103614-05 or equivalent).

P15 primary XMC connector

8 differential pairs (PCIe standard, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.

System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin for system management.

Variable power (5V or 12V): 8 pins at 1A per pin.

P16 XMC connector

4 differential pairs (PCIe, Serial RapidIO, or Xilinx Aurora).

17 LVDS pairs or 34 SelectIO signals (differential pairs grouped per VITA 46.0 X38s).

2 global clock pairs.

Vcco pins are powered by 2.5V and support the 2.5V I/O standards.

P4 PMC rear I/O connector

64-pin female receptacle header

(AMP 120527-1 or equivalent).

64 I/O connections (30 LVDS pairs plus two global clocks).

Vcco pins powered by 2.5V and support the 2.5V I/O standards.

VHDCR connector

36-position connector (Samtec VHDCR-36-01-M-RA) mates with industry-standard VHDCI cable assemblies.

SFP+ host connector

SFP transceiver signals route directly to Kintex-7 FPGA. 10.3125Gb/s maximum data rate.

SFP+ copper (Gigabit Ethernet) or fibre optic modules available from Acromag.

#### Environmental

Operating temperature

XMC-7K325F-LF: -40 to 55°C.

XMC-7K410F-LF: -40 to 55°C.

Storage temperature

-55 to 125°C.

Relative humidity

5 to 95% non-condensing.

Power

3.3V (±5%): 7.8W typical.

12V (±5%): 2.7W typical.

3.3V AUX (±5%): 57μW typical.

MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-7K-EDK is required to configure FPGA.

#### XMC Modules

[XMC-7K325F-LF](#)

User-configurable Kintex-7 FPGA, 325k logic cells plus SFP front I/O

[XMC-7K410F-LF](#)

User-configurable Kintex-7 FPGA, 410k logic cells plus SFP front I/O

#### Accessories

[5025-921](#)

Cable, VHDCI 36-pin to SCSI-2, 6 feet long.

[5028-449](#)

Cable, copper twin-ax, SFP to SFP, 1 meter long.

[5028-455](#)

Transceiver, 10/100/1000BASE-T copper SFP, up to 1.25Gb/s bi-directional data links.

[5028-452](#)

Transceiver, short-wavelength SFP, up to 2.125Gb/s bi-directional data links.

#### Software

[XMC-7KA-EDK](#)

Engineering Design Kit (one kit required)

[PMCSW-API-VXW](#)

VxWorks® 32-bit software support package

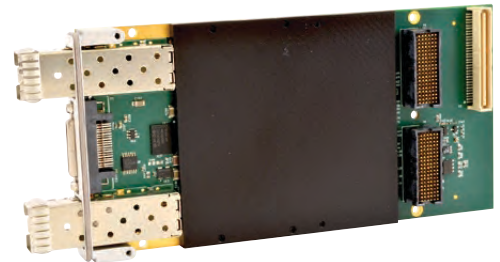
[PCISW-API-WIN](#)

Windows® DLL software support package

[PCISW-API-LNX](#)

Linux® support (website download only)

XMC-7K325F-LF shown with heatsink



ISO9001  
AS9100



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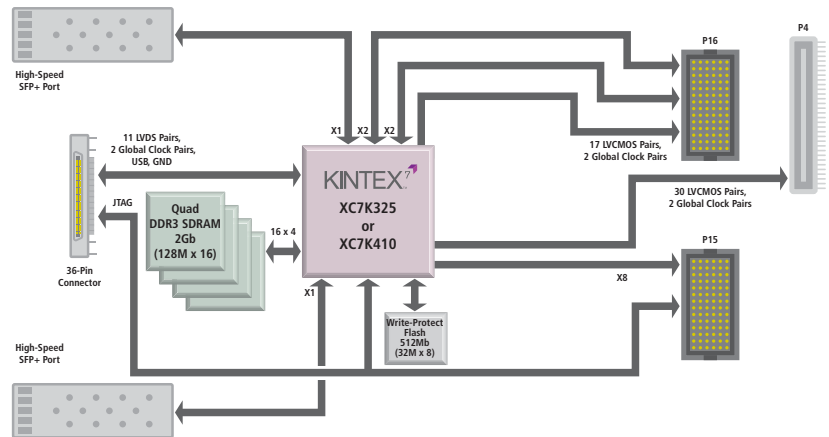
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# XMC Modules

## XMC-7KWP User-Configurable Kintex-7 FPGA Modules with Dual SFP+ Ports



KINTEX<sup>7</sup>



XMC module ♦ Kintex-7 FPGA ♦ 10-Gigabit Ethernet ♦ Write-protected flash

### Description

Acromag's XMC-7KWP modules feature a high-performance user-configurable Xilinx® Kintex®-7 FPGA enhanced with high-speed memory and a high-throughput serial interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing. For security, the FPGA's configuration flash is write-protected.

Two versions of this module are available, offering a choice of an FPGA device with 325k or 410k logic cells.

Front I/O adds dual SFP+ ports and a VHDCR connector. The two SFP+ ports each provide a copper or fibre interface of up to 10.3125Gbps. They also support a Gigabit Ethernet interface. The VHDCR connector interfaces JTAG, USB, and 22 SelectIO.

The rear I/O provides 4-lane high-speed serial interface on the P16 XMC port for customer-installed soft cores. P16 also supports 34 SelectIO channels. The P4 port adds another 60 SelectIO and global clock lines. SelectIO signals are Kintex-7 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL).

With Acromag's Kintex-7 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with Vivado® or ISE® Design Suite. And with ChipScope™ Pro tools, you can rapidly debug logic and serial interfaces.

### Key Features & Benefits

- Reconfigurable Xilinx Kintex-7 FPGA with 325k or 410k logic cells
- 128M x 64-bit DDR3 SDRAM
- 32M x 16-bit parallel flash memory for MicroBlaze FPGA program code storage
- FPGA bitstream storage flash write-protected unless access jumper installed
- 8-lane high-speed serial interface on rear P15 connector for PCIe Gen 1/2 (standard), Serial RapidIO, 10Gb Ethernet, Xilinx Aurora
- 4-lane high-speed interfaces on rear P16 connector for customer-installed soft cores
- Dual SFP+ ports for Fibre Channel or 10GbE
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- 22 SelectIO, 2 global clock pairs, JTAG, USB, and ground signals via front 36-pin connector
- DMA support provides data transfer between system memory and the on-board memory
- Support for Xilinx ChipScope™ Pro interface

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## XMC-7KWP User-Configurable Kintex-7 FPGA Modules w Dual SFP+ Ports

### Performance Specifications

#### FPGA

FPGA device

Xilinx Kintex-7 FPGA.

Model XC7K325T FPGA with 326,080 logic cells and 840 DSP48E1 slices or Model XC7K410T with 406,720 logic cells and 1540 DSP48E1 slices.

#### FPGA configuration

Download via JTAG or flash memory. Installation of 2mm pitch jumper shunt required for writing to flash memory.

#### Example FPGA program

IP integrator block diagram provided for bus interface, front & rear I/O control, and SDRAM memory interface controller. See EDK Kit.

#### I/O Processing

##### Front high-speed I/O

Two x1 lanes via SFP+ connectors for Gigabit Ethernet and Fibre Channel interface.

##### Front user I/O

36-pin connector provides JTAG connection, USB signals, 2 global differential clock pairs, 11 LVDS signal pairs, and 2 ground signals.

##### Rear high-speed I/O

12 high-speed serial lanes.

x8 lanes via P15 and x4 lanes via P16.

##### Rear user I/O

P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.

P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

#### Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7K module (see [www.acromag.com](http://www.acromag.com) for more information).

#### XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### Electrical

XMC PCIe bus interface (P15 and P16)

One 114-pin male connector

(Samtec ASP-103614-05 or equivalent).

##### P15 primary XMC connector

8 differential pairs (PCIe standard, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.

System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin for system management.

Variable power (5V or 12V): 8 pins at 1A per pin.

##### P16 XMC connector

4 differential pairs (PCIe, Serial RapidIO, or Xilinx Aurora).

17 LVDS pairs or 34 SelectIO signals (differential pairs grouped per VITA 46.0 X38s).

2 global clock pairs.

Vcco pins are powered by 2.5V and support the 2.5V I/O standards.

##### P4 PMC rear I/O connector

64-pin female receptacle header

(AMP 120527-1 or equivalent).

64 I/O connections (30 LVDS pairs plus two global clocks).

Vcco pins powered by 2.5V and support the 2.5V I/O standards.

##### VHDCR connector

36-position connector (Samtec VHDCR-36-01-M-RA) mates with industry-standard VHDCI cable assemblies.

##### SFP+ host connector

SFP transceiver signals route directly to Kintex-7 FPGA.

10.3125Gb/s maximum data rate.

SFP+ copper (Gigabit Ethernet) or fibre optic modules available from Acromag.

##### JTAG voltage level

2.5V default.

Resistor stuff option for 3.3V (consult factory).

#### Environmental

##### Operating temperature

XMC-7KWP-325F: -40 to 55°C.

XMC-7KWP-410F: -40 to 55°C.

##### Storage temperature

-55 to 125°C.

##### Relative humidity

5 to 95% non-condensing.

##### Power

3.3V (±5%): 7.8W typical.

12V (±5%): 2.7W typical.

3.3V AUX (±5%): 57µW typical.

##### MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-7KA-EDK is required to configure FPGA.

#### XMC Modules

[Go to on-line ordering page >](#)

##### XMC-7KWP-325F

User-configurable Kintex-7 FPGA, 325k logic cells plus SFP front I/O, write protected flash

##### XMC-7KWP-410F

User-configurable Kintex-7 FPGA, 410k logic cells plus SFP front I/O, write protected flash

#### Accessories

##### 5025-921

Cable, VHDCI 36-pin to SCSI-2, 6 feet long.

##### 5028-449

Cable, copper twin-ax, SFP to SFP, 1 meter long.

##### 5028-455

Transceiver, 10/100/1000BASE-T copper SFP, up to 1.25Gb/s bi-directional data links.

##### 5028-452

Transceiver, short-wavelength SFP, up to 2.125Gb/s bi-directional data links.

#### Software

##### XMC-7KA-EDK

Engineering Design Kit (one kit required)

##### PMCSW-API-VXW

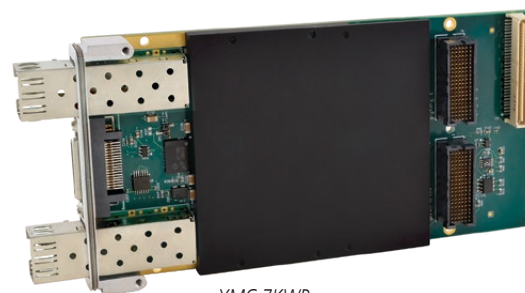
VxWorks® 32-bit software support package

##### PCISW-API-WIN

Windows® DLL software support package

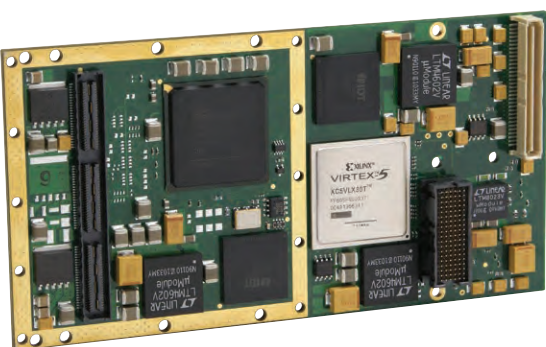
##### PCISW-API-LNX

Linux® support (website download only)

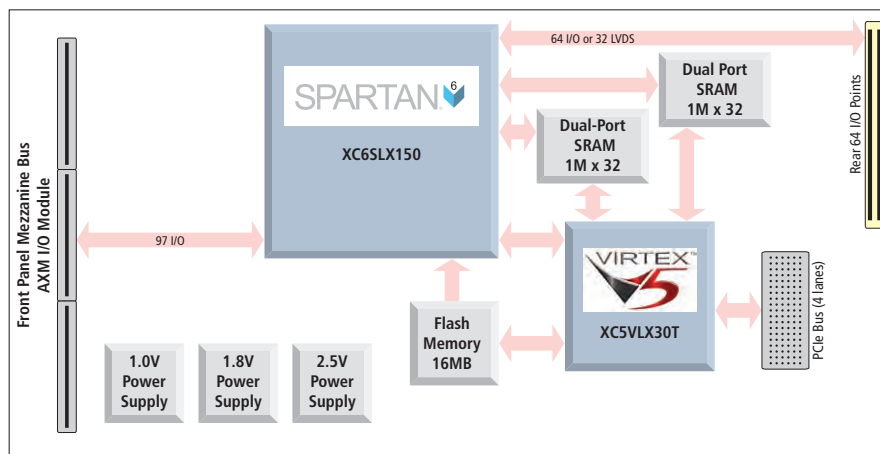


XMC-7KWP

## XMC-SLX User-Configurable Spartan-6 FPGA Modules with Plug-In I/O



SPARTAN<sup>6</sup>



### XMC module with PCIe interface ♦ Logic-optimized Spartan-6 FPGA ♦ I/O extension mezzanine modules

#### Description

Acromag's cost-effective [XMC-SLX](#) modules feature a user-configurable Xilinx® Spartan®-6 FPGA enhanced with high-speed memory and a high-throughput PCIe interface. Field I/O interfaces to the FPGA via the rear J4/P4 connector and/or with optional front mezzanine plug-in I/O modules. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

Large, high-speed memory banks enable efficient data handling. The dual-port SRAM facilitates high-speed DMA transfers to the bus or CPU. A high-bandwidth PCIe interface ensures fast data throughput.

64 I/O lines are accessible through the rear (J4) connector. Additional I/O processing is supported on a separate mezzanine card that plugs into the FPGA base board. A variety of these external AXM I/O cards are available to interface your analog and digital I/O signals.

Take advantage of the conduction-cooled design for use in hostile environments. Conduction efficiently dissipates heat if there is inadequate cooling air flow. Optional extended temperature models operate reliably from -40 to 85°C.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board VHDL debugging.



Plug in an AXM analog or digital I/O module for additional I/O signal processing capabilities.



VPX air-cooled and REDI versions are available

#### Key Features & Benefits

- Reconfigurable Xilinx Spartan-6 FPGA with 147,433 logic cells
- PCIe bus 4-lane Gen 1 interface
- 256k x 64-bit dual-ported SRAM provides direct links from the PCIe bus and to the FPGA (optional 1M x 64-bit)
- Supports both front and rear I/O connections
- 64 I/O or 32 LVDS lines direct to FPGA via rear (J4) connector
- Plug-in I/O extension modules are available for the front mezzanine
- FPGA code loads from the PCIe bus or from flash memory
- Other memory options available (call factory)
- Supports dual DMA channel data transfer to the CPU/bus
- Support for Xilinx ChipScope™ Pro interface
- Designed for conduction-cooled host card or -40 to 85°C operation in air-cooled systems

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## XMC-SLX User-Configurable Spartan-6 FPGA Modules with Plug-In I/O

### Performance Specifications

#### FPGA

##### FPGA Device

Xilinx Spartan-6 FPGA.

Model XC6SLX150-3FG676 FPGA with 147,433 logic cells and 180 DSP48A1 slices.

##### FPGA configuration

Download via PCIe bus or flash memory.

##### Example FPGA program

VHDL provided for bus interface, front & rear I/O control, SRAM read/write interface logic, and SDRAM memory interface controller. See EDK kit.

#### I/O Processing

Acromag AXM I/O modules:

AXM modules plug into the XMC module's front mezzanine for additional I/O lines. Analog and digital I/O AXM modules are sold separately.

##### Rear I/O

64 I/O (32 LVDS) lines supported with a direct connection between the FPGA and the rear I/O connector (J4).

#### Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-SLX module (see [www.acromag.com](http://www.acromag.com) for more information).

#### XMC Compliance

Conforms to PCI Express 1.1a electrical and protocol standards. 2.5Gbps data rate per lane per direction.

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### Environmental

##### Operating temperature

-0 to 70°C or -40 to 85°C (E versions).

##### Storage temperature

-55 to 125°C.

##### Relative humidity

5 to 95% non-condensing.

##### Power

3.3V (±5%): 700mA typical, 840mA maximum.

12V (±5%): 640mA typical, 804mA maximum.

##### MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-SLX-EDK is required to configure FPGA.

#### XMC Modules

##### XMC-SLX150

User-configurable Spartan-6 FPGA, 150k logic cells, 256 x 64-bit dual-port SRAM

##### XMC-SLX150E

Same as XMC-SLX150 with extended temp. range

##### XMC-SLX150-1M

User-configurable Spartan-6 FPGA, 150k logic cells, 1M x 64-bit dual-port SRAM

##### XMC-SLX150E-1M

Same as XMC-SLX150-1M with extended temp. range

#### AXM Plug-In I/O Extension Modules

For more information, see [www.acromag.com](http://www.acromag.com).

##### AXM-A30

2 analog input 100MHz 16-bit A/D channels

##### AXM-D02

30 RS485 differential I/O channels

##### AXM-D03

16 CMOS and 22 RS485 differential I/O channels

##### AXM-D04

30 LVDS I/O channels

##### AXM-??

Custom I/O configurations available, call factory.

#### Software

For more information, see [www.acromag.com](http://www.acromag.com).

##### XMC-SLX-EDK

Engineering Design Kit (one kit required)

##### PMCSW-API-VXW

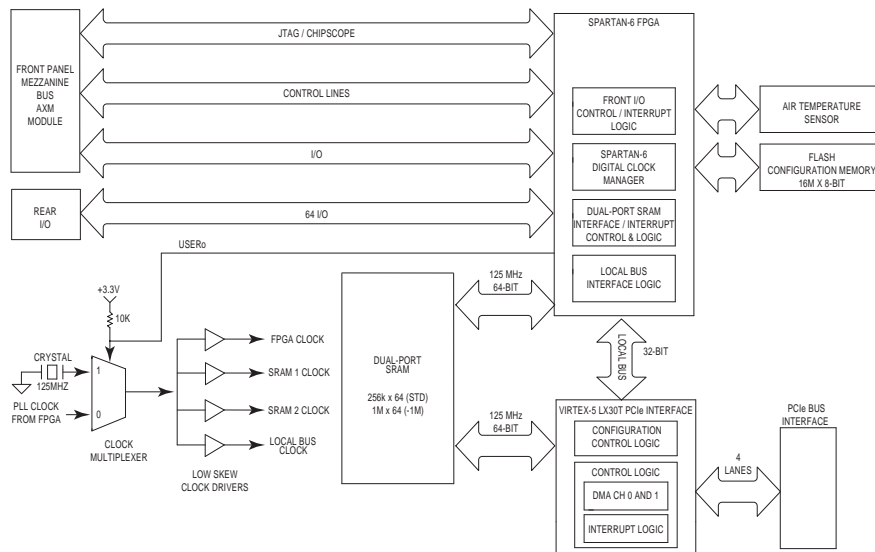
VxWorks® software support package

##### PCISW-API-WIN

Windows® DLL software support package

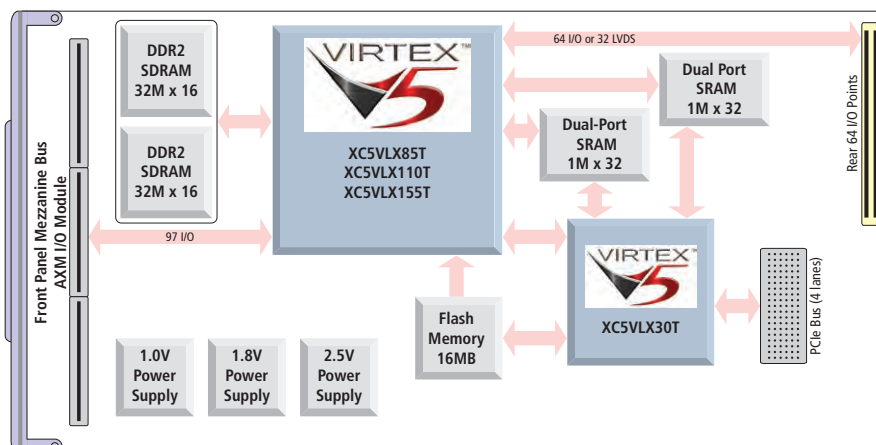
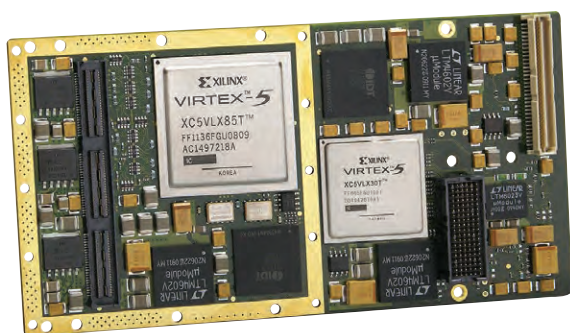
##### PCISW-API-LNX

Linux® support (website download only)



# XMC Modules

## XMC-VLX User-Configurable Virtex-5 FPGA Modules with Plug-In I/O



### XMC module with PCIe interface ♦ Logic-optimized Virtex-5 FPGA ♦ I/O extension mezzanine modules

#### Description

##### Models

XMC-VLX85: 85k logic cells  
XMC-VLX110: 110k logic cells  
XMC-VLX155: 155k logic cells

Acromag's **XMC-VLX** mezzanine modules feature a configurable Xilinx® Virtex™-5 FPGA enhanced with multiple high-speed memory buffers and a high-throughput PCIe interface. Field I/O interfaces to the FPGA via the rear J4/P4 connector and/or with optional front mezzanine plug-in I/O modules. The result is a powerful and flexible I/O processor module that is capable of executing your custom instruction sets and algorithms.

Three models provide a choice of logic-optimized FPGAs to match your performance requirements. Although there is no limit to the uses for these boards, several applications are ideal. Typical uses include hardware simulation, military servers, communications, in-circuit diagnostics, signal intelligence, and image processing.

64 I/O lines are accessible through the rear (J4) connector. Additional I/O processing is supported on a separate mezzanine card that plugs into the FPGA base board. A variety of these external I/O cards are available to interface for your analog and digital I/O signals.

Large, high-speed memory banks provide efficient data handling. Generous DDR2 SDRAM buffers store captured data prior to FPGA processing. Afterward, data is moved to dual-port SRAM for high-speed DMA transfer to the bus or CPU. Our high-bandwidth PCIe interface ensures fast data throughput.

Take advantage of the conduction-cooled design for use in hostile environments. Conduction efficiently dissipates heat if there is inadequate cooling air flow. Optional extended temperature models operate reliably from -40 to 85°C.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board VHDL debugging.



Plug in an AXM analog or digital I/O module for additional I/O signal processing capabilities.

#### Key Features & Benefits

- Reconfigurable Xilinx Virtex-5 FPGA
- PCIe bus 4-lane Gen 1 interface
- Supports both front and rear I/O connections
- 64 I/O or 32 LVDS lines direct to FPGA via rear (J4) connector
- Plug-in I/O extension modules are available for the front mezzanine
- FPGA code loads from the PCIe bus or from flash memory
- 1M x 64-bit dual-ported SRAM provides direct links from the PCIe bus and to the FPGA
- 32M x 32-bit DDR2 SDRAM is directly accessed through the FPGA
- Other memory options available (call factory)
- Supports dual DMA channel data transfer to the CPU/bus
- Support for Xilinx ChipScope™ Pro interface
- Designed for conduction-cooled host card or -40 to 85°C operation in air-cooled systems



Tel 248-295-0310 ■ solutions@acromag.com ■ www.acromag.com ■ 30765 Wixom Rd, Wixom, MI 48393 USA

## XMC-VLX User-Configurable Virtex-5 FPGA Modules with Plug-In I/O

### Performance Specifications

#### ■ FPGA

##### FPGA Device

Xilinx Virtex-5 FPGA.

##### Model XMC-VLX85:

XC5VLX85T-1FF1136 FPGA with 82,944 logic cells and 48 DSP48E slices.

##### Model XMC-LX110:

XC5VLX110T-1FF1136 FPGA with 110,592 logic cells and 64 DSP48E slices.

##### Model XMC-LX155:

XC5VLX155T-1FF1136 FPGA with 155,648 logic cells and 128 DSP48E slices.

##### FPGA configuration

Download via PCIe bus or flash memory.

##### Example FPGA program

VHDL provided for bus interface, front & rear I/O control, SRAM read/write interface logic, and SDRAM memory interface controller. See EDK kit.

#### ■ I/O Processing

##### Acromag AXM I/O modules:

AXM modules plug into the XMC module's front mezzanine for additional I/O lines. Analog and digital I/O AXM modules are sold separately.

##### Rear I/O

64 I/O (32 LVDS) lines supported with a direct connection between the FPGA and the rear I/O connector (J4).

#### ■ Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-VLX module (see [www.acromag.com](http://www.acromag.com) for more information).

#### ■ XMC Compliance

Conforms to PCI Express 1.1a electrical and protocol standards. 2.5Gbps data rate per lane per direction.

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### ■ Environmental

##### Operating temperature

-0 to 70°C or -40 to 85°C (E versions).

##### Storage temperature

-55 to 125°C.

##### Relative humidity

5 to 95% non-condensing.

##### Power

3.3V (±5%): 700mA typical, 840mA maximum

+12V (±5%): 820mA typical, 984mA maximum

##### MTBF

Contact the factory.

### Ordering Information

#### ■ XMC Modules

##### [XMC-VLX85](#)

User-configurable Virtex-5 FPGA, 85k logic cells

##### [XMC-VLX85E](#)

Same as XMC-VLX85 with extended temp. range

##### [XMC-VLX110](#)

User-configurable Virtex-5 FPGA, 110k logic cells

##### [XMC-VLX110E](#)

Same as XMC-VLX110 with extended temp. range

##### [XMC-VLX155](#)

User-configurable Virtex-5 FPGA, 155k logic cells

##### [XMC-VLX155E](#)

Same as XMC-VLX155 with extended temp. range

##### [XMC-VLX-EDK](#)

Engineering Design Kit (one kit required)

#### ■ AXM Plug-In I/O Extension Modules

For more information, see [www.acromag.com](http://www.acromag.com).

##### [AXM-A30](#)

2 analog input 100MHz 16-bit A/D channels

##### [AXM-D02](#)

30 RS485 differential I/O channels

##### [AXM-D03](#)

16 CMOS and 22 RS485 differential I/O channels

##### [AXM-D04](#)

30 LVDS I/O channels

##### [AXM-??](#)

Custom I/O configurations available, call factory.

#### ■ Software

For more information, see [www.acromag.com](http://www.acromag.com).

##### [PMCSW-API-VXW](#)

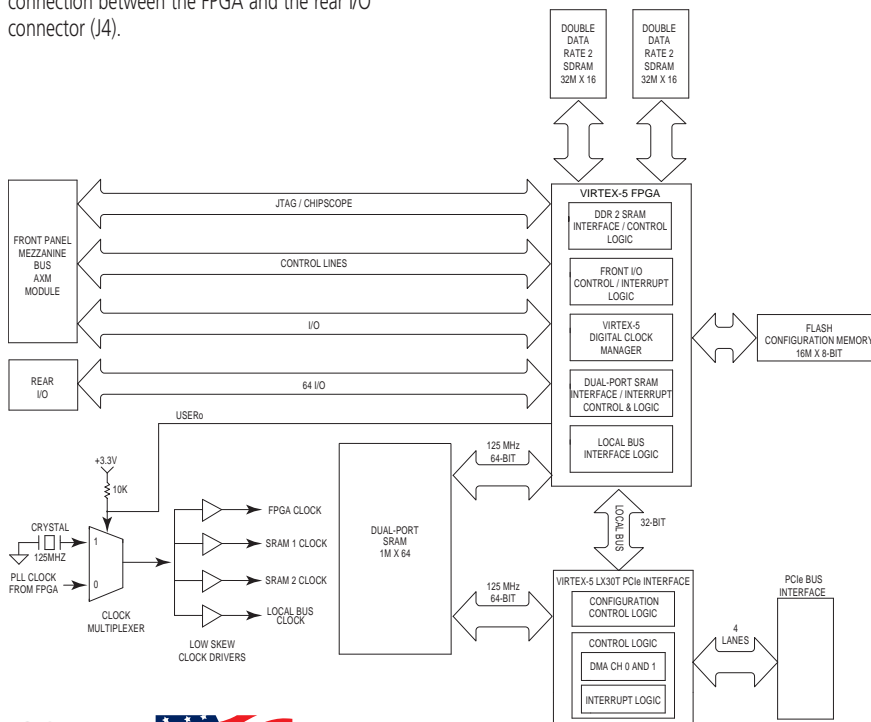
VxWorks® software support package

##### [PCISW-API-WIN](#)

Windows® DLL software support package

##### [PCISW-API-LNX](#)

Linux™ support (website download only)



ISO9001  
AS9100



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## PMC-LX40/LX60 User-configurable Virtex-4 FPGA Modules with plug-in I/O

- PMC-LX40: 41,472 logic cells (XC4VLX40)
- PMC-LX60: 59,904 logic cells (XC4VLX60)

### Description

Acromag's PMC-LX boards use a high-performance Xilinx® Virtex-4™ FPGA, but maintain a relatively low price point. They are optimized for high-performance logic, featuring a high logic-to-feature ratio and a high I/O-to-feature ratio. Two modules let you select an FPGA to match your logic requirements.

Although there is no limit to the uses for Acromag's FPGA boards, several applications are ideal for this new technology. Typical uses include hardware simulation, communication processing, in-circuit diagnostics, military servers, and telecommunication.

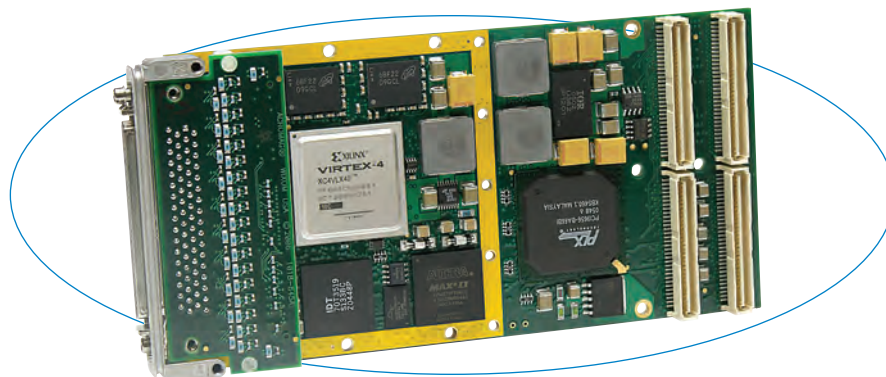
I/O processing is handled on a separate mezzanine card that plugs into the FPGA base board. A variety of these external I/O cards offer an interface for your analog and digital I/O signals. See the AXM I/O Card for more details. Additionally, 64 I/O lines are supported via the rear (J4) connector.

Plenty of DRAM memory is available for receipt and transfer of high-speed data from the I/O data ports on the front and rear of the board. Dual Ported SRAM memory is supplied for storage of data to be passed, via DMA transfer, to the PCI bus. One of the dual ports is attached to the FPGA and the other to the local bus.

The PCI bus interface is handled by a PLX® PCI 9656 device which provides 64-bit 66MHz bus mastering with dual-channel DMA support.

Take advantage of the optional conduction cooling for use in hostile environments. Conduction cooling provides efficient heat dissipation in environments where there is inadequate cooling air flow.

Acromag provides software utilities and examples to simplify your programming and get you started quickly. A JTAG interface enables on-board VHDL simulation.



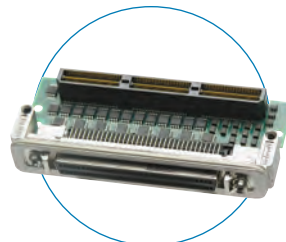
Download your own logic programs into the user-configured FPGA to quickly create a custom I/O module. Shown with optional plug-in I/O module.

### Features

- Customizable FPGA (Xilinx Virtex-4 XC4VLX40/60) with up to 60K logic cells and 64 XtremeDSP™ slices
- Supports both front and rear I/O
- Plug-in I/O modules are available for front mezzanine
- 64 I/O lines supported with direct connection to FPGA via rear (J4) connector
- FPGA code loads from PCI bus or flash memory
- 256K x 36-bit dual-ported SRAM
- 32Mb x 32-bit DDR DRAM
- Supports dual DMA channel data transfer to CPU
- Supports both 5V and 3.3V signalling
- Conduction cooled or 0 to 70°C operating range



The base board is ready for conduction-cooled applications.



Plug-in AXM modules sold separately for analog and digital I/O.

### Specifications

#### FPGA

FPGA: Xilinx Virtex-4 FPGA

PMC-LX40: XC4VLX40 FPGA with 41,472 logic cells and 64 DSP slices

PMC-LX60: XC4VLX60 FPGA with 59,904 logic cells and 64 DSP slices

FPGA configuration: Downloadable via PCI bus or from flash memory.

Example FPGA program: VHDL provided implements interface to PCI bus IC, interface to dual port SRAM, PLL control, ADC, and DAC control. Program requires user proficiency with Xilinx software tools. See Engineering Design Kit.

#### I/O Processing

AXM modules: for front mezzanine:

Acromag AXM modules attach to the board to provide I/O. A variety of modules are available and are sold separately.

Rear I/O:

32 LVDS I/O lines supported with a direct connection between the FPGA and the rear I/O connector (J4).

#### Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a PMC-LX module. (see Design Kit for details)

#### PMC Compliance

Conforms to PCI Local Bus Specification, Revision 2.2 and CMC/PMC Specification, P1386.1.

Electrical/Mechanical Interface: Single-Width Module.

PCI bus clock frequency: 66MHz.

64-bit PCI Master: Implemented by PLX PCI 9656 device.

Signaling: 5V and 3.3V compliant.

Interrupts (INTA#): Interrupt A is used to request an interrupt.

#### Environmental

Operating temperature: 0 to 70°C

Storage temperature: -55 to 105°C.

Relative humidity: 5 to 95% non-condensing.

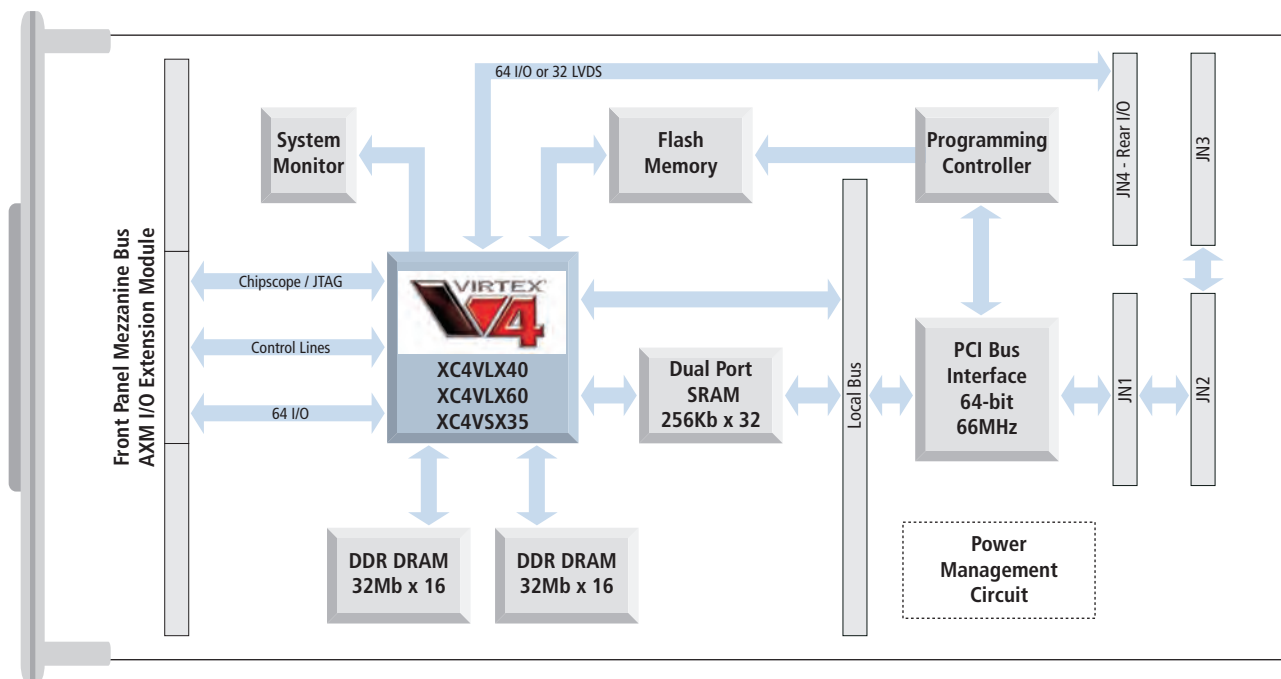
Power: Consult factory. Operates from 3.3V supply.

MTBF: Hours at 25°C MIL-HDBK-217F, Notice 2

PMC-LX40 773,246; PMC-LX60 870,489

All trademarks are the property of their respective owners.





## Ordering Information

### PMC Modules

#### PMC-LX40

User-configurable Virtex-4 FPGA with 41,472 logic cells

#### PMC-LX60

User-configurable Virtex-4 FPGA with 59,904 logic cells

#### PMC-LX-EDK

Engineering Design Kit (one kit required)

**Software** (see [software documentation](#) for details)

#### PMCSW-API-VXW

VxWorks® software support package

#### PCISW-API-WIN

Windows® DLL software support

#### PCISW-API-LNX

Linux™ support (website download only)

### AXM Plug-In I/O Modules

For more information, see [AXM data sheet](#).

#### AXM-A30

2 16-bit 100MHz A/D channels

#### AXM-D02

30 RS485 differential I/O channels

#### AXM-D03

16 CMOS and 22 RS485 differential I/O channels

#### AXM-D04

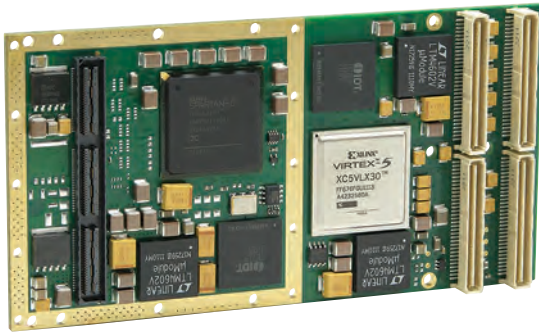
30 LVDS I/O channels

#### AXM-??

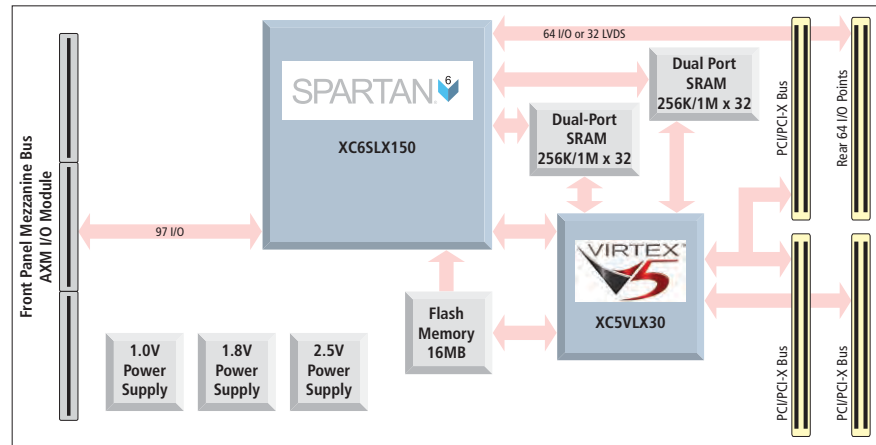
Custom I/O configurations available, call factory.

## PMC-SLX User-Configurable Spartan-6 FPGA Modules with Plug-In I/O

24 HOUR STOCK ITEM  
2 YEAR WARRANTY



SPARTAN-6



### PMC module with PCI-X interface ♦ Logic-optimized Spartan-6 FPGA ♦ I/O extension mezzanine modules

#### Description

Acromag's cost-effective PMC-SLX modules feature a user-configurable Xilinx® Spartan®-6 FPGA enhanced with high-speed memory and a high-throughput PCI-X interface. Field I/O interfaces to the FPGA via the rear J4/P4 connector and/or with optional front mezzanine plug-in I/O modules. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

Large, high-speed memory banks enable efficient data handling. The dual-port SRAM facilitates high-speed DMA transfers to the bus or CPU. A high-bandwidth PCI-X interface ensures fast data throughput.

64 I/O lines are accessible through the rear (J4) connector. Additional I/O processing is supported on a separate mezzanine card that plugs into the FPGA base board. A variety of these external AXM I/O cards are available to interface your analog and digital I/O signals.

Take advantage of the conduction-cooled design for use in hostile environments. Conduction efficiently dissipates heat if there is inadequate cooling air flow. Optional extended temperature models operate reliably from -40 to 85°C.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board VHDL debugging.



Plug in an AXM analog or digital I/O module for additional I/O signal processing capabilities.

#### Key Features & Benefits

- Reconfigurable Xilinx Spartan-6 FPGA with 147,433 logic cells
- PCI-X bus 100MHz 64-bit interface
- 256k x 64-bit dual-ported SRAM provides direct links from the PCI bus and to the FPGA (optional 1M x 64-bit)
- Supports both front and rear I/O connections
- 64 I/O or 32 LVDS lines direct to FPGA via rear (J4) connector
- Plug-in I/O extension modules are available for the front mezzanine
- FPGA code loads from the PCI-X bus or from flash memory
- Other memory options available (call factory)
- Supports dual DMA channel data transfer to the CPU/bus
- Support for Xilinx ChipScope™ Pro interface
- Designed for conduction-cooled host card or -40 to 85°C operation in air-cooled systems

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## PMC-SLX User-Configurable Spartan-6 FPGA Modules with Plug-In I/O

### Performance Specifications

#### ■ FPGA

##### FPGA Device

Xilinx Spartan-6 FPGA.

Model XC6SLX150-3FG676 FPGA with 147,433 logic cells and 180 DSP48A1 slices.

##### FPGA configuration

Download via PCI-X bus or flash memory.

##### Example FPGA program

VHDL provided for bus interface, front & rear I/O control, SRAM read/write interface logic, and SDRAM memory interface controller. See EDK kit.

#### ■ I/O Processing

Acromag AXM I/O modules:

AXM modules plug into the PMC module's front mezzanine for additional I/O lines. Analog and digital I/O AXM modules are sold separately.

##### Rear I/O

64 I/O (32 LVDS) lines supported with a direct connection between the FPGA and the rear I/O connector (J4).

#### ■ Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a PMC-SLX module (see [www.acromag.com](http://www.acromag.com) for more information).

#### ■ PMC Compliance

Conforms to PCI Local Bus Specification, Revision 3.0 and CMC/PMC Specification, P1386.1.

Electrical/Mechanical Interface: Single-Width Module.

PCI Bus Modes: Supports PCI-X at 100MHz, 66MHz and Standard PCI at 66MHz and 33MHz

PCI-X Master/Target: 32-bit or 64-bit interface

Signaling: 3.3V compliant.

Interrupts (INTA#): Interrupt A is used to request an interrupt.

#### ■ Environmental

##### Operating temperature

-0 to 70°C or -40 to 85°C (E versions).

##### Storage temperature

-55 to 125°C.

##### Relative humidity

5 to 95% non-condensing.

##### Power

3.3V (±5%): 700mA typical, 840mA maximum.

5V (±5%): 1600mA typical, 2160mA maximum.

##### MTBF

Contact the factory.

### Ordering Information

NOTE: PMC-SLX-EDK is required to configure FPGA.

#### ■ PMC Modules

##### PMC-SLX150

User-configurable Spartan-6 FPGA, 150k logic cells, 256 x 64-bit dual-port SRAM

##### PMC-SLX150E

Same as PMC-SLX150 with extended temp. range

##### PMC-SLX150-1M

User-configurable Spartan-6 FPGA, 150k logic cells, 1M x 64-bit dual-port SRAM

##### PMC-SLX150E-1M

Same as PMC-SLX150-1M with extended temp. range

#### ■ AXM Plug-In I/O Extension Modules

For more information, see [www.acromag.com](http://www.acromag.com).

##### AXM-A30

2 analog input 100MHz 16-bit A/D channels

##### AXM-D02

30 RS485 differential I/O channels

##### AXM-D03

16 CMOS and 22 RS485 differential I/O channels

##### AXM-D04

30 LVDS I/O channels

##### AXM-??

Custom I/O configurations available, call factory.

#### ■ Software

For more information, see [www.acromag.com](http://www.acromag.com).

##### PMC-SLX-EDK

Engineering Design Kit (one kit required)

##### PMCSW-API-VXW

VxWorks® software support package

##### PCISW-API-WIN32

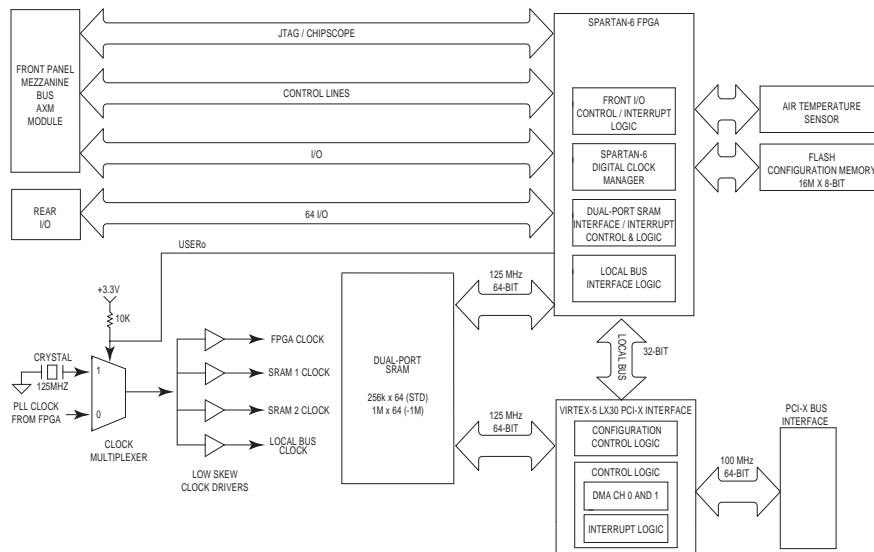
32-bit Windows® driver (DLL) software package

##### PCISW-API-WIN64

64-bit Windows® driver (DLL) software package

##### PCISW-API-LNX

Linux™ support (website download only)



## PMC-SX35 User-configurable Virtex-4 FPGA Modules with plug-in I/O

### Description

Acromag's PMC-SX boards use a high-performance Xilinx® Virtex-4™ FPGA, but maintain a relatively low price point. They are optimized for high-performance digital signal processing to help you build custom pre/post-co-processing hardware or high-performance filters. You can create more than 40 different functions (MACs, multipliers, adders, and muxes).

Although there is no limit to the uses for Acromag's FPGA boards, typical applications include sonar and radar processing.

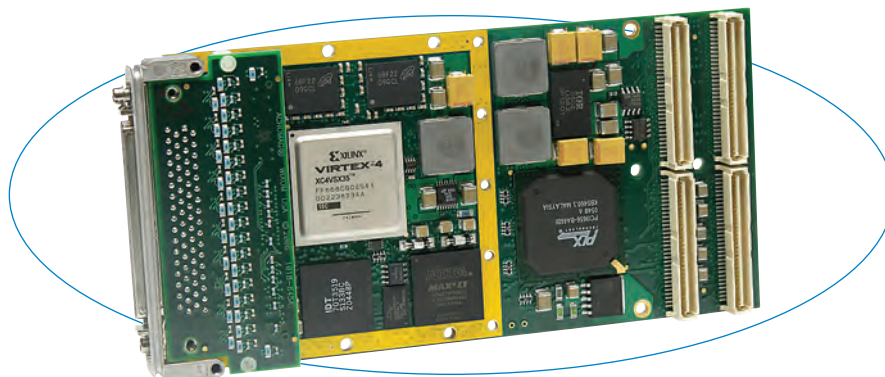
I/O processing is handled on a separate mezzanine card that plugs into the FPGA base board. A variety of these external I/O cards offer an interface for your analog and digital I/O signals. See the [AXM I/O Card](#) for more details. Additionally, 64 I/O lines are supported via the rear (J4) connector.

Plenty of DRAM memory is available for receipt and transfer of high-speed data from the I/O data ports on the front and rear of the board. Dual Ported SRAM memory is supplied for storage of data to be passed, via DMA transfer, to the PCI bus. One of the dual ports is attached to the FPGA and the other to the local bus.

The PCI bus interface is handled by a PLX® PCI 9656 device which provides 64-bit 66MHz bus mastering with dual-channel DMA support.

Take advantage of the optional conduction cooling for use in hostile environments. Conduction cooling provides efficient heat dissipation in environments where there is inadequate cooling air flow.

Acromag provides software utilities and examples to simplify your programming and get you started quickly. A JTAG interface enables on-board VHDL simulation.



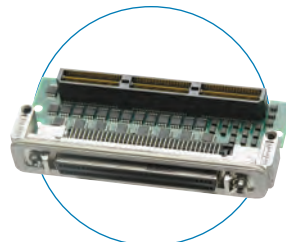
Download your own logic programs into the user-configured FPGA to quickly create a custom I/O module. Shown with optional plug-in I/O module.

### Features

- Customizable FPGA (Xilinx Virtex-4 XC4VSX35) with up to 34K logic cells and 192 XtremeDSP™ slices
- Supports both front and rear I/O
- Plug-in I/O modules are available for front mezzanine
- 64 I/O lines supported with direct connection to FPGA via rear (J4) connector
- FPGA code loads from PCI bus or flash memory
- 256K x 36-bit dual-ported SRAM
- 32Mb x 32-bit DDR DRAM
- Supports dual DMA channel data transfer to CPU
- Supports both 5V and 3.3V signalling
- Conduction cooled or 0 to 70°C operating range



The base board is ready for conduction-cooled applications.



Plug-in AXM modules sold separately for analog and digital I/O.

### Specifications

#### FPGA

FPGA: Xilinx Virtex-4 FPGA XC4VSX35 with 34,560 logic cells and 192 DSP slices.

FPGA configuration: Downloadable via PCI bus or from flash memory.

Example FPGA program: VHDL provided implements interface to PCI bus IC, interface to dual port SRAM, PLL control, ADC, and DAC control. Program requires user proficiency with Xilinx software tools. See Engineering Design Kit.

#### I/O Processing

AXM modules: for front mezzanine:

Acromag AXM modules attach to the board to provide I/O. A variety of modules are available and are sold separately.

Rear I/O:

32 LVDS I/O lines supported with a direct connection between the FPGA and the rear I/O connector (J4).

#### Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a PMC-SX module. (see Design Kit for details)

#### PMC Compliance

Conforms to PCI Local Bus Specification, Revision 2.2 and CMC/PMC Specification, P1386.1.

Electrical/Mechanical Interface: Single-Width Module.

PCI bus clock frequency: 66MHz.

32-bit PCI Master: Implemented by PLX PCI 9056 device.

Signaling: 5V and 3.3V compliant.

Interrupts (INTA#): Interrupt A is used to request an interrupt.

#### Environmental

Operating temperature: 0 to 70°C

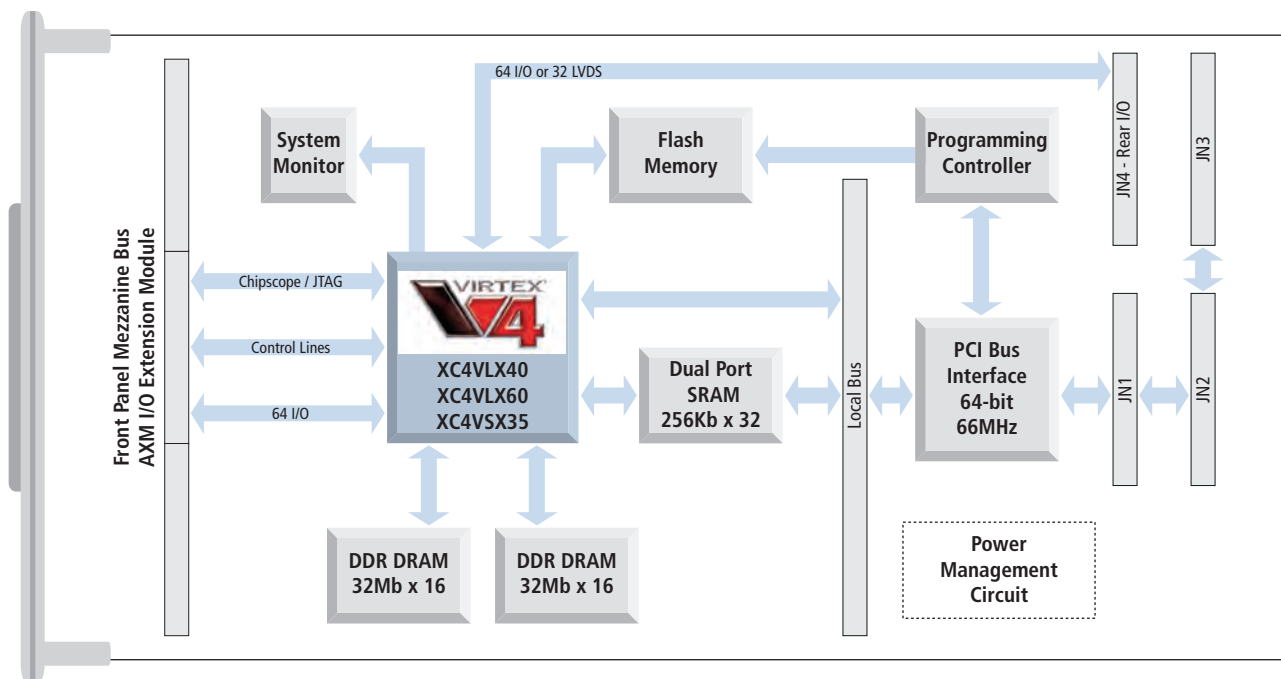
Storage temperature: -55 to 105°C.

Relative humidity: 5 to 95% non-condensing.

Power: Consult factory. Operates from 3.3V supply.

MTBF: 869,686 hrs. at 25°C, MIL-HDBK-217F, Notice 2.





## Ordering Information

### PMC Modules

#### PMC-SX35

User-configurable Virtex-4 FPGA with 34,560 logic cells

#### PMC-SX-EDK

Engineering Design Kit (one kit required)

### AXM Plug-In I/O Modules

For more information, see [AXM data sheet](#).

#### AXM-A30

2 16-bit 100MHz A/D channels

#### AXM-D02

30 RS485 differential I/O channels

#### AXM-D03

16 CMOS and 22 RS485 differential I/O channels

#### AXM-D04

30 LVDS I/O channels

#### AXM-??

Custom I/O configurations available, call factory.

**Software** (see [software documentation](#) for details)

#### PMCSW-API-VXW

VxWorks® software support package

#### PCISW-API-WIN

Windows® DLL software support

#### PCISW-API-LNX

Linux® support (website download only)

## PMC-VFX70 User-Configurable Virtex-5 FPGA Modules with Plug-In I/O

- XC5VFX70T FPGA: 71,680 logic cells and embedded PowerPC 440 processor 32-bit RISC core

### Description

Acromag's PMC-VFX boards feature a reconfigurable Xilinx® Virtex™-5 FPGA enhanced with multiple high-speed memory buffers and a high-throughput PCI-X interface. Field I/O interfaces to the FPGA via the rear J4/P4 connector and/or with optional front mezzanine plug-in I/O modules. The result is a powerful and flexible I/O processor module that is capable of executing your custom instruction sets and algorithms.

The on-board FPGA has a hard core PowerPC 440 block to handle the most complex and memory-intensive computing applications. Offload your CPU-intensive operations such as video and 3D data processing or fixed-point math for superior system performance. The PowerPC core also enables system-on-chip functionality with real-time processing capabilities.

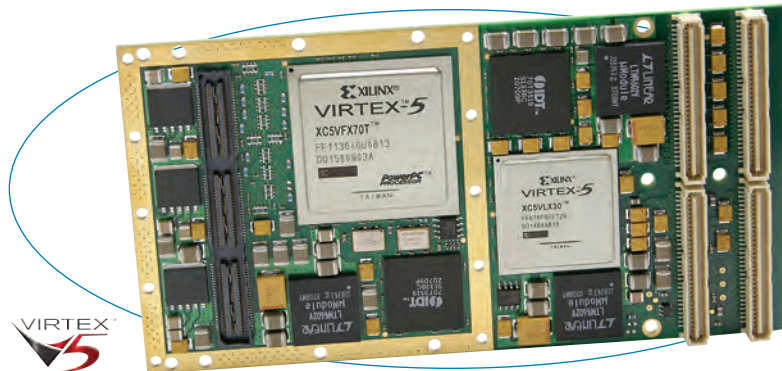
64 I/O lines are provided via the rear (J4) connector. Additional I/O processing is supported on a separate mezzanine card that plugs into the FPGA base board. A variety of these external I/O cards offer an interface for your analog and digital I/O signals. See the AXM I/O Card data sheet (Bulletin 8400-458) for more details.

Large, high-speed memory banks provide efficient data handling. Generous DDR2 SDRAM buffers store captured data prior to FPGA processing. Afterward, data is moved to dual-port SRAM for high-speed DMA transfer to the system. Our high-bandwidth PCI-X interface ensures fast data throughput.

Take advantage of the module's support of conduction cooling for efficient dissipation of heat in environments with inadequate cooling air flow. Optional extended temperature models operate from -40 to 85°C.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board VHDL simulation.

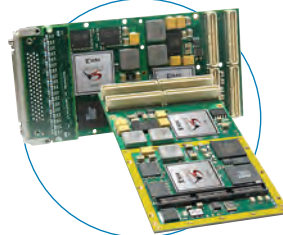
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Download your own programs into the reconfigurable FPGA to quickly create custom I/O module. Optional I/O modules plug into the front mezzanine.

### Features

- Reconfigurable Xilinx Virtex-5 FPGA
- PCI-X bus 100MHz 64-bit interface
- Supports both front and rear I/O connections
- 64 I/O or 32 LVDS lines direct to FPGA via rear (J4)
- Plug-in I/O modules available for front mezzanine
- FPGA code loads from PCI bus or 32MB flash memory
- Two banks of 256K x 32-bit dual-ported SRAM
- Two banks of 64M x 16-bit DDR2 SDRAM
- Other memory options available (contact factory)
- Supports dual DMA channel data transfer to CPU/bus
- Supports 3.3V signalling
- Support for Xilinx ChipScope™ Pro interface
- Conduction-cooled or -40 to 85°C operating range



Plug-in AXM I/O or use base board for conduction-cooled applications.



Plug-in modules sold separately for analog and digital I/O functions.

### Specifications

#### FPGA

FPGA: Xilinx Virtex-5 FPGA XC5VFX70T FPGA with 71,680 logic cells and PowerPC processor block  
FPGA configuration: Download via PCI bus or flash memory.  
Example FPGA program: VHDL provided for local bus interface, control of front & rear I/O, SRAM read/write interface logic, and SDRAM memory interface controller. See EDK kit.

#### I/O Processing

Acromag AXM I/O modules: for front mezzanine:  
AXM modules attach to the board for additional I/O lines.  
Analog and digital I/O AXM modules are sold separately.  
Rear I/O:  
64 I/O (32 LVDS) lines supported with a direct connection between the FPGA and the rear I/O connector (J4).

#### Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a PMC-VFX module.

#### PMC Compliance

Conforms to PCI Local Bus Specification, Revision 3.0 and CMC/PMC Specification, P1386.1.

Electrical/Mechanical Interface: Single-Width Module.

PCI Bus Modes: Supports PCI-X at 100MHz, 66MHz and Standard PCI at 66MHz and 33MHz

PCI-X Master/Target: 32-bit or 64-bit interface

Signaling: 3.3V compliant.

Interrupts (INTA#): Interrupt A is used to request an interrupt.

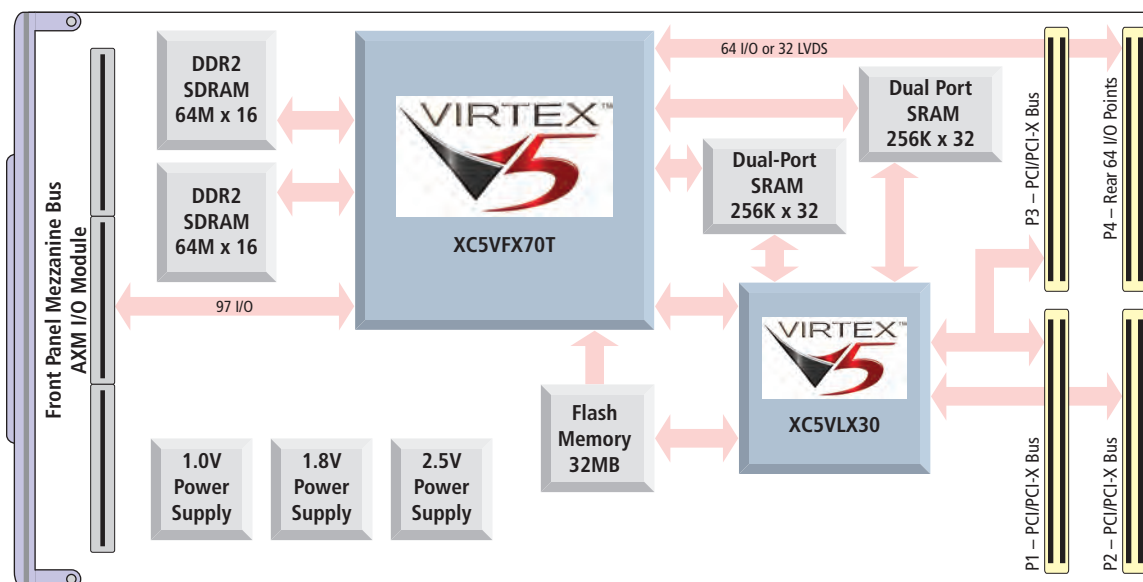
#### Environmental

Operating temperature: 0 to 70°C or -40 to 85°C (E versions)  
Storage temperature: -55 to 105°C.

Relative humidity: 5 to 95% non-condensing.

Power: Consult factory. Operates from 3.3V supply.

MTBF: Consult factory.



## Ordering Information

### PMC Modules

#### PMC-VFX70

User-configurable Virtex-5 FPGA with 71,680 logic cells and PowerPC processor block

#### PMC-VFX70E

Same as PMC-VFX70 with extended temperature range

#### PMC-VFX-EDK

Engineering Design Kit (one kit required)

### AXM Plug-In I/O Extension Modules

For more information, see [AXM data sheet](#).

#### AXM-A30

2 analog input 105MHz 16-bit A/D channels

#### AXM-D02

30 RS485 differential I/O channels

#### AXM-D03

16 CMOS and 22 RS485 differential I/O channels

#### AXM-D04

30 LVDS I/O channels

#### AXM-??

Custom I/O configurations available, call factory.

### Software (see [software documentation](#) for details)

#### PMCSW-API-VXW

VxWorks® software support package

#### PCISW-API-WIN

Windows® DLL software support

#### PCISW-API-LNX

Linux® support (website download only)

## PMC-VLX85/110/155 User-Configurable Virtex-5 FPGA Modules with Plug-In I/O

- PMC-VLX85: 82,944 logic cells (XC5VLX85T)
- PMC-VLX110: 110,592 logic cells (XC5VLX110T)
- PMC-VLX155: 155,648 logic cells (XC5VLX155T)

### Description

Acromag's PMC-VLX boards feature a reconfigurable Xilinx® Virtex™-5 FPGA enhanced with multiple high-speed memory buffers and a high-throughput PCI-X interface. Field I/O interfaces to the FPGA via the rear J4/P4 connector and/or with optional front mezzanine plug-in I/O modules. The result is a powerful and flexible I/O processor module that is capable of executing your custom instruction sets and algorithms.

Three models provide a choice of logic-optimized FPGAs to match your performance requirements. Although there is no limit to the uses for these boards, several applications are ideal. Typical uses include hardware simulation, communications, military servers, in-circuit diagnostics, signal intelligence, and image processing.

64 I/O lines are provided via the rear (J4) connector. Additional I/O processing is supported on a separate mezzanine card that plugs into the FPGA base board. A variety of these external I/O cards offer an interface for your analog and digital I/O signals. See the [AXM I/O Card](#) data sheet for more details.

Large, high-speed memory banks provide efficient data handling. Generous DDR2 SDRAM buffers store captured data prior to FPGA processing. Afterward, data is moved to dual-port SRAM for high-speed DMA transfer to the bus or CPU. Our high-bandwidth PCI-X interface ensures fast data throughput.

Take advantage of conduction cooling for use in hostile environments. Conduction efficiently dissipates heat in environments with inadequate cooling air flow. Optional extended temperature models operate from -40 to 85°C.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board VHDL simulation.

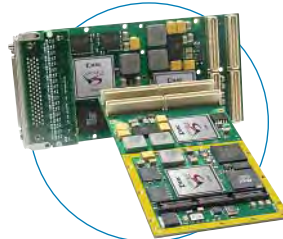
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Download your own programs into the reconfigurable FPGA to quickly create custom I/O module. Optional I/O modules plug into the front mezzanine.

### Features

- Reconfigurable Xilinx Virtex-5 FPGA
- PCI-X bus 100MHz 64-bit interface
- Supports both front and rear I/O connections
- 64 I/O or 32 LVDS lines direct to FPGA via rear (J4)
- Plug-in I/O modules are available for front mezzanine
- FPGA code loads from PCI bus or flash memory
- Two banks of 256Kb x 32-bit dual-ported SRAM
- Two banks of 32Mb x 16-bit DDR2 SDRAM
- Other memory options available (contact factory)
- Supports dual DMA channel data transfer to CPU/bus
- Supports 3.3V signalling
- Support for Xilinx ChipScope™ Pro interface
- Conduction-cooled or -40 to 85°C operating range



Plug-in AXM I/O or use base board for conduction-cooled applications.



Plug-in modules sold separately for analog and digital I/O functions.

### Specifications

#### FPGA

FPGA: Xilinx Virtex-5 FPGA

PMC-VLX85: XC5VLX85T FPGA with 82,944 logic cells

and 48 DSP48E slices

PMC-LX110: XC5VLX110T FPGA with 110,592 logic cells

and 64 DSP48E slices

PMC-LX155: XC5VLX155T FPGA with 155,648 logic cells

and 128 DSP48E slices

FPGA configuration: Download via PCI bus or flash memory.

Example FPGA program: VHDL provided for local bus interface, control of front & rear I/O, SRAM read/write interface logic, and SDRAM memory interface controller. See EDK kit.

#### I/O Processing

Acromag AXM I/O modules: for front mezzanine:

AXM modules attach to the board for additional I/O lines.

Analog and digital I/O AXM modules are sold separately.

Rear I/O:

64 I/O (32 LVDS) lines supported with a direct connection between the FPGA and the rear I/O connector (J4).

#### Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a PMC-VLX module

#### PMC Compliance

Conforms to PCI Local Bus Specification, Revision 3.0 and CMC/PMC Specification, P1386.1.

Electrical/Mechanical Interface: Single-Width Module.

PCI Bus Modes: Supports PCI-X at 100MHz, 66MHz and Standard PCI at 66MHz and 33MHz

PCI-X Master/Target: 32-bit or 64-bit interface

Signaling: 3.3V compliant.

Interrupts (INTA#): Interrupt A is used to request an interrupt.

#### Environmental

Operating temperature: 0 to 70°C or -40 to 85°C (E versions)

Storage temperature: -55 to 105°C.

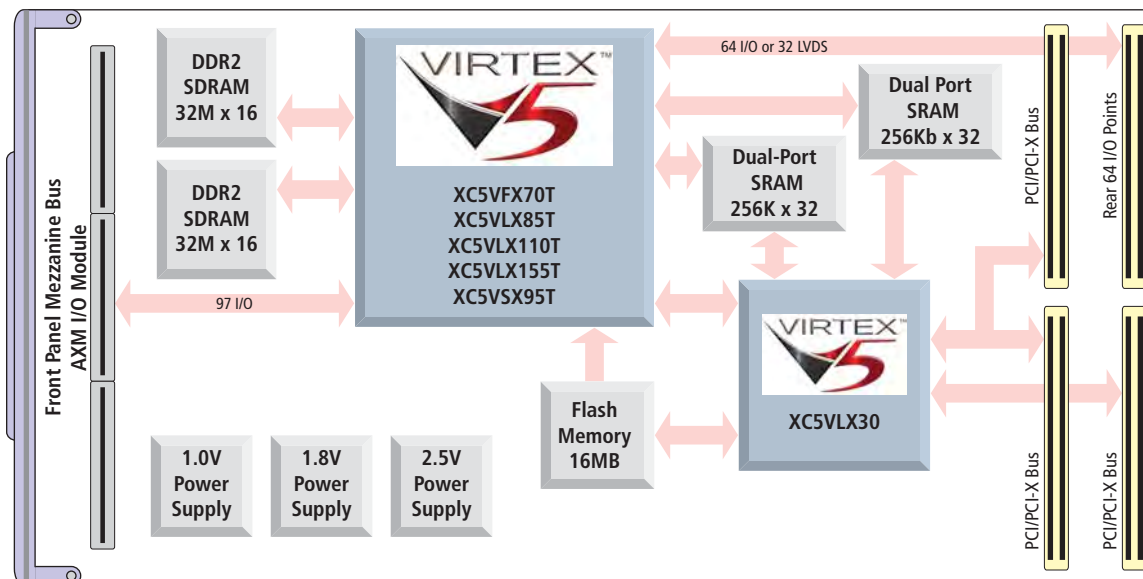
Relative humidity: 5 to 95% non-condensing.

Power: Consult factory. Operates from 3.3V supply.

MTBF: Hours at 25°C, MIL-HDBK-217F, Notice 2

VLX-85: 633,360; VLX-10: 624,625; VLX-155: call factory.





## Ordering Information

### PMC Modules

#### PMC-VLX85

User-configurable Virtex-5 FPGA with 82,944 logic cells

#### PMC-VLX85E

Same as PMC-VLX85 with extended temperature range

#### PMC-VLX110

User-configurable Virtex-5 FPGA with 110,592 logic cells

#### PMC-VLX110E

Same as PMC-VLX110 with extended temperature range

#### PMC-VLX155

User-configurable Virtex-5 FPGA with 155,648 logic cells

#### PMC-VLX155-1M

Same as PMC-VLX155 plus 1MB x 64 dual port SRAM

#### PMC-VLX155E

Same as PMC-VLX155 with extended temperature range

#### PMC-VLX-EDK

Engineering Design Kit (one kit required)

### AXM Plug-In I/O Extension Modules

For more information, see [AXM data sheet](#).

#### AXM-A30

2 analog input 100MHz 16-bit A/D channels

#### AXM-D02

30 RS485 differential I/O channels

#### AXM-D03

16 CMOS and 22 RS485 differential I/O channels

#### AXM-D04

30 LVDS I/O channels

#### AXM-??

Custom I/O configurations available, call factory.

### Software

(see [software documentation](#) for details)

#### PMCSW-API-VXW

VxWorks® software support package

#### PCISW-API-WIN32

32-bit Windows driver software package with DLLs and demonstration programs for PMC, XMC, PCI, and cPCI products. Supplied on CD-ROM. Windows® DLL software support.

#### PCISW-API-WIN64

64-bit Windows driver software package with DLLs and demonstration programs for PMC, XMC, PCI, and cPCI products. Supplied on CD-ROM. Windows® DLL software support

#### PCISW-API-LNX

Linux® support (website download only)

## PMC-VSX95 User-Configurable Virtex-5 FPGA Modules with Plug-In I/O

- PMC-VSX95: 94,208 logic cells and 640 DSP48E slices (XC5VSX95T)

### Description

Acromag's PMC-VSX boards feature a reconfigurable Xilinx® Virtex™-5 FPGA enhanced with multiple high-speed memory buffers and a high-throughput PCI-X interface. Field I/O interfaces to the FPGA via the rear J4/P4 connector and/or with optional front mezzanine plug-in I/O modules. The result is a powerful and flexible I/O processor module that is capable of executing your custom instruction sets and algorithms.

The on-board FPGA is a DSP-optimized version of the Virtex-5 FPGA. Although there is no limit to the uses for these boards, several applications are ideal. Typical uses include hardware simulation, communications, military servers, in-circuit diagnostics, signal intelligence, and image processing.

64 I/O lines are provided via the rear (J4) connector. Additional I/O processing is supported on a separate mezzanine card that plugs into the FPGA base board. A variety of these external I/O cards offer an interface for your analog and digital I/O signals. See the AXM I/O Card data sheet (Bulletin 8400-458) for more details.

Large, high-speed memory banks provide efficient data handling. Generous DDR2 SDRAM buffers store captured data prior to FPGA processing. Afterward, data is moved to dual-port SRAM for high-speed DMA transfer to the bus or CPU. Our high-bandwidth PCI-X interface ensures fast data throughput.

Take advantage of conduction cooling for use in hostile environments. Conduction efficiently dissipates heat in environments with inadequate cooling air flow. Optional extended temperature models operate from -40 to 85°C.

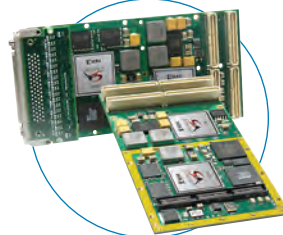
Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board VHDL simulation.



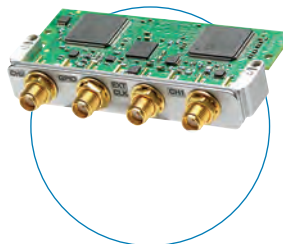
Download your own programs into the reconfigurable FPGA to quickly create custom I/O module. Optional I/O modules plug into the front mezzanine.

### Features

- Reconfigurable Xilinx Virtex-5 FPGA (VSX95T)
- PCI-X bus 100MHz 64-bit interface
- Supports both front and rear I/O connections
- 64 I/O or 32 LVDS lines direct to FPGA via rear (J4)
- Plug-in I/O modules are available for front mezzanine
- FPGA code loads from PCI bus or flash memory
- Two banks of 256Kb x 32-bit dual-ported SRAM
- Two banks of 32Mb x 16-bit DDR2 SDRAM
- Other memory options available (contact factory)
- Supports dual DMA channel data transfer to CPU/bus
- Supports 3.3V signalling
- Support for Xilinx ChipScope™ Pro interface
- Conduction-cooled or -40 to 85°C operating range



Plug-in AXM I/O or use base board for conduction-cooled applications.



Plug-in modules sold separately for analog and digital I/O functions.

### Specifications

#### FPGA

FPGA: Xilinx Virtex-5 FPGA

PMC-VSX95: XC5VSX95T FPGA with 94,208 logic cells and 640 DSP48E slices

FPGA configuration: Download via PCI bus or flash memory.

Example FPGA program: VHDL provided implements local bus interface, control of front and rear I/O, SRAM read/write interface logic, and SDRAM memory interface controller. Program requires user proficiency with Xilinx software tools. See Engineering Design Kit.

#### I/O Processing

Acromag AXM I/O modules: for front mezzanine:

AXM modules attach to the board for additional I/O lines. Analog and digital I/O AXM modules are sold separately.

Rear I/O:

64 I/O (32 LVDS) lines supported with a direct connection between the FPGA and the rear I/O connector (J4).

#### Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a PMC-VSX module.

#### PMC Compliance

Conforms to PCI Local Bus Specification, Revision 3.0 and CMC/PMC Specification, P1386.1.

Electrical/Mechanical Interface: Single-Width Module.

PCI Bus Modes: Supports PCI-X at 100MHz, 66MHz and Standard PCI at 66MHz and 33MHz

PCI-X Master/Target: 32-bit or 64-bit interface

Signaling: 3.3V compliant.

Interrupts (INTA#): Interrupt A is used to request an interrupt.

#### Environmental

Operating temperature: 0 to 70°C or -40 to 85°C (E versions)

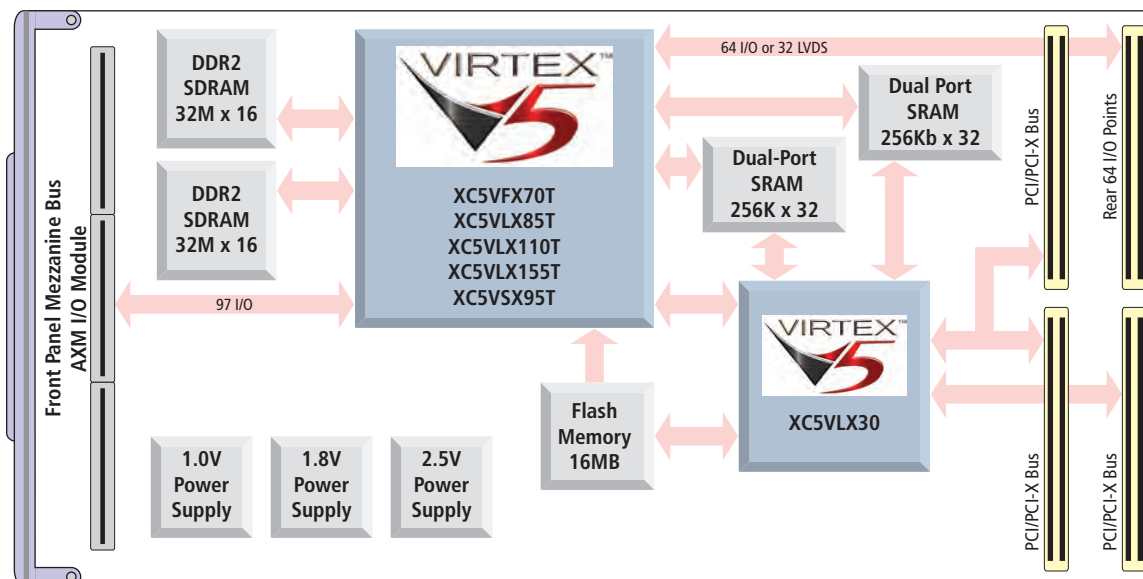
Storage temperature: -55 to 105°C.

Relative humidity: 5 to 95% non-condensing.

Power: Consult factory. Operates from 3.3V supply.

MTBF: 630,959 hours at 25°C, MIL-HDBK-217F, Notice 2

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## Ordering Information

### PMC Modules

#### PMC-VSX95

User-configurable Virtex-5 FPGA with 94,208 logic cells

#### PMC-VSX95E

Same as PMC-VSX95 with extended temperature range

#### PMC-VSX-EDK

Engineering Design Kit (one kit required)

### AXM Plug-In I/O Extension Modules

For more information, see [AXM data sheet](#).

#### AXM-A30

2 analog input 100MHz 16-bit A/D channels

#### AXM-D02

30 RS485 differential I/O channels

#### AXM-D03

16 CMOS and 22 RS485 differential I/O channels

#### AXM-D04

30 LVDS I/O channels

#### AXM-??

Custom I/O configurations available, call factory.

### Software

(see [software documentation](#) for details)

#### PMCSW-API-VXW

VxWorks® software support package

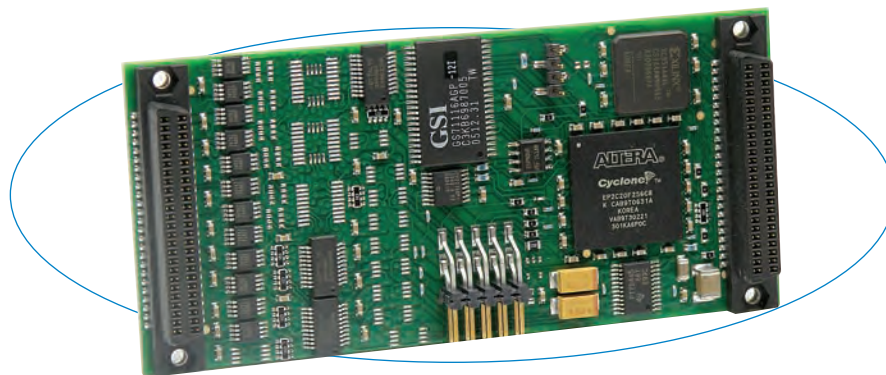
#### PCISW-API-WIN

Windows® DLL software support

#### PCISW-API-LNX

Linux™ support (website download only)

## IP-EP200 JTAG-Reconfigurable Cyclone™ II FPGA Digital I/O Modules



This series of plug-in mezzanine modules provides a user-customizable Altera® Cyclone II FPGA on an Industry Pack (IP) module. The module allows users to develop and store their own instruction set in the FPGA for adaptive computing applications. Typical uses include specialized communication systems over RS422/485 networks, test fixture simulation of signals over TTL-switched lines, and analysis of acquired data using specialized mathematical formulas such as those developed with MathWorks's MatLab® software.

The FPGA on Acromag's IP-EP200 modules can control up to 48 TTL or 24 RS485 I/O signals or a mix of both types. Another model interfaces 24 LVDS I/O channels. User application programs are downloaded through the JTAG port or via the IP bus directly into the FPGA. A pre-programmed internal CPLD facilitates initialization by acting as the bus controller during power-up and while the program is downloading. This bus controller is limited to functions necessary for power-up and downloading. After the program downloads, the FPGA takes control of the IP bus and the CPLD disables.

### Features

- Altera Cyclone II EP2C200 FPGA
- Four models available:
  - IP-EP201: 48 TTL I/O lines
  - IP-EP202: 24 differential RS485 I/O lines
  - IP-EP203: 24 TTL and 12 RS485 I/O lines
  - IP-EP204: 24 LVDS I/O lines
- FPGA programmable via JTAG port or IP bus
- Local static RAM (64K x 16) under FPGA control
- LVTTTL external clock connected directly to the FPGA
- Supports 8MHz and 32MHz IP bus
- Programmable PLL-based clock synthesizer
- Example FPGA design code provided as VHDL
  - 8MHz IP bus interface
  - Digital I/O control register
  - others
- Hardware support for DMA and memory space

These modules support adaptive computing applications with an FPGA running custom programs to control system communication.

### Specifications

#### FPGA

FPGA: Altera Cyclone II EP2C200.

FPGA configuration: Downloadable via JTAG port or IP bus.

Clock: Cypress CY22150 (or equivalent).

Generates frequencies from 250kHz to 100MHz

Input/output signals:

- IP-EP201: 48 TTL lines
- IP-EP202: 24 differential RS485 lines
- IP-EP203: 24 TTL lines and 12 RS485
- IP-EP204: 24 LVDS lines

All models: LVTTTL external clock input

IP bus clock frequency: Supports 8 and 32MHz clocks.

ID space: 8-bit data.

I/O space: 8 or 16-bit data.

Memory space: Wired to FPGA but not supported with example FPGA design firmware.

Interrupt support: Two IP request levels.

DMA support: Wired to FPGA but not supported with example FPGA design firmware.

IP logic interface: CPLD maintains ID space and two locations in IO space for FPGA configuration. Remaining IO space and INT space are defined by the configured FPGA.

Example FPGA program: VHDL provided implements IP bus interface to IO, ID, and INT space. Requires user proficiency with VHDL and Altera Quartus® II software tools. See Engineering Design Kit.

#### IP Compliance (ANSI/VITA 4)

Meets IP specifications per ANSI/VITA 4-1995.

IP data transfer cycle types supported: Input/output (IOSel\*), ID read (IDSel\*), Interrupt select (INTSel\*).

Access times (8MHz or 32MHz clock):

- ID space read: 1 wait state (375nS cycle @ 8MHz).
- Registers read/write: 1 wait state (375nS cycle @ 8MHz).
- Interrupt read/write: 1 wait state (375nS cycle @ 8MHz).

#### Environmental

Operating temperature: 0 to 70°C or -40 to 85°C (E models).

Storage temperature: -55 to 125°C.

Relative humidity: 5 to 95% non-condensing.

MTBF: Consult factory.

### Engineering Design Kit

Engineering Design Kit: Provides user with basic information required to develop a custom FPGA program for download to the Altera FPGA. This kit must be ordered with the first purchase of an IP-EP200 module.

Kit on CD-ROM includes:

- Schematics (.pdf)
- Parts list and part location drawing (.pdf)
- Example VHDL source file (.vhd)
- Example assignments file (.qsf)
- Example configuration file (.hex)
- Programming guide (.pdf)

Only one Design Kit purchase is required. User should be fluent in use of Altera Quartus design tools. Additionally, user should also purchase either the IPSW-API-VXW (VxWorks source code library) or the IPSW-API-WIN (Windows DLL driver package). These programs include important driver support programs to assist in transferring developer code between user's processor and EPC20 FPGA.

### Ordering Information

#### Industry Pack Modules

IP-EP201: 48 TTL I/O lines

IP-EP201E: Same as above w/extended temperature range

IP-EP202: 24 differential RS485 I/O lines

IP-EP202E: Same as above w/extended temperature range

IP-EP203: 24 TTL and 12 RS485 I/O lines

IP-EP203E: Same as above w/extended temperature range

IP-EP204: 24 LVDS I/O lines

IP-EP204E: Same as above w/extended temperature range

IP-EP2-EDK: Engineering Design Kit (one kit required)

Acromag offers a wide selection of [Industry Pack Carrier Cards](#).

**Software** (see [software documentation](#) for details)

IPSW-API-VXW: VxWorks® software support package

IPSW-API-WIN: Windows® DLL driver software support pkg.

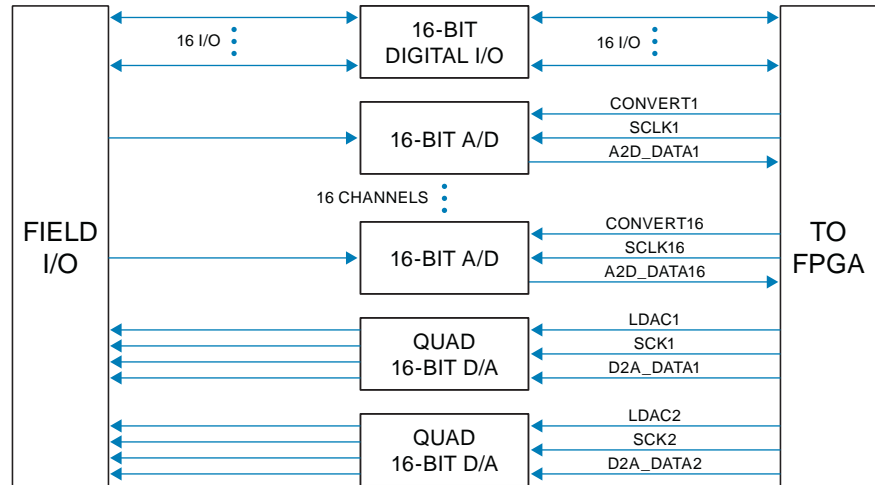
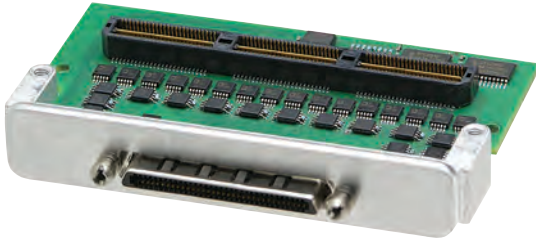
IPSW-LINUX: Linux™ support (website download only)

See [accessories documentation](#) for additional information.



# Extension I/O Modules

## AXM-A75 Multi-function I/O extension module for Acromag FPGA cards



16 analog inputs, simultaneous A/D ♦ 8 analog outputs, simultaneous D/A ♦ 16 digital I/O channels

### Description

The AXM-75 is a multi-function I/O module that adds A/D, D/A, and digital I/O signal processing functions to an FPGA board. These extension I/O modules plug directly onto many Acromag reconfigurable FPGA cards equipped with an AXM mezzanine connector.

### Analog Input

There are sixteen differential analog input channels on the AXM-A75. Each input has its own high-speed 16-bit A/D converter offering the ability to simultaneously sample all channels.

At the beginning of the analog signal chain is a low-pass filter to remove any unwanted EMI. A programmable gain instrumentation amplifier scales the input and provides giga-ohm input impedance. Serial FLASH memory is included to store factory calibration constants.

### Analog Output

Two quad serial input DAC devices drive eight analog output channels. Each channel has its own high-speed 16-bit D/A converter allowing simultaneous updates to all outputs.

### Digital I/O

Sixteen bi-directional digital I/O channels provide the ability to monitor and control discrete devices. Each I/O channel is individually configurable as an input or output for great flexibility to match your requirements

### Key Features & Benefits

- 16 channels of analog input capable of simultaneous sampling
- 16-bit 500kHz A/D converter on each channel
- Analog input range of  $\pm 10.24$  volts
- Programmable gain of 1x, 2x, 4x, or 8x
- 8 channels of analog output capable of simultaneous updates
- Each A/D channel includes a 2K sample FIFO
- FIFO status interrupts configurable for half-full or overflow conditions
- Dual quad 16-bit serial input D/A converters with 10 $\mu$ s settling time
- Analog output range of  $\pm 10$  volts
- 16 channels of general-purpose digital I/O
- Front panel 68-pin VHDCI receptacle for field I/O connections
- Example VHDL code provided in the base board's Engineering Design Kit to control sample rate and gain selection



AXM extension I/O modules plug into a mezzanine connector on many Acromag FPGA boards to provide additional I/O signal processing capabilities.

# Extension I/O Modules



## AXM-A75 Multi-function I/O extension module for Acromag FPGA cards

### Performance Specifications

#### ■ Analog Input

##### Input configuration

16 differential channels with a separate A/D converter on each channel.

##### A/D resolution

16 bits.

##### Input range

±10.24 volts.

##### Programmable gain

1x, 2x, 4x, or 8x.

##### Input impedance

1 giga-ohm.

##### Maximum throughput rate

2 $\mu$ S A/D (500kHz).

##### A/D trigger

FPGA controlled.

##### Signal-to-noise ratio

69dB (25°C) typical.

##### Signal-to-noise and distortion

67dB (25°C) typical.

#### ■ Analog Output

##### Output configuration

8 channels with a separate D/A converter for each channel provided by two quad serial input DACs. Double buffering allows the simultaneous updating of all channels.

##### D/A resolution

16 bits.

##### Output range

±10 volts.

##### Settling time

10 $\mu$ S (100kHz).

#### ■ Digital I/O

##### I/O configuration

16 bi-directional I/O channels, individually configured.

##### I/O range

5V TTL.

##### Output type

Open collector type with open drain outputs.

##### Pull-up resistor

Digital I/O lines are pulled high via a 4.75k ohm resistor to +5 volts.

#### ■ Physical

Acromag AXM I/O modules plug into a PMC or XMC FPGA module's front mezzanine for additional I/O lines. Analog and digital I/O AXM modules are sold separately.

##### Size

12.7 mm high x 42.1 mm deep x 74.0 mm wide (0.500 inches x 1.659 inches x 2.913 inches).

**The AXM-A75 exceeds the allowable mezzanine envelope as defined in IEEE 1386-2001 and may not be compatible with all PMC/XMC carriers. See user manual for details.**

##### Stacking height

5.0 mm (0.315 in).

##### Weight

41.3 g (1.46 oz).

##### Connectors

I/O: 68-pin VHDCI receptacle.

Mezzanine: High-speed 150-pin header.

#### ■ Environmental

##### Operating temperature

-40 to 85°C.

##### Storage temperature

-55 to 125°C.

##### Relative humidity

5 to 95% non-condensing.

##### Power

+3.3V: 39mA typical, 50mA maximum.

+5V: 54mA typical, 65mA maximum.

+12V: 103mA typical, 115mA maximum.

-12V: 92mA typical, 115mA maximum.

##### MTBF

Contact the factory.

##### Electromagnetic Compatibility (EMC)

Minimum immunity per European Norm EN61000-6-2:2005.

##### Electrostatic Discharge (ESD) Immunity

4KV direct contact and 8KV air-discharge to the enclosure port per IEC61000-4-2.

##### Radiated Field Immunity (RFI)

10V/m, 80 to 1000MHz AM; 3V/m, 1.4 to 2.0GHz;

1V/m, 2.0 to 2.7GHz, per IEC61000 4 3.

##### Electrical Fast Transient Immunity (EFT)

2KV to power, and 1KV to signal I/O per IEC61000-4-4.

##### Conducted RF Immunity (CRFI)

10Vrms, 150KHz to 80MHz, per IEC61000-4-6.

##### Surge Immunity

0.5KV to power and 1KV to signal per IEC61000-4-5.

##### Emissions

Per European Norm EN61000-6-4:2007.

##### Radiated Frequency Emissions

30 to 1000MHz per CISPR16 Class A.

### Ordering Information

#### ■ AXM Plug-In I/O Extension Modules

For more information, see [www.acromag.com](http://www.acromag.com).

##### [AXM-A75](#)

16 analog inputs, 8 analog outputs, and 16 digital I/O

##### [AXM-??](#)

Custom I/O configurations available, call factory.

#### ■ Accessories

For more information, see [www.acromag.com](http://www.acromag.com).

##### [5025-288](#)

Termination Panel for 68-pin SCSI-3 cable to connect field I/O Signals to the board.

##### [5028-420](#)

Termination shielded cable, 34-wire pairs, ultra SCSI/VHDCI male and SCSI-3 male connectors. Recommended for all I/O connections to model 5025-288 termination panel. 2 meters long.

##### [XMC FPGA Modules](#)

##### [PMC FPGA Modules](#)

ISO9001  
AS9100

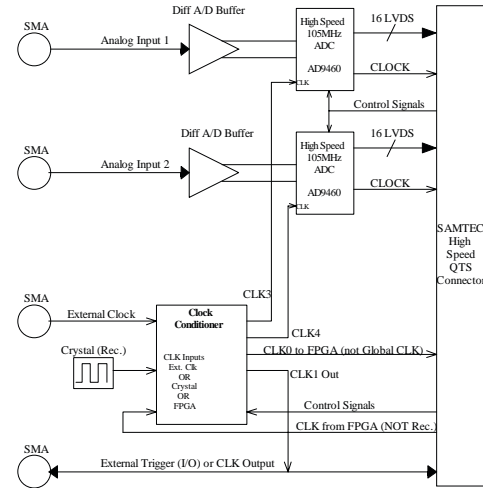
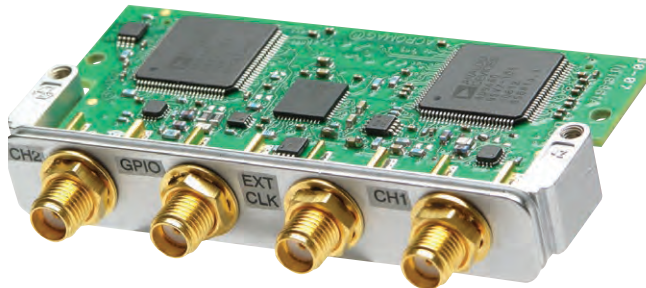


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# Extension I/O Modules

## AXM-A30 Analog I/O Extension Modules for PMC FPGA Boards



High Speed Analog Input ♦ 2 Differential Channels ♦ 2 16-bit A/D Channels

### Description

AXM Series extension modules offer numerous I/O options for Acromag's PMC modules with configurable FPGAs. These extension modules plug into the front mezzanine on Acromag's PMC-LX/SX (Virtex®-4 FPGA), and PMC-VLX/VSX/VFX (Virtex-5 FPGA) modules.

### AXM-A30 Analog Input

This module features two 105MHz 16-bit A/D channels. An external clock and trigger can be used to control sampling.

An internal precision clock conditioner provides the functions of jitter cleaning/reconditioning, multiplication, and distribution of a reference clock.

Each clock distribution block includes a programmable divider, a phase synchronization circuit, and a programmable delay. This allows multiple integer-related and phase-adjusted copies of the reference to be distributed to multiple system components.

### Key Features & Benefits

- Analog Input
- Input configuration: Two differential channels using two Analog Devices AD9460 A/D converter
- A/D resolution: 16 bits
- Input range: 3.4V peak-to-peak, centered at 0V, into a 50 ohm load
- External clock input: 3.3V peak-to-peak
- Input clock range: 1-105MHz
- Maximum throughput rate:  
1 channel (max.): 9.5nS (105MHz)  
2 channels (max.): 9.5nS (105MHz)  
A/D trigger: External source, FPGA controlled
- Input clock controller: Precision clock conditioner combines the functions of jitter cleaning/reconditioning, multiplication, and distribution of a reference clock
- Signal-to-noise ratio: 69dB (25°C) typical
- Signal-to noise and distortion: 67dB (25°C) typical
- General purpose I/O: Low voltage TTL



AXM modules attach to PMC Modules with user-configurable FPGAs.

# Extension I/O Modules



## AXM-A30 Analog I/O Extension Modules for PMC FPGA Boards

### Performance Specifications

#### ■ AXM-A30 Analog Input

##### Input configuration

Two differential channels using two Analog Devices AD9460 A/D converter.

##### A/D resolution

16 bits.

##### Input range

3.4V peak-to-peak, centered at 0V, into a 50 ohm load.

##### External clock input:

3.3V peak-to-peak.

##### Input clock range:

1-105MHz.

##### Maximum throughput rate

1 channel (max.): 9.5nS (105MHz).

2 channels (max.): 9.5nS (105MHz).

##### A/D trigger

External source, FPGA controlled.

##### Input clock controller:

Precision clock conditioner combines the functions of jitter cleaning/reconditioning, multiplication, and distribution of a reference clock.

##### Signal-to-noise ratio

69dB (25°C) typical.

##### Signal-to-noise and distortion

67dB (25°C) typical.

General purpose I/O: Low voltage TTL.

#### ■ Physical

Acromag's AXM Series extension modules offer numerous I/O options for Acromag's PMC modules with configurable FPGA. These extension modules plug into the front mezzanine on Acromag's PMC-LX/SX (Virtex@-4 FPGA), and PMC-VLX/VSX/VFX (Virtex-5 FPGA) modules. Analog and digital I/O AXM modules are sold separately.

##### Size

11.5 mm high x 31.0 mm deep x 74.0 mm wide  
(0.453 inches x 1.220 inches x 2.913 inches).

##### Stacking height

5.0 mm (0.197 inches).

##### Weight

41.3 g (1.46 oz).

##### Connectors

Front field I/O: Four SMA PCB jack female receptacle connectors.

*Complies with PMC Specification P1386.1 for a single-width PMC module when installed on a supported PMC module.*

#### ■ Environmental

##### Operating temperature

-0 to 70°C.

##### Storage temperature

-55 to 105°C.

##### Relative humidity

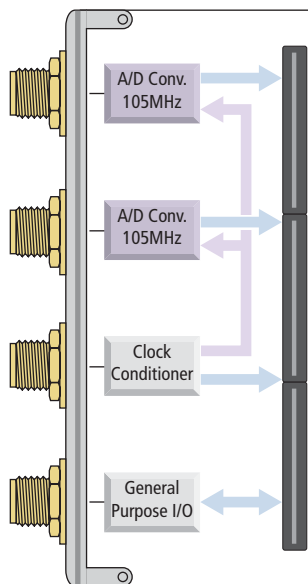
5 to 95% non-condensing.

##### Power

4.5 Watts typical.

##### MTBF

1,972,542 hrs. at 25°C, MIL-HDBK-217F, Notice 2.



### Ordering Information

#### ■ AXM Plug-In I/O Modules

For more information, see [www.acromag.com](http://www.acromag.com).

##### [AXM-A30](#)

2 analog input channels

AXM-??

Custom I/O configurations available, call factory.

#### ■ Accessories

For more information, see [www.acromag.com](http://www.acromag.com).

##### [XMC FPGA Modules](#)

##### [PMC FPGA Modules](#)

ISO9001  
AS9100  MADE IN USA

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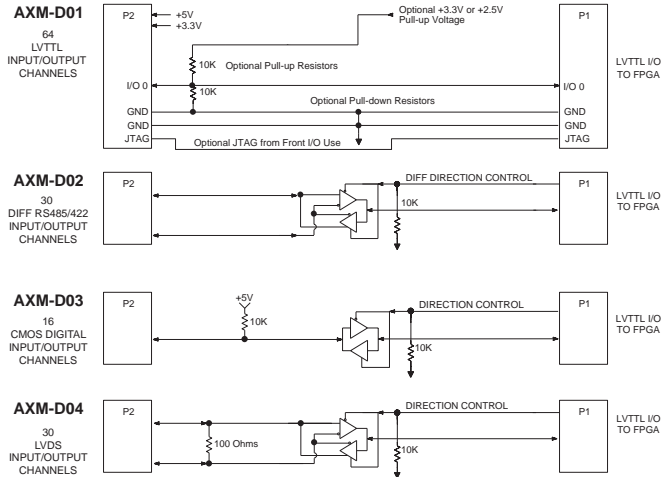
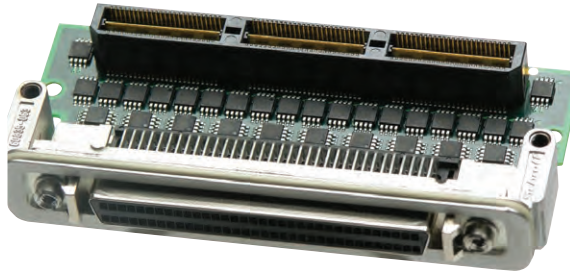
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# Extension I/O Modules



## AXM Series Digital I/O Extension Modules



Plug-In I/O Modules ♦ Choose from four I/O Options ♦ JTAG Support Option

### Description

AXM Series extension modules offer numerous I/O options for Acromag's PMC and XMC modules with configurable FPGAs. These extension modules plug into the front mezzanine on Acromag's I/O compatible FPGAs.

#### AXM-D01 LVTTTL I/O

This module provides 64 LVTTTL I/O channels for straight through I/O. custom modules are available for optional pull-ups, pull-downs, JTAG, and fusted power for front I/O use.

#### AXM-D02 RS-485 Differential I/O

This module provides 30 differential I/O channels. Data direction, either input or output, on each channel is independently controlled. Eight of the channels support programmable change-of-state interrupts. JTAG option.

#### ACR5264 LVDS and RS-485 Differential I/O

This module provides 30 differential I/O channels. Data direction, either input or output, on each channel is independently controlled. Eight of the channels support programmable change-of-state interrupts. 16 LVDS and 14 RS-485 differential I/O channels.

#### AXM-D03 CMOS and RS-485 Differential I/O

This module provides 16 CMOS and 22 RS-485 differential I/O channels. Data direction, either input or output, on each channel is independently controlled. Eight of the channels support programmable change-of-state interrupts.

#### AXM-DX03 CMOS and RS-485 Differential I/O

Same as AXM-D03 above except 16 CMOS and 24 RS-485 differential I/O channels. Provides a replacement for legacy PMC-DX503/2003 FPGA modules when used with PMC/XMC-SLX.

#### AXM-D04 LVDS

This module provides 30 channels of low voltage differential signaling with independently configured direction. Interrupts are programmable on eight of the channels for any bit change of state or level. JTAG option



AXM modules attach to PMC Modules with user-configurable FPGAs.

### Key Features & Benefits

- Various modules allows users to select the Front I/O required for their application.
- Differential RS485/RS422 can be configured for input or output with independent direction control.
- Interface with 5V compliant input/output CMOS channels which can be configured as input or output with independent direction control.
- Low voltage differential signaling can be configured for input or output with independent direction control.
- The EDK board provides the standard Xilinx JTAG interface to allow direct programming of the FPGA and an interface with ChipScope®.
- Example code provides interrupts that are software programmable for any bit Change-Of-State or level on 8 channels.
- Example Design – The example VHDL design, provided in the base board EDK, includes control of all I/O, and eight Change-Of-State interrupts.

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# Extension I/O Modules



## AXM Series Digital I/O Extension Modules

### Performance Specifications

#### AXM-D01

Channel configuration: 64 channel bi-directional LVTTTL signals are independently direction controlled. LVTTTL I/O characteristics: all I/O characteristics are determined by the FPGA.

#### AXM-D02

Channel configuration: 30 bi-directional differential signals with independently configured direction. Channels to the FPGA are buffered using EIA RS485/RS422 line transceivers. Optional JTAG access via front connector.

Differential driver output voltage:

1.5V minimum., 3.3V maximum with 54 ohm load.

#### ACR5264

Channel configuration: 16 channels of low voltage differential signaling with independently configured I/O direction and 14 bi-directional differential signals with independently configured direction.

RS485 channels: Same as AXM-D02

LVDS channels: Same as AXM-D04

#### AXM-D03

Channel configuration: 16 bi-directional CMOS transceivers (input/output direction controlled as pairs of channels) and 22 bi-directional differential signals with independently configured direction.

Differential channels: Same as AXM-D02.

CMOS I/O electrical characteristics:

VoH: 3.8V minimum    Vol: 0.55V maximum

IoH: -32.0mA    IoL: 32.0mA

ViH: 3.5V minimum    ViL: 1.5V maximum

#### AXM-DX03

Same as AXM-D03 above except 16 CMOS and 24 RS-485 differential I/O channels. Provides a replacement for legacy PMC-DX503/2003 FPGA modules when used with PMC/XMC-SLX.

#### AXM-D04

Channel configuration: 30 channels of low voltage differential signaling with independently configured I/O direction. Optional JTAG access via front connector.

LVDS I/O electrical characteristics:

LVDS driver output voltage: 247mV min., 454mV max.

Common mode output voltage: 1.37V max.

LVDS Input Threshold Voltage: -50mV min., 50mV max.

### Physical Dimensions

#### Size

11.5 mm high x 31.0 mm deep x 74.0 mm wide  
(0.453 inches x 1.220 inches x 2.913 inches)

#### Stacking height

8.0 mm (0.315 inches).

#### PMC Compliance

Complies with PMC Specification P1386.1 for a single-width PMC module when attached to the PMC front mezzanine.

#### Connectors

Front field I/O: 68-pin, SCSI-3, female receptacle header (AMP 5787394-7 or equivalent).

### Environmental

#### Operating temperature

-40 to 85°C

#### Storage temperature

-55 to 150°C

#### Relative humidity

5 to 95% non-condensing

#### Power:

1.5W typical (AXM-D02, AXM-D03)

0.6W typical (AXM-D04)

#### MTBF

Hours are at 25°C, MIL-HDBK-217F, Notice 2

AXM-D01: TBD

AXM-D02: 3,559,276 hours

AXM-D03: 3,921,522 hours

AXM-DX03: TBD

AXM-D04: 6,534,197 hours

### Ordering Information

#### AXM Plug-In I/O Modules

##### [AXM-D01](#)

64 bi-directional LVTTTL I/O channels

##### [AXM-D02](#)

30 RS-485 Differential I/O channels

##### [ACR5264](#)

Same as AXM-D02 except 16 LVDS and 14 RS485 I/O channels

##### [AXM-D02-JTAG](#)

Same as AXM-D02 plus JTAG support

##### [AXM-D03](#)

16 CMOS and 22 RS485 differential I/O channels

##### [AXM-DX03](#)

16 CMOS and 24 RS485 differential I/O channels

##### [AXM-D04](#)

30 LVDS I/O channels

##### [AXM-D04-JTAG](#)

Same as AXM-D04 plus JTAG support

##### [AXM-??](#)

Custom I/O configurations available, call factory.

#### Accessories

##### [5025-288](#)

Termination Panel for 68-pin SCSI-3 cable to connect field I/O Signals to the board.

##### [5028-432](#)

Round shielded cable, 34 twisted pairs, SCSI-3 male connector at both ends. Connects model 5025-288 termination panel to the board. 2 meters long.

##### [XMC FPGA Modules](#)

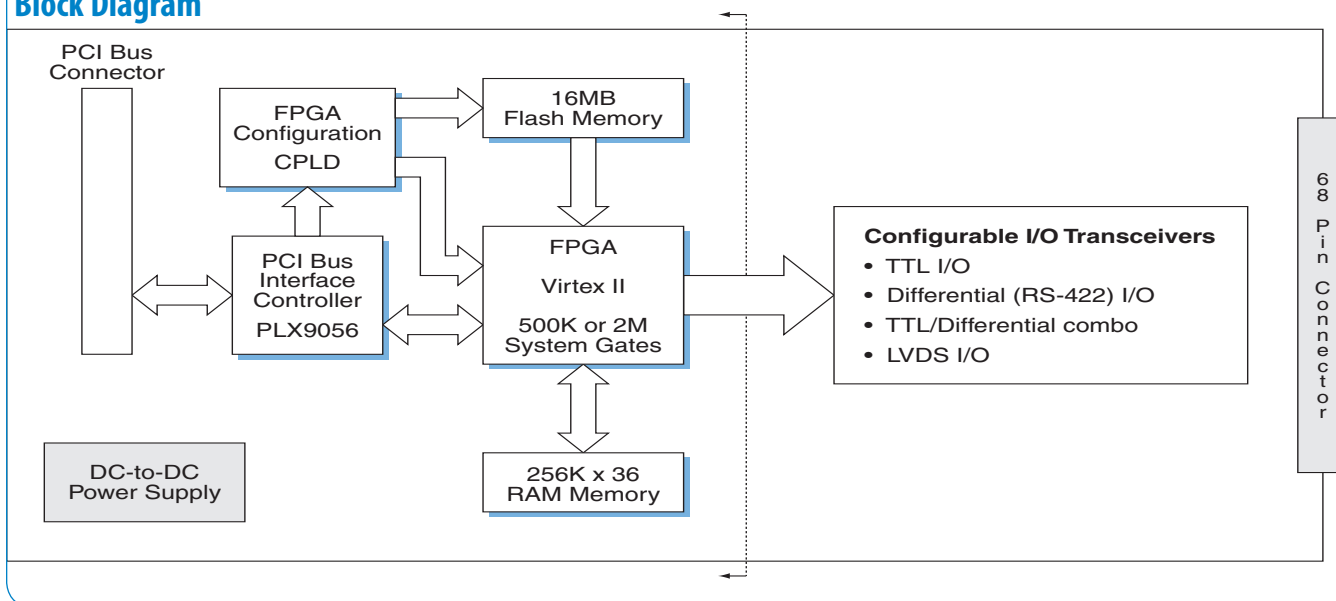
##### [PMC FPGA Modules](#)

ISO9001  
AS9100  MADE IN USA

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## Block Diagram



## Engineering Design Kit

This kit provides you with the basic information required to develop a custom FPGA program for download to the Xilinx FPGA. Utilities help you load VHDL into the FPGA, and to establish DMA transfers between the FPGA and the CPU. It is also recommended that users should be familiar with Xilinx development tools.

Acromag's Engineering Design Kit includes:

- Parts list and location
- Schematics
- Compiled FPGA file
- Example VHDL code provided as selectable blocks of code

Local Bus — example interface between PLX PCI9056 and FPGA

SRAM — example code for read and write transfers to SRAM

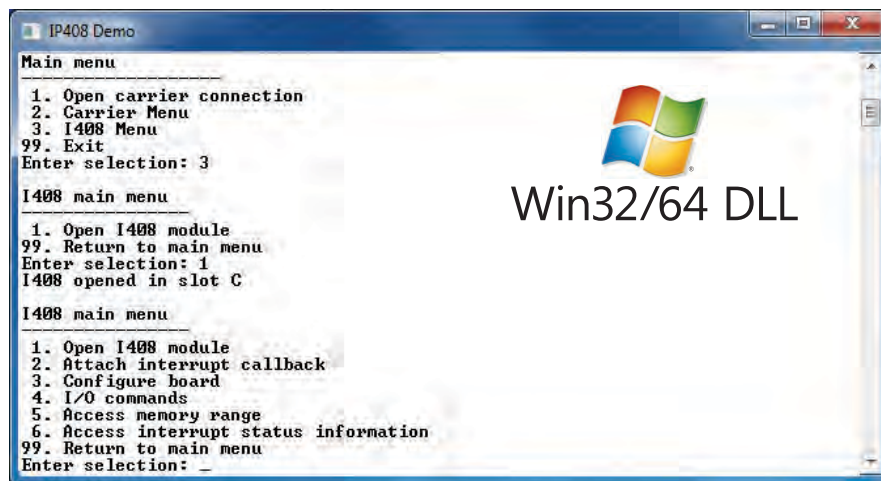
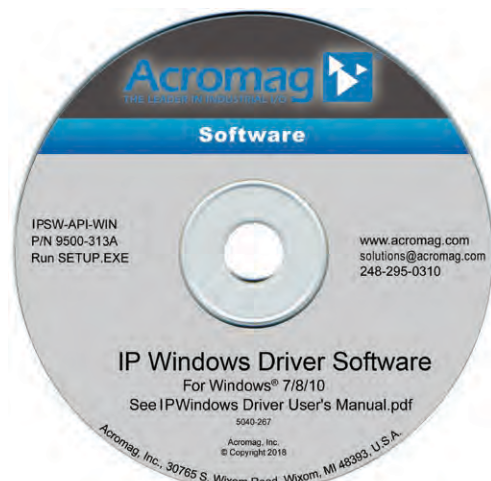
Interrupts — examples of change-of-state monitoring and interrupts to the PCI bus

Field I/O — examples of direction control and I/O read/write capability

Pin definitions — configuration file containing definition of all user I/O pins communicating with the FPGA

# Software Support

## IPSW AcroPack® and Industry Pack Driver Software for Windows® Operating Systems



For Windows 10 / 8 / 7 ♦ Supports Acromag AcroPack & Industry Pack modules & carriers ♦ Includes DLLs

### Description

#### Application Programming Interface

Acromag's software development tools greatly simplify the interface between the I/O boards and your Windows-based application program. These packages provide DLL driver level support for Acromag's line of Industry Pack products. In addition, "C" source demonstration programs provide easy-to-use tools to test the operation of the module.

#### Demonstration Programs

Powerful programs let you fully exercise your hardware before developing the actual application. These diagnostics will save you hours troubleshooting and debugging your applications. You can set addresses, set up registers, read real-world inputs, or drive outputs. The demonstration programs step you through the exact functions that are called in your application.



Windows Embedded  
Standard



Microsoft  
Visual Studio

ISO9001  
AS9100



### Key Features & Benefits

- Easy installation procedure
- Documentation with step-by-step instructions
- Support for active Acromag Industry Pack I/O and Industry Pack FPGA modules and carriers
- Support for 32-bit and 64-bit systems
- Demonstration Programs
- Driver level support for desktop and embedded Windows level programming environments
- Compatible with Windows Embedded Standard applications
- Verifies operation of your I/O boards with a demonstration program to ensure proper hardware performance before attaching your application

### User-Friendly Licensing

Acromag's PCI Windows driver software is provided with a full site license. This allows anyone at your location to use this software without any additional charges. No run-time license is required.

You do not need to order additional software for different models within the family.

### Ordering Information

#### ■ Software

For more information, see [www.acromag.com](http://www.acromag.com).

##### APSW-API-WIN

64-bit and 32-bit Windows® DLL driver and demonstration software for AcroPack Modules and PCIe carriers on CD ROM.

##### IPSW-API-WIN

64-bit and 32-bit Windows® DLL driver and demonstration software for Industry Pack Modules, PCI, and cPCI carriers.

##### IPSW-VME-WIN

64-bit and 32-bit Windows® driver software package for Industry Pack modules with DLLs and demonstration programs for VME carrier models. Works with TS1148 chipset including the XVME-6300 and XVME-6400. Supplied on CD-ROM.

##### IPSW-A7VME-WIN

64-bit and 32-bit Windows software package for Industry Pack modules and VME carriers. Works with Acromag Series XVME6500 and XVME6700 SBCs. Supplied on CD-ROM.

*NOTE: For PMC, XMC, PCI, and cPCI modules and carrier cards support software, please refer to PCISW-API-WIN.*

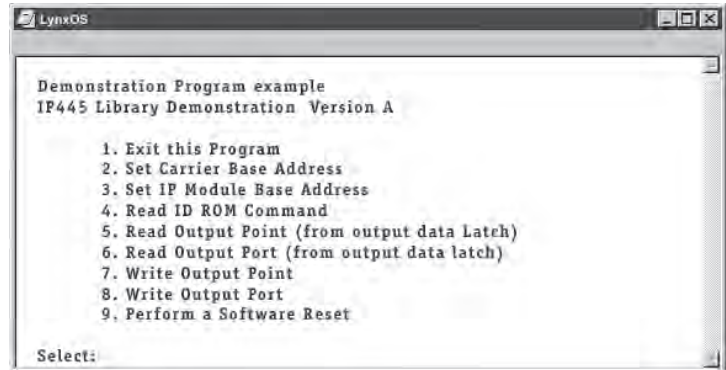
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## Linux® Libraries I/O Function Routines



*This free software utility is available for download from Acromag's website.*

### Simplify interfacing between Acromag I/O boards and your software ♦ Demonstration Program

#### Description

##### IPSW-API-LNX

Support for Industry Pack modules and carriers

##### PCISW-API-LNX

Support for PCI/CompactPCI boards and PMC modules

##### APSW-API-LNX

Support for AcroPack® modules and carriers

#### Application Programming Interface (API)

Acromag's software development tools greatly simplify the interface between the I/O boards and your software application program. The Linux libraries are supplied as "C" source code. These libraries provide easy-to-use function routines that quickly integrate with your application. Function routines are ready for use "as-is," but they are also easily customized for your unique application.

#### Demonstration Program

This powerful program lets you fully exercise the libraries and your hardware before running the actual application. These diagnostics will save you hours troubleshooting and debugging your applications. You can set addresses, set up registers, read real-world inputs, or drive outputs. The demonstration program steps you through the exact functions that are called in your application.

#### Key Features & Benefits

- Easy installation procedure
- Readme files with step-by-step instructions
- Programming tools for most Acromag I/O boards (excludes serial I/O and VME products)
- Demonstration program
- Downloadable at no charge from the Acromag website
- Source code provided to ensure maximum flexibility in implementing your driver
- Verify operation of your I/O modules and carrier cards with a demonstration program to ensure proper hardware operation before attaching your application

#### Ordering Information

*NOTE: This unsupported software is available ONLY by download from Acromag's website.*

##### [IPSW-API-LNX](#)

Linux example libraries for Industry Pack modules and PCI/CompactPCI carrier cards

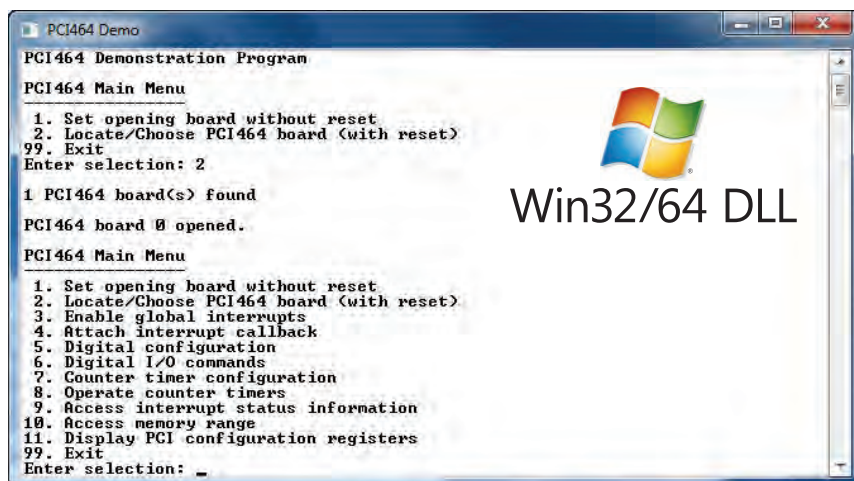
##### [PCISW-API-LNX](#)

Linux example libraries for PCI, CompactPCI, and PMC modules.

##### [APSW-API-LNX](#)

Linux example libraries for AcroPack® modules and carriers.

## PCISW-API-WIN PCI Driver Software for Windows® Operating Systems



For Windows 10 / 8 / 7 / Vista ♦ Supports Acromag XMC, PMC, PCI, CompactPCI cards ♦ Includes DLLs

### Description

#### Application Programming Interface

Acromag's software development tools greatly simplify the interface between the I/O boards and your Windows-based application program. This package provides DLL driver level support for Acromag's complete line of PMC, XMC, PCI and cPCI products. In addition, "C" source demonstration programs provide easy-to-use tools to test the operation of the module.

#### Demonstration Programs

Powerful programs let you fully exercise your hardware before developing the actual application. These diagnostics will save you hours troubleshooting and debugging your applications. You can set addresses, set up registers, read real-world inputs, or drive outputs. The demonstration programs step you through the exact functions that are called in your application.

### Key Features & Benefits

- Easy installation procedure
- Documentation with step-by-step instructions
- Support for all active Acromag I/O PMC, XMC, PCI and CompactPCI boards and all Acromag FPGA PMC, XMC, PCI and CompactPCI boards except PMC CX family Virtex-II boards.
- Support for 32-bit and 64-bit systems
- Demonstration Programs
- Driver level support for desktop and embedded Windows level programming environments
- Compatible with Windows Embedded Standard applications
- Verifies operation of your I/O boards with a demonstration program to ensure proper hardware performance before attaching your application



### Ordering Information

#### ■ Software

For more information, see [www.acromag.com](http://www.acromag.com).

#### PCISW-API-WIN

32 or 64-bit Windows driver software package with DLLs and demonstration programs for PMC, XMC, PCI, and cPCI products. Supplied on CD-ROM.

*NOTE: For Industry Pack module and carrier card support software, please refer to IPSW-API-WIN.*

#### User-Friendly Licensing

Acromag's PCI Windows driver software is provided with a full site license. This allows anyone at your location to use this software without any additional charges. No run-time license is required.

Each package supports all active PCI-based (PMC, XMC, PCI, CompactPCI) products. You do not need to order additional software for different models within the family. (does not support PMC CX family Virtex-II boards)



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## VxWorks® Libraries I/O Function Routines



The VxWorks software libraries provide a simple API to quickly integrate Acromag's I/O boards with your application program.

Supports any CPU target with quick modification ♦ API easily convertible for any operating system

### Description

#### Application Programming Interface (API)

Acromag's software development tools greatly simplify the interface between the I/O boards and your software application program. VxWorks libraries are supplied as "C" source code. These libraries provide easy-to-use function routines that quickly integrate with your application. Function routines are ready for use "as-is," but they are also easily customized for your unique application.

This powerful program lets you fully exercise the libraries and your hardware before running the actual application. These diagnostics will save you hours troubleshooting and debugging your applications. You can set addresses, set up registers, read real-world inputs, or drive outputs. The demonstration program steps you through the exact functions that are called in your application.

#### Target any CPU

Acromag provides direct support for VxWorks when using PowerPC, x86 and 68000 CPU boards. The VxWorks C Library includes support for x86 PCI, MV167 and MV2700 CPU boards. Each library contains detailed information on integrating with the CPU's Board Support Package (BSP). The libraries also include instructions for implementing this software with other manufacturer's CPU board BSPs. Use with Industry Pack carriers from third-party board vendors is also supported.

The IPSW-API-VXW library package offers support for Acromag carriers. Other carriers are compatible, but require some minor modifications. Acromag uses a very innovative modular programming technique. This allows new carrier files to be created without affecting any of the complex IP module files or interrupt service routines.

#### User-Friendly Licensing

Acromag's VxWorks software libraries are provided with a full site license. This allows anyone at your location to use this software without any additional charges. Additionally, no run-time license is required either.

The VxWorks software libraries include support for the full family of boards or modules, not just certain models unless otherwise noted.

### Key Features & Benefits

- Easy installation procedure
- Readme files with step-by-step instructions
- Quickly creates libraries
- Targeted support for Power PC, x86, and 68000 series CPUs
- Supports any CPU target with quick modification
- API easily convertible for any operating system
- Source code provided to ensure maximum flexibility in implementing your application
- Ability to verify operation of your modules and carriers with a demonstration program to ensure proper hardware operation before attaching your application

### Ordering Information

#### APSW-API-VXW

VxWorks software support package for AcroPack modules and carriers.

#### IPSW-A7VME-VXW

VxWorks software support package for Acromag VME SBC Series XVME6500 and XVME6700 when used with Industry Pack modules.

#### IPSW-API-VXW

VxWorks software support package for Industry Pack modules and carriers.

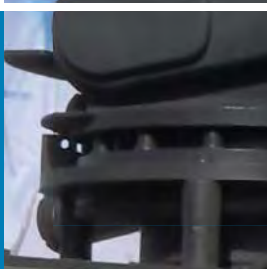
#### PMCSW-API-VXW

VxWorks software support package for XMC, PMC, PCI, and CompactPCI products (supports all Acromag PMC modules and PCI or cPCI boards except IP carriers).

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