

## **Known Differences Between XMC-7AWP and XMC-7A200**

### **Purpose:**

On the following pages is the “Known Differences Between **XMC-7AWP** and existing **XMC-7A200**”. The XMC-7AWP modules Non-Volatile memory can be write protected. The XMC-7A200 Non-Volatile memory cannot be write protected. In order to accomplish this a second XC7A50 FPGA is added to the XMC-7AWP to handle configuration of the 7A200 FPGA without the need for is Non-Volatile flash memory.

The XMC-7AWP module like the XMC-7A200CC module provides an XC7A200 Xilinx reprogrammable FPGA.

### **XMC-7A200 Non-Volatile Memory Write Protection**

Flash device for configuration of the XC7A200 FPGA is not write protected.

### **XMC-7A200 Configuration**

The XC7A200 FPGA connected direct to the PCIe bus. Configuration of the XC7A200 FPGA is from on board flash.

### **XMC-7A200 AXM Connector**

Compatible with Acromag AXM modules. AXM signals configurable as 3.3 volt or 2.5 volt I/O. Contains 44 LVDS pairs, 2 Global Clock pairs, 4 LVTTTL I/O and JTAG.

### **XMC-7AWP Non-Volatile Memory Write Protection**

The boards only flash device for configuration of the XC7A50 FPGA can be write protected.

### **XMC-7AWP Configuration**

The XC7A50 FPGA handles configuration of the XC7A200 FPGA over the PCIe bus. Configuration of the XC7A200 FPGA will only be possible with download of the configuration bitstream from the system over the PCIe bus. The XC7A200 FPGA does not connect to the PCIe bus.

### **XMC-7AWP AXM Connector**

Not compatible with Acromag AXM modules. AXM signals forced to 2.5 volt I/O standard. AXM +5 volt pins are not driven with 5 volts. Contains 44 LVDS pairs, 2 Global Clock pairs, 4 LVTTTL I/O and JTAG.