VPX4812A/4814A

Single-Slot 3U VPX Bus
XMC Carrier Card with P16 Support
VPX Switch Card

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 General Information

The VPX4812A is an XMC Carrier Card Module in the 3U VPX form factor, targeted for processing, communications, and display applications in the commercial, military, and aerospace markets.

The VPX4812A provides support for Rear I/O connections from the XMC P16 connector. The TRANS-V112 is a development Rear Transition Module for the VPX4812A used to bring out Rear I/O connections through the backplane.

The VPX4812A supports up to four VPX Fat Pipe (x4) connections to other cards in the system at Gen 2.0 speeds. The VPX4812A can be used as a switch card allowing an upstream Fat Pipe or Double Fan Pipe connection – typically to a CPU – to communicate with up to three downstream Fat Pipe connections or a single Double Fat Pipe connection.

The VPX4812A also provides support for a VPX Double Fat Pipe (x8) connection to an XMC card at Gen 2.0 speeds.

The VPX4814A disconnects the PCIe connection on the fourth bottom-most Fat Pipe of P1 allowing it to be used in systems with an Ethernet control plane interface. This provides the VPX4814A with the ability to be used as an XMC Carrier Card in the majority of the standard OpenVPX profiles.

The information and features for the VPX4812A listed in this manual are also applicable to the VPX4814A model with the exception of the PCIe connection noted previously.

Key Features

- 24-Channel 5-Port PCI Express Gen. 2.0 Switch
- The XMC site is PCIe 8-Lanes Gen. 2.0
- Module conforms to VPX Spec. VITA 46.0, 46.4, and 46.9
- The XMC site supports X24s+X8d+X12d I/O mapping (VITA 46.9)
- 16 Lanes PCI Express to backplane (VITA 46.0 and 46.4)
- Supports Non-Transparent Bridging Applications
- 3U VPX form factor supporting OpenVPX/VITA 65
- Air and conduction cooled variants available
- REDI covers supporting VITA 48 available

Introduction

The VPX4812A has two primary functions that can be utilized in a VPX system simultaneously.

1. XMC Carrier Card – The VPX4812A supports a Double Fat Pipe (x8) connection from an XMC module to the on-board PCIe switch. The voltage used to power the XMC module can be toggled between 5V or 12V using a DIP switch located on the VPX4812A.

2. VPX Switch Card – The VPX4812A contains a 24-lane 5-port PCIe switch capable of Gen 2.0 speeds. When utilizing the VPX4812A as a switch card, a CPU module configured to be an upstream port can communicate with up to three downstream VPX cards in the system as well as an XMC module on the 4812A.

The VPX4812A supports the use of non-transparent bridging using the on-board PCIe switch. By utilizing non-transparent bridging (NTB), the VPX4812A can be used to implement multi-hosted topologies including intelligent adapter cards, dual-host systems with redundancy, and even blade server systems.

Module and Backplane Profiles

The VPX4812A conforms to OpenVPX switch module profile MOD3-SWH-4F-16.4.5-2. This switch profile is intended to be used in the OpenVPX backplane profile BKP3-CEN06-15.2.12-n shown below.

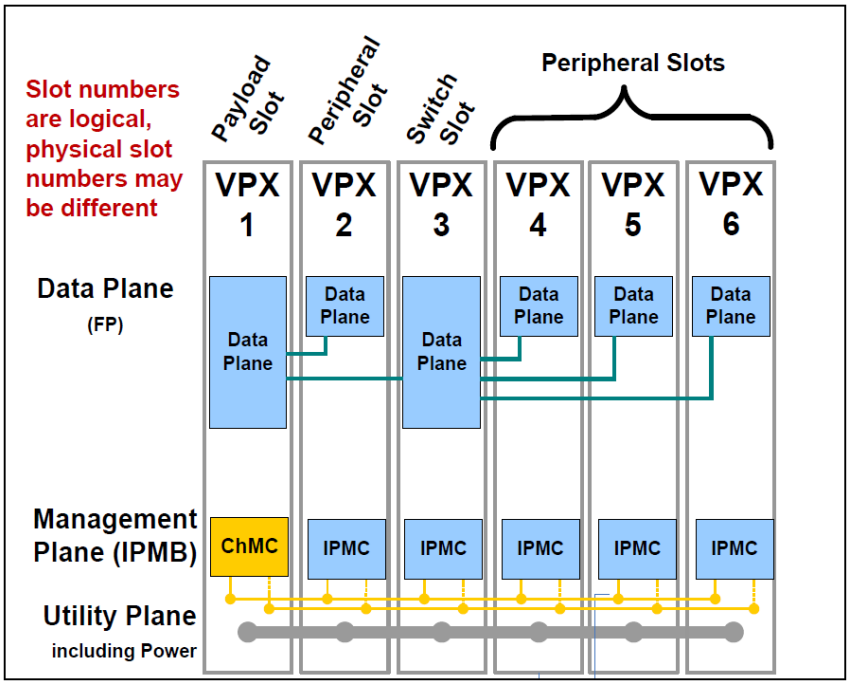


Figure 1: OpenVPX Backplane Profile BKP3-CEN06-15.2.12-n

The VPX4812A also conforms to OpenVPX peripheral module profile MOD3-PER-1F-14.3.2 when used as an XMC carrier card. Typically, this peripheral profile can be used in a wide range of OpenVPX backplane profiles but due to the PCIe switch connections on P1, the VPX4812A may be incompatible with profiles that contain other plane interfaces on P1. Check the VPX connector pinout in this manual against the intended backplane topology to ensure compatibility.

The VPX4814A disconnects the lower four PCIe lanes on P1 while retaining all of the XMC carrier card functionality of the VPX4812A. This allows it to be used as an XMC carrier card in a wider range of OpenVPX backplane profiles including profiles that contain Ethernet control plane interfaces on P1.

Build Levels

The VPX4812A/14A is available in three electrically compatible build levels, each of which is carefully tailored to a particular set of requirements and environments. All three levels fully support the power and versatility of VPX, so no matter how large or diversified your project, absolute compatibility is assured at all stages of development. The three build levels have three basic mechanical configurations, both in accordance with the VITA 46.0 VPX standard and the VITA 48 REDI standard:

1. Air (convection) cooled modules are intended for use in standard industrial chassis.

2. Conduction-cooled modules are intended for use in sealed Air Transportable Racking (ATR) and other conduction-cooled environments.

3. REDI cover, Conduction-cooled modules are intended for use in sealed Air Transportable Racking (ATR) and other conduction-cooled environments.

2.0 Ordering Information

Available Models	
VPX4812A-LF	VPX4812A Air-cooled Model
VPX4812A-CC-LF	VPX4812A Conduction-cooled Model
VPX4812A-REDI-LF	VPX4812A REDI Model
VPX4814A-LF	VPX4814A Air-cooled Model
VPX4814A-CC-LF	VPX4814A Conduction-cooled Model
VPX4814A-REDI-LF	VPX4814A REDI Model

3.0 Preparation For Use

Unpacking and Inspection

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened.

If the carrier's agent is absent when the carton is opened, and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

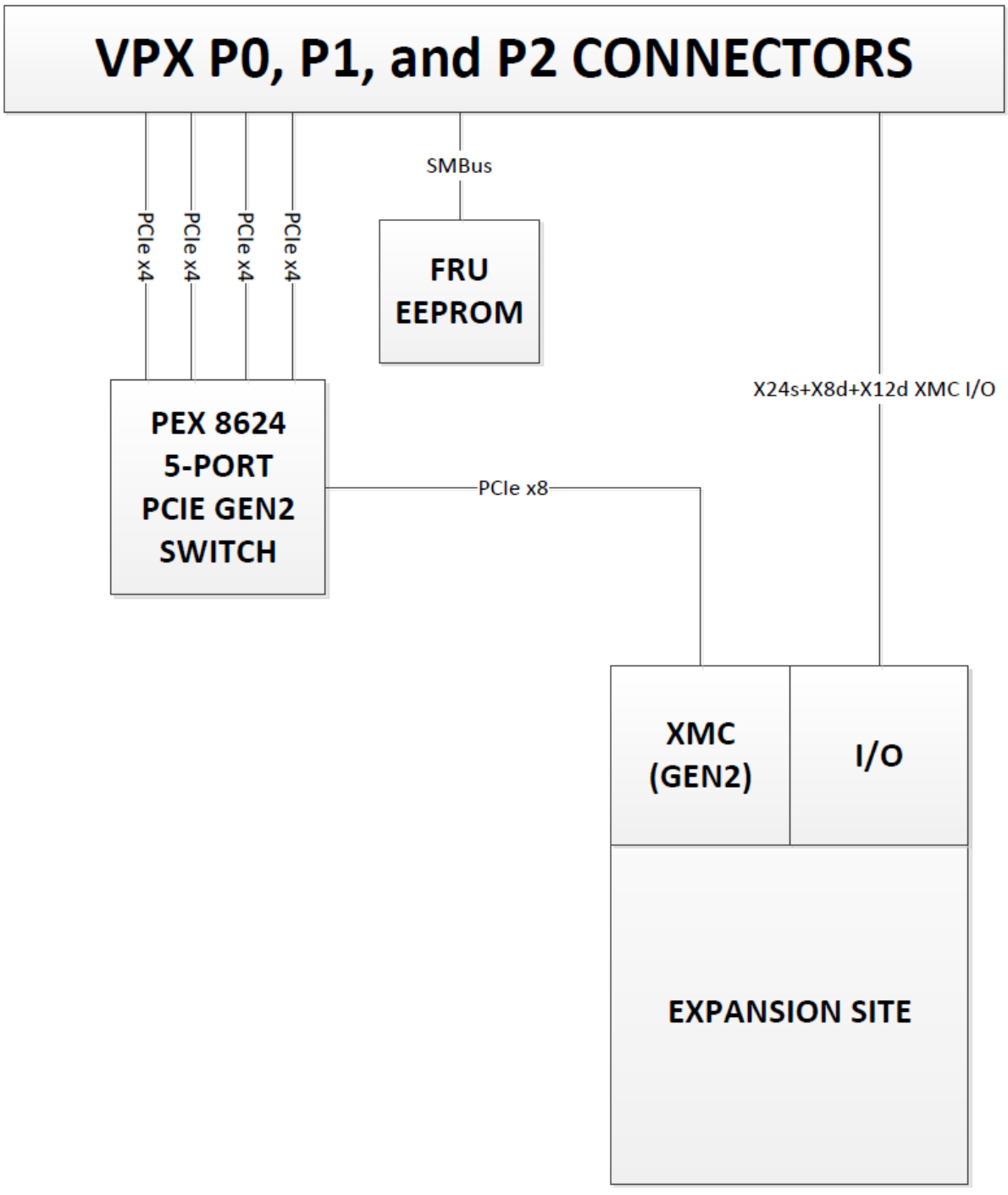
The board utilizes static sensitive components and should only be handled at a static-safe workstation.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

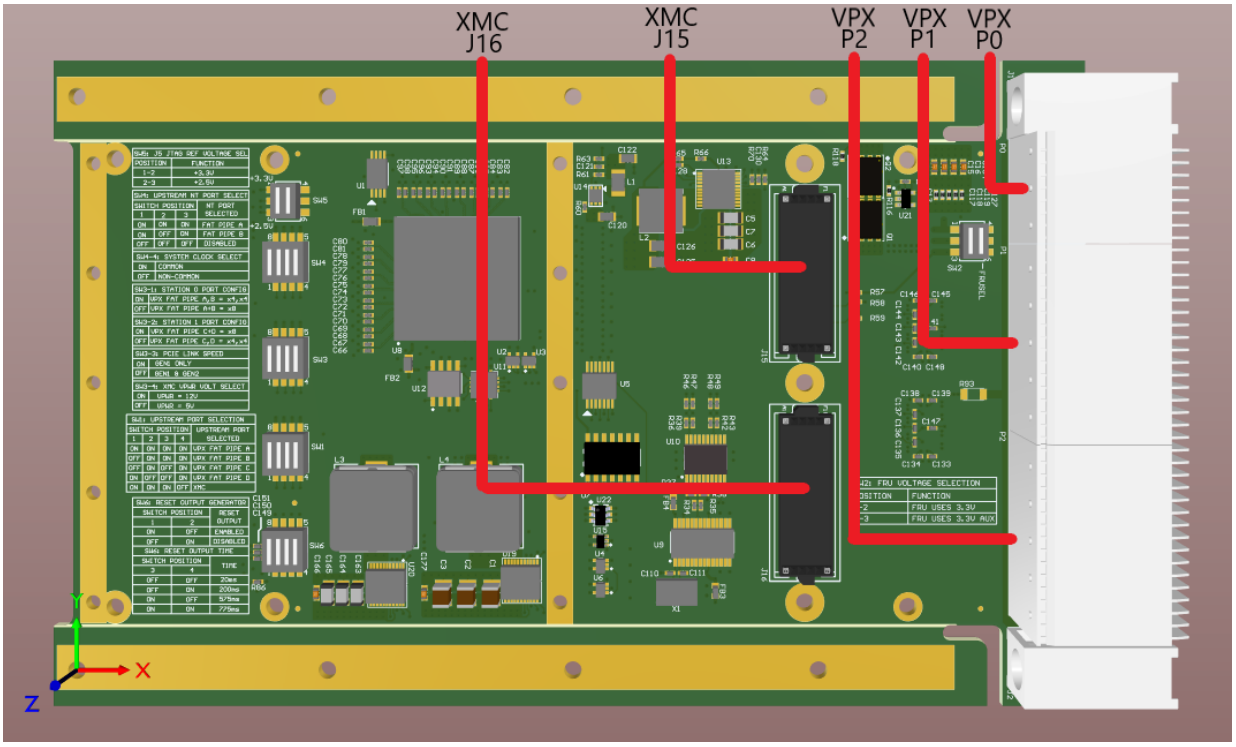
Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics.

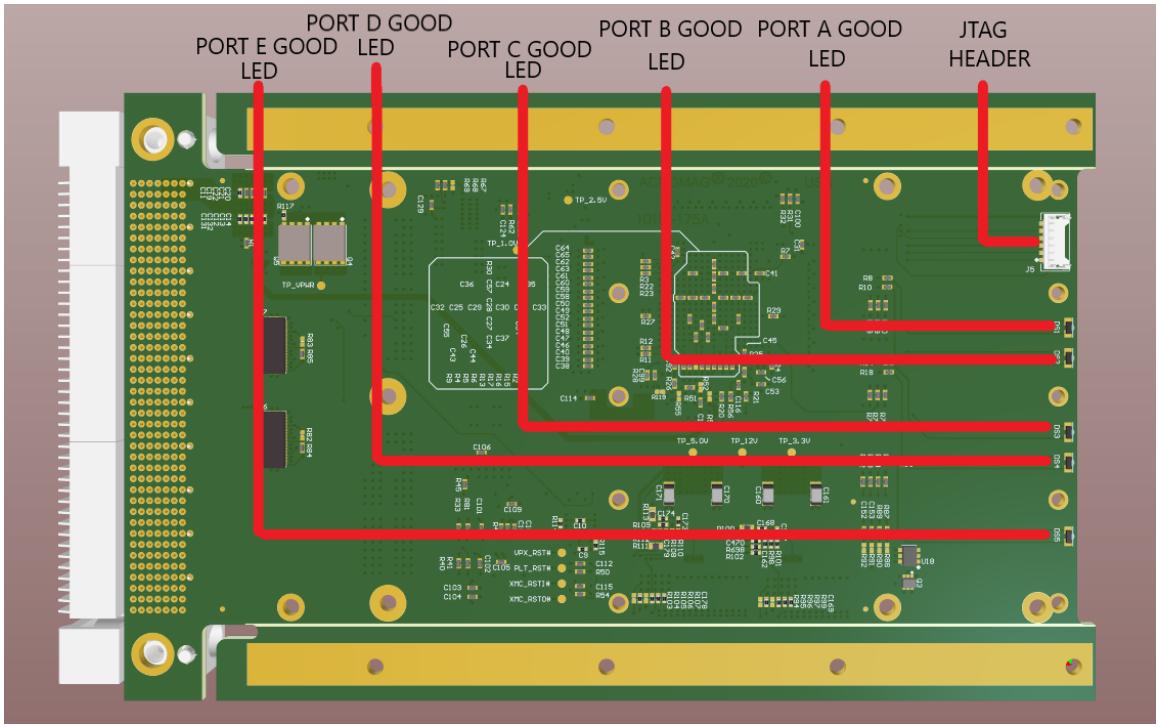
If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

4.0 Operational Block Diagram



5.0 Board Layout





6.0 Connectors

P0 Connector

P0 Wafer	A	B	C	D	E	F	G
1	NC	NC	NC	NC	+12 V	+12 V	+12 V
2	NC	NC	NC	NC	+12 V	+12 V	+12 V
3	NC	NC	NC	NC	NC	NC	NC
4	NVMRO	SYS_RST#	GND	-12V_AUX	GND	NC	NC
5	SMB_DATA	SMB_CLK	GND	+3.3V AUX	GND	NC	NC
6	GA0#	GA1#	GND	+12V_AUX	GND	GA2#	GA3#
7	NC	NC	GND	NC	NC	GND	NC
8	GND	NC	NC	GND	REF_CLK P	REF_CLK N	GND

 # = Low true signal

P1 Connector

P1 Wafer	A	B	C	D	E	F	G
1	PCIE_VPX_P0_RXP	PCIE_VPX_P0_RXN	GND	PCIE_VPX_P0_TXP	PCIE_VPX_P0_TXN	GND	NC
2	GND	PCIE_VPX_P1_RXP	PCIE_VPX_P1_RXN	GND	PCIE_VPX_P1_TXP	PCIE_VPX_P1_TXN	GND
3	PCIE_VPX_P2_RXP	PCIE_VPX_P2_RXN	GND	PCIE_VPX_P2_TXP	PCIE_VPX_P2_TXN	GND	NC
4	GND	PCIE_VPX_P3_RXP	PCIE_VPX_P3_RXN	GND	PCIE_VPX_P3_TXP	PCIE_VPX_P3_TXN	GND
5	PCIE_VPX_P4_RXP	PCIE_VPX_P4_RXN	GND	PCIE_VPX_P4_TXP	PCIE_VPX_P4_TXN	GND	NC
6	GND	PCIE_VPX_P5_RXP	PCIE_VPX_P5_RXN	GND	PCIE_VPX_P5_TXP	PCIE_VPX_P5_TXN	GND
7	PCIE_VPX_P6_RXP	PCIE_VPX_P6_RXN	GND	PCIE_VPX_P6_TXP	PCIE_VPX_P6_TXN	GND	NC
8	GND	PCIE_VPX_P7_RXP	PCIE_VPX_P7_RXN	GND	PCIE_VPX_P7_TXP	PCIE_VPX_P7_TXN	GND
9	PCIE_VPX_P8_RXP	PCIE_VPX_P8_RXN	GND	PCIE_VPX_P8_TXP	PCIE_VPX_P8_TXN	GND	NC
10	GND	PCIE_VPX_P9_RXP	PCIE_VPX_P9_RXN	GND	PCIE_VPX_P9_TXP	PCIE_VPX_P9_TXN	GND
11	PCIE_VPX_P10_RXP	PCIE_VPX_P10_RXN	GND	PCIE_VPX_P10_TXP	PCIE_VPX_P10_TXN	GND	NC
12	GND	PCIE_VPX_P11_RXP	PCIE_VPX_P11_RXN	GND	PCIE_VPX_P11_TXP	PCIE_VPX_P11_TXN	GND
13	PCIE_VPX_P12_RXP[1]	PCIE_VPX_P12_RXN[1]	GND	PCIE_VPX_P12_TXP[1]	PCIE_VPX_P12_TXN[1]	GND	NC
14	GND	PCIE_VPX_P13_RXP[1]	PCIE_VPX_P13_RXN[1]	GND	PCIE_VPX_P13_TXP[1]	PCIE_VPX_P13_TXN[1]	GND
15	PCIE_VPX_P14_RXP[1]	PCIE_VPX_P14_RXN[1]	GND	PCIE_VPX_P14_TXP[1]	PCIE_VPX_P14_TXN[1]	GND	NC
16	GND	PCIE_VPX_P15_RXP[1]	PCIE_VPX_P15_RXN[1]	GND	PCIE_VPX_P15_TXP[1]	PCIE_VPX_P15_TXN[1]	GND

Note 1: These signals are unconnected on all VPX4814A models.

RX is defined as a signal that is an input to the VPX4812A.
TX is defined as a signal that is an output from the VPX4812A.

P2 Connector

P2 Wafer	A	B	C	D	E	F	G
1	J16_SIO11_P	J16_SIO11_N	GND	J16_SIO10_P	J16_SIO10_N	GND	NC
2	GND	J16_SIO9_P	J16_SIO9_N	GND	J16_SIO8_P	J16_SIO8_N	GND
3	J16_SIO7_P	J16_SIO7_N	GND	J16_SIO6_P	J16_SIO6_N	GND	NC
4	GND	J16_SIO5_P	J16_SIO5_N	GND	J16_SIO4_P	J16_SIO4_N	GND
5	J16_SIO3_P	J16_SIO3_N	GND	J16_SIO2_P	J16_SIO2_N	GND	NC
6	GND	J16_SIO1_P	J16_SIO1_N	GND	J16_SIO0_P	J16_SIO0_N	GND
7	J16_DP01_N	J16_DP01_P	GND	J16_DP00_N	J16_DP00_P	GND	NC
8	GND	J16_DP03_N	J16_DP03_P	GND	J16_DP02_N	J16_DP02_P	GND
9	J16_DP11_N	J16_DP11_P	GND	J16_DP10_N	J16_DP10_P	GND	NC
10	GND	J16_DP13_N	J16_DP13_P	GND	J16_DP12_N	J16_DP12_P	GND
11	J16_DP05_N	J16_DP05_P	GND	J16_DP04_N	J16_DP04_P	GND	NC
12	GND	J16_DP07_N	J16_DP07_P	GND	J16_DP06_N	J16_DP06_P	GND
13	J16_DP09_N	J16_DP09_P	GND	J16_DP08_N	J16_DP08_P	GND	NC
14	GND	J16_DP15_N	J16_DP15_P	GND	J16_DP14_N	J16_DP14_P	GND
15	J16_DP17_N	J16_DP17_P	GND	J16_DP16_N	J16_DP16_P	GND	NC
16	GND	J16_DP19_N	J16_DP19_P	GND	J16_DP18_N	J16_DP18_P	GND

J15 Connector

	A	B	C	D	E	F
1	PCIE_XMC_P0_RXP	PCIE_XMC_P0_RXN	+3.3V	PCIE_XMC_P1_RXP	PCIE_XMC_P1_RXN	VPWR
2	GND	GND	NC	GND	GND	XMC_RSTI#
3	PCIE_XMC_P2_RXP	PCIE_XMC_P2_RXN	+3.3V	PCIE_XMC_P3_RXP	PCIE_XMC_P3_RXN	VPWR
4	GND	GND	JTAG_TCK	GND	GND	XMC_RSTO#
5	PCIE_XMC_P4_RXP	PCIE_XMC_P4_RXN	+3.3V	PCIE_XMC_P5_RXP	PCIE_XMC_P5_RXN	VPWR
6	GND	GND	JTAG_TMS	GND	GND	+12V
7	PCIE_XMC_P6_RXP	PCIE_XMC_P6_RXN	+3.3V	PCIE_XMC_P7_RXP	PCIE_XMC_P7_RXN	VPWR
8	GND	GND	JTAG_TDI	GND	GND	-12V_AUX
9	NC	NC	NC	NC	NC	VPWR
10	GND	GND	JTAG_TDO	GND	GND	GA0#
11	PCIE_XMC_P0_TXP	PCIE_XMC_P0_TXN	NC	PCIE_XMC_P1_TXP	PCIE_XMC_P1_TXN	VPWR
12	GND	GND	GA1#	GND	GND	NC
13	PCIE_XMC_P2_TXP	PCIE_XMC_P2_TXN	+3.3V_AUX	PCIE_XMC_P3_TXP	PCIE_XMC_P3_TXN	VPWR
14	GND	GND	GA2#	GND	GND	SMB_DATA
15	PCIE_XMC_P4_TXP	PCIE_XMC_P4_TXN	NC	PCIE_XMC_P5_TXP	PCIE_XMC_P5_TXN	VPWR
16	GND	GND	NVRAM_LOCK	GND	GND	SMB_CLK
17	PCIE_XMC_P6_TXP	PCIE_XMC_P6_TXN	NC	PCIE_XMC_P7_TXP	PCIE_XMC_P7_TXN	NC
18	GND	GND	NC	GND	GND	NC
19	PCIE_VPX REF_CLK P	PCIE_VPX REF_CLK N	NC	NC	ROOT0#	NC

 # = Low true signal

J16 Connector

	A	B	C	D	E	F
1	J16_DP00_P	J16_DP00_N	NC	J16_DP01_P	J16_DP01_N	NC
2	GND	GND	NC	GND	GND	NC
3	J16_DP02_P	J16_DP02_N	NC	J16_DP03_P	J16_DP03_N	NC
4	GND	GND	NC	GND	GND	NC
5	J16_DP04_P	J16_DP04_N	NC	J16_DP05_P	J16_DP05_N	NC
6	GND	GND	NC	GND	GND	NC
7	J16_DP06_P	J16_DP06_N	NC	J16_DP07_P	J16_DP07_N	NC
8	GND	GND	J16_SIO10_N	GND	GND	J16_SIO11_N
9	J16_DP08_P	J16_DP08_N	J16_SIO10_P	J16_DP09_P	J16_DP09_N	J16_SIO11_P
10	GND	GND	J16_SIO8_N	GND	GND	J16_SIO9_N
11	J16_DP10_P	J16_DP10_N	J16_SIO8_P	J16_DP11_P	J16_DP11_N	J16_SIO9_P
12	GND	GND	J16_SIO6_N	GND	GND	J16_SIO7_N
13	J16_DP12_P	J16_DP12_N	J16_SIO6_P	J16_DP13_P	J16_DP13_N	J16_SIO7_P
14	GND	GND	J16_SIO4_N	GND	GND	J16_SIO5_N
15	J16_DP14_P	J16_DP14_N	J16_SIO4_P	J16_DP15_P	J16_DP15_N	J16_SIO5_P
16	GND	GND	J16_SIO2_N	GND	GND	J16_SIO3_N
17	J16_DP16_P	J16_DP16_N	J16_SIO2_P	J16_DP17_P	J16_DP17_N	J16_SIO3_P
18	GND	GND	J16_SIO0_N	GND	GND	J16_SIO1_N
19	J16_DP18_P	J16_DP18_N	J16_SIO0_P	J16_DP19_P	J16_DP19_N	J16_SIO1_P

J5 Connector – JTAG Header

Pin Number	Description
1	JTAG_TDI
2	JTAG_TDO
3	GND
4	JTAG_TCK
5	JTAG_TMS
6	JTAG_VREF

7.0 Switch Settings

The following describes the VPX4812A switches with their default positions and their functions.

SW1 – Upstream Port Selection				
Switch Position				Selected Upstream Port
1	2	3	4	
ON	**ON**	**ON**	**ON**	**VPX Fat Pipe A (default)**
OFF	ON	ON	ON	VPX Fat Pipe B
OFF	ON	OFF	ON	VPX Fat Pipe C
ON	OFF	OFF	ON	VPX Fat Pipe D
ON	ON	ON	OFF	XMC

SW2 (FRUSEL)	**1-2 (default)**	FRU uses 3.3V
	2-3	FRU uses 3.3V_AUX
	4-5	Unused
	5-6	Unused

SW3-1 (STATION 0 PORT CONFIG)	**ON (default)**	VPX Fat Pipe A = x4, VPX Fat Pipe B = x4
	OFF	VPX Fat Pipe A = x8, VPX Fat Pipe B = Disabled

SW3-2 (STATION 1 PORT CONFIG)	ON	VPX Fat Pipe C = x8, VPX Fat Pipe D = Disabled
	OFF (default)	VPX Fat Pipe C = x4, VPX Fat Pipe D = x4

SW3-3 (PCIE LINK SPEED)	ON	Force Gen 1.0 Speed Only
	OFF (default)	Allow Gen 1.0 & Gen 2.0 Speeds

SW3-4 (XMC VPWR VOLT SELECT)	ON	VPWR = +12V
	OFF (default)	VPWR = +5V

SW4-1:3 – Upstream NT Port Selection			
Switch Position			Selected NT Upstream Port
1	2	3	
ON	ON	ON	VPX Fat Pipe A
ON	OFF	ON	VPX Fat Pipe B
OFF	**OFF**	**OFF**	**NT Mode Disabled (default)**

Note: In addition to the switch configuration, there are settings for the PEX8624 that must be programmed to the on-board EEPROM device to enable Non-Transparent Mode.

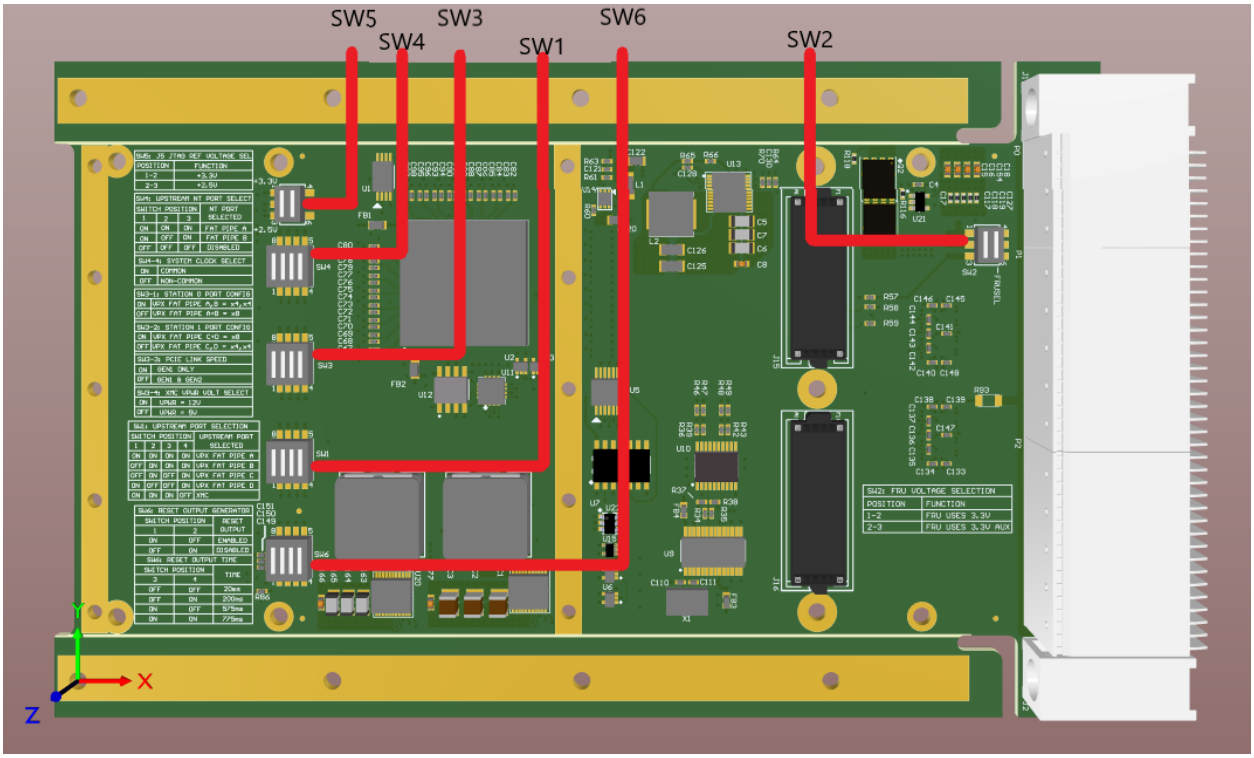
SW4-4 (SYSTEM CLOCK SELECT)	ON	**(Common)** Uses the 100MHz reference clock pins on the VPX bus generated by the CPU board for PCIe timing. (Pins E8 & F8 on the VPX P0 connector)
	OFF (default)	**(Non-Common)** Uses the 100MHz reference clock generated on board for PCIe timing.

Note: Best system stability may be achieved with the use of a 100MHz common clock connection from the SBC, especially at Gen 2.0 link speeds. If the system does not provide a common clock, then non-common clock mode must be used.

SW5 (JTAG VREF SELECT)	**1-2 (default)**	JTAG_VREF = +3.3V
	2-3	JTAG_VREF = +2.5V
	4-5	Unused
	5-6	Unused

Configuration Switch SW6			
Function	**1**	**2**	**Description**
System Reset Delay Generator	ON	OFF	Enabled
	OFF	**ON**	**Disabled (default)**
	3	**4**	**Description**
System Reset Delay Time	**OFF**	**OFF**	**20ms (default)**
	OFF	ON	200ms
	ON	OFF	575ms
	ON	ON	775ms

Note: Configuration Switch SW6 is used to configure the on-board system reset delay circuit. When enabled, the VPX SYSRESET signal will be held down on power-up for a configurable amount of time. This can be used to allow extra time for a particularly large FPGA program to load before reset is de-asserted, for instance.



Front Panel Layout

VPX4812A Front Panel

On the front panel of air-cooled VPX4812A assemblies, there are 5 port status LED's. The first four LED's indicate the PCIe link status for each of the four Fat Pipe connections to other slots on the VPX backplane. The fifth LED on the front panel indicates the PCIe link status of an XMC module connected to the VPX4812A. The table below describes what the LED On/Off patterns indicate about the corresponding port states.

Port Status LED On/Off Patterns, by State

State	LED Pattern
Link is down	Off
Link is up, Gen 2.0 speed, all Lanes are up	On
Link is up, Gen 2.0 speed, reduced Lanes are up	Blinking, 0.5 seconds On, 0.5 seconds Off
Link is up, Gen 1.0 speed, all Lanes are up	Blinking, 1.5 seconds On, 0.5 seconds Off
Link is up, Gen 1.0 speed, reduced Lanes are up	Blinking, 0.5 seconds On, 1.5 seconds Off

8.0 Handling

Modules should be handled in ESD-safe work areas in order to prevent damage to sensitive components from electrostatic discharges. These areas must be designed and maintained to prevent ESD damage.

ESD Safe Work Area Guidelines

1. Module should be handled at properly designated work areas only.

2. Designated ESD safe work areas must be checked periodically to ensure their continued safety from ESD. The areas should be monitored for the following:
    a. Proper grounding methods.
    b. Static dissipation of work surfaces.
    c. Static dissipation of floor surfaces.
    d. Operation of ion blowers and ion air guns.

3. Designated work areas must be kept free of static generating materials such as Styrofoam, vinyl, plastic, fabrics, or any other static generating materials.

4. Work areas must be kept clean and neat in order to prevent contamination of the work area.

5. Modules should be handled by the edges. Avoid touching component leads.

    NOTE: *When not installed in a system, modules must be enclosed in shielded bags or boxes. There are three types of ESD protective enclosure materials this module was shipped in an approved ESD bag.*

6. Whenever handling the module, the operator must be properly grounded by one of the following:
    a. Wearing a wrist strap connected to earth ground.
    b. Wearing heel grounders and have both feet on a static dissipative floor surface.

7. Stacking of modules should be avoided to prevent physical damage.

9.0 Installation

IMPORTANT: The VPX4812A/VPX4814A has been specifically design for use with 3U VPX backplanes and my not be compatible with some 6U backplanes. Plugging the board into an unsupported 6U VPX backplane may cause permanent damage.

Consult the enclosure documentation to ensure that the VPX4812A's power requirements are compatible with those supplied by the backplane.

Board Keying

The 3U VPX backplane specification requires all backplane slots to have two guide pins: one above the J0 connector and one below the J2 connector. As well as providing correct alignment, these pins are keyed to prevent cards from being inserted into incorrect backplane slot(s) to avoid electrical incompatibility.

The VPX4812A has receptacles for these guide pins (see the Connectors section). By default, these are not keyed. Please contact the factory to discuss keying requirements.

Installation Notes

1. Keying may dictate the backplane slot(s) into which the VPX4812A can be inserted.
2. Air-cooled versions have an ejector handle to ensure that the backplane connectors mate properly with the backplane. The captive screws at the top and bottom of the front panel allow the VPX4812A to be tightly secured in position, which provides continuity with system chassis ground.
3. Conduction-cooled and REDI versions have screw driven wedge locks at the top and bottom of the board to provide the necessary mechanical/thermal interface. Correct adjustment requires a calibrated torque wrench set to between 0.6 and 0.8 Nm.

10.0 Specifications

Physical

Height:	100.00 mm (3.937 in.)
Width:	160.00 mm (6.299 in.)
Board Thickness:	1.575 mm (0.062 in.)
Unit Weight (air-cooled):	5.10 Oz (0.14 Kg)
Unit Weight (conduction-cooled):	8.34 Oz (0.24 Kg)
Unit Weight (REDI):	12.37 Oz (0.35 Kg)

Front Panel

VPX4812A-LF and VPX4814A-LF front panel is 1.0" based on VITA 48.1. Please contact factory for IEEE 1101.10 1.0" and 0.8" front panel options.

Power Requirements

The VPX4812A is aligned with the latest power distribution recommendations from VITA 65.0-2019 which states that Plug-In Modules should only use VS1 (12V), 3.3V_AUX, and VBAT as power inputs from the backplane and derive all other voltage rails from that. The VPX4812A/VPX4814A does not utilize VS2 (3.3V) or VS3 (5V) from the backplane.

Power Consumption

No XMC Card Installed:

+3.3V (VS2):	Unused
+5V (VS3):	Unused
+12V (VS1):	0.4A typ. 1.0A max.

XMC Card Installed[1]:

+3.3V (VS2):	Unused
+5V (VS3):	Unused
+12V (VS1):	20A max. [2]
VPWR (12V):	8A[3]
VPWR (5V):	8A[3]

Note 1: The power supplied to the XMC card can be toggled between 5V or 12V depending on the card's requirements.

Note 2: The current carrying capacity of the VPX connector interface is the limiting factor for power delivery.

Note 3: The limiting factor is the current carrying capacity of the XMC connectors. With 8 VPWR pins rated @1A per pin, the maximum current draw capability is 8A.

Caution

If VPWR is set to 12V, you must ensure that the XMC card is capable of handling a 12V supply voltage. If the XMC card is not capable of handling a 12V supply voltage, ensure that the VPWR switch is set to supply 5V.

Auxiliary Supply

The following functions may be powered from the 3.3V Auxiliary supply (VPX +3.3V_AUX line):

FRU EEPROM
TEMP SENSOR

Power-Up/Reset Sequence

Upon the +12V (VS1) rail reaching 90% (10.8V), the on-board regulators are enabled to generate the required voltages on the board. Once all of the on-board regulators' outputs are stable and the backplane SYSRST# signal is de-asserted, the on-board circuitry will be taken out of reset.

The VPX4812A/VPX4814A contains an optional, configurable power-up reset delay circuit. If enabled, the circuit will assert the backplane SYSRST# signal for a configurable length of time determined by the configuration of SW6. This is intended to be used in situations where a device in the system requires longer than the 100ms requirement of the PCI Express specification to load and configure itself for enumeration.

Bus Compliance

VITA 46.0, 46.4, 46.9, 48 and 65
MIL Spec 217-F MTBF – TBD

Form Factor

3U VPXbus 3.94" (100mm) x 6.3" (160mm)

Flammability

The circuit board is made by an UL recognized manufacturer and has a flammability rating of UL94V-1.

Environmental

Caution

The VPX4812A requires air-flow of at least 200 linear-feet/minute for the **air cooled version**, plus what is required for an XMC device installed on this module. If the **conduction cooled** version is operating on an extender card, it requires air-flow of at least 300 linear-feet/minute across it. Versions using the **REDI covers** must not be operated outside of a fully configured and fully installed conduction cooled REDI system.

Thermal

	OPERATING	NON-OPERATING
Air-cooled	0° to 70°C*	-40° to 85°C
Conduction-cooled	-40° to 85°C*[1]	-40° to 85°C
REDI Cover, Conduction-cooled	-40° to 85°C*[2]	-40° to 85°C

* w/ 200 lfm airflow
[1] must operate in a fully installed conduction-cooled rack
[2] must operate in a fully installed conduction-cooled REDI rack

Relative Humidity

5% to 95% non-condensing

Vibration and Shock Standards

Vibration, Random Operating: Designed to comply with VITA 47 Class V1. Shall withstand vibration from 5 to 100Hz. with Power Spectral Density (PSD) = 0.04g2/Hz, for 1 hour per axis. Testing shall be in accordance with MIL-STD-810, Method 514, Procedure 1

Shock, Operating: Designed to comply with VITA 47 Class OS1, 20g, 11ms half sine and terminal sawtooth shock pulses. 3 shock pulses in each direction along 3 axes (36 shocks, total). Testing shall be in accordance with MIL-STD-810, Method 516, Procedure 1.

EMI/EMC Regulatory Compliance

Caution

This module generates, uses, and can radiate electromagnetic energy. It may cause or be susceptible to EMI if not installed and used in a cabinet with adequate EMI protection.

The VPX4812A/14A is designed using good EMC practices and, when used in a suitably EMC-compliant chassis, should maintain the compliance of the total system.

The VPX4812A/14A is complies with EMC Directive 2004/108/EC.

- **Immunity per EN 61000-6-2:**
  Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2.
  Radiated Field Immunity (RFI), per IEC 61000-4-3.
  Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4.
  Surge Immunity, per IEC 61000-4-5.
  Conducted RF Immunity (CRFI), per IEC 61000-4-6.
- **Emissions per EN 61000-6-4:**
  Enclosure Port, per CISPR 16.
  Low Voltage AC Mains Port, per CISPR 16.

Note: This is a Class A product

- **RoHS Directive 2011/65/EU – All Models**
  In compliance per EN 50581

Air-cooled build levels of the VPX4812A/14A are designed for use in systems meeting VDE class B, EN and FCC regulations for EMC emissions and susceptibility.

Conduction cooled and REDI build levels of the VPX4812A/14A are intended for integration into EMC hardened cabinets/boxes.

11.0 Service and Repair

Service and Repair Assistance

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

Preliminary Service Procedure

Before beginning repair, be sure that all of the procedures in the "Preparation for Use" section have been followed. Also, refer to the documentation for the XMC module to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Where to Get Help

If the problem persists, the next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

Go to the "Support" tab to access:

- Application Notes
- Frequently Asked Questions (FAQ's)
- Product Knowledge Base
- Tutorials
- Software Updates/Drivers

Acromag's application engineers can also be contacted directly for technical assistance via email, telephone, or FAX through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab. When needed, complete repair services are also available.

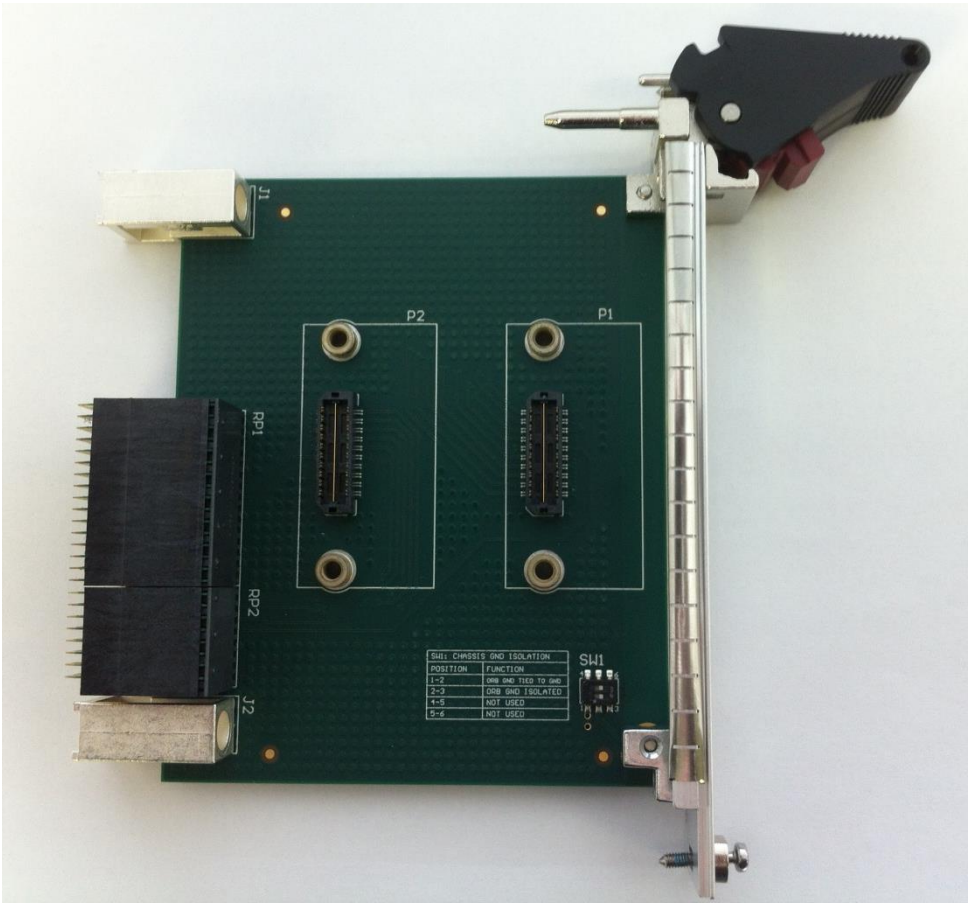
- Email: solutions@acromag.com
- Phone: 248-295-0310

Appendix A – Accessory Modules

TRANS-V112

The TRANS-V112 is a development rear transition module for the VPX4812A and is used in backplanes that bring out the rear I/O signals from the VPX4812A. If you are using a custom backplane, you will not need the RTM.

The TRANS-V112 brings out the P16 rear I/O signals from the XMC slot on the VPX4812A. The signals are brought out by two high speed Samtec differential pair connectors (PN QTH-020-01-F-D-DP-A-K).



Switch Settings

SW1 (ORBGND)	**1-2 (default)**	Orb ground is connected to digital ground.
	2-3	Orb ground is isolated from digital ground.
	4-5	Unused
	5-6	Unused

Connectors

RP1 Connector

RP1 Wafer	A	B	C	D	E	F	G
1	Unused	Unused	GND	Unused	J16_SIO10_N	GND	Unused
2	GND	Unused	Unused	GND	J16_SIO8_P	J16_SIO8_N	GND
3	Unused	Unused	GND	Unused	J16_SIO6_N	GND	Unused
4	GND	Unused	Unused	GND	J16_SIO4_P	J16_SIO4_N	GND
5	Unused	Unused	GND	Unused	J16_SIO2_N	GND	Unused
6	GND	Unused	Unused	GND	J16_SIO0_P	J16_SIO0_N	GND
7	Unused	Unused	GND	Unused	J16_DP00_P	GND	Unused
8	GND	Unused	Unused	GND	J16_DP02_N	J16_DP02_P	GND
9	J16_SIO11_P	J16_SIO11_N	GND	J16_SIO10_P	Unused	GND	Unused
10	GND	J16_SIO9_P	J16_SIO9_N	GND	Unused	Unused	GND
11	J16_SIO7_P	J16_SIO7_N	GND	J16_SIO6_P	Unused	GND	Unused
12	GND	J16_SIO5_P	J16_SIO5_N	GND	Unused	Unused	GND
13	J16_SIO3_P	J16_SIO3_N	GND	J16_SIO2_P	Unused	GND	Unused
14	GND	J16_SIO1_P	J16_SIO1_N	GND	Unused	Unused	GND
15	J16_DP01_N	J16_DP01_P	GND	J16_DP00_N	Unused	GND	Unused
16	GND	J16_DP03_N	J16_DP03_P	GND	Unused	Unused	GND

RP2 Connector

RP2 Wafer	A	B	C	D	E	F	G
1	J16_DP11_N	J16_DP11_P	GND	J16_DP10_N	Unused	Unused	Unused
2	GND	J16_DP13_N	J16_DP13_P	GND	Unused	Unused	Unused
3	J16_DP05_N	J16_DP05_P	GND	J16_DP04_N	Unused	Unused	Unused
4	GND	J16_DP07_N	J16_DP07_P	GND	Unused	Unused	Unused
5	J16_DP09_N	J16_DP09_P	GND	J16_DP08_N	Unused	Unused	Unused
6	GND	J16_DP15_N	J16_DP15_P	GND	Unused	Unused	Unused
7	J16_DP17_N	J16_DP17_P	GND	J16_DP16_N	Unused	Unused	Unused
8	GND	J16_DP19_N	J16_DP19_P	GND	Unused	Unused	Unused
9	Unused	Unused	Unused	Unused	J16_DP10_P	GND	Unused
10	Unused	Unused	Unused	Unused	J16_DP12_N	J16_DP12_P	GND
11	Unused	Unused	Unused	Unused	J16_DP04_P	GND	Unused
12	Unused	Unused	Unused	Unused	J16_DP06_N	J16_DP06_P	GND
13	Unused	Unused	Unused	Unused	J16_DP08_P	GND	Unused
14	Unused	Unused	Unused	Unused	J16_DP14_N	J16_DP14_P	GND
15	Unused	Unused	Unused	Unused	J16_DP16_P	GND	Unused
16	Unused	Unused	Unused	Unused	J16_DP18_N	J16_DP18_P	GND

P1 Connector

Pin Number	Description
1	J16_DPO0_P
2	J16_DPO10_P
3	J16_DPO0_N
4	J16_DPO10_N
5	J16_DPO1_P
6	J16_DPO11_P
7	J16_DPO1_N
8	J16_DPO11_N
9	J16_DPO2_P
10	J16_DPO12_P
11	J16_DPO2_N
12	J16_DPO12_N
13	J16_DPO3_P
14	J16_DPO13_P
15	J16_DPO3_N
16	J16_DPO13_N
17	J16_DPO8_P
18	J16_DPO9_P
19	J16_DPO8_N
20	J16_DPO9_N
21	J16_SIO0_P
22	J16_SIO1_P
23	J16_SIO0 _N
24	J16_SIO1_N
25	J16_SIO2_P
26	J16_SIO3_P
27	J16_SIO2_N
28	J16_SIO3_N
29	J16_SIO4_P
30	J16_SIO5_P
31	J16_SIO4_N
32	J16_SIO5_N
33	J16_SIO6_P
34	J16_SIO7_P
35	J16_SIO6_N
36	J16_SIO7_N
37	J16_SIO8_P
38	J16_SIO9_P
39	J16_SIO8_N
40	J16_SIO9_N

P2 Connector

Pin Number	Description
1	J16_DP04_P
2	J16_DP14_P
3	J16_DP04_N
4	J16_DP14_N
5	J16_DP05_P
6	J16_DP15_P
7	J16_DP05_N
8	J16_DP15_N
9	J16_DP06_P
10	J16_DP16_P
11	J16_DP06_N
12	J16_DP16_N
13	J16_DP07_P
14	J16_DP17_P
15	J16_DP07_N
16	J16_DP17_N
17	J16_DP18_P
18	J16_DP19_P
19	J16_DP18_N
20	J16_DP19_N
21	J16_SIO10_P
22	J16_SIO11_P
23	J16_SIO10_N
24	J16_SIO11_N
25	NC
26	NC
27	NC
28	NC
29	NC
30	NC
31	NC
32	NC
33	NC
34	NC
35	NC
36	NC
37	NC
38	NC
39	NC
40	NC

Certificate of Volatility

Certificate of Volatility				
Acromag Model VPX4812A-LF VPX4814A-LF TRANS-V112-LF	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) □ Yes ■ No				
Type (SRAM, SDRAM, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Type (SRAM, SDRAM, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No				
Type (EEPROM, Flash, etc.) EEPROM – AT25640B	Size: 64-KB	User Modifiable ■ Yes □ No	Function: Store settings for PEX8624 PCIe switch	Process to Sanitize: Device can be accessed via SPI through the PEX8624. Device can be sanitized by writing 0's to all bits.
Type (EEPROM, Flash, etc.) EEPROM – PCA9500BS	Size: 2-kbit	User Modifiable ■ Yes □ No	Function: Misc. storage	Process to Sanitize: Device can be accessed via backplane I2C bus. Device can be sanitized by writing 0's to all bits.
Type (EEPROM, Flash, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Other capabilities: Does device contain media storage capabilities: □ Yes ■ No If yes explain Is this device capable of wireless transmission: □ Yes ■ No If yes explain				

Acromag Representative				
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Revision History

The following table shows the revision history for this document:

Release Date	Version	EGR/DOC	Description of Revision
07 MAY 2020	A	MDW/ARP	Initial Acromag release.