AP730 and AP731 Multifunction I/O AcroPacks

Analog Input, Analog Output And Digital I/O Modules

USER'S MANUAL

ACROMAG INCORPORATED
30765 South Wixom Road
Wixom, MI 48393-2417 U.S.A.
Tel: (248) 295-0310
Email: solutions@acromag.com

8501149B

Table of Contents

1. RELATED PUBLICATIONS

The following manuals and part specifications provide the necessary information for an in depth understanding of this product.

ADC Data Sheet	LTC2333-16 Buffered 8-Channel, 16-Bit, 800ksps Differential +/-10.24V
DAC Data Sheet	AD5761 Multiple Range, 16-Bit, Bipolar/Unipolar (AP730E-LF model only)
DAC Data Sheet	AD5721 Multiple Range, 12-Bit, Bipolar/Unipolar (AP731E-LF model only)

2. GENERAL INFORMATION

Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the AcroPack module.

Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind regarding this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag.

Trademark, Trade Name and Copyright Information

Class A Product Warning

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, etc.) are capable of being recycled. Final

disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

AcroPack Information – All Models

The AcroPack IO modules are based on the PCI Express Mini Card Electromechanical specification and are 70mm in length with an added 100 pin field I/O connector.

The AcroPack is 19.05mm longer than the full length mini PCIe card at 50.95mm. It has the same mPCIe board width of 30mm and uses the same mPCIe standard board hold down standoff and screw keep out areas.

Ordering Information

The AcroPack ordering options are given in the following table.

Table 2.1 AP73x Modules

Model Number	Description
AP730E-LF	16 Digital I/O, 8 Differential Analog In (16-Bit), 4 Analog Out (16-Bit)
AP731E-LF	16 Digital I/O, 8 Differential Analog In (16-Bit), 4 Analog Out (12-Bit)

Operating temperature range: -40°C to 85°C. Applications requiring operating temperatures above 70°C will require purchase of AcroPack Heatsink Accessory AP-CC-01. See Appendix A for installation instructions.

DAC Key Features

High Channel Count – Individual control of four channels of Digital to Analog Converter (DAC) with voltage output is provided.

Flexible Operating Modes – Each channel may be independently configured to operate in direct access, single burst, continuous, or streaming (FIFO) mode.

Flexible Trigger – Each channel can be independently configured for software trigger, on-board timer trigger, or external trigger mode. The module can accept an external trigger or be the trigger source for synchronizing with other modules.

Flexible Memory Allocation – The on-board 64K x 16-bit sample memory is shared among the four channels. The amount of memory allocated to each channel is configurable.

Continuous Output Mode - Continuous conversions are implemented by continuously cycling through the waveform memory, from Start Address to End Address, until halted by software. The interval between conversions is controlled by the interval timer. Conversions are initiated by issue of a software or external trigger.

FIFO Output Mode - Each of the channel's FIFOs can be filled/loaded with new data without stopping output waveform generation.

Single Conversion Mode - Conversions are started with the Start Address and can continue until the channel's End Address is reached.

AP730, 16-Bit Resolution - Each channel contains its own 16-bit, Digital to Analog Converter (DAC) with 7.5uS output settling time.

AP731, 12-Bit Resolution - Each channel contains its own 12-bit, Digital to Analog Converter (DAC) with 7.5uS output settling time.

Software selectable output range - Provides six voltage ranges:

0 to 10 Volts, 0 to 5 Volts, +/-10 Volts, +/-5 Volts, +/-3 Volts,
- 2.5V to +7.5 Volts

Reliable Software Calibration - Calibration coefficients stored on-board provide the means for accurate software calibration of the module.

ADC Key Features

ADC 16-Bit Resolution - 16-bit capacitor-based successive approximation Analog to Digital Converter (ADC) with integral sample and hold and reference.

1.264µsec Conversion Time - A maximum conversion rate of 791,139.24Hz is supported.

High Density - Monitors up to 8 differential analog inputs (acquisition mode and channels are selected via programmable control registers).

1026 Sample FIFO Buffer – A single 1026 sample deep FIFO is available for buffering data from the 8 differential channels. This allows the external processor to service more tasks within a given time. Data tagging is implemented for easy channel identification. The FIFO buffer can be read through host generated PCIe read transactions or through DMA transactions.

Interrupt Upon FIFO Threshold Reached – FIFO interrupt generation is also supported. Upon reaching a FIFO programmable threshold condition an interrupt can be generated to minimize CPU interaction.

Automatic DMA Transfers Upon FIFO Threshold Reached – In Auto DMA Mode, DMA transfers will automatically be started when the FIFO threshold has been met to minimize CPU interaction.

FIFO Full, Empty and Threshold Reached Flags – FIFO Full, Empty and Threshold Reached flag bits are available to implement software polling schemes for FIFO buffer data control.

Programmable Control of Channels Converted – Up to 8 differential analog inputs are monitored. Channels 0 to 7 are converted sequentially. Channels may be individually enabled/disabled for conversion.

User Programmable Conversion Timer – A programmable conversion timer is available to control the time between conversion of the next channel data.

Continuous Conversion Mode – All channels selected for conversion are continually digitized with the interval between conversions controlled by the programmed conversion timer register. Scanning is initiated by a software or external trigger. Scanning is stopped by software control.

Single Cycle Conversion Mode – All channels selected for conversion are digitized once with the time between channels controlled by a programmable timer. Single cycle conversion mode is initiated by a software or external trigger.

External Trigger Input or Output – The external trigger input is assigned to a field I/O line. The external trigger output is assigned to another field I/O line. This external trigger may be enabled or disabled. As an output, this signal provides a means to synchronize other modules to a single AP73x timer reference.

Calibration Constants – Factory calibration constants used to correct gain and offset errors are stored in on-board flash memory. Gain and offset correction constants are stored for each analog to digital channel and each of the supported ranges.

ADC Ranges Selected via Control Register - Both bipolar and unipolar ranges are programmable available via control register.

Bipolar ranges of +/-10.24, +/-10, +/-5.12, +/-5.0

Unipolar ranges of +10.24 to 0, +10.0 to 0, +5.12 to 0.

Selected range applies to each channel and can be individually selected on a per channel basis.

Counter/Timer Key Features

32-Bit Counter/Timer – A multifunction 32-bit counter is provided for implementation of: waveform generation, event counting, watchdog timing, pulse-width measurement, or period measurement.

Quadrature Position Measurement – Three input signals can be used to determine bi-directional motion. The sequence of logic high pulses for two input signals, A and B, indicate direction and a third signal (index) is used to initialize the counter. X1, X2, and X4 decoding is also implemented. X1 decoding executes one count per duty cycle of the A and B signals, while X2, and X4 execute two and four counts per duty cycle, respectively.

Pulse Width Modulation – The counter can be programmed for pulse width modulation. The duration of the logic high and low levels of the output signal can be independently controlled. An external gate signal can also be used to start/stop generation of the output signal.

Watchdog Timer – The counter can be configured as a countdown timer for implementation as a watchdog timer. A gate-off signal is available for use to stop the countdown operation. Interrupt generation upon a countdown to zero condition is available.

Event Counter – The counter can be configured to count input pulses or events. A gate-off signal is provided to control count-up or count down with each event. Interrupt generation upon programmed count condition is available.

Frequency Measurement – The counter can be configured to count how many active edges are received during a period defined by an external count enable signal. An interrupt can be generated upon measurement complete.

Pulse-Width or Period Measurement – The counter can be configured to measure pulse-width or waveform period. In addition, an interrupt can be generated upon measurement complete.

One-Shot and Repetitive One-Shot – A one-shot pulse waveform may also be generated by the counter. The duration of the pulse and the delay until the pulse goes active is user programmable. A repetitive one-shot can be initiated with repetitive trigger pulses.

Programmable Interface Polarity – The polarities of the counter's external trigger, input, and output pins are programmable for active high or low operation. These counter control signals are available through the board's field connector.

Internal or External Triggering – A software or hardware trigger is selectable to initiate quadrature position measurement, pulse width modulation, watchdog countdown, event counting, frequency measurement, pulse-width measurement, period measurement, or one-shot operation.

CMOS Compatible Thresholds – Input and output signal thresholds are at 3.3-volt levels.

Digital Input/Output Key Features

16 Digital Input/Output Channels – Interface with up to 16 input/output channels which can be configured as input or output in groups of eight channels.

TTL Compatible Thresholds – Input and output thresholds are at 5V TTL levels. Buffer input channels include hysteresis for increased noise immunity.

Programmable Change of State/Level Interrupts – Interrupts are software programmable for any bit Change-Of-State or level on all 16 channels.

Power Up and System Reset is Failsafe – For safety, the digital channels are configured for input upon power-up.

PCIe Interface Features

- **PCIe Bus** – The example design includes a PCI Express Generation 1 interface operating at a bus speed of 2.5 Gbps per lane per direction.
- **PCIe Bus Master** – The PCIe interface logic becomes the bus master to perform DMA transfers.

- **DMA Operation** – The design includes a DMA controller to move data between the FPGA memory and the PCIe bus interface.
- **Compatibility** – PCI Express Base Specification v2.1 compliant PCI Express Endpoint. Provides one interrupt.

Signal Interface Products

This AcroPack Module will mate directly to all Acromag AP carriers. Once connected, the module is accessed via a 50 pin or 68 pin front panel connector.

Accessory cables and termination panels are also available. For optimum performance with the AP73x module, use of the shortest possible length of shielded I/O cable is recommended.

Software Support

The AcroPack series products require support drivers specific to your operating system. Supported operating systems include: Linux®, Windows®, and VxWorks®.

Windows

Acromag provides software products (sold separately) to facilitate the development of Windows applications interfacing with AcroPack modules, VPX I/O board products, and PCIe I/O Cards. This software (model APSW-API-WIN) consists of low-level drivers and Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

VxWorks

Acromag provides a software product (sold separately) consisting of VxWorks software. This software (Model APSW-API-VXW) is composed of VxWorks (real time operating system) libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

Linux

Acromag provides a software product consisting of Linux software. This software (Model APSW-API-LNX) is composed of Linux libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

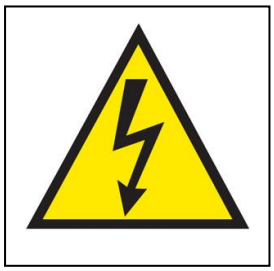
References

The following resources regarding AcroPack modules are available for download on Acromag's website or by contacting your sales representative.

- PCI Express MINI Card Electromechanical Specification, REV 1.2
  https://www.acromag.com/

3. PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.

WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

Unpacking and Inspection

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

Card Cage Considerations

Refer to the specifications section for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

In an air-cooled assembly, adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and

to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

In a conduction cooled assembly, adequate thermal conduction must be provided to prevent a temperature rise above the maximum operating temperature.

Board Installation

Power should be removed from the board when installing AP modules, cables, termination panels, and field wiring. The AP73x has no hardware jumpers or switches to configure.

Field I/O Connector

The field I/O interface connector P2 provides a mating interface between the AP73x module and the carrier board. Table 3.1 lists pin assignments for each of the AP73x field I/O signals. Every other pin of the 100 pin P2 connector is left unconnected.

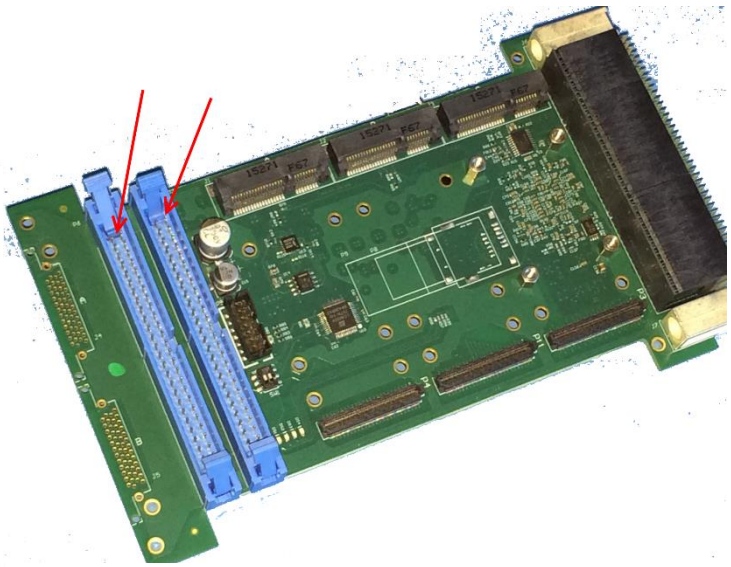
IMPORTANT: All unused analog input pins should be tied to analog ground. Floating unused inputs can drift outside the input range causing temporary saturation of the input analog circuits. Recovery from saturation is slow and affects the reading of the desired channels.

Table 3.1 Field I/O Connector Pin Assignments

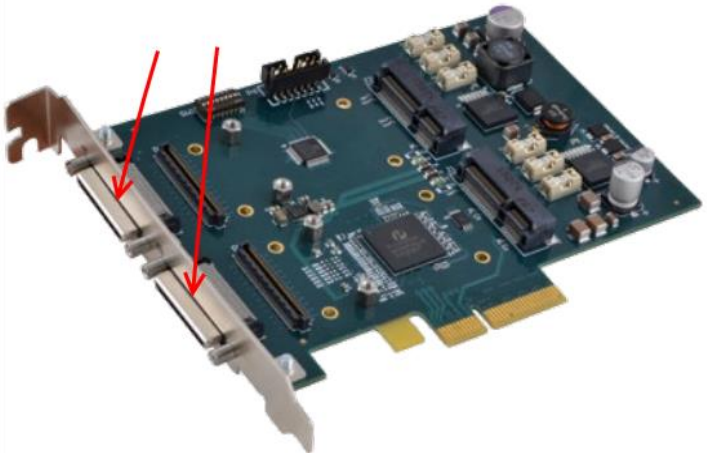
Carrier Connector Ribbon[1]	Carrier Connector 50 Pin Champ[2]	Carrier Connector 68 Pin Champ[3]	Module P2 Pin Number	Field I/O Signal
1	1	1	2	Analog In CH0+
2	26	35	1	Analog In CH0-
3	2	2	6	Analog In CH1+
4	27	36	5	Analog In CH1-
5	3	3	10	Analog In CH2+
6	28	37	9	Analog In CH2-
7	4	4	14	Analog In CH3+
8	29	38	13	Analog In CH3-
9	5	5	18	Analog In CH4+
10	30	39	17	Analog In CH4-
11	6	6	22	Analog In CH5+
12	31	40	21	Analog In CH5-
13	7	7	26	Analog In CH6+
14	32	41	25	Analog In CH6-
15	8	8	30	Analog In CH7+

Carrier Connector Ribbon[1]	Carrier Connector 50 Pin Champ[2]	Carrier Connector 68 Pin Champ[3]	Module P2 Pin Number	Field I/O Signal
16	33	42	29	Analog In CH7-
17	9	9	34	COMMON
18	34	43	33	COMMON
19	10	10	38	Analog Out CH0
20	35	44	37	COMMON
21	11	11	42	Analog Out CH1
22	36	45	41	COMMON
23	12	12	46	Analog Out CH2
24	37	46	45	COMMON
25	13	13	50	Analog Out CH3
26	38	47	49	COMMON
27	14	14	54	COMMON
28	39	48	53	COMMON
29	15	15	58	Dig CH0/CNT InA
30	40	49	57	Dig CH1/CNT InB
31	16	16	62	Dig CH2/CNT InC
32	41	50	61	Dig CH3/ADC Trig In
33	17	17	66	Dig CH4/DAC Trig In
34	42	51	65	Dig CH5
35	18	18	70	COMMON
36	43	52	69	COMMON
37	19	19	74	Dig CH6
38	44	53	73	Dig CH7
39	20	20	78	Dig CH8/DAC Trig Out
40	45	54	77	Dig CH9/ADC Trig Out
41	21	21	82	COMMON
42	46	55	81	COMMON
43	22	22	86	Dig CH10
44	47	56	85	Dig CH11
45	23	23	90	Dig CH12
46	48	57	89	Dig CH13
47	24	24	94	Dig CH14
48	49	58	93	Dig CH15
49	25	25	98	Counter Output
50	50	59	97	COMMON

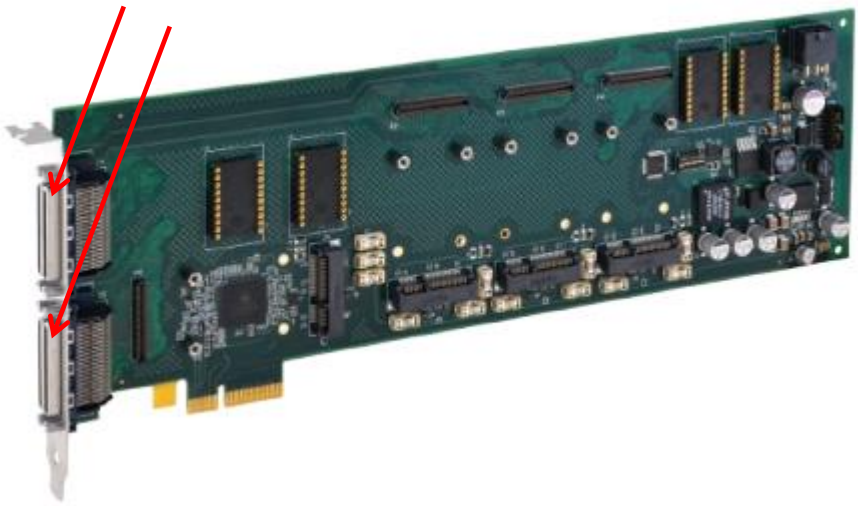
Note 1: VPX4500-CC-LF is an example of a carrier that uses the ribbon cable connector see image of carrier.



Note 2: APCe7020E-LF is an example of a carrier that uses the 50-pin Champ connector see image of carrier.



Note 3: APCe7040E-LF is an example of a carrier that uses the 68-pin Champ connector see image of carrier.



Noise and Grounding Considerations

The board is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

Logic Interface Connector

The AP module logic edge connector interfaces to the mating connector on the carrier board. The pin assignments of this connector are standard for all AP modules according to the PCI Express MINI Card Electromechanical Specification, REV 1.2 (with exceptions shown in Table 3.2 and noted below).

Power supplies +5, +12, and -12 Volt have been assigned to pins that are reserved in the mini-PCIe specification. The Present signal is grounded on the AP module. In addition, COEX1, COEX2 – wireless transmitter controls, are reassigned to JTAG signals TMS and TCK. Lastly, UIM_C4, UIM_C8 – reserved User Identity Module signals are reassigned to JTAG signals TDI and TDO.

Table 3.2 Mini-PCIe Connector

Pin #	Name	Pin #	Name
51	**+5V**[2]	52	+3.3V[3]
49	**+12V**[2]	50	GND
47	**-12V**[2]	48	+1.5V
45	**Present**[2]	46	N.C. (LED_WPAN#)[1]
43	GND	44	N.C. (LED_WLAN#)[1]
41	+3.3V[3]	42	N.C. (LED_WWAN#)[1]
39	+3.3V[3]	40	GND
37	GND	38	N.C. (USB_D+)[1]
35	GND	36	N.C. (USB_D-)[1]
33	PETp0	34	GND
31	PETn0	32	SMB_DATA[4]
29	GND	30	SMB_CLK[4]
27	GND	28	+1.5V
25	PERp0	26	GND
23	PERn0	24	+3.3V[3]
21	GND	22	PERST#
19	**TDI** (UIM_C4)[1]	20	N.C. (W_DISABLE#)[1]
17	**TDO** (UIM_C8)[1]	18	GND
15	GND	16	N.C.(UIM_VPP)[1]
13	RECLK+	14	N.C.(UIM_RESET)[1]
11	REFCLK-	12	N.C.(UIM_CLK)[1]
9	GND	10	N.C.(UIM_DATA)[1]
7	N.C.(CLKREQ#)[1]	8	N.C.(UIM_PWR)[1]
5	**TCK** (COEX2)[1]	6	+1.5V
3	**TMS** (COEX1)[1]	4	GND
1	N.C.(WAKE#)[1]	2	+3.3V[3]

1. **Note 1:** Signals are not applicable for the AP73x implementation. Pins are either "no connects" on the module or are repurposed for JTAG.
2. **Note 2:** +5, +12, and -12 Volt power supplies have been assigned to pins that are reserved in the mini-PCIe specification. The Present signal is tied to circuit common on the AP module.
3. **Note 3:** All +3.3Vaux power pins are changed to system +3.3V power.
4. **Note 4:** The SM bus signals SMB_CLK and SMB_DATA will be used to clock a carrier location serial stream from the carrier. These signals are under the control of the AcroPack module.

4. PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the board.

PCIe Configuration Address Space

This AP73x module is PCI Express Base Specification Revision v2.1 compliant.

The PCIe bus is defined to address three distinct address spaces: I/O, memory, and configuration space. This board can be accessed via the PCIe bus memory, and configuration spaces.

The card's configuration registers are initialized by system software at power-up to configure the card. The board is a Plug-and-Play PCIe card. As a Plug-and-Play card the board's base address and system interrupt request are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCIe bus configuration access is used to read/write the PCIe card's configuration registers.

When the computer is first powered-up, the computer's system configuration software scans the PCIe bus to determine what PCIe devices are present. The software also determines the configuration requirements of the PCIe card.

The system software accesses the configuration registers to determine how many blocks of memory space the module requires. It then programs the board's configuration registers with the unique memory base address.

Since this board is not fixed in address space, its device driver must use the mapping information stored in the board's Configuration Space registers to determine where the board is mapped in memory space.

The configuration registers are also used to indicate that the board requires an interrupt request. The system software then programs the configuration registers with the interrupt request assigned to the board.

Configuration Registers

The PCIe specification requires software driven initialization and configuration via the Configuration Address space. This board provides 512 bytes of configuration registers for this purpose. It contains the configuration registers shown in 4.1 to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers and the Interrupt Register which must be read to determine the base address assigned to the board and the interrupt request that goes active on a board interrupt request.

Table 4.1 Configuration Registers

Reg. Num.	D31 D24	D23 D16	D15 D8	D7 D0
0	**Device ID** 0x7073 AP730E-LF 0x7072 AP731E-LF		**Vendor ID** 16D5	
1	Status		Command	
2	Class Code=118000			Rev ID=00
3	BIST	Header	Latency	Cache
4:5	64-bit Memory Base Address for Memory Accesses to PCIe interrupt, I/O registers, System Monitor registers, and Flash memory. 1M Space **(BAR0)**			
6:10	Not Used			
11	**Subsystem ID** 0x7073 AP730E-LF 0x7072 AP731E-LF		**Subsystem Vendor ID** 16D5	
12	Not Used			
13,14	Reserved			
15	Max_Lat	Min_Gnt	Inter. Pin	Inter. Line

This board is allocated a 1M byte block of memory (BAR0), to access the PCIe interrupt, DAC registers, ADC registers, Counter Timer registers, Digital I/O registers, XADC registers, Flash memory.

BAR0 Memory Map

The BAR0 memory address space is used to access the devices listed in the table below. Note that the base address for the board (BAR0) in memory space must be added to the addresses shown to properly access these registers.

Table 4.2 BAR0 Registers

BAR0 Base Address	Size	Description
0x0000_0000→0x0000_0FFF	4K	CDMA (see Xilinx Document PG034)
0x0000_1000→0x0000_1FFF	4K	PCIe AXI Bridge Control (see Xilinx Document PG054)
0x0000_2000→0x0000_2FFF	4K	Interrupt Controller
0x0000_3000→0x0000_3FFF	4K	XADC System Monitor (see Xilinx Document DS790)
0x0000_4000→0x0000_4FFF	4K	Firmware Revision
0x0000_5000→0x0000_5FFF	4K	Flash AXI QSPI
0x0000_6000→0x0000_6FFF	4K	Location in System
0x0000_7000→0x0000_7FFF	4K	M07_AXI_Custom (ADC, Counter, Digital I/O)
0x0000_8000→0x0000_FFFF	32K	Reserved
0x0001_0000→0x0001_7FFF	32K	Block RAM

BAR0 Base Address	Size	Description
0x0001_8000→0x0003_FFFF	164K	Reserved
0x0004_0000→0x0004_0213	1K	DAC Registers
0x0004_0214→0x0005_FFFF	127K	Reserved
0x0006_0000→0x0007_FFFF	128K	Sample Memory Part of DAC Memory space
0x0008_0000→0x000F_FFFF	524K	AXI to PCIe BAR0

CDMA Memory Map

The Central Direct Memory Access (CDMA) controller can access the AXI to PCI bridge (BAR0), the ADC FIFO memory, and the DAC Sample Memory.

Table 4.3 CDMA Memory Map

BAR0 Base Address	Size	Description
0x0000_1000→0x0000_1FFF	4K	PCIe AXI Bridge Control (see Xilinx Document PG054)
0x0000_7000→0x0000_7FFF	4K	M07_AXI_Custom (ADC, Counter, Digital I/O)
0x0001_0000→0x0001_7FFF	32K	Block RAM
0x0004_000→0x0004_0213	1K	DAC Registers
0x0004_0214→0x0005_FFFF	127K	Reserved
0x0006_0000→0x0007_FFFF	128K	Sample Memory

Scatter Gather Memory Map

The scatter-gather engine can access the block RAM Memory only. The scatter-gather descriptor list must be located in this memory. The block RAM can hold 512 descriptors (64 bytes/Descriptor).

Table 4.4 Scatter Gather Memory Map

BAR0 Base Address	Size	Description
0x0001_0000→0x0001_7FFF	32K	Block RAM

AXI-CDMA

The AXI Central Direct Memory Access (CDMA) core is a soft Xilinx Intellectual Property core. The CDMA provides direct memory access between system memory over the PCIe bus and the memory resident on the XCM730 module.

The basic mode of operation for the CDMA is Simple DMA. In this mode, the CDMA executes one programmed DMA command and then stops. This requires that the CDMA registers need to be set up by system software over the PCIe bus for each DMA operation required.

Scatter Gather is a mechanism that allows for automated DMA transfer scheduling via a pre-programmed instruction list of transfer descriptors. This instruction list is programmed by the user software application into a memory-resident data structure that must be accessible by the AXI CDMA Scatter Gather interface. This list of instructions is organized into what is

referred to as a transfer descriptor chain. Each descriptor has an address pointer to the next descriptor to be processed. The last descriptor in the chain generally points back to the first descriptor in the chain but it is not required. The AXI CDMA Tail Descriptor Pointer register needs to be programmed with the address of the first word of the last descriptor of the chain. When the AXI CDMA executes the last descriptor and finds that the Tail Descriptor pointer register contents matches the address of the completed descriptor, the Scatter Gather Engine stops descriptor fetching and waits. See the Xilinx AXI Central Direct Memory Access product guide PG034 for additional details for Scatter Gather operations.

Table 4.5 AXI-CDMA

BAR0 Base Addr+	Bit(s)	Description
0x0000_0000	31:0	CDMA Control Register
0x0000_0004	31:0	CDMA Status Register
0x0000_0008	31:0	Current Descriptor Pointer Register
0x0000_000C	31:0	Reserved
0x0000_0010	31:0	Tail Descriptor Pointer Register
0x0000_0014	31:0	Reserved
0x0000_0018	31:0	Source Address Register
0x0000_001C	31:0	Reserved
0x0000_0020	31:0	Destination Address Register
0x0000_0024	31:0	Reserved
0x0000_0028	31:0	Bytes to Transfer Register

Note that any registers/bits not mentioned will remain at the default value: logic low.

CDMA Control Register (Read/Write) – (BAR0 + 0x0000)

This register provides software application control of the AXI CDMA.

Table 4.6 CDMA Control Register (Read/Write) – (BAR0 + 0x0000)

Bit(s)	Function	
0	This bit is reserved for future definition and will always return zero.	
1	The bit will always return one.	
2	Soft reset control for the AXI CDMA core. Setting this bit to a '1' causes the AXI CDMA to be reset. Reset is accomplished gracefully. Committed AXI4 transfers are then completed. Other queued transfers are flushed. After completion of a soft reset, all registers and bits are in the Reset State.	
	0	Reset Not in Progress
	1	Reset in Progress

Bit(s)	Function	
3	This bit controls the transfer mode of the CDMA. Setting this bit to a '1' causes the AXI CDMA to operate in a Scatter Gather mode. Note: This bit must only be changed when the CDMA engine is IDLE (CDMA Status bit-1 = '1'). Changing the state of this bit at any other time has undefined results. Note: This bit must be set to a 0 then back to 1 by the software application to force the CDMA Scatter Gather engine to use a new value written to the CDMA Current Descriptor Pointer register. Note: This bit must be set prior to setting Bit-13 of this CDMA Control register.	
	0	Simple DMA Mode
	1	Scatter Gather Mode
4	This bit enables the keyhole read (FIXED address AXI transaction). Note: This value should not be changed when a transfer is in progress. This value should remain constant until all the descriptors are processed (for SG = 1). CDMA shows unexpected behavior if the value is changed in the middle of a transfer. Note: It is the responsibility of the slave device to enforce the functionality.	
	0	Key Hole Read Disabled
	1	Key Hole Read Enabled
5	Key Hole Write. Writing 1 to this enables the keyhole write (FIXED address AXI transaction). This value should not be changed when a transfer is in progress. This value should remain constant until all the descriptors are processed (for SG = 1). CDMA shows unexpected behavior if this value is changed in the middle of a transfer.	
	0	Key Hole Write Disabled
	1	Key Hole Write Enabled
6	Cyclic BD Enable. When set to 1, you can use the CDMA in Cyclic Buffer Descriptor (BD) mode without any user intervention. In this mode, the Scatter Gather module ignores the Completed bit of the BD. With this feature, you can use the same BDs in cyclic manner without worrying about any errors. This bit should be set before updating the TAILDESC register. Changing this bit while the transfer is in progress will generate undefined results.	

Bit(s)	Function	
	0	Cyclic BD Disabled
	1	Cyclic BD Enabled
11-7	Reserved	
12	Interrupt on Complete Interrupt Enable. When set to '1', it allows an interrupt after completed DMA transfers.	
	0	Interrupt on Complete Disabled
	1	Interrupt on Complete Enabled
13	Interrupt on Delay Timer Interrupt Enable. When set to '1', it allows a delayed interrupt out. This is only used with Scatter Gather assisted transfers.	
	0	Delayed Interrupt Disabled
	1	Delayed Interrupt Enabled
14	Interrupt on Error Interrupt Enable. When set to '1', it allows an error to generate an interrupt out.	
	0	Error Interrupt Disabled
	1	Error Interrupt Enabled
15	Reserved	
23-16	Interrupt Threshold value. This field is used to set the Scatter Gather interrupt coalescing threshold. When Interrupt On Complete interrupt events occur, an internal counter counts down from the Interrupt Threshold setting. When the count reaches zero, an interrupt out is generated by the CDMA engine. Note: The minimum setting for the threshold is 0x01. A write of 0x00 to this register has no effect. If the CDMA is built with Scatter Gather disabled (Simple Mode Only), the default value of the port is zeros.	
31-24	Interrupt Delay Time Out. This value is used for setting the interrupt delay time out value. The interrupt time out is a mechanism for causing the CDMA engine to generate an interrupt after the delay time period has expired. This is used for cases when the interrupt threshold is not met after a period of time, and the CPU desires an interrupt to be generated. Timer begins counting when the CDMA is IDLE (CDMA Status bit-1 = '1'). This generally occurs when the CDMA has completed all scheduled work defined by the transfer descriptor chain (reached the tail pointer) and has not satisfied the Interrupt Threshold count. Note: Setting this value to zero disables the delay timer interrupt.	

CDMA Status Register (Read/Write) – (BAR0 + 0x0004)

This register provides status of the AXI CDMA.

Table 4.7 CDMA Status Register (Read/Write) – (BAR0 + 0x0004)

Bit(s)	Function	
0	This bit is reserved for future definition and will always return zero.	
1	CDMA Idle. Indicates the state of AXI CDMA operations. When set and in Simple DMA mode, the bit indicates the programmed transfer has completed and the CDMA is waiting for a new transfer to be programmed. Writing to the "Bytes to Transfer" register in Simple DMA mode causes the CDMA to start (not Idle). When set and in Scatter Gather mode, the bit indicates the Scatter Gather Engine has reached the tail pointer for the associated channel and all queued descriptors have been processed. Writing to the tail pointer register automatically restarts CDMA Scatter Gather operations.	
	0	Not Idle
	1	CDMA is Idle
2	Reserved	
3	Scatter Gather Included. This bit indicates the AXI CDMA has been implemented with Scatter Gather support included (C_SG_ENABLE = 1). This is used by application software (drivers) to determine if Scatter Gather Mode can be utilized.	
	0	Scatter Gather not included
	1	Scatter Gather is included
4	DMA Internal Error. This bit indicates that an internal error has been encountered by the DataMover on the data transport channel. This error can occur if a 0 value Byte to Transfer register is fed to the AXI DataMover, or DataMover has an internal processing error. A Bytes to Transfer register value of 0 only happens if the register is written with zeros (in Simple DMA mode) or a Bytes to Transfer register value of zero is specified in the Control word of a fetched descriptor (Scatter Gather Mode). This error condition causes the AXI CDMA to gracefully halt. The CDMA Status register bit-1 is set to '1'when the CDMA has completed shut down. A reset (soft or hard) must be issued to clear the error condition.	
	0	No CDMA Internal Errors
	1	CDMA Internal Error detected. CDMA Engine halts.

Bit(s)	Function	
5	DMA Slave Error. This bit indicates that an AXI slave error response has been received by the AXI DataMover during an AXI transfer (read or write). This error condition causes the AXI CDMA to gracefully halt. The CDMA Status register bit-1 is set to '1' when the CDMA has completed shut down. A reset (soft or hard) must be issued to clear the error condition.	
	0	No CDMA Slave Errors
	1	CDMA Slave Error detected. CDMA Engine halts.
6	DMA Decode Error. This bit indicates that an AXI decode error has been received by the AXI DataMover. This error occurs if the DataMover issues an address that does not have a mapping assignment to a slave device. This error condition causes the AXI CDMA to halt gracefully. The CDMA Status register bit-1 is set to '1' when the CDMA has completed shut down. A reset (soft or hard) must be issued to clear the error condition.	
	0	No CDMA Decode Errors
	1	CDMA Decode Error detected. CDMA Engine halts.
7	Reserved	
8	Scatter Gather Internal Error. This bit indicates that an internal error has been encountered by the Scatter Gather Engine. This error condition causes the AXI CDMA to gracefully halt. The CDMA Status register bit-1 is set to 1 when the CDMA has completed shut down. A reset (soft or hard) must be issued to clear the error condition.	
	0	No Scatter Gather Internal Errors
	1	Scatter Gather Internal Error. CDMA Engine halts.
9	Scatter Gather Slave Error. This bit indicates that an AXI slave error response has been received by the Scatter Gather Engine during an AXI transfer (transfer descriptor read or write). This error condition causes the AXI CDMA to gracefully halt. The CDMA Status register bit-1 is set to 1 when the CDMA has completed shut down. A reset (soft or hard) must be issued to clear the error condition.	
	0	No Scatter Gather Slave Errors
	1	Scatter Gather Slave Error. CDMA Engine halts.

Bit(s)	Function	
10	Scatter Gather Decode Error. This bit indicates that an AXI decode error has been received by the Scatter Gather Engine during an AXI transfer (transfer descriptor read or write). This error occurs if the Scatter Gather Engine issues an address that does not have a mapping assignment to a slave device. This error condition causes the AXI CDMA to gracefully halt. The CDMA Status register bit-1 is set to 1 when the CDMA has completed shut down. A reset (soft or hard) must be issued to clear the error condition.	
	0	No Scatter Gather Decode Errors
	1	Scatter Gather Decode Error. CDMA Engine halts.
11	Reserved	
12	Interrupt on Complete. When set to 1, this bit indicates an interrupt event has been generated on completion of a DMA transfer (either a Simple or Scatter Gather). If the Interrupt on Complete (bit-12) of the CDMA Control register = '1', an interrupt is generated from the AXI CDMA. A CPU write of 1 clears this bit to 0. **Note:** When operating in Scatter Gather mode, the criteria specified by the interrupt threshold must also be met.	
	0	No Interrupt on complete
	1	Interrupt on complete active
13	Interrupt on Delay. When set to 1, this bit indicates an interrupt event has been generated on a delay timer time out. If the Interrupt on Delay Timer bit-13 of the CDMA Control register = '1', an interrupt is generated from the AXI CDMA. A CPU write of 1 clears this bit to 0.	
	0	No Delay Interrupt
	1	Delay Interrupt Active
14	Interrupt on Error. When set to 1, this bit indicates an interrupt event has been generated due to an error condition. If the Interrupt on Error bit-14 of the CDMA Control register = '1', an interrupt is generated from the AXI CDMA. A CPU write of 1 clears this bit to 0.	
	0	No Error Interrupt
	1	Error Interrupt Active
15	Reserved	
23-16	Interrupt Threshold Status. This field reflects the current interrupt threshold value in the Scatter Gather Engine.	

Bit(s)	Function
31-24	Interrupt Delay Time Status. This field reflects the current interrupt delay timer value in the Scatter Gather Engine.

CDMA Current Descriptor Pointer Register (Read/Write) – (BAR0 + 0x0008)

Table 4.8 CDMA Current Descriptor Pointer Register (Read/Write) – (BAR0 + 0x0008)

Bit(s)	Function
5-0	Writing to these bits has no effect and they are always read as zeros.
31-6	Current Descriptor Pointer. This register field is written by the software application (in Scatter Gather Mode) to set the starting address of the first transfer descriptor to execute for a Scatter Gather operation. The address written corresponds to a 32-bit system address with the least significant 6 bits truncated. This register field must contain a valid descriptor address prior to the software application writing the CDMA Tail Descriptor Pointer register value. Failure to do so results in an undefined operation by the CDMA. On error detection, the Current Descriptor Pointer register is updated to reflect the descriptor associated with the detected error. **Note:** The register should only be written by the Software application when the AXI CDMA is Idle.

CDMA Tail Descriptor Pointer Register (Read/Write) – (BAR0 + 0x0010)

This register provides Tail Descriptor Pointer for the AXI CDMA Scatter Gather Descriptor Management.

Table 4.9 CDMA Tail Descriptor Pointer Register (Read/Write) – (BAR0 + 0x0010)

Bit(s)	Function
5-0	Writing to these bits has no effect and they are always read as zeros.

Bit(s)	Function
31-6	Tail Descriptor Pointer. This register field is written by the software application (in Scatter Gather Mode) to set the current pause pointer for descriptor chain execution. The AXI CDMA Scatter Gather Engine pauses descriptor fetching after completing operations on the descriptor whose current descriptor pointer matches the tail descriptor pointer. When the AXI CDMA is in Scatter Gather Mode, a write by the software application to this register causes the AXI CDMA Scatter Gather Engine to start fetching descriptors starting from the Current Descriptor Pointer register value. If the Scatter Gather engine is paused at a tail pointer pause point, the Scatter Gather engine restarts descriptor execution at the next sequential transfer descriptor. If the AXI CDMA is not idle, writing to this register has no effect except to reposition the Scatter Gather pause point. **Note:** The software application must not move the tail pointer to a location that has not been updated with valid transfer descriptors. The software application must process and reallocate all completed descriptors, clear the completed bits and then move the tail pointer. The software application must move the pointer to the last descriptor address it has updated.

CDMA Source Address Register (Read/Write) – (BAR0 + 0x0018)

This register provides the source address for simple DMA transfers by AXI CDMA.

If a location in system memory is the source address, it must be set with the AXI aperture base address 0x00080000 + the least significant 19-bits of the system memory address.

In addition, the physical address of the location in system memory must be set in the Address Translation Register which is described in the PCIe AXI-Bridge Control section.

Table 4.10 CDMA Source Address Register (Read/Write) – (BAR0 + 0x0018)

Bit(s)	Function
31-0	Source Address Register. This register is used by Simple DMA operations as the starting read address for DMA data transfers. The address value written can be at any byte offset. **Note:** The software application should only write to this register when the AXI CDMA is Idle.

CDMA Destination Address Register (Read/Write) – (BAR0 + 0x0020)

This register provides the destination address for simple DMA transfers by AXI CDMA.

If a location in system memory is the destination address it must be set with the AXI aperture base address 0x00080000 + the least significant 19-bits of the system memory address.

In addition, the physical address of the location in system memory must be set in the Address Translation Register which is described in the PCIe AXI-Bridge Control section.

Table 4.11 CDMA Destination Address Register (Read/Write) – (BAR0 + 0x0020)

Bit(s)	Function
31-0	Destination Address Register. This register is used by Simple DMA operations as the starting write address for DMA data transfers. **Note:** The software application should only write to this register when the AXI CDMA is Idle.

CDMA Bytes To Transfer Register (Read/Write) – (BAR0 + 0x0028)

This register provides the value for the number of bytes to transfer for Simple DMA transfers by the AXI CDMA.

Table 4.12 CDMA Bytes to Transfer Register (Read/Write) – (BAR0 + 0x0028)

Bit(s)	Function
22-0	Bytes to Transfer. This register field is used for Simple DMA transfers and indicates the desired number of bytes to DMA from the Source Address to the Destination Address. A maximum of 8,388,606 bytes of data can be specified by this field for the associated transfer. Writing to this register also initiates the Simple DMA transfer. Note: A value of zero (0) is not allowed and causes a DMA internal error to be set by AXI CDMA. The software application should only write to this register when the AXI CDMA is Idle.
31-23	Writing to these bits has no effect, and they are always read as zeros.

Scatter Gather Transfer Descriptor Definition

This defines the format and contents of the AXI CDMA Scatter Gather Transfer Descriptors. These are used only by the SG function if the CDMACR.SGMode bit is set to 1. A transfer descriptor consists of eight 32-bit words. The

descriptor represents the control and status information needed for a single CDMA transfer plus address linkage to the next sequential descriptor. Each descriptor can define a single CDMA transfer of up to 524,287 Bytes of data. A descriptor chain is defined as a series of descriptors that are sequentially linked through the address linkage built into the descriptor format.

The AXI CDMA SG Engine traverses the descriptor chain following the linkage until the last descriptor of the chain has been completed. The relationship and identification of the AXI CDMA transfer descriptor words is shown in the table below.

Note: Transfer Descriptors must be aligned on sixteen 32-bit word alignment that is 16x4 Bytes = 64 Bytes. Example valid offsets are 0x00, 0x40, 0x80, and 0xC0.

Table 4.13 Scatter Gather Transfer Descriptor Definition

Address Space Offset	Name	Description
0x00	NXTDESC_PNTR	Next Descriptor Pointer
0x04		Reserved
0x08	SA	Source Address
0x0C		Reserved
0x10	DA	Destination Address
0x14		Reserved
0x18	CONTROL	Transfer Control
0x1C	STATUS	Status

Transfer Descriptor NXTDESC_PNTR

This word provides the address pointer to the first word of the next transfer descriptor in the descriptor chain.

Table 4.14 Transfer Descriptor NXTDESC_PNTR

Bit(s)	Function
5-0	These bits are reserved and fixed to zeros. This forces the address value programmed in this register to be aligned to 64-byte aligned addresses.
31-6	Next Descriptor Pointer. This field is an address pointer (most significant 26 bits) to the first word of the next transfer descriptor to be executed by the CDMA SG Engine. The least-significant 6 bits of this register are appended to this value when used by the SG Engine forcing transfer descriptors to be loaded in memory at 64-byte address alignment.

Transfer Descriptor Source Address

This word provides the starting address for the data read operations for the associated DMA transfer.

Table 4.15 Transfer Descriptor Source Address

Bit(s)	Function
31-0	Source Address. This value specifies the starting address for data read operations for the associated DMA transfer. The address value can be at any byte offset.

Transfer Descriptor Destination Address

This word provides the starting address for the data write operations for the associated DMA transfer.

Table 4.16 Transfer Descriptor Destination Address

Bit(s)	Function
31-0	Destination Address. This value specifies the starting address for data write operations for the associated DMA transfer. The address value can be at any byte offset.

Transfer Descriptor Control Word

This word provides the starting address for the data write operations for the associated DMA transfer.

Table 4.17 Transfer Descriptor Control Word

Bit(s)	Function
22-0	Bytes to Transfer. This field in the Control word specifies the desired number of bytes to DMA from the Source Address to the Destination Address. A maximum of 524,287 bytes of data can be specified by this field for the associated transfer. A value of zero (0) is not allowed and causes a DMA internal error to be set by AXI CDMA.
31-23	Reserved

Transfer Descriptor Status Word

This word provides the starting address for the data write operations for the associated DMA transfer.

Table 4.18 Transfer Descriptor Status Word

Bit(s)	Function
27-0	Reserved

Bit(s)	Function
28	DMA Internal Error. This bit indicates that an internal error was encountered by the AXI CDMA DataMover on the data transport channel during the execution of this descriptor. This error can occur if a 0 value BTT (bytes to transfer) is fed to the AXI DataMover or if the DataMover has an internal processing error. A BTT of 0 only happens if the BTT field in the transfer descriptor CONTROL word is programmed with a value of zero. This error condition causes the AXI CDMA to gracefully halt. The CDMASR.IDLE bit is set to 1 when the CDMA has completed shutdown. 0 = No CDMA Internal Errors 1 = CDMA Internal Error detected. CDMA Engine halts at this descriptor
29	DMA Slave Error. This bit indicates that an AXI slave error response was received by the AXI CDMA DataMover during the AXI transfer (read or write) associated with this descriptor. This error condition causes the AXI CDMA to halt gracefully. 0 = No CDMA Slave Errors 1 = CDMA Slave Error received. CDMA Engine halts at this descriptor.
30	DMA Decode Error. This bit indicates that an AXI decode error was received by the AXI CDMA DataMover. This error occurs if the DataMover issues an address that does not have a mapping assignment to a slave device. This error condition causes the AXI CDMA to halt gracefully. 0 = No CDMA Decode Errors 1 = CDMA Decode Error received. CDMA Engine halts at this descriptor
31	Transfer Completed. This indicates to the software application that the CDMA Engine has completed the transfer as described by the associated descriptor. The software application can manipulate any descriptor with the Completed bit set to 1. 0 = Descriptor not completed 1 = Descriptor completed. If the CDMA SG Engine fetches a descriptor, with this bit set to 1, the descriptor is considered a stale descriptor. An SGIntErr is flagged in the AXI CDMA Status register and the AXI CDMA engine halts with no update to the descriptor.

Simple CDMA Programming Example

1. Verify the CDMA is idle. Read CDMA Status register bit-1 as logic '1'.

2. Program the CDMA Control register bit-12 to the desired state for interrupt generation on transfer completion.

3. Write the source address for the transfer to the Source Address register at 0x0018. In this example, the source is the system memory. The following is required:

a. Given physical address of buffer of 0x0000333012345678.

b. AXIBAR2PCIEBAR_0U <offset 00001208> = 0x00003330.

(offset 00001000 is PCIe AXI Bridge Control base + 208 = AXIBAR2PCIEBAR_0)

c. AXIBAR2PCIEBAR_0L <offset 0000120C> = 0x12345678.

The least significant 19 bits of this address 0x12345678 must be added to the AXI BAR0 Aperture Base address. The new AXI address is 0x00080000 +0x0045678 = 0x000C5678. Write the value 0x000C5678 to the CDMA Source Address register at location 0x0020.

4. Write the destination address to the Destination Address register at 0x0020. For this example, the destination will be the sample buffer of the DAC interface. Write 0x0006_0000 to the Destination Address register at 0x0020.

5. Write the number of bytes to transfer to the CDMA Bytes to Transfer register 0x0028. Writing this register also starts the transfer.

6. Poll the CDMA Status register bit-1 (CDMA idle) for logic '1'.

8. When ready for another transfer. Go back to step 1.

AXI-BAR0 Aperture Base Address

The AXI BAR0 aperture base address of 0x00080000 is set as the base address on the AXI bus used to reach system host memory for CDMA transfers.

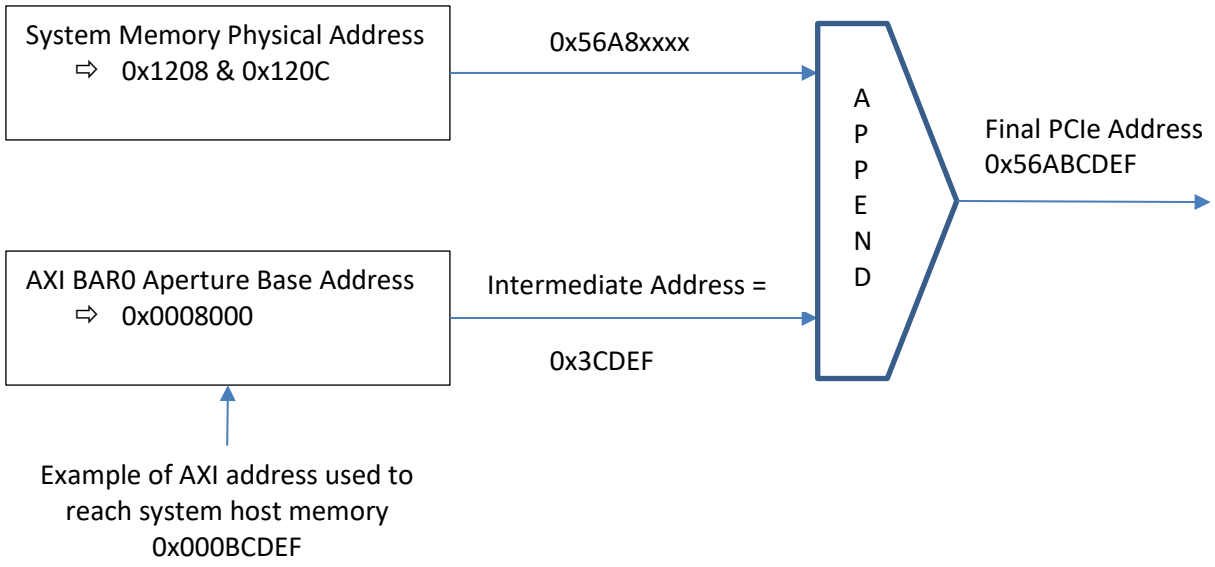
In Xilinx Vivado IP Integrator the address map will show that a 512K address space for the AXI BAR0 Aperture Base Address is reserved. This 512K address space is fixed for this module.

Table 4.19 AXI-BAR0 Aperture Base Address

0x00080000→0x000FFFFF	512K	Window into PCIe Interface AXI BAR0 Aperture Base Address

The following is another example of how the AXI BAR0 aperture base address is used.

For example, if the system buffer physical address 0x56ABCDEF were given, then the AXI Base Address Translation Configuration registers at BAR0 + 0x1208 and 0x120C must be set to 0x0 and 0x56ABCDEF, respectively. The least significant 19 bits of this address 0x56ABCDEF must be added to the AXI BAR0 Aperture Base address. The new AXI address is 0x00080000 + 0x003CDEF = 0x000BCDEF. These values are then appended by the PCIe AXI bridge to give the final PCIe address of the system memory location.



PCIe AXI-Bridge Control

The PCIe AXI Bridge is an interface between the AXI bus and the PCIe system. This bridge provides the address translation between the AXI4 memory-mapped embedded system and the PCIe system. The AXI Bridge for PCIe translates the AXI memory read or writes to PCIe Transaction Layer Packets (TLP) packets and translates PCIe memory read and write request TLP packets to AXI interface commands.

Table 4.20 PCIe AXI Bridge Control Registers

BAR0 Base Addr+	Bit(s)	Description
0x0000_1000→ 0x0000_1140	31:0	See Xilinx pg055 Memory Map
0x0000_1144	31:0	PHY Status/Control Register
0x0000_1148→ 0x0000_1204	31:0	See Xilinx pg055 Memory Map (These registers are not used)
0x0000_1208	31:0	Address Translation Register Upper AXIBAR2PCIEBAR_0U
0x0000_120C	31:0	Address Translation Register Lower AXIBAR2PCIEBAR_0L
0x0000_1210	31:0	Address Translation Register Upper AXIBAR2PCIEBAR_1U
0x0000_1214	31:0	Address Translation Register Lower AXIBAR2PCIEBAR_1L
0x0000_1210→ 0x0000_1FFF	31:0	See Xilinx pg055 Memory Map

PHY Status/Control Register (Read) – (BAR + 0x1144)

This register provides the status of the current PHY state, as well as control of speed and rate switching for Gen2-capable cores.

Table 4.21 PHY Status/Control Register (Read) – (BAR + 0x1144)

Bit(s)	Function	
0	Reports the current link rate.	
	0	2.5 GT/s
	1	5.0 GT/s
2-1	Reports the current link width.	
	00	x1
	01	x2
	10	x4
	11	x8
8-3	Reports the current Link Training and Status State Machine state. Encoding is specific to the underlying Integrated Block.	
	010110	L0 state and core can send/receive data packets
10-9	Reports the current lane reversal mode.	
	00	No reversal
	01	Lanes 1:0 reversed
	10	Lanes 3:0 reversed
	11	Lanes 7:0 reversed
11	Reports the current PHY Link-up state.	
	0	Link down
	1	Link up
15-12	Reserved	
31-16	See Xilinx pg055 PHY Status/Control Register	

AXI Base Address Translation Configuration Register

The address space for PCIe is different than the AXI address space. To access one address space from another address space requires an address translation process.

These registers are needed for DMA transfers that move data to the system memory buffer. Two AXI to Host address translation BARs are provided to support scatter-gather DMA operation: AXIBAR2PCIEBAR_0 and AXIBAR2PCIEBAR_1. It is expected that two host memory regions will be used, one which contains the scatter-gather descriptor list, and the other which contains DAC or ADC samples. The memory region holding the scatter-gather descriptor list must be physically contiguous. The memory region holding DAC or ADC samples is not required to be contiguous. The location of the system memory buffer is loaded into these registers. For data transfers that cross non-contiguous page boundaries, the scatter-gather descriptor list

must include updates to the AXI to Host address translation BARs for each non-contiguous region.

AXI Base Address Translation Configuration register at BAR0 + 0x1208 must be written with the most significant 32 bits of the address in system memory to which the DMA transfer is to read or write. An example of the C code used to set this register with the physical address is shown below.

AXI Base Address Translation Configuration register at BAR0 + 0x120C must be written with the least significant 32 bits of the address in system memory to which the DMA transfer is to read or write.

This sets the system memory physical address which will be appended with the values written into either the DMA source or destination registers at 0x1018 or 0x1020, respectively. See the example in the CDMA section for additional details.

Interrupt Controller

The AXI Interrupt Controller concentrates multiple interrupt inputs from peripheral devices to a single interrupt output to the system processor using the PCIe bus. The interrupt controller contains programmer accessible registers that allow interrupts to be enabled, queried and cleared under software control over the PCIe bus interface.

Table 4.22 Interrupt Controller Registers

BAR0 Base Addr+	Bit(s)	Description
0x0000_2000	31:0	Interrupt Status Register
0x0000_2004	31:0	Interrupt Pending Register
0x0000_2008	31:0	Interrupt Enable Register
0x0000_200C	31:0	Interrupt Acknowledge Register
0x0000_2010	31:0	Set Interrupt Enable Register
0x0000_2014	31:0	Clear Interrupt Enable Register
0x0000_2018	31:0	Reserved
0x0000_201C	31:0	Master Enable Register

Note that any registers/bits not mentioned will remain at the default value: logic low.

Interrupt Status Register (Read/Write) – (BAR0 + 0x2000)

This Interrupt Status register (ISR) at BAR0 base address + offset 0x2000 is used to monitor board interrupts. When read, the contents of this register indicate the presence or absence of an active interrupt for each of the active interrupting sources. Each bit in this register that is set to a '1' indicates an active interrupt signal on the corresponding interrupt input. Bits that are '0'are not active. The bits in the ISR are independent of the interrupt enable bits in the Interrupt Enable register. Interrupts, even if not enabled can still show up as active in the ISR.

Table 4.23 Interrupt Status Register (Read/Write) – (BAR0 + 0x2000)

Bit(s)	Function	
3-0	When set indicates DAC channel 0 to 3 requires service.	
	0	No service required
	1	In a single burst mode indicates burst complete. In FIFO mode, indicates FIFO is half full.
4	When set indicates an AXI CDMA interrupt. See the CDMA section for more information on the source of the interrupt.	
	0	Interrupt Inactive
	1	Interrupt Active
5	When set indicates that the ADC Data FIFO contains a number of samples equal to or greater than the value stored in the FIFO Full Threshold Register	
	0	Interrupt Inactive
	1	Interrupt Active
6	When set indicates a Counter interrupt. See the Counter section for more information on the source of the interrupt.	
	0	Interrupt Inactive
	1	Interrupt Active
7	When set indicates a Digital interrupt. See the Digital section for more information on the source of the interrupt.	
	0	No active Digital interrupt
	1	Active Digital interrupt

The ISR register is writable by software only until the Hardware Interrupt Enable bit in the MER has been set. Given these restrictions, when this register is written to, any data bits that are set to '1' will activate the corresponding interrupt just as if a hardware input became active. Data bits that are zero have no effect. This allows software to generate interrupts for test purposes.

Interrupt Pending Register (Read) – (BAR0 + 0x2004)

This Interrupt Pending register (IPR) at BAR0 base address + offset 0x2004 is used to monitor board interrupts. Reading the contents of this register indicates the presence or absence of an active interrupt signal that is also enabled. Each bit in this register is the logical AND of the bits in the Interrupt Status register and the Interrupt Enable register.

Table 4.24 Interrupt Pending Register (Read) – (BAR0 + 0x2004)

Bit(s)	Function	
3-0	When set indicates DAC channel 0 to 3 is pending.	
	0	No Interrupt Pending
	1	In a single burst mode indicates burst complete. In FIFO mode, indicates FIFO is half full.
4	When set indicates an AXI CDMA interrupt is pending. See the CDMA section for more information on the source of the interrupt.	
	0	No Interrupt Pending
	1	Interrupt Pending
5	When set indicates that the ADC Data FIFO threshold met or exceeded interrupt is pending.	
	0	No Interrupt Pending
	1	Interrupt Pending
6	When set indicates a Counter interrupt is pending. See the Counter section for more information on the source of the interrupt.	
	0	No Interrupt Pending
	1	Interrupt Pending
7	When set indicates a Digital interrupt is pending. See the Digital section for more information on the source of the interrupt.	
	0	No Interrupt Pending
	1	Interrupt Pending

Interrupt Enable Register (Read/Write) – (BAR0 + 0x2008)

This is a read/write register. Writing a '1' to a bit in this register enables the corresponding Interrupt Status bit to cause assertion of the interrupt output. The Interrupt Enable bit set to '0' does not inhibit an interrupt condition from being captured. It will still show up in the Interrupt Status register even when not enabled here. To show up in the Interrupt Pending register it needs to be enabled here. Writing a '0' to a bit disables, or masks, the generation of an interrupt output for the corresponding interrupt input signal. Note however, that disabling an interrupt input is not the same as clearing it. Disabling an active interrupt prevents that interrupt from reaching the IRQ output. When it is re-enabled, the interrupt immediately generates a request on the IRQ output. An interrupt must be cleared by writing to the Interrupt Acknowledge Register, as described below. Reading this Interrupt Enable register indicates which interrupt inputs are enabled; where a '1' indicates the input is enabled and a '0' indicates the input is disabled.

Table 4.25 Interrupt Enable Register (Read/Write) – (BAR0 + 0x2008)

Bit(s)	Function	
3-0	When set indicates DAC channel 0 to 3 interrupts are enabled.	
	0	Interrupt Disabled (default)
	1	Interrupt Enabled
4	When set indicates an AXI CDMA interrupt is enabled. See the CDMA section for more information on the source of the interrupt.	
	0	Interrupt Disabled (default)
	1	Interrupt Enabled
5	When set indicates that the ADC Data FIFO threshold met or exceeded interrupt is enabled.	
	0	Interrupt Disabled (default)
	1	Interrupt Enabled
6	When set indicates a Counter interrupt is enabled. See the Counter section for more information on the source of the interrupt.	
	0	Interrupt Disabled (default)
	1	Interrupt Enabled
7	When set indicates a Digital interrupt is enabled. See the Digital section for more information on the source of the interrupt.	
	0	Interrupt Disabled (default)
	1	Interrupt Enabled

Interrupt Acknowledge Register (Write) – (BAR0 + 0x200C)

The Interrupt Acknowledge register is a write-only location that clears the interrupt request associated with selected interrupt inputs. Note that writing one to a bit in the Interrupt Acknowledge register clears the corresponding bit in the Interrupt Status register and clears the same bit in the Interrupt Acknowledge register.

Writing a '1' to a bit location in the Interrupt Acknowledge register will clear the interrupt request that was generated by the corresponding interrupt input. An interrupt input that is active and masked by writing a '0' to the corresponding bit in the Interrupt Enable register will remain active until cleared by acknowledging it. Unmasking an active interrupt causes an interrupt request output to be generated (if the Master Interrupt Enable bit-0 in the Master Enable register is set). Writing 0s has no effect as does writing a '1' to a bit that does not correspond to an active input or for which an interrupt input does not exist. The bit locations in the Interrupt Acknowledge Register correspond with the bit locations given in the Interrupt Enable Register.

Table 4.26 Interrupt Acknowledge Register (Write) – (BAR0 + 0x200C)

Bit(s)	Function
3-0	Clear DAC channel 0 to 3 interrupt request.
4	Clear AXI CDMA interrupt request.
5	Clear ADC Data FIFO threshold met or exceeded interrupt request.
6	Clear Counter interrupt request.
7	Clear Digital interrupt request.
31-8	Reserved

Set Interrupt Enable Register (Write) – (BAR0 + 0x2010)

Set Interrupt Enable register is a location used to set Interrupt Enable register bits in a single atomic operation, rather than using a read / modify / write sequence. Writing a '1' to a bit location in the Set Interrupt Enable register will set the corresponding bit in the Interrupt Enable register. Writing 0s does nothing, as does writing a '1' to a bit location that corresponds to a non-existing interrupt input. The bit locations in the Set Interrupt Enable Register correspond with the bit locations given in the Interrupt Enable Register.

Table 4.27 Set Interrupt Enable Register (Write) – (BAR0 + 0x2010)

Bit(s)	Function
3-0	Set DAC channel 0 to 3 interrupt request.
4	Set AXI CDMA interrupt request.
5	Set ADC Data FIFO threshold met or exceeded interrupt request.
6	Set Counter Interrupt request.
7	Set Digital Interrupt request
31-8	Reserved

Clear Interrupt Enable Register (Write) – (BAR0 + 0x2014)

Clear Interrupt Enable register is a location used to clear Interrupt Enable register bits in a single atomic operation, rather than using a read / modify / write sequence. Writing a '1' to a bit location in Clear Interrupt Enable register will clear the corresponding bit in the Interrupt Enable register. Writing 0s does nothing, as does writing a '1' to a bit location that corresponds to a non-existing interrupt input. The bit locations in the Clear Interrupt Enable Register correspond with the bit locations given in the Interrupt Enable Register.

Table 4.28 Clear Interrupt Enable Register (Write) – (BAR0 + 0x2014)

Bit(s)	Function
3-0	Clear DAC channel 0 to 3 interrupt request.
4	Clear AXI CDMA interrupt request.
5	Clear ADC Data FIFO threshold met or exceeded interrupt request.
6	Clear Counter Interrupt request.
7	Clear Digital Interrupt request.
31-8	Reserved

Master Enable Register (Read/Write) – (BAR0 + 0x201C)

This is a 2-bit, read / write register. The two bits are mapped to the two least significant bits of the location. The least significant bit contains the Master Enable bit and the next bit contains the Hardware Interrupt Enable bit. Writing a '1' to the Master Enable bit enables the IRQ output signal. Writing a '0' to the Master Enable bit disables the IRQ output, effectively masking all interrupt inputs. The Hardware Interrupt Enable bit is a write-once bit. At reset, this bit is reset to '0', allowing the software to write to the Interrupt Status register to generate interrupts for testing purposes, and disabling any hardware interrupt inputs. Writing a '1' to this bit enables the hardware interrupt inputs and disables software generated inputs. Writing a '1' also disables any further changes to this bit until the device has been reset. Writing 1s or 0s to any other bit location does nothing. When read, this register will reflect the state of the Master Enable and Hardware Interrupt Enable bits. All other bits will read as 0s.

Table 4.29 Master Enable Register (Read/Write) – (BAR0 + 0x201C)

Bit(s)	FUNCTION	
0	Master IRQ Enable	
	0	All Interrupts Disabled
	1	All Interrupts Enabled
1	Hardware Interrupt Enable	
	0	Software Interrupts Enabled
	1	Hardware Interrupts Only Enabled
31-2	Not Used (bits are read as logic "0")	

AXI XADC Analog to Digital Converter (System Monitor) (Read) – (BAR0 + 0x3000)

The XADC Analog to Digital Converter is used to monitor the die temperature and supply voltages of the FGPA. The XADC channel sequencer is configured to continuously sample the temperature, Vccint and Vccaux channels. The results from the A/D conversions can be read at the addresses given in column one of Table 4.30.

Data bits 15 to 4 of these registers hold the "ADCcode" representing the temperature, Vccint, or Vccaux value. Data bits 3 to 0 are not used.

The 12-bits output from the ADC can be converted to temperature using the following equation.

$$Temperature(°C) = \frac{ADCcode \times 503.975}{4096} - 273.15$$

The 12-bits output from the ADC can be converted to voltage using the following equation.

$$SupplyVoltage(volts) = \frac{ADCcode}{4096} \times 3V$$

Additional information regarding the XADC can be found in the Xilinx XADC product guide PG019 and the user guide UG480

Table 4.30 System Monitor Register Map

Address	Status Register
0x0000_3200	Temperature
0x0000_3204	V_{CCINT}
0x0000_3208	V_{CCAUX}
0x0000_3280	Maximum Temperature
0x0000_3284	Maximum V_{CCINT}
0x0000_3288	Maximum V_{CCAUX}
0x0000_3290	Minimum Temperature
0x0000_3294	Minimum V_{CCINT}
0x0000_3298	Minimum V_{CCAUX}

The expected values for V_{CCINT}, $V_{CCINT,}$ and Temperature are shown in Table 4.31.

Table 4.31 Expected Operating Parameters

Parameter	Min	Max
V_{CCINT} Volts	0.95	1.05
V_{CCAUX}	1.71	1.89
Temperature (recommended)	-40°C	100°C

Firmware Revision Register (Read) – (BAR0 + 0x4000)

This is a read only register located at BAR0 + 0x4000. The ASCII code representing the current revision of the MCS firmware file is readable from this location. For example, if the firmware is at revision A then this register will read 0x41 in the least significant byte or B= 0x42, C=0x43, etc.

AXI Quad SPI

The serial flash memory is accessed through the AXI Quad SPI interface. For a thorough understanding of the interface refer to the Xilinx product guide pg153 and the commands section of the flash memory data sheet S25FL1-K_00. Following is a description of the AXI Quad SPI registers. The AXI Quad SPI interface has been configured as a standard mode (Quad message not

supported), master mode enabled, no FIFOs, and the interrupt output is not connected. The clock frequency ratio is set at 2 resulting in a 31.25MHz SPI clock. With the interrupt output unconnected, the Quad SPI IP Interrupt Status Register is still useful for reporting error conditions.

Table 4.32 AXI Quad SPI Register Map (BAR0 + 0x50xx)

Address	Register
0x0000_5040	Quad SPI Software Reset Register
0x0000_5060	Quad SPI Control Register
0x0000_5064	Quad SPI Status Register
0x0000_5068	Quad SPI Data Transmit Register
0x0000_506C	Quad SPI Data Receive Register
0x0000_5070	Quad SPI Slave Select Register
0x0000 5020	Quad SPI IP Interrupt Status Register

Quad SPI Software Reset Register (Write) – (BAR0 + 0x5040)

The Software Reset Register (SRR) permits resetting the core independently of other cores in the system. Writing 0x0000_000a to the SRR resets the core register for four AXI clock cycles. Any other write access generates undefined results and results in an error. The bit assignment in the software reset register is shown in and described in Table 4.33. Any attempt to read this register returns undefined data.

Table 4.33 Quad SPI Software Reset Register (BAR0 + 0x5040)

Bit(s)	Software Reset Register
0 - 31	The only allowed operation on this register is a write of 0x0000000a, which resets the AXI Quad SPI core

Quad SPI Control Register (Read/Write) – (BAR0 + 0x5060)

The SPI Control Register (SPICR) allows programmer control over various aspects of the AXI Quad SPI core. The bit assignment in the SPICR is described in Table 4.34.

Table 4.34 Quad SPI Control Register (BAR0 + 0x5060)

Bit(s)	Quad SPI Control Register	
0	Local loopback mode:	
	0	Normal Operation
	1	Loopback mode. The transmitter output is internally connected to the receiver input. The receiver and transmitter operate normally, except that received data (from remote slave) is ignored.
1	SPI system enable: Setting this bit to 1 enables the SPI devices as noted here. When set to:	

Bit(s)	Quad SPI Control Register	
	0	SPI system disabled. Both master and slave outputs are in 3-state and slave inputs are ignored.
	1	SPI system enabled. Master outputs active (for example, IO0 (MOSI) and SCK in idle state) and slave outputs become active if SS becomes asserted. The master starts transferring when transmit data is available.
2	Master (SPI master mode): Setting this bit configures the SPI device as a master or a slave. When set to:	
	0	Slave configuration
	1	Master configuration
3	Clock Polarity: Setting this bit defines the clock polarity. When set to:	
	0	Active-High clock; SCK idles low.
	1	Active-Low clock; SCK idles high.
4	Clock phase: Setting this bit selects one of two fundamentally different transfer formats.	
	0	Data valid on first SCK edge after SS asserted
	1	Data valid on second SCK edge after SS asserted
5	TX FIFO reset: When written with '1', this bit forces a reset of the transmit FIFO to the empty condition. This bit will read as '0'.	
	0	Transmit FIFO normal operation
	1	Reset transmit FIFO pointer
6	RX FIFO reset: When written with '1', this bit forces a reset of the receive FIFO to the empty condition. This bit will read as '0'.	
	0	Receive FIFO normal operation
	1	Reset receive FIFO pointer
7	Manual slave select assertion enable: This bit forces the data in the slave select register to be asserted on the slave select output anytime the device is configured as a master and the device is enabled (SPE asserted). When set to:	
	0	Slave select output asserted by master core logic.
	1	Slave select output follows data in slave select register.
8	Master transaction inhibit:	

Bit(s)	Quad SPI Control Register	
	This bit inhibits master transactions. This bit has no effect on slave operation. When set to:	
	0	Master transactions enabled.
	1	1 = Master transactions disabled. Note: This bit immediately inhibits the transaction. Setting this bit while transfer is in progress would result in unpredictable outcome.
9	LSB first: This bit selects LSB first data transfer format. The default transfer format is MSB first. When set to:	
	0	MSB first transfer format.
	1	LSB first transfer format. Note: In Dual/Quad SPI mode, only the MSB first mode of the core is allowed.
10 - 31	Reserved	

Quad SPI Status Register (Read) – (BAR0 + 0x5064)

The Quad SPI Status Register (SPISR) is a read-only register that provides the status of some aspects of the AXI Quad SPI core to the programmer. The bit assignment in the SPISR is described in Table 4.35. Writing to the SPISR does not modify the register contents.

Table 4.35 Quad SPI Status Register (BAR0 + 0x5064)

Bit(s)	Quad SPI Status Register	
0	Receive Register Empty: This bit is set High when the receive register is empty.	
	0	Rx register Is not empty
	1	Rx register is empty
1	Receive Register Full: This bit is set High when the Receive Register is full.	
	0	Rx register not full
	1	Rx register full
2	Transmit Register empty: This bit is set to High when the transmit register is empty. This bit goes High as soon as the TX register becomes empty.	
	0	Tx register not empty
	1	Tx register empty
3	Transmit Register Full: This bit is set High when the transmit register is full.	
	0	Tx register not full
	1	Tx register full
4	Mode-fault error flag:	

Bit(s)	Quad SPI Status Register	
	This flag is set if the SS signal goes active while the SPI device is configured as a master. MODF is automatically cleared by reading the SPISR. A Low-to-High MODF transition generates a single-cycle strobe interrupt.	
	0	No error
	1	Error condition detected
5	Slave_Mode_Select flag: This flag is asserted when the core is configured in slave mode. Slave_Mode_Select is activated as soon as the master SPI core asserts the chip select pin for the core.	
	0	Asserted when core configured in slave mode and selected by external SPI master
	1	Default in standard mode
6	CPOL_CPHA_Error flag: When set indicates an invalid combination of CPOL and CPHA has been selected.	
	0	Default.
	1	The CPOL and CPHA are set to 01 or 10.
7	Slave mode error flag.	
	0	Master mode is set in the control register (SPICR).
	1	This bit is set when the core is configured with dual or quad SPI mode and the master is set to 0 in the control register (SPICR).
8	MSB error flag	
	0	Default
	1	LSB first bit set in SPICR (not valid for quad mode)
9	Loopback error flag	
	0	Default. The loopback bit in the control register is at default state.
	1	When the SPI command, address, and data bits are set to be transferred in other than standard SPI protocol mode and this bit is set in control register (SPICR).
10	Command error flag	
	0	Default
	1	The first entry in SPI DTR FIFO is incompatible with the command list for the attached flash device
11 - 31	Reserved	

Quad SPI Data Transmit Register (Write) – (BAR0 + 0x5068)

The Quad SPI Data Transmit Register (SPI DTR) is written with the data to be transmitted on the SPI bus. After the SPE bit is set to 1 in master mode or spisel is active in the slave mode, the data is transferred from the SPI DTR to the shift register.

If a transfer is in progress, the data in the SPI DTR is loaded into the shift register as soon as the data in the shift register is transferred to the SPI DRR and a new transfer starts. The data is held in the SPI DTR until replaced by a subsequent write. The SPI DTR is described in Table 4.36.

This register cannot be read and can only be written when it is known that space for the data is available. If an attempt to write is made on a full register, the AXI write transaction completes with an error condition. Reading the SPI DTR is not allowed and the read transaction results in undefined data.

Table 4.36 Quad SPI Data Transmit Register (BAR0 + 0x5068)

Bit(s)	Quad SPI Data Transfer Register
0 - 7	SPI transmit data
8 - 31	Reserved

Quad SPI Data Receive Register (Read) – (BAR0 + 0x506C)

The Quad SPI Data Receive Register (SPI DRR) is used to read data that is received from the SPI bus. This is a double-buffered register. The received data is placed in this register after each complete transfer.

If the SPI DRR was not read and is full, the most recently transferred data is lost and a receive overrun interrupt occurs.

If an attempt is made to read an empty receive register, it gives out an error in the Status register. Writes to the SPI DRR do not modify the register contents and return with a successful OK response.

The power-on reset values for the SPI DRR are unknown. When known data has been written into the SPI DRR during core transactions, the data in this register can be considered for reading. The SPI DRR is described Table 4.37.

IMPORTANT: Based on the command that is issued to the SPI device, a certain unwanted number of bytes are written to the Receive register. These bytes have to be discarded.

Table 4.37 Quad SPI Data Receive Register (BAR0 + 0x506C)

Bit(s)	Quad SPI Data Receive Register
0 - 7	SPI receive data
8 - 31	Reserved

Quad SPI Slave Select Register (Read/Write) – (BAR0 + 0x5070)

The SPI Slave Select Register (SPISSR) contains an active-low, slave select vector SS of length one. The bit assignment in the SPISSR is described in Table 4.38.

Table 4.38 Quad SPI Slave Select Register (BAR0 + 0x5070)

Bit(s)	Quad SPI Slave Select Register
0	Set to zero to select flash device
1 - 31	Reserved

Quad SPI IP Interrupt Status Register (Read/Write) – (BAR0 + 0x5020)

The IP Interrupt Status Register (IPISR) collects all of the events. Bit assignments are described in Table 4.39. The interrupt register is a read/toggle-on-write register. Writing a 1 to a bit position within the register causes the corresponding bit to toggle. All register bits are cleared on reset.

Table 4.39 IP Interrupt Status Register (BAR0 + 0x5020)

Bit(s)	IP Interrupt Status Register
0	Mode-fault error. This interrupt is generated if the SS signal goes active while the SPI device is configured as a master. This bit is set immediately on SS going active.
1	Slave mode-fault error. This interrupt is generated if the SS signal goes active while the SPI device is configured as a slave, but is not enabled. This bit is set immediately on SS going active and continually set if SS is active and the device is not enabled.
2	Data transmit register empty. It is set when the last byte of data has been transferred out to the external flash memory. In master mode if this bit is set to 1, no more SPI transfers are permitted.
3	Data transmit register underrun. This bit is set at the end of a SPI element transfer by a one-clock period strobe to the interrupt register when data is requested from an empty transmit register by the SPI core logic to perform a SPI transfer. This can occur only when the SPI device is configured as a slave in standard SPI configuration and is enabled by the SPE bit as set. All zeros are loaded in the shift register and transmitted by the slave in an under-run condition.
4	Data receive register full. This bit is set at the end of the SPI element transfer, when the receive register has been filled by a one-clock period strobe to the interrupt register.
5	Data receive register overrun. This bit is set by a one-clock period strobe to the interrupt register when an attempt to write data to a full receive register is made by the SPI core logic to complete a SPI transfer. This can occur when the SPI device is in either master or slave mode (in standard SPI mode) or if the IP is configured in SPI master mode (dual or quad SPI mode).
6	Reserved
7	Slave select mode.

Bit(s)	IP Interrupt Status Register
	The assertion of this bit is applicable only when the core is configured in slave mode in standard SPI configuration. This bit is set when the other SPI master core selects the core by asserting the slave select line. This bit is set by a one-clock period strobe to the interrupt register. Note: This bit is applicable only in standard SPI slave mode.
8 – 31	Reserved

Serial Flash Write/Read Example

This section describes a suggested sequence for accessing the serial Flash. This example reads the Manufacturer's ID and device ID from the flash.

One time, at startup, write the Quad SPI Software Reset Register and the Quad SPI Control registers.

Write 0x0000000A to address 0x00005040 to reset the interface

Write 0x000000E6 to address 0x00005060 to configure the Quad SPI interface as a master, set the Clock Phase and Polarity, and select manual slave select mode.

At the start of each Flash command
Write 0x00000000 to address 0x00005070 to select the slave device.

Write 0x00000090 to address 0x00005068 to write the Flash command to initiate the read ID register sequence to the transmit data register.

Read from 0x00005064 until bit 1, receive register full is set.

Read from 0x0000506C to empty the receive data register.

Write 0x00000000 to address 0x00005068 to write command byte 2 to the transmit data register.

Read from 0x00005064 until bit 1, receive register full is set.

Read from 0x0000506C to empty the receive data register.

Write 0x00000000 to address 0x00005068 to write command byte 3 to the transmit data register.

Read from 0x00005064 until bit 1, receive register full is set.

Read from 0x0000506C to empty the receive data register.

Write 0x00000000 to address 0x00005068 to write command byte 4 to the transmit data register.

Read from 0x00005064 until bit 1, receive register full is set.

Read from 0x0000506C to empty the receive data register. The value should be 0x00.

Write 0x00000000 to address 0x00005068 to write command byte 5 to the transmit data register.

Read from 0x00005064 until bit 1, receive register full is set.

Read from 0x0000506C to empty the receive data register. The value should be the manufacturer's ID 0x01.

Write 0x00000000 to address 0x00005068 to write command byte 6 to the transmit data register.

Read from 0x00005064 until bit 1, receive register full is set.

Read from 0x0000506C to empty the receive data register. The value should be the device ID 0x15.

At the end of each Flash command
Write 0x00000001 to address 0x00005070 to de-select the slave device.

Location in System Register (Read) – (BAR0 + 0x6000)

The Location Register provides the interface to the carrier's Slot ID CPLD. A read of this register triggers a serial transfer from the carrier's Slot ID CPLD to the Location Register. The unique ID enables system software to distinguish a particular AcroPack module from other similar modules.

Table 4.40 Slot ID Register (BAR0 +0x6000)

Bit(s)	Location in System Register	
0 - 2	Carrier site	
	"000"	site "A"
	"001"	site "B"
	⋮	⋮
	"111"	site "H"
3 - 7	Carrier identification. These bits are set by the backplane global address (VPX carrier).	
8 – 31	Reserved	

ADC, Digital I/O and Counter Memory Map

The memory space starting at BAR0 base address plus offset 0x7000 to 0x7FFF is reserved to access the ADC control registers, the Digital I/O registers and the Counter Timer registers.

Table 4.41 ADC/Digital/Counter Memory Map

BAR0 Base Address	Bit(s)	Description
0x0000 7000	31:0	Global Interrupt Status Register
0x0000 7004	31:0	Global Interrupt Enable Register
0x0000 7008	31:0	ADC Control Register
0x0000 700C	31:0	ADC Range Enable Channel 0 to 7
0x0000 7010	31:0	Not Used

BAR0 Base Address	Bit(s)	Description
0x0000 7014	31:0	ADC Conversion Time Register
0x0000 7018	31:0	ADC FIFO Full Threshold
0x0000 701C	31:0	ADC Start Conversion Register
0x0000 7020	31:0	ADC FIFO Data and Tag Register
0x0000 7024→ 0x0000 703C	31:0	Not Used
0x0000 7040	31:0	16-bit Digital I/O Register
0x0000 7044	31:0	Digital I/O Direction Control Register
0x0000 7048	31:0	Digital I/O Interrupt Type Register
0x0000 704C	31:0	Digital I/O Interrupt Polarity Register
0x0000 7050	31:0	Debounce Enable Register
0x0000 7054	31:0	Debounce Duration Select Register
0x0000 7058→ 0x0000 706C	31:0	Not Used
0x0000 7070	31:0	Counter Trigger, Stop, Load Read Back, and Toggle Constant Register
0x0000 7074	31:0	Counter Control Register
0x0000 7078	31:0	Counter Interrupt Information Register
0x0000 707C	31:0	Counter Read Back Register
0x0000 7080	31:0	Counter Constant A Register 1
0x0000 7084	31:0	Counter Constant A Register 2
0x0000 7088	31:0	Counter Constant B Register 1
0x0000 708C	31:0	Counter Constant B Register 2
0x0000 7090→ 0x0000 709C	31:0	Not Used
0x0000 70A0	15:0	ADC Channel 0 Offset
0x0000 70A4	15:0	ADC Channel 1 Offset
0x0000 70A8	15:0	ADC Channel 2 Offset
0x0000 70AC	15:0	ADC Channel 3 Offset
0x0000 70B0→ 0x0000 70BC	15:0	ADC Channel 4- 7 Offset
0x0000 70C0→ 0x0000 70DC	31:0	Not Used
0x0000 70E0	17:0	ADC Channel 0 Gain
0x0000 70E4	17:0	ADC Channel 1 Gain
0x0000 70E8	17:0	ADC Channel 2 Gain
0x0000 70EC	17:0	ADC Channel 3 Gain
0x0000 70F0→ 0x0000 70FC	17:0	ADC Channel 4- 7 Gain
0x0000 7100→ 0x0000 7FFF	31:0	Not Used

The module will respond to addresses that are "NOT USED." The board will return "0" for all address reads that are not used or reserved.

Global Interrupt Status Clear Register (Read/Write) – (BAR0 + 7000H)

The Interrupt Status Register reflects the status of each of the Digital interrupting channels, and Counter Timer interrupts.

Read of this bit reflects the interrupt pending status.

0 = Interrupt Not Pending

1 = Interrupt Pending

A function that does not have interrupts enabled will never set its interrupt status flag.

Write a logic "1" to this bit to release/clear a pending interrupt.

However, if the condition which caused the interrupt to occur remains, the interrupt will be generated again (unless disabled via its Interrupt Enable Register). Writing "0" to a bit location has no effect; that is, a pending interrupt will remain pending.

The Interrupt Status register at the base address + offset 7000H is used to control digital channels 0 through 15 via data bits 0 to 15, and counter interrupt via bit-24. For example, channel 0 is controlled via data bit-0.

The function of each of the interrupt register bits are described in the following table. This register can be read or written with either 8-bit, 16-bit, or 32-bit data transfers. A power-up or system reset sets all interrupt register bits to 0.

Table 4.42 Global Interrupt Status Clear Register (Read/Write) – (BAR0 + 7000H)

Bit	Function
0	Digital Channel 0 Interrupt Pending/Clear
1	Digital Channel 1 Interrupt Pending/Clear
:	:
15	Digital Channel 15 Interrupt Pending/Clear
16	NOT USED
:	NOT USED
23	NOT USED
24	Counter/Timer Interrupt Pending/Clear
31-25	NOT USED

Note that any registers/bits not mentioned will remain at the default logic level low.

Global Interrupt Enable Register (Read/Write) – (BAR0 + 7004H)

The Interrupt Enable Register provides a mask bit for each of the interrupting functions. A "0" bit will prevent the corresponding function from generating an external interrupt. A "1" bit will allow the corresponding function to generate an interrupt.

The Interrupt Enable register at the base address + offset 7004H is used to control channels 0 through 15 via data bits 0 to 15, and counter interrupt via bit-24. For example, digital channel 0 is controlled via data bit-0.

All function interrupts are disabled (set to "0") following a power-on or software reset. Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers.

Table 4.43 Global Interrupt Enable Registers (Read/Write) – (BAR0 + 7004H)

Bit	Function
0	Digital Channel 0 Interrupt Enable
1	Digital Channel 1 Interrupt Enable
:	:
15	Digital Channel 15 Interrupt Enable
16	NOT USED
:	NOT USED
23	NOT USED
24	Counter/Timer Interrupt Enable
31-25	NOT USED

Note that any registers/bits not mentioned will remain at the default logic low.

ADC Control Register (Read/Write) – (BAR0 + 7008H)

This read/write register is used to enable single or continuous conversions, select & control external trigger input/output modes, monitor FIFO status, and issue a software reset to all but DAC logic, and issue software reset to ADC logic.

The function of each of the control register bits is described in the following table.

Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers.

Table 4.44 ADC Control Register (Read/Write) – (BAR0 + 7008H)

Bit(s)	Function	
1 to 0	Conversion Mode:	
	00	Conversions are disabled.
	01	Enable Single Conversion Mode. A single conversion is initiated per software start convert or external trigger. The internal channel timer controls the start conversion of all channels. Conversions must be disabled and reenabled between consecutive single conversions.

Bit(s)	Function	
	10	Enable Continuous Conversion Mode. Conversions are initiated by a software start or external trigger and continued by internal hardware triggers generated at the frequency set by the interval timer registers.
	11	Reserved
3 to 2	Not Used	
5 to 4	External Trigger Mode: As an output, internal timer triggers are generated on the External Trigger out pin of the field I/O connector. The External Trigger output signal can be used to synchronize the conversion of multiple modules. Note that the External Trigger input can be sensitive to external EMI noise which can cause erroneous external triggers. If External Trigger input or output is not required, the External Trigger should be configured as disabled.	
	00	External Trigger Disabled
	01	External Trigger Input
	10	External Trigger Output
	11	Reserved
6	Auto DMA Transfer: With Auto DMA Transfer enabled, a DMA transfer of <threshold> size will be automatically kicked off in hardware. Note that the CDMA control, source and destination registers as well as the FIFO threshold register must be set properly prior to setting this bit.	
	0	Hardware initiated DMA transfers disabled.
	1	DMA transfers are initiated automatically in hardware when the FIFO threshold has been met or exceeded.
7	Not Used	
8 status	FIFO Empty Status:	
	0	FIFO Empty
	1	FIFO Not Empty
9 status	FIFO Threshold Status:	
	0	FIFO has less than the number of samples defined by the Threshold Register.
	1	FIFO Threshold Reached. This bit is set when the FIFO contains the number of data samples set by the Threshold Register.
10 status	FIFO Full Status:	
	0	FIFO Not Full.
	1	FIFO Full
11	0	ADC channels 0 to 7 not Busy

Bit(s)	Function	
Busy Status	1	ADC channels 0 to 7 Busy
13 to 12	Not Used	
14	1 = Software Reset This software reset bit will reset the global interrupt enable, digital I/O registers, digital direction registers to input, digital I/O interrupt enable, interrupt type, interrupt polarity, debounce enables, debounce durations, counter logic to cleared and disabled states.	
15	1 = Software Reset The software reset bit will clear this Control Register, the Channel Enable Register, and FIFO buffer. It will also reset the FIFO Threshold Register to its default value of 1023 decimal and set the gain and offset registers to one (0x10000) and zero, respectively.	
31 to 16	Not Used	

Digital channel 3 is the ADC External Trigger Input (active high) and digital channel 9 is the ADC External Trigger output (active high).

Note that any registers or bits not mentioned will remain at the default logic low.

ADC Range Select Channel Enable Register (Read/Write) – (BAR0 + 700CH)

Channels 0 to 7 share the one ADC range control of bits 23 to 0 at BAR0 + 0x0000 700C. A write to this register will set the corresponding ADC range as designated in the following table. Read of this register will return the current setting for corresponding channels.

Bipolar range selections that are available include:

+10.24 Vdc to -10.24 Vdc

+10.0 Vdc to -10.0 Vdc

+5.12 Vdc to -5.12 Vdc

+5.0 Vdc to -5.0 Vdc

Unipolar ranges selections that are available include:

+10.24 Vdc to 0 Vdc

+10.0 Vdc to 0 Vdc

+5.12 Vdc to 0 Vdc.

The output data coding is in binary two's compliment for all bipolar ranges and in straight binary format for all unipolar ranges. The digital output code corresponding to each of the given ideal analog input values is given in the following table.

Most sensors, signal conditioning amplifiers and filter networks with less than 10kΩ of source impedance can drive the ADC directly. All unused ADC inputs should be tied to ground.

Table 4.45 ADC Range Select Register and Corresponding Digital Output Codes – (BAR0 + 700CH)

Bit(s)	Function
2 to 0	ADC Channel 0
5 to 3	ADC Channel 1
8 to 6	ADC Channel 2
11 to 9	ADC Channel 3
14 to 12	ADC Channel 4
17 to 15	ADC Channel 5
20 to 18	ADC Channel 6
23 to 21	ADC Channel 7
31 to 24	NOT USED

Bits 23 – 0	DESCRIPTION	ANALOG INPUT	
111	+ Full Scale Minus One LSB	10.2396 Volts	7FFF hex
	Midscale	0 Volts	0 hex
	One LSB Below Midscale	-312.5 µV	FFFF hex
	Minus Full Scale	-10.24 Volts	8000 hex
110	+ Full Scale	9.9996 Volts	7FFF hex
	Midscale	0 Volts	0 hex
	One LSB Below Midscale	-305.176 µV	FFFF hex
	Minus Full Scale	-10.0 Volts	8000 hex
101	+ Full Scale	10.23984 Volts	FFFF hex
	Midscale	5.12 Volts	8000 hex
	One LSB Below Midscale	-156.25 µV	7FFF hex
	Minus Full Scale	0 Volts	0000 hex
100	+ Full Scale	9.999847 Volts	FFFF hex
	Midscale	5.0 Volts	8000 hex
	One LSB Below Midscale	5.0 -152.588 µV = 4.99984 V	7FFF hex
	Minus Full Scale	0 Volts	0000 hex
011	+ Full Scale	5.119843 Volts	7FFF hex
	Midscale	0 Volts	0 hex
	One LSB Below Midscale	-156.25 µV	FFFF hex
	Minus Full Scale	-5.12 Volts	8000 hex
010	+ Full Scale	4.999847 Volts	7FFF hex
	Midscale	0 Volts	0 hex
	One LSB Below Midscale	-152.588 µV	FFFF hex
	Minus Full Scale	-5.0 Volts	8000 hex
001	+ Full Scale	5.11992 Volts	FFFF hex
	Midscale	2.56 Volts	8000 hex

Bits 23 – 0	DESCRIPTION	ANALOG INPUT	
	One LSB Below Midscale	2.56 V -78.125 µV = 2.55992 V	7FFF hex
	Minus Full Scale	0 Volts	0000 hex
000	Channel Disabled		
Only those channels enabled are stored into the channel data FIFO			

Note that any register or bits not mentioned will remain at the default logic low.

ADC Conversion Time Register (Read/Write) – (BAR0 + 7014H)

Timed periodic triggering can be used to achieve precise time intervals between conversions. The Conversion Timer register is a 32-bit register value that controls the interval time between conversions of all enabled channels.

The Channel Conversion Timer is used to control the frequency at which the conversion cycle is repeated for all enabled channels. For example, upon software or external trigger, channel 0 is converted. The time programmed into the Conversion Timer Register determines when channel 1 is converted. If Continuous Conversions are selected via the Control Register, the conversions will continue until disabled.

The 32-bit Conversion Timer value divides a 62.5MHz clock signal. The output of the Conversion Timer is used to precisely generate periodic trigger pulses to control the frequency at which all enabled channels are converted. The time period between trigger pulses is described by the following equation:

(Conversion Timer Value + 1) ÷ 62,500,000Hz = T (in seconds)

Where:

T = the desired time period between trigger pulses in seconds.

Conversion Timer Value can be a minimum of 78 decimal 0x4E hex and the maximum value is 4,294,967,295 decimal 0xFFFFFFFF hex.

The maximum period of time which can be programmed to occur between simultaneous conversions is (4,294,967,295 + 1) ÷ 62,500,000 = 68.71947 seconds. The minimum time interval which can be programmed to occur is (78 + 1) ÷ 62,500,000 = 1.264µ seconds. This minimum of 1.264µs is defined by the minimum conversion time of the hardware.

The 1.264µ seconds maximum sample rate corresponds to a maximum sampling frequency of 791,139.24Hz. The maximum analog input frequency should be band limited to one half the sample frequency. An anti-aliasing filter should be added to remove unwanted signals above ½ the sample frequency in the input signal (before the ADC) for critical applications.

The register's contents are cleared upon reset.

ADC FIFO Full Threshold Register (Read/Write) – (BAR0 + 7018H)

The FIFO Full Threshold register is a 10-bit register that is used to control when an interrupt will be generated and/or a DMA transfer will occur. The events enabled in the ADC Control Register will occur when the FIFO contains the number of samples equal to the FIFO Full Interrupt Threshold value. This register allows selection of any FIFO depth from 5 up to 1023 samples in the 1026 sample FIFO.

This register's contents are cleared upon reset. Any register bits not used will remain at the default value logic low.

An interrupt request will remain asserted to the system as long as the FIFO threshold is met or exceeded, and interrupts are enabled. The interrupt request can be removed by 1) disabling interrupts on the module or 2) reading the FIFO until it has fewer samples in it than defined by the threshold register. Note that ADC Data FIFO met or exceeded interrupts must first be enabled in the interrupt enable register at BAR0+ 0x2010. Please see Interrupt Controller section for more details on interrupts. The default FIFO Full Interrupt Threshold is 1023 samples. A reset will program it to this default value.

ADC Start Conversion Register (Write) – (BAR0 + 701C)

The Start Convert register is write-only and is used to trigger conversions by setting data bit-0 to a logic one. This method of starting conversions is most useful for its simplicity and for when precise timing of conversion is not critical. Typically, software triggering is used for initiating the first conversion. The desired mode of data acquisition must first be configured by setting the following registers to the desired values and modes: Interrupt, Control, ADC Channel Enable, ADC Conversion Timers and CDMA, if necessary.

Data bit-0 must be a logic one to initiate data conversions.

ADC FIFO Channel Data and Tag Register (Read/Write) – (BAR0 + 7020H)

Channels 0 to 7 share a 1026 sample deep FIFO buffer. The FIFO samples are 16-bit data values with a 3-bit channel tag.

The FIFO will be cleared by implementing a software or hardware reset. Any bits not used will remain at the default logic low.

Table 4.46 ADC FIFO Channel Data and Tag Register (Read/Write) – (BAR0 + 7020)

Bit(s)	Function
15 to 0	FIFO Channel Data
18 to 16	FIFO Channel Tag
31 to 19	NOT USED

Gain and offset correction will be applied to each sample prior to writing the result into the FIFO. The addition and multiplication operations are done in FPGA hardware using the FPGA's DSP blocks. The gain and offset registers are set to one and zero respectively upon reset to pass uncorrected ADC values to

the FIFO. Typical start-up operations would include reading factory calibration constants from the flash memory and writing the appropriate correction values for the gain and offset registers for each ADC.

Since all channels share the same FIFO, channel data tagging is implemented. The tag value identifies the channel to which the data corresponds.

Care should be taken when reading data from the FIFO buffer to ensure the FIFO is not empty when a new read is initiated. The FIFO Empty status bit can be read, in the control register, prior to reading the FIFO to avoid reading erroneous data.

If the FIFO exceeds 1026 samples, no more data will be written to the FIFO until data is read and space is freed. It is recommended that interrupts or Auto DMA Transfer be enabled upon meeting the FIFO's set threshold condition.

Modes of Conversion

The AP73x provides two methods of analog input operation for maximum flexibility with different applications. The following sections describe the Features of each method and how to best use them.

Single Conversion Mode

In Single Conversion mode of operation, conversions are initiated by a software or external trigger. Upon the trigger, channels 0 to 7 will be sequentially converted. All channels enabled with a valid range code in the ADC Range Enable Channel 0 to 7 will be tagged with their channel number and stored to FIFO memory. No additional conversions will be initiated unless a new software or external trigger is generated.

To select this mode of operation bits 1 and 0 of the Channel Control register must be set to digital code "01". Then, issuing a software start convert or external trigger will initiate conversions. The Conversion Timer must also be programmed for this mode of operation.

This mode of operation can be used to initiate conversions based upon external triggers. This can be used to synchronize multiple modules to a single module running in a continuous conversion mode. The external trigger of an "master" must be programmed as an output. The external trigger output signal of that module must then be connected to the external trigger input signal of all other modules that are to be synchronized. These other modules must be programmed for Single Conversion mode and external trigger input. Data conversion can then be initiated via the Start Convert bit of the master module configured for continuous conversion mode.

Continuous Conversion Mode

In the Continuous Conversion mode of operation, the hardware controls the continuous conversions of all enabled channels. All channels 0 to 7 are converted at the rate specified by the Conversion Timer.

To initiate this mode of operation bits 1 and 0 of the Channel Control register must be set to digital code "10". Then, issuing a software start convert or external trigger will initiate the continuous conversions of all enabled channels.

Automatic DMA Transfer

In the case where data must be quickly read from the FIFO, Auto DMA Transfer is recommended. Initiate this mode of operation by setting bit 6 of the ADC Control Register to '1'.

Auto-DMA Mode will automatically start a DMA transfer in the amount of the threshold value, once the threshold value is met. The CDMA Control Register, Source and Destination Registers must be properly written before the start of conversions. Keyhole Reading must be enabled in the CDMA control register. It is recommended that DMA completion interrupts be used to signal when new data is available at the specified destination.

When choosing a FIFO threshold value, the conversions time, number of channels enabled and the time for a DMA transfer to complete in the system must be considered.

Programming Considerations

The AP73x provides different methods of analog input acquisition to give the user maximum flexibility for each application. Examples are presented in the following sections to illustrate programming the different modes of operation.

Continuous Conversion Mode with Interrupt Example

This example will enable channels 0 through 7 for the continuous conversion mode of operation. Interrupts are enabled and an interrupt threshold of 430 samples is programmed. The Conversion Timer will be set for a 1.344µ second interval. Conversions can be initiated via software or external trigger.

1. Execute write of 0020H to the Interrupt Enable Register at Base Address + 2008H. This will enable FIFO Threshold met or exceeded interrupts on the module.
2. Execute write of 0002H to the Control Register at Base Address + 7008H. This selects continuous conversion mode.
3. Execute write of 00FF FFFFH to the ADC Range Enable Channel Register at Base Address + 700CH. This will permit the values corresponding to channels 0 to 7 to be stored in the data FIFO using the +/-10.24-volt input range.
4. Execute write of 53H to the Conversion Timer register at Base Address + 7014H. This sets the interval time between conversions to 1.344µ seconds.
5. Execute write of 1AEH to the FIFO Full Threshold register at Base Address + 7018H. The AP73x will issue an interrupt to the system when 430 or more samples are present in the FIFO.

6. Execute write of 0001H to the Start Convert Bit at Base Address + 701CH. This starts the sequential conversion of channels 0 to 7. The interval between channel conversions is 1.344µ seconds.

Single Conversion Mode Example

This example will enable channels 0, 3 and 6 for the single conversion mode of operation. Conversions can be initiated via software or external trigger.

1. Execute write of 0001H to the Control Register at Base Address + 7008H. This enables single conversion mode.
2. Execute write of 1C0E07H to the ADC Range Enable Channel Register at Base Address + 700CH. This will permit the values corresponding to channels 0, 3, and 6 to be stored in the data FIFO using the +/- 10.24-volt input range.
3. Execute write of 0001H to the Start Convert Bit at Base Address + 701CH. This starts the conversion of channels 0, 3 and 6.

Automatic DMA Mode Example

This example will show how to use the Auto-DMA mode to transfer data quickly from the FIFO to a destination location.

1. Execute write of 0010H to the Interrupt Enable Register at Base Address + 2008H. This will enable AXI CDMA interrupts.
2. Execute write of 5010H to the CDMA Control Register at Base Address + 0000H. This will enable Simple DMA mode with keyhole read and interrupt on complete.
3. Execute write of 7020H to the CDMA Source Register at Base Address + 0018h
4. Write CDMA Destination Register. Refer to the AXI-BAR0 Aperture Base Address section for more information on how to obtain a destination address in host memory.
5. Execute write of 0042H to the Control Register at Base Address + 7008H. This will enable continuous conversion mode and auto-DMA.
6. Execute write of 00FF FFFFH to the ADC Range Enable Channel 0 to 7 Register at Base Address + 700CH. This will permit the values corresponding to channels 0 to 7 to be stored in the data FIFO using the +/-10.24-volt input range.
7. Execute write of 3E7H to the Conversion Timer Register at Base Address + 7014H for a conversion time of 16µs.
8. Execute write of 200H (512 decimal) to the Threshold Register at Base Address + 7018H.
9. Execute write of 0001H to the Start Convert Bit at Base Address + 701CH. This will start continuous conversion of all channels. When the FIFO threshold is met, a DMA transfer of 512 samples will take place and the completion of the transfer will be signaled in the form of a

DMA completion interrupt. Conversions will not stop; the FIFO will continuously be filled, and samples will be transferred until conversions are disabled via the ADC Control Register.

Digital Input/Output Registers (Read/Write) – (BAR0 + 7040H)

Sixteen possible input/output channels numbered 0 through 15 may be individually accessed via these registers. The Input/Output Digital register is used to monitor/read or set/write channels 0 through 15. Channels 0 to 15 are accessed at the carrier base address +7040H via data bits 0 to 15.

Channel read/write operations use 8-bit, 16-bit, or 32-bit data transfers with the lower ordered bits corresponding to the lower-numbered channels for the register of interest. All input/output channels are configured as inputs on a power-on or software reset. The unused upper 16 bits of this register are "Not Used" and will always read low (0's).

If counter control input signals are used or an ADC or DAC trigger signal is enabled for input, then the Direction Control Register bit-0 must also be set to low '0' enabling inputs for channels 0 to 7.

- Digital channel 0 is CNT InA
- Digital channel 1 is CNT InB
- Digital channel 2 is CNT inC
- Digital channel 3 is ADC external trigger input (active high)
- Digital channel 4 is DAC external trigger input (active high)

If ADC or DAC trigger output signal is enabled, then Digital Direction Control Register bit-1 must be set to high '1' enabling outputs (channels 8 to 15).

- Digital channel 8 is DAC external trigger output (active high)
- Digital channel 9 is ADC external trigger output (active high)

Digital Direction Control Register (Read/Write) – (BAR0 + 7044H)

The data direction (input or output) of the 16 digital channels is selected via bit-0 and bit-1 of this register. The data direction of channels 0 to 7 are set/controlled via bit-0 while the data direction for bits 8 to 15 are controlled via bit-1. Setting a bit high configures the corresponding channel data direction for output. Setting the control bit low configures the corresponding channel data direction for input.

The Counter control, ADC and DAC trigger signals can be enabled to use Digital Port bits 0 to 4 as input. DAC and ADC trigger output signals are assigned to Digital bits 8 and 9 as outputs.

If counter control input signals are used or an ADC or DAC trigger signal is enabled for input, then the Direction Control Register must also be set as input for channels 0 to 7.

If ADC or DAC trigger signal is enabled for output, then the data Direction Control Register must also be set as output for channels 8 to 15.

The default power-up state of these registers is logic low. Thus, all channels are configured as inputs on system reset or power-up. The unused upper bits of this register are "Not Used" and will always read low (0's). Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers.

Interrupt Type (COS or H/L) Configuration Register (Read/Write) – (BAR0 + 7048H)

The Interrupt Type Configuration Registers determine the type of input channel transition that will generate an interrupt for each of the 16 possible interrupting channels. A "0" bit selects interrupt on level. An interrupt will be generated when the input channel level specified by the Interrupt Polarity Register occurs (i.e. Low- or High-level transition interrupt). A "1" bit means the interrupt will occur when a Change-Of-State (COS) occurs at the corresponding input channel (i.e. any state transition, low to high or high to low).

The Interrupt Type Configuration register at base address + offset 7048H is used to control channels 0 through 15. For example, channel 0 is controlled via data bit-0. All bits are set to "0" following a reset which means that, if enabled, the inputs will cause interrupts for the levels specified by the digital input channel Interrupt Polarity Register.

Channel read or write operations use 8-bit, 16-bit, or 32-bit data transfers. Note that interrupts will not occur unless they are enabled.

The Interrupt Status register at the carrier's base address + offset 7000H is used to monitor pending interrupts corresponding to channels 0 through 15. For example, channel 0 is monitored via data bit-0.

Interrupt Polarity Registers (Read/Write) – (BAR0 + 704CH)

The Interrupt Polarity Register determines the level that will cause a channel interrupt to occur for each of the channels enabled for level interrupts. A "0" bit specifies that an interrupt will occur when the corresponding input channel is low (i.e. a "0" in the digital input channel data register). A "1" bit means that an interrupt will occur when the input channel is high (i.e. a "1" in the digital input channel data register). Note that no interrupts will occur unless they are enabled by the Interrupt Enable Register. Further, the Interrupt Polarity Register will have no effect if the Change-of-State (COS) interrupt type is configured by the Interrupt Type Configuration Register.

The Interrupt Polarity register at the carrier's base address + offset 704CH is used to control channels 0 through 15. For example, channel 0 is controlled via data bit-0.

All bits are set to "0" following a reset which means that the inputs will cause interrupts when they are below TTL threshold (provided they are enabled for interrupt on level).

Debounce Enable Register (Read/Write) – (BAR0 + 7050H)

This register controls debounce enable for each of the 16 digital channels. It controls whether each individual channel is to be passed through the debounce logic before being recognized by the circuitry. A "0" disables the debounce logic for the corresponding channel, and a "1" enables the debounce logic. Debounce applies to both inputs and event sense inputs. Bit 0 of each register corresponds to the lowest numbered I/O point, while Bit 15 corresponds to the highest numbered I/O point.

Furthermore, after enabling the debounce circuitry, wait at least three times the programmed debounce duration prior to reading the input ports or event signals to ensure valid data.

All bits are set to "0" following a reset. Thus, on reset and power-up debounce will be disabled by default. These registers are read/write registers that can be accessed with 8-bit, 16-bit, or 32-bit data transfers.

Debounce Duration Select Register (Read/Write) – (BAR0 + 7054H)

This register controls the duration required by each input signal before it is recognized by each individual input. Two bits control the debounce duration for each channel. A 31.25MHz internal system clock is used for debounce. The debounce times are selected as shown below.

All bits are set to "0" following a reset. Thus, on reset and power-up debounce will be disabled by default. These registers are read/write registers that can be accessed with 8-bit, 16-bit, or 32-bit data transfers.

Table 4.47 Debounce Duration Register (Read/Write) – (BAR0 + 7054H)

Bit(s)	Function	
1 to 0	Channel 0 Debounce Value	
	00	4us
	01	64us
	10	1ms
	11	8ms
3 to 2	Channel 1 Debounce Value	
	00	4us
	01	64us
	10	1ms
	11	8ms
. . .	Channel x Debounce Value	
	00	4us
	01	64us
	10	1ms
	11	8ms
29 to 28	Channel 14 Debounce Value	
	00	4us
	01	64us
	10	1ms
	11	8ms
31 to 30	Channel 15 Debounce Value	
	00	4us
	01	64us
	10	1ms
	11	8ms

Counter Trigger, Stop, Load, Readback and Toggle Register (Write) – (BAR0 + 7070H)

Bit-0 of this register is used to implement software triggering the counter timer. Writing a 1 to trigger bit-0 of this register will cause the counter function to be triggered. The contents of bit-0 is not stored and merely acts to trigger the counter.

Triggering may be used to initiate quadrature position measurement, pulse width modulation, watchdog timer (initiates countdown), event counting, frequency measurement, pulse-width measurement, period measurement, or one-shot mode.

Bit-8 is used to implement software load of the read back register for the counter/timer. Writing a "1" to the load read back register bit-8 will cause the current count to be loaded into the read back register. Bit-8 is not stored and merely acts to load the counters read back register.

Other methods are available to load the read back register. At the end of pulse, period or frequency measurement the read back register is automatically loaded. With Event Counting a pulse on CNT InA when Control

register bits 5 and 4 are set "11" will load the read back register. With Quadrature mode a pulse on CNT InC when the Control register bits 9, 8 and 7 are set to "111" will load the read back register.

Bit-16 is used to disable the counter. Writing a "1" to the counter stop bit-16 of this register will cause the counter to be disabled. Bits 2, 1, and 0 of the counter control register are cleared to "000" thus disabling the counter. Bit-16 of this register is not stored and merely acts to stop the counter when set logic high.

Bit-24 is used to toggle Counter Constant A and Counter Constant B. Writing a "1" to the bit-24 will cause the counter to use the values in Counter Constant A Register 2 and Counter Constant B Register 2. Writing a "0" will cause the counter to use the values in Counter Constant A Register 1 and Counter Constant B Register 1. By default, a counter will always use the values in Counter Constant A Register 1 and Counter Constant B Register 1. Bit-24 is a read/write bit. Power-up or system reset clears the Toggle Counter Constants bit-24 to "0".

Table 4.48 Counter Trigger Register (Write) – (BAR0 + 7070H)

Bit(s)	Function
0	Counter Trigger
7-1	NOT USED
8	Load Counter Read Back Register
15-9	NOT USED
16	Counter Stop
23-17	NOT USED
24	Counter Toggle
31-25	NOT USED

Counter Control Register (Read/Write) – (BAR0 + 7074H)

This register is used to configure counter/timer functionality. It defines the counter mode, output polarity, input polarity, and clock source. The Counter Control Register is cleared (set to 0) following a reset, thus disabling the counter/timer. Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers.

Eight modes of operation are provided: quadrature position measurement, pulse width modulation, watchdog timer, event counting, frequency measurement, pulse width measurement, period measurement, and one-shot pulse mode. The following sections describe the features of each method of operation and how to best use them.

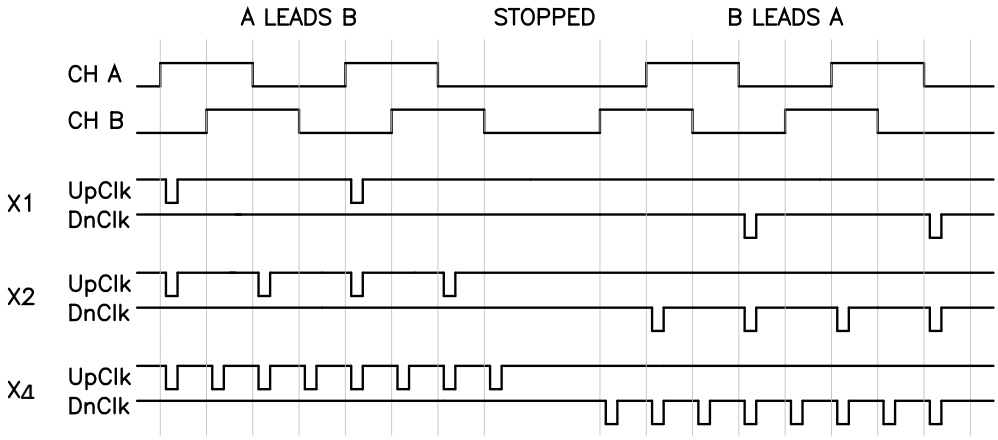
If counter/timer function is used, then digital channels 0 to 2 are required and Digital Direction Control Register bit 0 must be set to low (input direction). Digital channel 0 is CNT InA, digital channel 1 is CNT InB and digital channel 2 is CNT InC.

Quadrature Position Measurement

The counter/timers may be used to perform position measurements from quadrature motion encoders. Bits 2 to 0 of the Counter Control Register set to logic "001" configures the counter for quadrature measurement.

A quadrature encoder can have up to three channels: A, B, and Index. When channel A leads channel B by 90° in a quadrature cycle, the counter increments. When channel B leads channel A by 90° in a quadrature cycle, the counter decrements. The number of increments or decrements per cycle depends on the type of encoding: X1, X2, or X4.

Figure 4.1 Quadrature Cycles with x4 Encoding



An X1 encoding Increment occurs on the rising edge of channel A when channel A leads channel B. An X1 encoding decrement occurs on the falling edge of channel A when channel B leads channel A.

For X2 encoding, two increments or decrements (on each edge of channel A) result from each cycle. The counter increments when A leads B and decrements when B leads A.

For X4 encoding, four increments or decrements (on each edge of channel A and B) result from each cycle. The counter increments when A leads B and decrements when B leads A.

Quadrature measurement must be triggered internally via the Counter Trigger Register. An initial software trigger starts quadrature position measurement operation.

CNT InA and CNT InB input signals are used to input the channel A and channel B input signals, respectively. The counter will increment when channel A leads channel B and will decrement when channel B leads channel A. Three rates of increments and decrements are available X1, X2, and X4 which are programmed via counter timer control register bits 5 and 4. Channel B is enabled for input by setting bit-6 to a logic "1".

CNT InC can be used for the Index signal. Encoders that have an index channel can cause the counter to reload with the Counter Constant B value in a specified phase of the quadrature cycle. Reload can be programmed to

occur in any one of the four phases in a quadrature cycle. You must ensure that the Index channel is high during at least a portion of the phase you specify for reload. The phase can be selected via the counter timer control register bits 9, 8, and 7 as seen in the following table.

CNT InC can alternately be used as an external load of the Read Back Register. The signal will be active high and will cause immediate load of the current count value into the Read Back Register. An interrupt will be generated upon hardware load of the Read Back Register (if interrupts are enabled). Load of the Read Back Register can also be implemented by software via the Load Read Back Register. The quadrature measurement value can be read from the Counter Read Back Register.

Table 4.49 Counter Control Register (Quadrature Position Measurement)

Bit(s)	Function	
2,1,0	Specifies the Counter Mode:	
	001	Quadrature Position Measurement
3	Output Polarity (Output Pin ACTIVE Level):	
	0	Active LOW (Default)[1]
	1	Active HIGH[1]
5, 4	CNT InA / Channel A	
	00	Disabled (Default)
	01	X1 Encoding
	10	X2 Encoding
	11	X4 Encoding
6	CNT InB / Channel B	
	0	Disabled (Default)
	1	Enabled
9,8,7	CNT InC / Index: Channel Interrupt/Reload occurs when Index signal=1 and the A & B input signals are as selected below. See Control bits 14 & 13 for additional interrupt/load control.	
	000	Disabled (Default) 101 and 110 also Disable
	001	A = 0 , B = 1
	010	A = 1 , B = 0
	011	A = 1 , B = 1
	100	A = 0 , B = 0
	CNT InC / Hardware Load Read Back Register	
	111	InC = 0: Inactive State InC = 1: Load Read Back Register on logic high pulse
12,11,10	Counter Operational Frequency Select	
	000	1.953125MHz
	001	3.90625MHz
	010	7.8125MHz
	011	15.625MHz
	100	62.5MHz
	101	Undefined

Bit(s)	Function	
	110	Undefined
	111	Undefined
14,13	Output and Interrupt Condition Select	
	00	No Output or Interrupt Selected
	01	Output and Interrupt on counter equal Constant A Register
	10	Output and Interrupt on Index and reload on Index
	11	Output and Interrupt on Index but do not reload counter on Index.
15	NOT USED	

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

An interrupt can be generated upon index reload, or when the counter value equals the constant value stored in the Counter Constant A Register. Interrupts must be enabled via the Enable/Disable Counter Interrupts Register. The interrupt type must also be selected via bits 13 and 14 of the Counter Control Register. The interrupt will remain pending until released by setting the required bit of the Counter/Timer Interrupt Status/Clear register. Note that interrupts in Quadrature Position Measurement are generated whenever the interrupt conditions exist. If a pending interrupt is cleared, but the interrupt conditions still exist, another interrupt will be generated.

The Counter Control register bits 14 and 13 are used to control the operation of the counter output signal. With bits 14 and 13 set to "01", the output signal will be driven active while the counter equals the counter Constant A value. With bit 14 set to logic "1" the output signal will be driven active while the index condition remains true.

Pulse Width Modulation

Pulse width modulated waveforms may be generated at the counter timer output. The pulse width modulated waveform is generated continuously. Pulse Width Modulation generation is selected by setting Counter Control Register bits 2 to 0 to logic "010".

Counter Constant A value controls the time until the pulse goes active. The duration of the pulse is set via the Counter Constant B register. Note that a high pulse will be generated if active high output is selected while a low pulse will be generated if active low output is selected.

The counter goes through a countdown sequence for each Counter Constant value. When the 0 count is detected, the output toggles to the opposite state. Then the second Counter Constant value is loaded into the counter, and the countdown resumes, decrementing by one for each rising edge of the clock selected via Control Register bits 12, 11, and 10. For example, a counter constant value of 3 will provide a pulse duration of 3 clock cycles of the selected clock. Note, when the maximum internal clock frequency is selected,

62.5MHz, a delay of one extra clock cycle will be added to the counter constant value.

CNT InA can be used as a Gate-Off signal to stop and start the counter and thus the pulse-width modulated output. When CNT InA is enabled via bits 5 and 4 of the control register for active low Gate-Off input, a logic low input will enable pulse-width modulation counting while a logic high will stop PWM counting. When CNT InA is enabled for active high Gate-Off operation, a logic high will enable PWM counting while a logic low will stop PWM counting.

CNT InC can be used to externally trigger Pulse Width Modulation generation. Additionally, PWM can be triggered internally via the Counter Trigger Register. An initial trigger, software or external, causes the pulse width modulated signal to be generated. After an initial trigger do not issue additional triggers. Triggers issued while running will cause the Constant A and B values to load at the wrong time. In addition, changing the Control register setting while running can also cause the Constant A and B values to load at the wrong time.

By enabling interrupts via the Enable/Disable Interrupts Register, an interrupt can be generated when the output pulse transitions from low to high and also for transitions from high to low. Thus, an interrupt is generated at each pulse transition.

Table 4.50 Counter Control Register (Pulse Width Modulation)

Bit(s)	Function	
2,1,0	Specifies the Counter Mode:	
	010	Pulse Width Modulation
3	Output Polarity (Output Pin ACTIVE Level):	
	0	Active LOW (Default)[1]
	1	Active HIGH
5, 4	CNT InA Polarity / Gate-Off Polarity	
	00	Disabled (Default)
	01	Active LOW In A=0 Counter is Enabled In A=1 Counter is Disabled
	10	Active HIGH In A=0 Counter is Disabled In A=1 Counter is Enabled
	11	Disabled
7, 6	Not Used	
9,8	CNT InC Polarity / External Trigger	
	00	Disabled (Default)
	01	Active LOW External Trigger
	10	Active HIGH External Trigger
	11	Disabled
12,11,10	Clock Enable Frequency	
	000	1.953125MHz

Bit(s)	Function	
	001	3.90625MHz
	010	7.8125MHz
	011	15.625MHz
	100	62.5MHz
	101	Undefined
	110	Undefined
	111	Undefined
15,14,13	Not Used	

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

Watchdog Timer Operation

The watchdog operation counts down from a programmed (Counter Constant A) value until it reaches 0. While counting, the counter output will be in its active state (the output polarity is programmable). Upon time-out, the counter output will return to its inactive state, and an optional interrupt may be generated. Watchdog operation is selected by setting Counter Control Register bits 2 to 0 to logic "011".

A timed-out watchdog timer will not re-cycle until it is reloaded and then followed with a new trigger. Failure to cause a reload would generate an automatic time-out upon re-triggering, since the counter register will contain the 0 it previously counted down to.

CNT InA input can be used to reload the counter with the Constant A register value. CNT InA reload input is enabled via Control register bits 5 and 4. The counter can also be reloaded via a software write to the Counter Constant A register. Writing to the Counter Constant A register will load the value directly into the counter even if watchdog counting is actively counting down.

CNT InC can be used to either continue/stop watchdog counting or as an external trigger input. When control register bits 9 and 8 are set to logic "11", CNT InC functions as a Continue/Stop signal. When the Continue/Stop signal is high the counter continues counting (when low the counter stops counting). Alternately, when control register bits 9 and 8 are set to logic "01" or "10", the CNT InC input functions as an external trigger input. The watchdog timer may also be internally triggered via the Trigger Control Register.

When triggered, the counter/timer contents are decremented by one for each clock cycle, until it reaches 0, upon which a watchdog timer time-out occurs. For example, a counter constant value of 30 will provide a time-out delay of 30 clock cycles of the selected clock. However, due to the asynchronous relationship between the trigger and the selected clock, one clock cycle of error can be expected. The counter can be read from the Counter Readback register at any time during watchdog operation.

Upon time-out, the counter output pin returns to its inactive state. The Counter/Timer Module will also issue an interrupt upon detection of a count value equal to 0, if enabled via the Interrupt Enable/Disable Register. This could be useful for alerting the host that a watchdog timer time-out has occurred and may need to be reinitialized. The interrupt will remain pending until the watchdog timer is reinitialized and the interrupt is released by setting the required bit of the Counter/Timer Interrupt Status/Clear register.

Table 4.51 Counter Control Register (Watchdog Timer)

Bit(s)	Function	
2,1,0	Specifies the Counter Mode:	
	011	Watchdog Function
3	Output Polarity (Output Pin ACTIVE Level):	
	0	Active LOW (Default)[1]
	1	Active HIGH
5, 4	CNT InA Polarity / Counter Reload	
	00	Disabled (Default)
	01	Active LOW In A=0 Counter Reinitialized In A=1 Inactive State
	10	Active HIGH In A=0 Inactive State In A=1 Counter Reinitialized
	11	Disabled
7, 6	Not Used	
9,8	CNT InC Polarity / External Trigger	
	00	Disabled (Default)
	01	Active LOW Trigger
	10	Active HIGH Trigger
	11	Gate-Off (Continue when high/Stop when low)
12,11,10	Clock Enable Frequency	
	000	1.953125MHz
	001	3.90625MHz
	010	7.8125MHz
	011	15.625MHz
	100	62.5MHz
	101	Undefined
	110	Undefined
	111	Undefined
15,14,13	Not Used	

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

Event Counting Operation

Positive or negative polarity events can be counted. Event Counting is selected by setting Counter Control Register bits 2 to 0 to logic "100" and setting bits 12 to 10 to logic "000".

Input pulses or events occurring at the input CNT InB of the counter will increment the counter until it reaches the Counter Constant A value. Upon reaching the count limit, an output pulse of 1.74μs will be generated at the counter output pin, and an optional interrupt may be generated. Additionally, the internal event counter is cleared. The counter will continue counting, again from 0, until it reaches the Counter Constant A value. Once triggered, event counting will continue until disabled via Control register bits 2 to 0.

CNT InA can be used as a Gate-Off signal to stop and start event counting, or as an active high hardware load of the Read Back Register signal. When CNT InA is enabled via bits 5 and 4 of the control register for active low Gate-Off input, a logic low input will enable event counting while a logic high will stop event counting. When CNT InA is enabled for active high Gate-Off operation, a logic high will enable event counting while a logic low will stop event counting. When CNT InA is enabled for hardware load of the Read Back Register, an active high signal will cause load of the Read Back Register and an interrupt will be generated (if interrupts are enabled). The Read Back Register can also be loaded by software via the Load Read Back Register.

CNT InB is used as the event input signal. Active high or low input events can be selected via Control register bits 7 and 6. A minimum event pulse width (CNT InB) of 30ns is required for correct pulse detection with input debounce disabled. Programmable clock selection is not required in event counter mode.

CNT InC can be used to either control up/down counting or as an external trigger input. When control register bits 9 and 8 are set to logic "11", CNT InC functions as an Up/Down signal. When the Up/Down signal is high the counter is in the count down mode (when low the counter counts up). The counter will not count down below a count of zero. Alternately, when control register bits 9 and 8 are set to logic "01" or "10", the CNT InC input functions as an external trigger input. Event counting may also be internally triggered via the Trigger Control Register.

The Counter Constant A Register holds the count-to value (constant). Reading the Counter Read Back Register will return the current count (variable). **The Counter Constant A value must not be left as 0**. The counter upon trigger starts counting from 0 and since the counter would match the count-to value the counter resets and starts counting from zero again.

If interrupts are enabled via the Enable/Disable Interrupts Register, an interrupt is generated when the number of input pulse events is equal to the Counter Constant A register value. The internal counter is then cleared and will continue counting events until the counter constant A value is again reached and a new interrupt generated. An interrupt will remain pending

until released by setting the required bit of the Counter's Interrupt Status/Clear register.

Table 4.52 Counter Control Register (Event Counting)

Bit(s)	Function	
2,1,0	Specifies the Counter Mode:	
	100	Event Counting
3	Output Polarity (Output Pin ACTIVE Level):	
	0	Active LOW (Default)[1]
	1	Active HIGH
5, 4	CNT InA Polarity / Gate-Off	
	00	Disabled (Default)
	01	Active LOW In A=0: Continue Counting In A=1: Stop Counting
	10	Active HIGH In A=0: Stop Counting In A=1: Continue Counting
	CNT InA Hardware Capture Count ModeDisabled	
	11	InA = logic high pulse: Causes load of the Read Back register
7, 6	CNT InB Polarity / Event Input	
	00	Disabled (Default)
	01	Active LOW Events
	10	Active HIGH Events
	11	Disabled
9,8	CNT InC Polarity / External Trigger	
	00	Disabled (Default)
	01	Active LOW Trigger
	10	Active HIGH Trigger
	11	Count Up when logic low /Down when logic high Count Control
12,11,10	Specifies the Counter Mode:	
	000	Event Counting
15,14,13	Not Used	

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

Frequency Measurement Operation

Frequency Measurement is selected by setting Counter Control Register bits 2 to 0 to logic "100" and setting bits 12 to 10 to logic "111". The counter counts how many CNT InB edges (low to high or high to low) are received during the CNT InA enable interval. The frequency is the number of counts divided by the duration of the CNT InA enable signal.

CNT InA is used as an enable signal to start frequency measurement. The CNT InA signal must be a pulse of known width. When CNT InA is configured (via bits 5 and 4 of the control register) as an active low enable input, a logic low input will enable frequency measurement while a logic high will stop frequency measurement. When CNT InA is configured as an active high enable signal, a logic high will enable frequency measurement while a logic low will stop frequency measurement.

CNT InB is used to input the signal whose frequency is to be measured. Input pulses occurring at input CNT InB of the counter are counted while the enable signal present on CNT InA is active. When the CNT InA signal goes inactive, the counter output will generate a 1.74μs output pulse and an optional interrupt.

CNT InC can be used as an external trigger input. When control register bits 9 and 8 are set to logic "01" or "10", the CNT InC input functions as an external trigger input. Frequency measurement may also be internally triggered via the Trigger Control Register. An initial trigger, software or external, starts frequency measurement upon the active edge of the CNT InA enable signal.

The Counter Constant A Register is not used for frequency measurement. Do not write to this register while the counter is actively counting since this will cause the counter to be loaded with the Constant A value.

Reading the Counter Read Back Register will return the current count (variable). A minimum event pulse width (30ns CNT InB) is required for correct pulse detection with input debounce disabled. With debounce enabled, a minimum event pulse width of 4.0μs is required for correct pulse detection. Programmable clock selection is not available for frequency measurement.

If interrupts are enabled via the Enable/Disable Interrupts Register, an interrupt is generated when the input CNT InA enable pulse goes inactive. An interrupt will remain pending until released by setting the required bit of the Interrupt Status/Clear register.

Table 4.53 Counter Control Register (Frequency Measurement)

Bit(s)	Function	
2,1,0	Specifies the Counter Mode:	
	100	Frequency Measurement
3	Output Polarity (Output Pin ACTIVE Level):	
	0	Active LOW (Default)[1]
	1	Active HIGH
5, 4	CNT InA Polarity / Enable Pulse of Known Width	
	00	Disabled (Default)
	01	Active LOW Pulse
	10	Active HIGH Pulse
	11	Disabled
7, 6	CNT InB Polarity / Signal Measured/Counted	
	00	Disabled (Default)

Bit(s)	Function	
	01	Active LOW Pulse Counted
	10	Active HIGH Pulse Counted
	11	Disabled
9,8	CNT InC Polarity / External Trigger	
	00	Disabled (Default)
	01	Active LOW Trigger
	10	Active HIGH Trigger
	11	Disabled
12,11,10	Specifies the Counter Mode:	
	111	Frequency Measurement
15,14,13	Not Used	

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

Input Pulse Width Measurement

Setting bits 2 to 0 of the Counter Control Register to logic "101" configures the counter for pulse-width measurement. After pulse-width measurement is triggered, the first input pulse is measured.

CNT InA is used to input the pulse to be measured. An active low or high pulse can be measured.

CNT InC can be used to externally trigger Pulse Width Measurement. Additionally, Pulse Width Measurement can be triggered internally via the Counter Trigger Register. An initial trigger, software or external, starts pulse width measurement at the beginning of the next active pulse.

For pulse-width measurement, the pulse-width being measured serves as an enable control for an up-counter whose value can be read from the Counter Read Back Register. When triggered, the counter is reset and then increments by one for each clock pulse while the input signal level remains in the active state (high or low according to the programmed polarity of input CNT InA). The resultant pulse-width is equivalent to the count value read from the Counter Read Back Register, multiplied by the clock period. An output pulse will be generated at the counter output pin to signal the completion of a given measurement. Note that the measured pulse may be in error by $\pm$ 1 clock cycle.

Reading a counter value of 0xFFFFFFFF hex indicates that the pulse duration is longer than the current counter size and clock frequency can measure. Upon reading of this overflow value, you must select a slower frequency and re-measure.

An interrupt can be generated upon completion of a given pulse width measurement (the pulse has returned to the opposite polarity), if enabled via the interrupt Enable/Disable Register. The interrupt will remain pending until released by setting the required bit of the Interrupt Status/Clear register.

Table 4.54 Counter Control Register (Pulse Width Measurement)

Bit(s)	Function	
2,1,0	Specifies the Counter Mode:	
	101	Pulse-Width Measurement
3	Output Polarity (Output Pin ACTIVE Level):	
	0	Active LOW (Default)[1]
	1	Active HIGH
5, 4	CNT InA Polarity / Pulse Polarity to be Measured	
	00	Disabled (Default)
	01	Active LOW Pulse is Measured
	10	Active HIGH Pulse is Measured
	11	Disabled
7, 6	Not Used	
9,8	CNT InC Polarity / External Trigger	
	00	Disabled (Default)
	01	Active LOW Trigger
	10	Active HIGH Trigger
	11	Disabled
12,11,10	Clock Enable Frequency	
	000	1.953125MHz
	001	3.90625MHz
	010	7.8125MHz
	011	15.625MHz
	100	62.5MHz
	101	Undefined
	110	Undefined
	111	Undefined
15, 14,13	Not Used	

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

Input Period Measurement

The counter/timer may be used to measure the period of an input signal at the counter input CNT InA. Setting bits 2 to 0 of the Counter Control Register to logic "110" configures the counter for period measurement. The first input cycle after period measurement is triggered will be measured.

CNT InA is used to input the signal to be measured. Period measurement can be initiated on the active low or high portion of the waveform. The period of signal is the time the signal is low added to the time the signal is high, before it repeats.

CNT InC can be used to externally trigger period measurement. Additionally, Period Measurement can be triggered internally via the Counter Trigger

Register. An initial trigger, software or external, starts period measurement at the beginning of the next active period.

The period being measured serves as an enable control for an up-counter whose value can be read from the Counter Read Back Register. When triggered the counter is reset. Then, the active polarity of CNT InA starts period measurement. The counter increments by one for each clock pulse during the input signal period (CNT InA). The resultant period is equivalent to the count value read from the Counter Read Back Register, multiplied by the clock period. A 1.728µs output pulse will be generated at the counter output pin to signal the completion of a given measurement. Note that the measured period may be in error by +1 clock cycle (16ns).

Reading a counter value of 0xFFFFFFFF hex indicates that the pulse duration is longer than the current counter size and clock frequency can measure. Upon reading of this overflow value, you must select a slower frequency and re-measure.

An interrupt can be generated upon completion of a given period measurement, if enabled via the Interrupt Enable/Disable Register. The interrupt will be generated upon completion of the first complete waveform cycle after the counter is triggered. The interrupt, once driven active, will remain pending until released by setting the required bit of the Interrupt Status/Clear register.

Table 4.55 Counter Control Register (Period Measurement)

Bit(s)	Function	
2,1,0	Specifies the Counter Mode:	
	110	Period Measurement
3	Output Polarity (Output Pin ACTIVE Level):	
	0	Active LOW (Default)[1]
	1	Active HIGH
5, 4	CNT InA Polarity / Signal Measured	
	00	Disabled (Default)
	01	Active LOW starts period measurement
	10	Active HIGH starts period measurement
	11	Disabled
7, 6	Not Used	
9,8	CNT InC Polarity / External Trigger	
	00	Disabled (Default)
	01	Active LOW Trigger
	10	Active HIGH Trigger
	11	Disabled
12,11,10	Clock Enable Frequency	
	000	1.953125MHz
	001	3.90625MHz
	010	7.8125MHz
	011	15.625MHz

Bit(s)	Function		
	100	62.5MHz	
	101	Undefined	
	110	Undefined	
	111	Undefined	
15,14,13	Not Used		

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

One Shot Pulse Mode

One-Shot pulse mode provides an output pulse that is asserted one time or repeated each time it is re-triggered. One-Shot generation is selected by setting Counter Control Register bits 2 to 0 to logic "111".

The Counter Constant A value controls the time until the pulse goes active. The duration of the pulse high or low is set via the Counter Constant B value. Note that the Constant B value defines the logic high pulse width, if active high output is selected, and a low pulse if active low output is selected.

The counter goes through a full countdown sequence for each Counter Constant value. When the 0 count is detected, on the next rising-edge of the clock, the output toggles to the opposite state, and the Counter Constant B value is loaded into the counter and countdown resumes, decrementing by one each clock cycle. For example, a counter constant value of 7 will provide a pulse duration of 7 clock cycles of the selected clock, then 16ns will be added for the count detection of 0.

CNT InA can be used as a Gate-Off signal to stop and start the counter and, thus output. When CNT InA is enabled via bits 5 and 4 of the control register for active low Gate-Off input, a logic low input will enable the one-shot counter while a logic high will stop the one-shot counter. When CNT InA is enabled for active high Gate-Off operation, a logic high will enable the one-shot counter while a logic low will stop the one-shot counter.

CNT InC can be used to externally trigger One-Shot pulse mode. Additionally, a one-shot pulse can be triggered internally via the Counter Trigger Register. An initial trigger, software or external, causes the one-shot signal to be generated with no additional triggers required. Additional triggers must not be input until the one-shot pulse has completed count down of the Constant B value.

If interrupts are enabled via the Enable/Disable Interrupts Register, an interrupt is generated when the pulse transitions from low to high and also when the pulse transitions from high to low. The interrupt will remain pending until released by setting the required bit of the Interrupt Status/Clear register.

Table 4.56 Counter Control Register (One-Shot Pulse Mode)

Bit(s)	Function	
2,1,0	Specifies the Counter Mode:	
	111	One-Shot Generation
3	Output Polarity (Output Pin ACTIVE Level):	
	0	Active LOW (Default)[1]
	1	Active HIGH
5, 4	CNT InA Polarity / Gate-Off Polarity	
	00	Disabled (Default)
	01	Active LOW In A=0 Output Enabled In A=1 Output Disabled
	10	Active HIGH In A=0 Output Disabled In A=1 Output Enabled
	11	Disabled
7, 6	Not Used	
9,8	CNT InC Polarity / External Trigger	
	00	Disabled (Default)
	01	Active LOW Trigger
	10	Active HIGH Trigger
	11	Disabled
12,11,10	Clock Enable Frequency	
	000	1.953125MHz
	001	3.90625MHz
	010	7.8125MHz
	011	15.625MHz
	100	62.5MHz
	101	Undefined
	110	Undefined
	111	Undefined
15,14,13	Not Used	

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

Counter Interrupt Information Register (Read Only) – (BAR0 + 7078H)

This read only register provides information on what type of interrupt has been generated. This is useful for Quadrature Position Measurement and Event Counting, as it is possible to have more than one interrupt condition in these modes. Each bit position is representative of an interrupt condition. The interrupt conditions for each of the bits can be seen in Table 4.57 below. A "1" indicates that the interrupt condition represented by that bit has occurred. The bit will remain a "1" until the pending interrupt is cleared by writing a "1" to the corresponding bit in the Interrupt Pending/Clear Register.

A power-up or system reset clears the Counter Interrupt Information Register, setting all bits to "0".

Table 4.57 Counter Interrupt Information Register (Read Only) – (BAR0 + 7078H)

Bit(s)	Function
0	Counter equal to value in Counter Constant A Register (available in Event Counting and Quadrature Position Measurement)
1	Read Back Register has been loaded by hardware (available in Event Counting and Quadrature Position Measurement)
2	Index Pulse (available in Quadrature Position Measurement)
3	High to Low or Low to High Transitions (available in Pulse Width Modulation or One-Shot Pulse Mode)
4	End of Measurement (available in Frequency Measurement, Input Period Measurement, or Input Pulse Width Measurement)
5	Time Out (available in Watchdog Timer)
31-6	Not Used

Note that any registers or bits not mentioned will remain at the default value logic low.

Counter Read Back Register (Read Only) – (BAR0 + 707CH)

This read-only register is a dynamic function register that returns the current value held in the counter. It is updated with the value stored in the internal counter each time a hardware or software load of the Read Back Register is implemented.

The internal counter is generally initialized with the value in the Counter Constant Register, and its value is incremented or decremented according to the application.

This register must be read using 32-bit accesses.

Counter Constant A Register 1 (Read/Write) – (BAR0 + 7080H)

This read/write register is used to store the counter/timer constant A value (initial value) for the various counting modes. It is necessary to load the constant value into the counter in one clock cycle. Thus, access to this register is allowed on a 32-bit basis, only. The Counter Constant Registers are cleared (set to 0) following a system or software reset.

The contents of the Counter Constant A Register 1 and Counter Constant A Register 2 can be toggled for the counter/timers. Writing a "1" to the counter's corresponding toggle counter constants bit will cause the counter to use the values in Counter Constant A Register 2. Writing a "0" will cause the counter to use the values in Counter Constant A Register 1. By default, a counter will always use the values in Counter Constant A Register 1.

Counter Constant A Register 2 (Read/Write) – (BAR0 + 7084H)

This read/write register is used to store the counter/timer constant A register 2 value (initial value) for the various counting modes. It is necessary to load the constant value into the counter in one clock cycle. Thus, access to this register is allowed on a 32-bit basis, only. The Counter Constant Registers are cleared (set to 0) following a system or software reset.

The contents of the Counter Constant A Register 1 and Counter Constant A Register 2 can be toggled for the counter/timers. Writing a "1" to the counter's corresponding toggle counter constants bit will cause the counter to use the values in Counter Constant A Register 2. Writing a "0" will cause the counter to use the values in Counter Constant A Register 1. By default, a counter will always use the values in Counter Constant A Register 1.

Counter Constant B Register 1 (Read/Write) – (BAR0 + 7088H)

This read/write register is used to store the counter/timer constant B Register 1 value (initial value) for the various counting modes. It is necessary to load the constant value into the counter in one clock cycle. Thus, access to this register is allowed on a 32-bit basis, only. The Counter Constant Registers are cleared (set to 0) following a system or software reset.

The contents of the Counter Constant B Register 1 and Counter Constant B Register 2 can be toggled for the counter/timers. Writing a "1" to the counter's corresponding toggle counter constants bit will cause the counter to use the values in Counter Constant B Register 2. Writing a "0" will cause the counter to use the values in Counter Constant B Register 1. By default, a counter will always use the values in Counter Constant B Register 1.

Counter Constant B Register 2 (Read/Write) – (BAR0 + 708CH)

This read/write register is used to store the counter/timer constant B register 2 value (initial value) for the various counting modes. It is necessary to load the constant value into the counter in one clock cycle. Thus, access to this register is allowed on a 32-bit basis, only. The Counter Constant Registers are cleared (set to 0) following a system or software reset.

The contents of the Counter Constant B Register 1 and Counter Constant B Register 2 can be toggled for the counter/timers. Writing a "1" to the counter's corresponding toggle counter constants bit will cause the counter to use the values in Counter Constant B Register 2. Writing a "0" will cause the counter to use the values in Counter Constant B Register 1. By default, a counter will always use the values in Counter Constant B Register 1.

ADC Channel X Offset Registers (Read/Write) – (BAR0 + 70A0H to 70DCH)

The offset register is a 16-bit 2's complement fractional number ranging from -128 to 127.99609375 weighted as shown in the table below. This offset number is added to the uncorrected ADC value to correct for offset errors.

All channels 0 to 7 have a unique offset register. Each ADC channel can be programmed for any one of the 7 available ADC ranges. The offset value

corresponding to the range and channel selected must be read from Flash memory and then written to its corresponding ADC offset channel register.

Channel 0 to Channel 7 coefficients start at 0x3F E800 to 0x3F E9BF as shown in Table 7.2.

For example, if Channel 3 is programmed for the 0 to 10.24 VDC unipolar range then the offset stored in Flash at 0x3FE8C8 must be read and then written to BAR0 + 0x70AC.

Flash Memory

0x3F E8CB	Channel 3 (0 to 10.24V) Offset Coefficient	0x3F E8C8

ADC Channel 3 Offset Register

0x0000 70AC	15:0	ADC Channel 3 Offset

Note that the coefficients are stored as 2's complement format to allow use of plus and minus values. The offset register value is added to the output value from the ADC to correct offset errors.

The offset registers are set to zero upon reset of the board so that uncorrected ADC values may be stored in the FIFO.

Table 4.58 Offset Constant Number Format

Bit	Binary Fixed Point
15	Sign bit -128
14	64
13	32
12	16
11	8
10	4
9	2
8	1
7	½
6	¼
5	1/8
4	1/16
3	1/32
2	1/64
1	1/128
0	1/256

ADC Channel X Gain Registers (Read/Write) – (BAR0 + 70E0H to 711CH)

The gain register is a 17-bit fixed point positive fractional number ranging from 0 to 1.999984 weighted as shown in the table below. The 17-bit fixed point number is least significant bit justified in a 32-bit register. This number is multiplied by the offset corrected ADC value to correct for gain errors.

All channels 0 to 7 have a unique gain register. Each ADC channel can be programmed for any one of the 7 available ADC ranges. The gain value corresponding to the range and channel selected must be read from Flash memory and then written to its corresponding ADC Gain register.

Channel 0 to Channel 7 coefficients start at 0x3F E800 to 0x3F E9BF as shown in Table 7.2.

For example, if Channel 3 is programmed for the 0 to 10.24 VDC unipolar range then the Gain Coefficient stored in Flash at 0x3FE8CC must be read and then written to BAR0 + 0x70EC.

Flash Memory

0x3F E8CF	Channel 3 (0 to 10.24V) Gain Coefficient	0x3F E8CC

ADC Channel 3 Gain Register

0x0000 70EC	17:0	ADC Channel 3 Gain

Gain correction values must be loaded from the flash to correct new ADC data. The gain registers are set to one upon reset of the board so that uncorrected ADC values may be stored in the FIFO.

Table 4.59 Gain Constant Number Format

Bit	Binary Fixed Point
31 – 17	(unused, read as 0)
16	1
15	½
14	¼
13	1/8
12	1/16
11	1/32
10	1/64
9	1/128
8	1/256
7	1/512
6	1/1024
5	1/2048
4	1/4096
3	1/8192
2	1/16536
1	1/32768
0	1/65536

DAC Registers

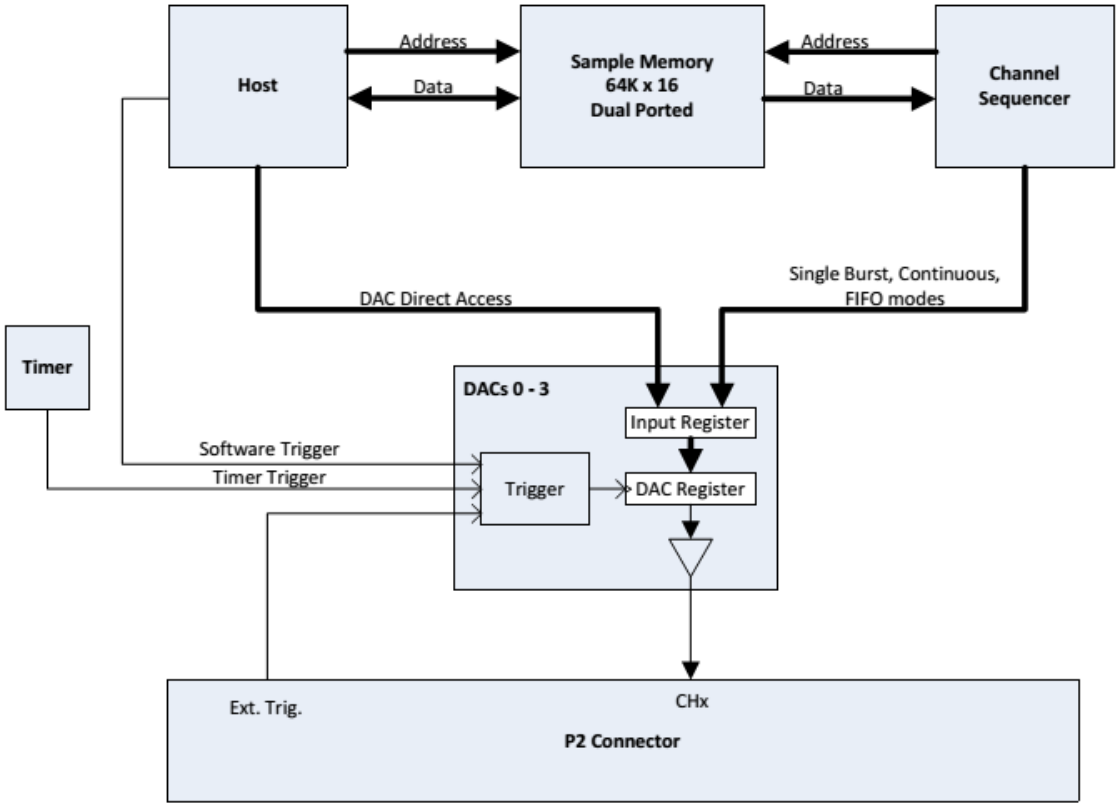
This section describes the AD57x1 interface shown in Figure 4.2 "AD57x1 DAC Converter Interface Block Diagram" that connects the AXI interface to the four DAC converters and the sample memory that is shared among all four

channels. Each of the channels can be independently configured to operate in one of four modes: direct access, single burst, continuous, or FIFO mode. In either single burst, continuous, or FIFO mode, a channel sequencer retrieves samples from the sample memory and writes the sample data to its DAC. The portion of sample memory allocated to each channel is programmable. There are six channel specific registers per channel and three registers that affect all channels.

Table 4.60 DAC Registers

BAR0 Base Addr+	Bits	Register Description
0x0004_0000	31:0	Channel 0 Start Address
0x0004_0004	31:0	Channel 0 End Address
0x0004_0008	31:0	Channel 0 FIFO
0x0004_000C	31:0	Reserved
0x0004_0010	31:0	Channel 0 Control
0x0004_0014	31:0	Channel 0 Status
0x0004_0018	31:0	Channel 0 DAC Direct Access
0x0004_001C	31:0	Reserved
0x0004_0020	31:0	Channel 1 Start Address
0x0004_0024	31:0	Channel 1 End Address
0x0004_0028	31:0	Channel 1 FIFO
0x0004_002C	31:0	Reserved
0x0004_0030	31:0	Channel 1 Control
0x0004_0034	31:0	Channel 1 Status
0x0004_0038	31:0	Channel 1 D/A Direct Access
0x0004_003C		Reserved
⋮	⋮	⋮
0x0004_0060	31:0	Channel 3 Start Address
0x0004_0064	31:0	Channel 3 End Address
0x0004_0068	31:0	Channel 3 FIFO
0x0004_006C	31:0	Reserved
0x0004_0070	31:0	Channel 3 Control
0x0004_0074	31:0	Channel 3 Status
0x0004_0078	31:0	Channel 3 DAC Direct Access
0x0004_007C	31:0	Reserved
⋮	⋮	⋮
0x0004_01FF	31:0	Reserved
0x0004_0200	31:0	Control
0x0004_0204	31:0	Timer Divider
0x0004_0208	31:0	Software Trigger
0x0004_020C	31:0	Reserved
⋮	⋮	⋮
0x0005_FFFC	31:0	Reserved
0x0006 0000	31:0	Sample Memory
⋮	⋮	⋮
0X0007 FFFC	31:0	Sample Memory

Figure 4.2 AD57x1 D/A Converter Interface Block Diagram



Addressing Sample Memory

The Sample Memory is a dual-port memory that provides buffer space for storage of waveforms. It is organized as 64K 16-bit values. To meet varying application requirements, the portion of the sample memory allocated to each channel is configurable. DAC channels that output a static value, or channels that are not used, do not require any of the sample memory. Channels that output a repetitive waveform at a lower frequency require a larger portion of sample memory than a channel with higher frequency output. Channels that output a non-repetitive waveform will require a continuous stream of data from the host. For these channels, a portion of the sample memory may be configured as a FIFO to buffer the data stream. The host processor can directly read and write the sample memory concurrent with the channel sequencer reads.

The address offset used by the host processor to access sample memory is a byte address relative to PCI BAR0.

Channel X Start Address

For channels configured in Single Burst mode, Continuous mode or FIFO mode, this register contains the start address in sample memory of the waveform to be written to the DAC. Addressing is relative to the first location in sample memory. A write to the Start Address register will also initialize the

hidden FIFO read and write pointers when the channel is configured in FIFO mode.

Table 4.61 Channel X Start Address

Bit(s)	Description
15-0	Start address
31-16	Reserved

Channel X End Address

For channels configured in Single Burst mode, Continuous mode, or FIFO mode, this register contains the end address in sample memory of the waveform to be written to the DAC. Addressing is relative to the first location in sample memory.

Table 4.62 Channel X End Address

Bit(s)	Description
15-0	End address
31-16	Reserved

Channel X FIFO

For channels configured in FIFO mode, write to this address to add one or two samples to the FIFO. A 32-bit write operation will write two samples, a 16-bit write operation adds one sample. Use the key hole feature of the DMA controller when the FIFO is the destination of the DMA transfer.

Table 4.63 Channel X FIFO

Bit(s)	Description
15-0	Sample 0
31-16	Sample 1

Channel X Control Register

The channel specific control and status registers configure each channel's operating mode and trigger mode, and include a FIFO underflow flag clear function.

Table 4.64 Channel X Control Register

Bit(s)	Description
1-0	Operating mode: 00-stopped 01-continuous 10-FIFO 11-Single burst
3-2	Trigger source: 00-software 01-timer 10-external 11-not used

Bit(s)	Description
4	When set, clear channel: Start Address Register is cleared to 0 End Address Register is cleared to 0 Internal Read Pointer is cleared to 0 Internal Write Pointer is cleared to 0 FIFO Empty Flag is set = 1 FIFO half full is set = 1 FIFO full set = 0
31-5	Reserved

Channel X Status Register

The channel specific status registers indicate the mode dependent status of each channel.

Table 4.65 Channel X Status Register

Bit(s)	Function
0	FIFO empty (read only) 0- FIFO not empty 1- FIFO empty
1	FIF0 half full (read only): 0-FIFO is more than half full 1-FIFO is half full or less
2	FIF0 full (read only): 0-FIFO is not full 1-FIFO is full
3	FIF0 underflow (write to reset): 0-underflow has not occured 1-an attempt was made to read from an empty FIFO Write '1' to this bit to clear it.
4	Burst Single Complete – (write to reset) this flag indicates the last sample in the burst has been copied to the D/A data register 0-burst in progress 1-burst complete Write '1' to this bit to clear it.
5	Busy – (read only) when operating in direct access mode, this bit indicates that a serial transfer to the D/A converter is in progress 0-not busy 1-busy
31-6	Reserved

Channel X DAC Direct Address

A write to this address issues a command to the DAC. The contents of the DAC Channel registers are serially transferred to their corresponding converter input buffer serially. This serial data transfer takes 1µs. Thus, a new write of the same DAC register can be performed no sooner than 1µs after the previous write. The Channel X Status register includes a bit to indicate the busy status of the write operation. The channel's Status busy bit will be set high upon initiation of a write operation and will remain high until the requested write operation has completed. New write accesses to the same DAC Channel register should not be initiated unless its write busy status bit is low. Read of the DAC registers is not supported.

Table 4.66 Channel X DAC Direct Access

Bit(s)	Description	
15-0	Voltage data or control data depending on address bits.	
19-16	Address 4-bits	
	0000	No Operation
	0001	Write to input register (no DAC output update, input register only written) a trigger is needed to transfer the data from the input register to the DAC register
	0010	Update DAC register from input register (Updates DAC output voltage)
	0011	Write and Update DAC register (Updates the input register and DAC register without waiting for a trigger)
	0100	Write to control register (see control register bit assignment below)
	0101	No Operation
	0110	No Operation
	0111	Software Data Reset (Reset to zero scale, midscale, or full scale as specified by PV1 and PV0 bits of control register)
	1000	Reserved
	1001	Disable daisy-chain functionality (executing this command tri-states unused SDO pin to save power)
	1010	Not supported (Read input register)
	1011	Not supported (Read DAC register)
	1101	No operation
	1110	No operation
	1111	Software full reset (Device set to power up state, output at GND and output buffer is powered down)
20	0 (this bit must be zero)	
31-21	Reserved	

When the Write to Control register address (bits 19-16) is selected (0100) bits 0-15 are control register bit as described below.

Bit(s)	Description	
2-0	Output Range (Software full reset is also issued when the output range is reconfigured.)	
	000	-10V to +10V
	001	0V to +10V
	010	-5V to +5V
	011	0V to +5V
	100	-2.5V to +7.5V
	101	-3V to +3V
	110	0V to 16V Not Supported
	111	0V to 20V Not Supported
4,3	Power-up Voltage	
	00	Zero scale
	01	Mid scale
	10	Full scale
	11	Full scale
5	0	Fixed at 0
6	Thermal Shutdown alert	
	0	Die temperature > 150C do not power down
	1	Die temperature > 150C power down
7	Data Format Control Bit When a channel is configured for 0-10 or 0-5 ranges, this bit is ignored and anything written to the DAC is treated as straight binary. See the table below for example corresponding codes.	
	0	Straight binary coded
	1	Twos complement coded
8	5% Over-range	
	0	5% over-range disabled
	1	5% over-range enabled
10,9	Clear voltage selection	
	00	Zero scale
	01	Mid scale
	10	Full scale
	11	Full scale
15-11	Not used	

Table 4.67 Data Format

Straight Binary	Decimal Code	Twos Complement
1111	+7	0111
1110	+6	0110
1101	+5	0101
1100	+4	0100
1011	+3	0011

Straight Binary	Decimal Code	Twos Complement
1010	+2	0010
1001	+1	0001
1000	0	0000
0111	-1	1111
0110	-2	1110
0101	-3	1101
0100	-4	1100
0011	-5	1011
0010	-6	1010
0001	-7	1001
0000	-8	1000

Control Register (Read/Write) – (BAR0 + 4 0200H)

This control register provides control functions that affect all channels.

Table 4.68 Control Register (Read/Write) – (BAR0 + 4 0200H)

Bit(s)	Description
0	Waveform Output Enable 0-stop waveform output 1-start waveform output
1	DAC reset 0-DAC normal operation 1-sets all outputs to ground output buffers powered down
2	DAC clear 0-DAC normal operation 1-sets all DAC outputs to their pre-configured value (zero-scale, mid-scale, full-scale) setup for each channel
3	Enable Trigger Output 0-output trigger disabled 1-outputs trigger to external devices
4	Software Reset 0-normal operation 1-resets the registers in the AD5761 interface
31-5	Reserved

Timer Divider Register (Read/Write) – (BAR0 + 4 0204H)

This 32-bit register controls the period of the internal trigger. The timer is clocked at a rate of 31.25 MHz. The period of the internal trigger is calculated by multiplying the Timer Divider register contents by 32 nano-seconds. The minimum recommended value is 310. With this value the frequency of triggering is 100 KHz, which is the maximum frequency the DACs can operate at and still settle to within 1 LSB accuracy.

Table 4.69 Timer Divider Register (Read/Write) – (BAR0 + 4 0204H)

Bit(s)	Description
31-0	Timer Divider- count of 32 ns clock periods between DAC output samples.

Software Trigger Register (Read/Write) – (BAR0 + 4 0208H)

Write to this address to trigger the DAC outputs for all channels configured to respond to a software trigger.

Table 4.70 Software Trigger Register (Read/Write) – (BAR0 + 4 0208H)

Bit(s)	Description
31-0	Any value can be written. Data is not stored.

5. DAC USE OF CALIBRATION DATA

Calibration data is provided in the form of calibration coefficients, so the user can adjust and improve the accuracy of the analog output voltage over the uncalibrated state. Each channel's unique offset and gain calibration coefficients are stored in Flash memory. The use of software calibration allows the elimination of hardware calibration potentiometers traditionally used in producing precision analog outputs. A comparison of the uncalibrated and software calibrated performance is shown to illustrate the importance of the software calibration.

Software calibration uses some fairly complex equations. Acromag provides software products (sold separately) to make communication with the board and calibration easy. It relieves you from having to turn the equations of the following sections into debugged software calibration code.

Uncalibrated Performance

The uncalibrated performance is affected by two primary error sources. These are the channel's offset and gain errors. The use of channel specific calibration coefficients to accurately adjust offset and gain is important because the worst-case uncalibrated error can be significant (although the typical uncalibrated errors observed may be much less). The maximum uncalibrated error is summarized as follows.

AP730 Model

AD5761 @ -40°C to 85°C:
Linearity Error is +/- 0.003% FSR maximum (i.e. +/-2 LSB).
Offset Error is +/- 0.05% FSR (i.e. full-scale range would be 20V SPAN for the -10 to 10V range) maximum.
Gain Error is +/- 0.1% FSR maximum.
Total Error +/- 0.153% FSR maximum (+/-98.5 LSB)

AP731 Model

AD5721 @ -40°C to 85°C:
Linearity Error is +/- 0.0122% FSR maximum (i.e. +/-0.5 LSB).
Offset Error is +/- 0.05% FSR (i.e. full-scale range would be 20V SPAN for the -10 to 10V range) maximum.
Gain Error is +/- 0.1% FSR maximum.
Total Error +/- 0.1512% FSR maximum (+/-6.2 LSB)

Typically, each error component is much less than its maximum and all error components do not reinforce each other. Thus, typical errors are much less than that shown above.

Calibrated Performance

Accurate calibration of the DAC can be accomplished through software control by using calibration coefficients to adjust the analog output voltage. Unique calibration coefficients are stored in Flash memory as 1/16 LSB's for

each specific channel. Once retrieved, the channel's unique offset and gain coefficients can be used to correct the data value sent to the DAC channel to accurately generate the desired output voltage.

The maximum calibrated error combining the linearity and adjusted offset and gain errors:

AP730 Model

AD5761
Linearity Error is +/-2 LSB
Offset Error is +/-0.0625 LSB
Gain Error is +/-0.0625 LSB
Total Error +/-2.125 LSB (+/- 0.0032% FSR) maximum

AP731 Model

AD5721 @ -40°C to 85°C:
Linearity Error is +/-0.5 LSB
Offset Error is +/-0.0625 LSB
Gain Error is +/-0.0625 LSB
Total Error +/-0.625 LSB (+/- 0.0152% FSR) maximum

Calibration coefficients are determined near room temperature. The Total Error does not include shifts over temperature.

Thus, correcting the value programmed to the DAC Channel Register using the stored calibration coefficients provides the means to obtain excellent accuracy.

Data is corrected using a couple of formulas. Equation (1) expresses the ideal relationship between the value (IdealCode) written to the DAC to achieve a specified voltage within output range assuming Straight Binary (also called Bipolar Offset Binary) or 2's Complement data format (see Table 5.1 and 5.2).

Equation (1)

IdealCode = [IdealSlope × DesiredVoltage] + IdealZeroCode

Where,

Table 5.1 AP730 Ideal Slope and Zero Values for Supported Ranges

Range	*IdealSlope*	*IdealZeroCode Straight Binary(2's Comp)*
-10 to 10V	3276.8	32768 (0)
-5 to 5V	6553.6	32768 (0)
-3 to 3V	10922.67	32768 (0)
-2.5 to 7.5V	6553.6	16384 (-16384)
0 to 10V	6553.6	0 (-32768)
0 to 5V	13107.2	0 (-32768)

Table 5.2 AP731 Ideal Slope and Zero Values for Supported Ranges

Range	*IdealSlope*	*IdealZeroCode Straight Binary(2's Comp)*

-10 to 10V	204.8	2048 (0)
-5 to 5V	409.6	2048 (0)
-3 to 3V	682.6	2048 (0)
-2.5 to 7.5V	409.6	1024 (-1024)
0 to 10V	409.6	0 (-2048)
0 to 5V	819.2	0 (-2048)

Using equation (1), one can determine the IdealCode for any desired voltage within the range. For example, if it is desired to output a voltage of +5 Volts for -10 to 10V range, equation (1) returns the result 49,152 for IdealCode for model AP730. If this value is used to program the DAC output (following conversion to Hex 0xC000), the output value will approach +5 Volts to within the uncalibrated error. This will be acceptable for some applications.

For applications needing better accuracy, the software calibration coefficients should be used to correct the IdealCode into the CorrectedCode required to accurately produce the output voltage. This is illustrated in equation (2):

Equation (2) AP730 Model

$$\textbf{CorrectedCode}=\left(\frac{\textbf{GainCoef}}{\textbf{65536×16}}+\textbf{1}\right)[\textbf{IdealSlope}\times\textbf{DesiredVoltage}]+\textbf{IdealZeroCode}+\frac{\textbf{OffsetCoef}}{\textbf{16}}$$

The GainCoef and OffsetCoef are stored and retrieved from Flash memory at the addresses shown in Table 7.1. Coefficients are unique to each of the 4 channels. The GainCoef and OffsetCoef values are calculated using the following equations at room temperature and then stored in Flash memory. Note that the coefficients are stored as 2's complement to allow use of plus and minus values.

AP730 Model

$$\text{GainCoef} = 65536\times16\left(\frac{ActualSlope}{IdealSlope}-1\right)$$

$$\text{OffsetCoef} = (\text{ActualZeroCode} - \text{IdealZeroCode})\times 16$$

$$\text{ActualSlope} = \left(\frac{Code2-Code1}{MeasuredV2-MeasuredV1}\right)$$

$$\text{ActualZeroCode} = \text{Code1} - (\text{ActualSlope}\times MeasuredV1)$$

Where:
Code1 = 655 (0x28F hex)
Code2 = 64880 (0xFD70 hex)

Measured values (MeasuredV2 and MeasuredV1) are taken using data averaging**.**

Equation (3) AP731 Model

$$\textbf{CorrectedCode}=\left(\frac{\textbf{GainCoef}}{\textbf{4096×16}}+\textbf{1}\right)[\textbf{IdealSlope}\times\textbf{DesiredVoltage}]+$$

IdealZeroCode+ $\frac{\textbf{OffsetCoef}}{\textbf{16}}$

AP731 Model

GainCoef = 4096×16 $\left(\frac{ActualSlope}{IdealSlope} - 1\right)$

OffsetCoef = $(\text{ActualZeroCode} - \text{IdealZeroCode}) \times 16$

ActualSlope = $\left(\frac{Code2 - Code1}{MeasuredV2 - MeasuredV1}\right)$

ActualZeroCode = $\text{Code1} - (\text{ActualSlope} \times MeasuredV1)$

Where:
Code1 = 40 (0x28 hex)
Code2 = 4055 (0xFD7 hex)

Measured values (MeasuredV2 and MeasuredV1) are taken using data averaging**.**

6. ADC USE OF CALIBRATION DATA

Factory calibration constants used to correct gain and offset errors are stored in on-board flash memory. Gain and offset correction constants are stored for each ADC. Software calibration uses some fairly complex equations. Acromag provides you with the AcroPack Software Library to make communication with the board and calibration easy. It relieves you from having to turn the equations of the following sections into debugged software calibration code. The functions are written in the "C" programming language and can be linked into your application.

Uncalibrated Performance

The uncalibrated performance is affected by two primary error sources. These are the external reference voltage and the Analog to Digital Converter (ADC). The untrimmed ADC's have significant offset and gain errors (see specifications) which reveal the need for software calibration.

Calibrated Performance

Very accurate calibration can be accomplished by applying external precision calibration voltages. The calibration voltages are used to determine two points of a straight line which defines the analog input characteristic.

The AP73x has one ADC circuit that implements all eight channels. Each of the eight ADC channels will have their own unique offset and gain errors for each of the seven ranges. The calibration voltages will need to be converted through each ADC circuit for each channel and the seven ranges to calculate the gain and offset calibration constants as shown in the equations below.

OffsetCorrection = -ActualIntercept (Equation 1)

ActualIntercept = CountCALHI – (*ActualSlope * VoltsCALHI*)

$$IdealSlope^{1} = \frac{2^{16}}{FullScaleRange} = \frac{2^{16}}{5.12} \; or \; \frac{2^{16}}{10} \; or \; \frac{2^{16}}{10.24} \; or \; \frac{2^{16}}{20} \; or \; \frac{2^{16}}{20.48}$$

[1] *IdealSlope* is calculated using the *FullScaleRange* which can be one of the following: 5.12V (0 to 5.12V), 10V (-5.0 to 5.0V or 0 to 10V), 10.24V (-5.12 to 5.12 or 0 to 10.24V), 20V (-10 to 10V), 20.48 (-10.24 to 10.24).

$$ActualSlope = \frac{CountCALHI - CountCALLO}{VoltsCALH - VoltsCALLO}$$

$$CorrectionFactor = \frac{IdealSlope}{ActualSlope}$$

*GainCorrection = CorrectionFactor * 2^16* (Equation 2)

Where:

CountCALHI = uncorrected ADC data (16-bit) with high external precision calibration voltage applied +4.88V recommended for 0 to 5.12V, -5.0 to 5.0V, and -5.12 to 5.12V ranges while +9.88V is recommended for 0 to 10V, 0 to 10.24V, -10.0 to 10.0V, and-10.24 to 10.24V ranges.

CountCALLO = uncorrected ADC data (16-bit) with high external precision calibration voltage applied -4.88V recommended for -5.0 to 5.0V, and -5.12 to 5.12V ranges while -9.88V is recommended for -10.0 to 10.0V, and-10.24 to 10.24V ranges, and 0.1V recommended for the 0 to 5.12V, 0 to 10V, and 0 to 10.24V ranges.

VoltsCALHI = actual external precision calibration voltage high

VoltCALLO = actual external precision calibration voltage low

Note that the equation given here can be used for both the unipolar and bipolar ranges. For unipolar ranges one must first XOR 0x8000 with the ADC count value.

The values calculated for *OffsetCorrection* and *GainCorrection* are stored in flash memory for each ADC channel. The values are then used in the following equation to correct each input sample for offset and gain errors.

$$CorrectedData = \frac{(CountIN + OffsetCorrection) * GainCorrection}{2^{16}} \quad \textit{(Equation 3)}$$

Note: The average of many ADC values (e.g. 2048) should be used when calculating new correction coefficients to reduce the measurement uncertainty.

Calibration Programming Example

Calibration constants are calculated and stored in flash memory in the factory, however, in the case that new constants must be calculated, the calibration parameters CountCALHI and CountCALLO need to be determined for each ADC channel for each of the ranges. These parameters are then used to calculate OffsetCorrection and GainCorrection constants.

Determination of CountCALLO Value

1. Execute write of 0200H to the Interrupt Enable Register at Base Address + 2008H. This will enable FIFO Threshold met or exceeded interrupts on the module.

2. Execute write of 0002H to the Control Register at Base Address + 7008H.

    a) Continuous Mode Enabled

    b) External Trigger Disabled

    c) Hardware initiated DMA transfers disabled

3. Execute write of 0007H to the ADC Range Enable Channel 0 to 7 Register at Base Address + 700CH. This will permit the values corresponding to channel 0 to be stored in the data FIFO.

4. Execute write of 53H to the Conversion Timer register at Base Address + 7014H. This sets the interval time between conversions to 1.344µ seconds.

5. Execute write of 3C0H to the FIFO Full Threshold register at Base Address + 7018H. Since interrupts are enabled in the control register, an interrupt

request will be issued when 960 values of the calibration voltage have been stored in the FIFO.

6. Apply a low (negative) calibration voltage, 0V is recommended, to channel 0. Execute write of 0001H to the Start Convert Bit at Base Address + 701CH. This starts the continuous mode of conversions.

7. Upon system interrupt execute write of 00H to the Control register at Base Address + 7008H. This disables conversions. Software must calculate a CountCALLO value for channel 0, by averaging the 960 values for channel 0. Note that more samples will reduce measurement uncertainty.

Determination of CountCALHI Value

8. Execute write of 0002H to the Control Register at Base Address + 7008H.

a) Continuous Mode Enabled

b) External Trigger Disabled

c) Hardware initiated DMA transfers disabled

9. Writing the Channel Enable register, Conversion Timer Value, and the FIFO Full Threshold is not necessary because they need not change from that programmed in the previous steps.

10. Apply a high (positive) calibration voltage, +9.88V is recommended, to channel 0. Execute write of 0001H to the Start Convert Bit at Base Address + 701CH. This starts the continuous mode of conversions.

11. Upon system interrupt execute write of 00H to the Control register at Base Address + 7008H. This disables conversions. Software must calculate a CountCALHI value for channel 0, by averaging the 960 values for channel 0. Note that more samples will reduce measurement uncertainty.

Calculate the Calibration Constants to Store in Flash

12. Use the CountCALLO and CountCALHI values in Equation 1 and Equation 2 in the beginning of this section to obtain new OffsetCorrection and GainCorrection constants for each ADC. These values can then be stored in the flash memory and loaded into the gain and offset registers.

13. Since OffsetCorrection and GainCorrection constants are known, corrected input data values can now be calculated. Data is corrected in firmware and stored into the FIFO.

7. FLASH MEMORY MAP

The Serial flash memory provides 4M bytes of non-volatile memory for storing the FPGA configuration bitstream. The lower portion of the flash address space is used to store the FPGA configuration bitstream. The upper portion is reserved for the storage of calibration constant and ASCII model identifier string as shown in the tables below. The serial flash is accessible through the AXI Quad SPI interface.

The calibration constants are calculated and stored in flash memory at the factory.

DAC Calibration Coefficients (Table 7.1)

Channel 0 coefficients start at 0x3F E000 to 0x3F E017 as shown in Table 7.1.

Channel 1 coefficients start at 0x3F E100 to 0x3F E117.

Channel 2 coefficients start at 0x3F E200 to 0x3F E217.

Channel 3 coefficients start at 0x3F E300 to 0x3F E317.

Note that the coefficients are stored as 2's complement numbers to allow use of plus and minus values.

Table 7.1 DAC Calibration Coefficient Map

Flash Addr	D15 down to D00	Flash Addr
0x3F E001	Channel 0 (-10.0 to 10.0V) Offset Coefficient	0x3F E000
0x3F E003	Channel 0 (-10.0 to 10.0V) Gain Coefficient	0x3F E002
0x3F E005	Channel 0 (0 to 10.0V) Offset Coefficient	0x3F E004
0x3F E007	Channel 0 (0 to 10.0V) Gain Coefficient	0x3F E006
0x3F E009	Channel 0 (-5.0 to 5.0V) Offset Coefficient	0x3F E008
0x3F E00B	Channel 0 (-5.0 to 5.0V) Gain Coefficient	0x3F E00A
0x3F E00D	Channel 0 (0 to 5.0V) Offset Coefficient	0x3F E00C
0x3F E00F	Channel 0 (0 to 5.0V) Gain Coefficient	0x3F E00E
0x3F E011	Channel 0 (-2.5 to 7.5V) Offset Coefficient	0x3F E010
0x3F E013	Channel 0 (-2.5 to 7.5V) Gain Coefficient	0x3F E012
0x3F E015	Channel 0 (-3 to 3V) Offset Coefficient	0x3F E014
0x3F E017	Channel 0 (-3 to 3V) Gain Coefficient	0x3F E016

Flash Addr	D15 down to D00	Flash Addr
0x3F E019→ 0x3F E0FF	Reserved	0x3F E018→ 0x3F E0FE
0x3F E101→ 0x3F E117	Channel 1 Coefficients	0x3F E100→ 0x3F E116
0x3F E119→ 0x3F E1FF	Reserved	0x3F E118→ 0x3F E1FE
0x3F E201→ 0x3F E217	Channel 2 Coefficients	0x3F E200→ 0x3F E216
0x3F E219→ 0x3F E2FF	Reserved	0x3F E218→ 0x3F E2FE
0x3F E301→ 0x3F E317	Channel 3 Coefficients	0x3F E300→ 0x3F E316
0x3F E319→ 0x3F E7FF	Reserved	0x3F E318→ 0x3F E7FE

ADC Calibration Coefficients (Table 7.2)

Channel 0 to Channel 7 coefficients start at 0x3F E800 to 0x3F E9BF as shown in Table 7.2.

Note that the coefficients are stored as 2's complement numbers to allow use of plus and minus values.

Table 7.2 ADC Calibration Coefficient Map

Flash Addr	D31 down to D00	Flash Addr
0x3F E803	Channel 0 (0 to 5.12V) Offset Coefficient	0x3F E800
0x3F E807	Channel 0 (0 to 5.12V) Gain Coefficient	0x3F E804
0x3F E80B	Channel 0 (-5.0 to 5.0V) Offset Coefficient	0x3F E808
0x3F E80F	Channel 0 (-5.0 to 5.0V) Gain Coefficient	0x3F E80C
0x3F E813	Channel 0 (-5.12 to 5.12V) Offset Coefficient	0x3F E810
0x3F E817	Channel 0 (-5.12 to 5.12V) Gain Coefficient	0x3F E814
0x3F E80B	Channel 0 (0 to 10V) Offset Coefficient	0x3F E818
0x3F E81F	Channel 0 (0 to 10V) Gain Coefficient	0x3F E81C
0x3F E823	Channel 0 (0 to 10.24V) Offset Coefficient	0x3F E820
0x3F E827	Channel 0 (0 to 10.24V) Gain Coefficient	0x3F E824
0x3F E82B	Channel 0 (-10.0 to 10.0 V) Offset Coefficient	0x3F E828

Flash Addr	D31 down to D00	Flash Addr
0x3F E82F	Channel 0 (-10.0 to 10.0V) Gain Coefficient	0x3F E82C
0x3F E833	Channel 0 (-10.24 to 10.24V) Offset Coefficient	0x3F E830
0x3F E837	Channel 0 (-10.24 to 10.24V) Gain Coefficient	0x3F E834
0x3F E83B	Channel 1	0x3F E838
0x3F E86F		0x3F E86C
0x3F E873	Channel 2	0x3F E870
0x3F E8A7		0x3F E8A4
0x3F E8AB	Channel 3	0x3F E8A8
0x3F E8DF		0x3F E8DC
0x3F E8E3	Channel 4	0x3F E8E0
0x3F E917		0x3F E914
0x3F E91B	Channel 5	0x3F E918
0x3F E94F		0x3F E94C
0x3F E953	Channel 6	0x3F E950
0x3F E987		0x3F E984
0x3F E98B	Channel 7	0x3F E988
0x3F E9BF		0x3F E9BC
⋮	Reserved	⋮
0x3F EFEF	Reserved	0x3F EFEC

Flash ASCII String Identifier

Table 7.3 Flash ASCII String Identifier

Flash Address	Bit(s)	AP73x Model
0x3F EFF0	7:0	A = 0x41
0x3F EFF1	7:0	P = 0x50
0x3F EFF2	7:0	7 = 0x37
0x3F EFF3	7:0	3 = 0x33
0x3F EFF4	7:0	0 = 0x30 (AP730), 1 = 0x31 (AP731)
0x3F EFF5	7:0	0 (null Character)
0x3F EFF6	7:0	Reserved
0x3F EFFF	7:0	Reserved

8. DAC SUGGESTED PROGRAMMING FOR STREAMING MODE

Streaming mode is available to support output of non-repetitive waveforms. In this mode, the host processor must keep the DACs supplied with data. The host must manage the transfer of data from host memory to the AP73x module. If all four channels were operating at the maximum frequency, the host would have to supply data at 0.8 M bytes/sec. The Central Direct Memory Access (CDMA) controller is included in the FPGA firmware to assist the host processor in moving data from host memory to the AP73x on-board sample memory. Each channel will be configured in FIFO mode to buffer the samples written by the host. The on-chip block memory will be used to store a scatter-gather descriptor chain list used by the CDMA controller. Host memory will hold sample data that has been scaled and corrected for gain and offset errors. For this example, it is assumed the host memory used to store the sample data is contiguous, which would allow the addresses in the AXI2PCIeBARs to remain constant. This section will describe the suggested programming sequence to support streaming data. The management of the DMA controller will be done within an interrupt handler.

1. Start in a known state by writing the Control Register with the Software Reset bit set to logic '1'.

2. Reset the DACs by writing the Control Register with the DAC reset bit set to logic '1'.

3. Configure each DAC channel by writing to the appropriate Channel Direct Access register. Set the output range, power-up voltage, clear voltage, and data format.

4. Set the initial output voltage for all DACs by writing the Control Register with the DAC clear bit set to logic '1'. This will power up the DAC outputs. The DACs will output the voltage configured with the previous step.

5. Set the FIFO size for each channel by writing the Channel Start Address and Channel End Address registers. If all channels will be outputting data at the same frequency, make all the FIFOs equal size.

6. Configure the operating mode of each channel as FIFO mode, and set the appropriate bits to select the trigger source.

7. Initialize the DMA scatter-gather descriptor chain list in block RAM. Up to four descriptors could be needed each time a transfer is initiated. All the host memory addresses written to the descriptors must take into consideration the address translation that is performed by the PCIe interface. The Next Descriptor Pointer field must be set for each of the four descriptors. The destination address will be the appropriate Channel FIFO register. Set the bytes to transfer field in the descriptor to one half the size of the sample memory allocated to each channel. The source address will be a host memory address where the next set of sample data for each channel is stored. Write zeroes to the Transfer Descriptor Status Word for each descriptor to indicate that it has not completed.

8. Reset the CDMA by writing the Reset bit in the CDMA Control Register.

9. Poll the CDMA control register until the Reset bit indicates reset is not in progress.

10. Configure the CDMA by writing the CMDA Control Register with Tail Pointer Mode enabled, Scatter Gather Mode selected, Key Hole write enabled, and Cyclic BD Disabled.

11. Write the address of the first scatter-gather descriptor to the CDMA Current Descriptor Pointer Register.

12. Write the address of the descriptor set up for each channel to the CDMA Tail Descriptor Pointer Register. This initiates the DMA transfers.

13. Poll the CDMA Status Register until the CDMA idle bit indicates the CDMA is in the idle state. Each of the FIFOs are now half full.

14. Write the Interrupt Enable register with 0xFF. This enables each DAC channel to generate interrupts. Since each channel is configured in FIFO mode, an interrupt will be generated when any of the channels' FIFOs becomes half full. Also, note the CDMA interrupt is not enabled.

15. Write the following fields of the Master Enable Register:

Master IRQ Enable = 1

Hardware Interrupt Enable = 1

16. Write the Waveform Output Enable bit in the Control Register to start waveform output. The DACs will output the data stored in their FIFOs at the rate of the trigger pulses.

17. Wait for an interrupt from the AP73x module.

18. Read the Interrupt Pending Register. Store the value read for later use in the DMA complete interrupt handler. For each DAC channel interrupt bit in the Interrupt Pending Register that is set to a logic '1' set up the scatter-gather descriptor to transfer up to one half of the channel's FIFO size.

19. For each DAC channel interrupt bit in the Interrupt Pending Register that is not set to a logic '1', remove the channel's descriptor from the scatter-gather chain.

20. Write the address of the scatter-gather descriptor of the first channel requiring service to the CDMA Current Descriptor Pointer Register.

21. Write the following fields of the CDMA control register:

Scatter Gather Mode = 1

Key Hole Write = 1

Cyclic BD Enable = 0

Interrupt on Complete Interrupt Enable = 1

Interrupt on Delay Timer = 0

Interrupt on Error Interrupt Enable = 1

Interrupt Threshold Value = number of descriptors to transfer

Interrupt Delay Timeout = 0

22. Write 0x100 to the Interrupt Enable Register. This disables all DAC channel interrupts and enables the CDMA interrupt.

23. Write the address of the descriptor of the last channel requiring service to the CMDA Tail Descriptor Pointer Register. This will initiate the DMA transfers.

24. Wait for an interrupt from the AP73x module.

25. Read the CMDA status register. Check for error bits that are set.

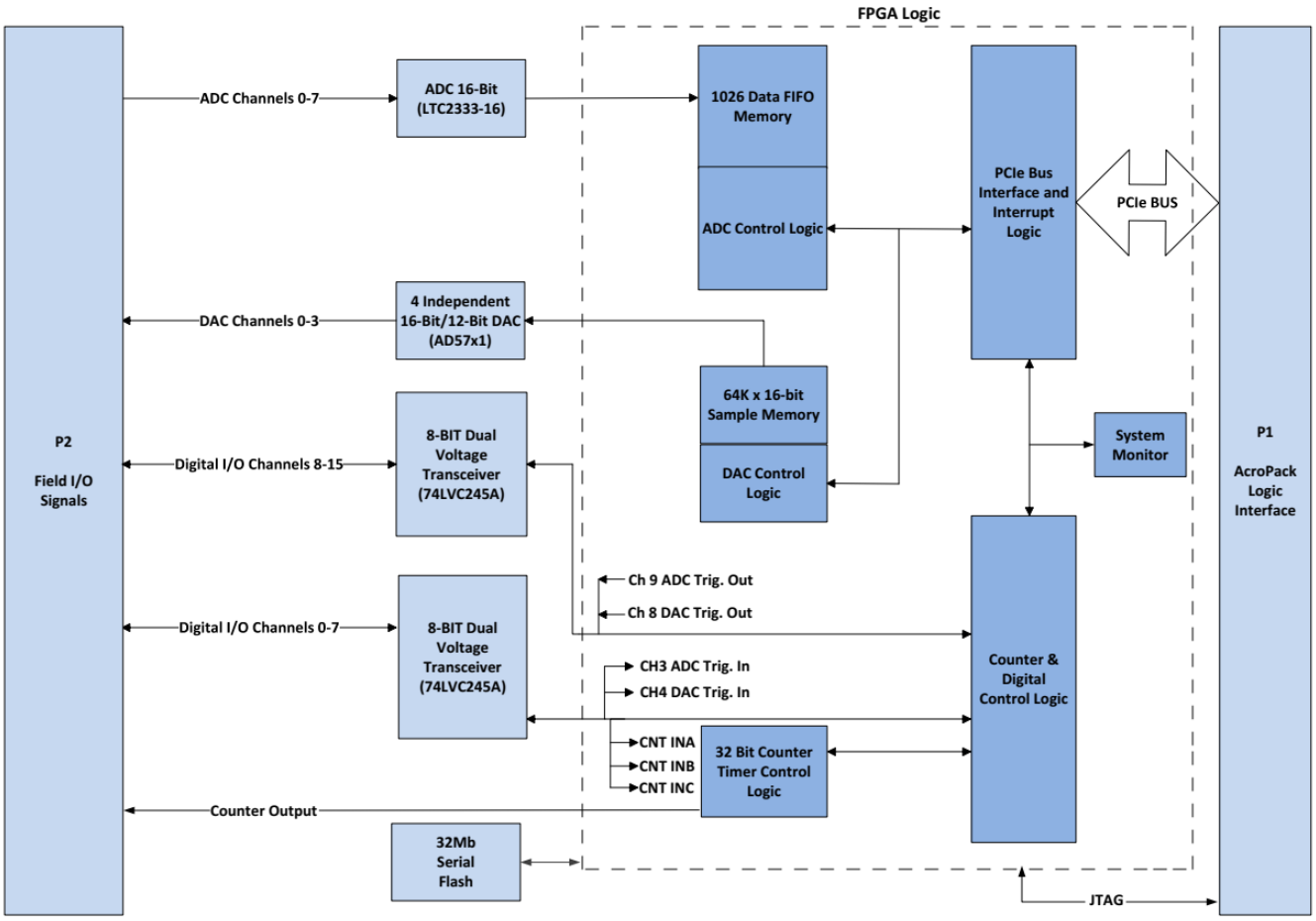
26. Write the Interrupt Acknowledge Register with the saved value from the Interrupt Pending Register from above. This will clear the interrupts for the channels that were serviced by the DMA transfer.

27. Write 0xFF to the Interrupt Enable Register to re-enable the DAC interrupts.

9. THEORY OF OPERATION

This section contains information regarding the design of the board. A description of the basic functionality of the circuitry used on the board is also provided. Refer to the AP73x block diagram, as you review this material.

AP73x BLOCK DIAGRAM



PCIe Interface Logic

The PCIe bus interface logic is embedded within the FPGA. This logic includes support for PCIe commands, including: configuration read/write, and memory read/write. A PCIe interface to the carrier/CPU board provides access to all board functions.

The PCIe bus endpoint interface logic is contained within the FPGA. This logic includes support for PCIe commands, including: configuration read/write, and memory read/write. In addition, the PCIe interface supports requester and/or completion accesses. Maximum payload size of up to 1024 bytes is supported.

The logic also implements interrupt requests via message signaled interrupts. Messages are used to assert and de-assert virtual interrupt lines on the link to emulate the Legacy PCI interrupt INTA# signal.

System Monitor (XADC)

The System Monitor provides status information for the 7 series device. The system monitor is located in the center of the FPGA die. The System Monitor function is built around dual 12-bit, 1-megasamples per second Analog-to-Digital Converter. The system monitor is used to measure FPGA physical operating parameters such as on-chip power supply voltages and die temperature.

Clock Generation

All clocks are derived from the 100 MHz PCIe REF_CLK signal. The PCIe interface includes a PLL that generates a 62.5 MHz clock that is used to clock the bus interfaces. The 62.5 MHz clock is further divided to produce a 31.25 MHz clock that is used to clock the timer and the serial interface to the ADC, DAC, and counter logic.

32Mb Serial Flash

The serial FLASH memory provides 32 megabits of non-volatile storage that is used for FPGA configuration and data storage. The FLASH device is Spansion part number S25FL132K or equivalent. The lower 2 megabytes of memory space are dedicated to storage of the FPGA bitstream. Calibration coefficients and identifier string are stored in the upper half of the flash.

An AXI Quad SPI v3.2 block provides the interface between the internal AXI bus and the Spansion FLASH device.

Counter Timer

Counter timer input control signals are available from the Digital I/O channels 0 to 2 which function as CNT InA, CNT InB, and CNT InC respectively. See Table 3.1 for the list of these signals and their corresponding pin assignments.

One counter output signal, drive by 60V MOSFET, is available at pin 98 of the P2 connector. The counter output MOSFET is +5 Volt with 1K pullup.

Digital Input/Output

Digital input/output signals to the FPGA are buffered using TTL drivers. Output operation is considered 'Fail-safe'. That is, the Digital Input/Output signals are always configured as input upon FPGA configuration during power-up. This is done for safety reasons to ensure reliable control under all conditions. After configured the digital channels can be set as output. 10K pullup resistors to +5 volts are tied to each of the digital I/O channels.

Analog Input

Up to 8 differential analog inputs are available. The ADC is a 16-bit, successive approximation converter with a built-in sample and hold circuit. The ADC can be configured on a channel to channel basis to one of the seven available ranges.

Bipolar ranges of +/-10.24, +/-10, +/-5.12, +/-5.0

Unipolar ranges of +10.24 to 0, +10.0 to 0, +5.12 to 0.

All channels can be configured individually to one of 7 ranges.

Analog Output

Up to 4 DAC 16-bit (AP730 model) or 12-bit (AP731 model) voltage output channels are available with a 7.5uS output settling time. Four individual DAC chips interface to an FPGA which provides the serial shift digital data that is converted.

Each channel may be independently configured to operate in direct access, single burst, continuous, or streaming (FIFO) mode.

The on-board 64K x 16-bit sample memory is shared among the four channels. The amount of memory allocated to each channel is configurable with a start and end address unique to each channel. This memory is used for the continuous, FIFO, and single conversion mode of operation.

Direct Access – Each DAC can be individually address and updated with direct register write operation.

Continuous Output Mode - Continuous conversions are implemented by continuously cycling through the waveform memory, from Start Address to End Address, until halted by software. The interval between conversions is controlled by the interval timer. Conversions are initiated by issue of a software or external trigger.

FIFO Output Mode - Each of the channel's FIFOs can be filled/loaded with new data without stopping output waveform generation.

Single Conversion Mode - Conversions are started with the Start Address and can continue until the channel's End Address is reached.

Software selectable output ranges available include:

0 to 10 Volts, 0 to 5 Volts, +/-10 Volts, +/-5 Volts, +/-3 Volts,
- 2.5V to +7.5 Volts

10.SERVICE AND REPAIR

Service and Repair Assistance

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

Preliminary Service Procedure

Before beginning repair, be sure that all of the procedures in Section 3, Preparation for Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the carrier and/or AP module with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Where to Get Help

If you continue to have problems, your next step should be to visit the Acromag website at https://www.acromag.com. Our website contains the most up-to-date product and software information.

Go to the "Support" tab or your specific AcroPack model ordering page.

Acromag's application engineers can also be contacted directly for technical assistance via email or telephone through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab. When needed, complete repair services are also available.

Phone: 248-295-0310
Email: solutions@acromag.com

11.SPECIFICATIONS

Physical

Length ..... 70.0 mm (2.756 in)
Width ..... 30.0 mm (1.181 in)
Stacking Height ..... 12.5 mm (0.492 in)

Unit Weight (does not include shipping material):
..... 0.299 ounces (8.48 g)

Power

Summarized below are the expected current draws for each of the specified power supply voltages on the AP73x. Typical is with digital and DAC output unloaded, maximum is with loaded outputs.

Power Supply Voltage	Current Draw
3.3 VDC +/- 5%	250mA typ., 300mA max.
1.5 VDC +/- 5%	260mA typ., 300mA max.
5.0 VDC +/- 5%	85mA typ., 280mA max.
+12 VDC +/- 5%	22mA typ., 30mA max.
-12 VDC +/- 5%	3.5mA typ., 15mA max.

Environmental

Operating Temperature ..... -40°C to +85°C
Applications requiring operating temperatures above 70°C will require purchase of *AcroPack Heatsink Accessory* ***AP-CC-01.*** An air cooled application will require a minimum airflow of 400 LFM.
Relative Humidity..... 5-95% non-condensing
Storage Temperature..... -55 to +125°C
Isolation ..... Not Isolated
EMC Directives ..... AcroPack complies with EMC Directive 2004/108/EC.
Immunity per EN 61000-6-2 ..... This is a Class A product
Electrostatic Discharge Immunity (ESD)
per IEC 61000-4-2.
Radiated Field Immunity (RFI)..... per IEC 61000-4-3.
Electrical Fast Transient Immunity (EFT)
per IEC 61000-4-4
Surge Immunity..... per IEC 61000-4-5.
Conducted RF Immunity (CRFI)..... per IEC 61000-4-6.

Emissions per EN 61000-6-4: ..... This is a Class A product

Enclosure Port ..... per CISPR 16
Low Voltage AC Mains Port..... per CISPR 16.

Vibration and Shock ..... This AcroPack is designed to comply with the following Vibration and Shock standards:
Vibration, Sinusoidal Operating .... Designed to comply with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis
Vibration, Random Operating..... Designed to comply with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis.
Shock, Operating..... Designed to comply with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3mS half sine, 18 shocks at 6 orientations for both test levels.

Reliability Prediction

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled,* G_BG_C. Note that this estimate is for the AP730 model with the 16-bit AD5761 DAC.

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	2,038,782	232.7	490.5
40°C	1,026,505	117.2	974.2

[1] FIT is Failures in 10^9 hours.

DAC Analog Output

Output Channels ..... Four Single Ended
Output Signal Type..... Voltage (Non-isolated)
Resolution 16-bits
Settling Time ..... 12.5 µs 20 V step to 1 LSB at 16-bit resolution maximum
8.5 µs 10 V step to 1 LSB at 16-bit resolution maximum
7.5 µs typical
Output Ranges ..... Bipolar: +/-10 Volts, +/-5 Volts, +/-3 Volts, - 2.5V to +7.5 Volts
Unipolar: 0 to 10 Volts, 0 to 5 Volts (software selectable)
Output Current..... -10mA to 10mA (Maximum); this corresponds to a minimum load resistance of 1KΩ with a 10V output.
Data Format ..... Input coding to the DAC is straight binary code when channel is configured for 0-10V or 0-5V ranges.
Two's complement coded for bipolar ranges (software selectable)
Monotonicity..... ±1 LSB maximum

The DAC is monotonic over the full operating temperature range. The output either increases or remains constant for increasing digital input code.

Linearity Error ..... ± 2 LSB (maximum)

Maximum Uncalibrated Error ..... AP730 (AD5761) @ -40°C to 85°C:
Linearity Error is +/- 0.003% FSR maximum (i.e. +/-2 LSB).
Offset Error is +/- 0.05% FSR (i.e. 20V SPAN) maximum.
Gain Error is +/- 0.1% FSR maximum.
Total Error +/- 0.153% FSR maximum (+/- 98.5 LSB)

..... AP731 (AD5721) @ -40°C to 85°C:
Linearity Error is +/- 0.0122% FSR maximum (i.e. +/-0.5 LSB).
Offset Error is +/- 0.05% FSR (i.e. 20V SPAN) maximum.
Gain Error is +/- 0.1% FSR maximum.
Total Error +/- 0.1512% FSR maximum (+/- 6.2 LSB)

Maximum Calibrated Error ..... The maximum calibrated error combining the linearity and adjusted offset and gain errors.
AP730:
Linearity Error is +/-2 LSB maximum
Offset Error is +/-0.0625 LSB maximum
Gain Error is +/-0.0625 LSB maximum
Total Error +/-2.125 LSB (+/- 0.0032% FSR) maximum
AP731:
Linearity Error is +/-0.5 LSB maximum
Offset Error is +/-0.0625 LSB maximum
Gain Error is +/-0.0625 LSB maximum
Total Error +/-0.625 LSB (+/- 0.0152% FSR) maximum
Calibration coefficients are determined near room temperature. The Total Error does not include shifts over temperature.

ADC Analog Input

Input Channels ..... 16 Differential
Input Signal Type..... Voltage (Non-isolated)
Resolution 16-bits
Conversion Rate..... 791,139.24Hz maximum
Settling Time ..... Full-Scale Step 420 ns to 0.005% of FSR
Input Ranges ..... Bipolar ranges of +/-10.24, +/-10, +/-5.12, +/-5.0

Unipolar ranges of 0 to+10.24, 0 to +10.0, 0 to+5.12.
(software selectable) Selected range applies to each channel and can be individually selected on a per channel basis.

Input Resistance..... >1000 GΩ typical
Input Leakage Current ..... 500pA maximum
Data Format ..... The output data coding is in binary two's compliment for all bipolar ranges and in straight binary format for all unipolar ranges.
No Missing Codes..... 16-bit
Linearity Error ..... ± 2 LSB All Ranges but 0V to 5.12V Range (maximum)
± 3 LSB 0V to 5.12V Range (maximum)
Maximum Uncalibrated Error ..... LTC2333-16 @ 25°C:
Offset Error ± 700 µV maximum
8.96 LSB (0 to 5.12V Range)
4.59 LSB (±5.0V and 0 to 10V Range)
4.48 LSB (±5.12V and 0 to 10.24V Range)
2.29 LSB (±10.0V Range)
2.24 LSB (±10.24V Range)
Gain Error is ± 0.1% FSR or (± 65.5 LSB) maximum.
Total Error
78 LSB (0 to 5.1V Range,)
73 LSB (±5.0V and 0 to 10V Range)
72 LSB (±5.12V and 0 to 10.24V Range)
70 LSB (± 10.0V Range)
70 LSB (± 10.24V Range)
The Total Error does not include shifts over temperature.
Maximum Calibrated Error ..... Total Error all but 0V to 5.12V Range ±2.125 LSB maximum
Total Error 0V to 5.12V Range ±3.125 LSB maximum
Calibration coefficients are determined near room temperature. The Total Error does not include shifts over temperature.

Counter/Timers

Counter Functions..... Quadrature Position Measurement, Pulse Width Modulation, Watchdog Timer, Event Counting, Frequency Measurement, Period Measurement, Pulse-Width Measurement, and One Shot/Repetitive

Counter Input..... CNT INA, CNT InB, CNT InC – these TTL input ports are used to control start/stop, reload, event input, trigger and up/down operations

Counter Output..... MOSFET output port is used for waveform output, watchdog active indicator, or 1.74µs pulse upon counter function completion. Counter output is programmable as active high or low.

Counter Output Pull-up Voltage ... +5V with 1K pull-up

Counter Output MOSFET BSS138PS
Vds: 60V maximum
Vgs: +/-20 V maximum
Id: 320 mA maximum
Rdson: 1.6 ohm maximum

Debounce Interval..... Input signals with a duration of less than 4.0µs are filtered with debounce enabled via Debounce Enable Register.

Counter Clock Enable Frequencies 62.5MHz, 15.625MHz, 7.8125MHz, 3.90625MHz, or 1.953125MHz

Minimum Input Event ..... 32 ns

Minimum Pulse Measurement ..... 32 ns

Minimum Period Measurement ... 64 ns

Minimum Gate/Trigger Pulse..... 32 ns

Counter Input/Output,
External Trigger Input/Output
Electrical Characteristics ..... VIH: 2.0V minimum
VIL: 0.8V maximum
IOH: –24 mA maximum
IOL: 24mA maximum
VOH: 3.7V minimum VCCA
VOL: 0.55V maximum VCCA

PCIe Bus Compliance

Compatibility..... This device meets or exceeds all written PCI Express specifications per revision 2.1 dated March 4, 2009.

Line Speed..... Gen1 (2.5Gbps) Available through system connector

Lane Operation 1-Lane

1M Memory Space Required ..... One Base Address Register (BAR)

PCIe Bus Data Rates

PCIe Gen 1 (1 lane)	Giga bit / second	Bytes / second
Signaling Rate	2.5 Gb/s	312 Mbyte/s
Ideal Rate[1]	2 Gb/s	250 Mbyte/s

Header Burden plus 4byte Sample Rate[2]	0.332 Gb/s	41.6 Mbyte/s
Actual Measured 4 Byte Read Rate[3]	0.019 Gb/s	2.35 Mbytes/s
Actual Measured DMA 4 Byte Read Rate[4]	0.327 Gb/s	40.9 Mbyte/s
Actual Measured 4 Byte Write Rate[5]	0.320 Gb/s	40 Mbyte/s

Note 1: PCIe x1 Gen 1 = 2.5GT/s (with 10-bit encoding we have a 20% loss in possible throughput due to encoding) giving 2.0 G bits/sec or 250M Bytes/sec.

Note 2: With PCIe we have a header for address and read/write command that is sent with every packet. This header is 20 Bytes with data payload of 4 Bytes (for our typical AcroPack). For each 4 Byte data sample, 24 Bytes are sent.

$\frac{250MByte/s}{24\,Bytes}$ = 10.4 M samples/sec or 41.6 M Bytes/sec or 0.332 G bit/sec

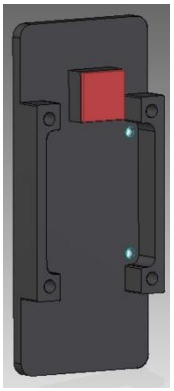
Note 3: For our typical AcroPack have measured back to back 4 Byte read operations completing every 1.7usec. A read operation starts with a host read request. The AcroPack must process the read and fetch the data and then generated the completion back to the host. The host then sends a message back that says I got it. This back and forth hand shaking slows down individual reads.

Note 4: DMA Read of 1024 sample takes 100us. Each sample is 4 Bytes. 100us/1024=0.0977us per sample or 4/0.0977us = 40.94Mbyte/s. We use DMA transfers to improve data transfers on the AP341/2 and AP225/235.

Note 5: Simple write operations are just as fast as DMA read operations. Write data is presented to the AcroPack in one transaction. Measured 4-byte back to back write accesses taking place every 100ns.

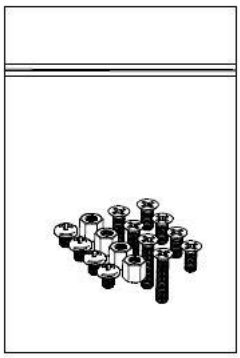
Appendix A

AP-CC-01 Heatsink Kit Installation



Bottom view

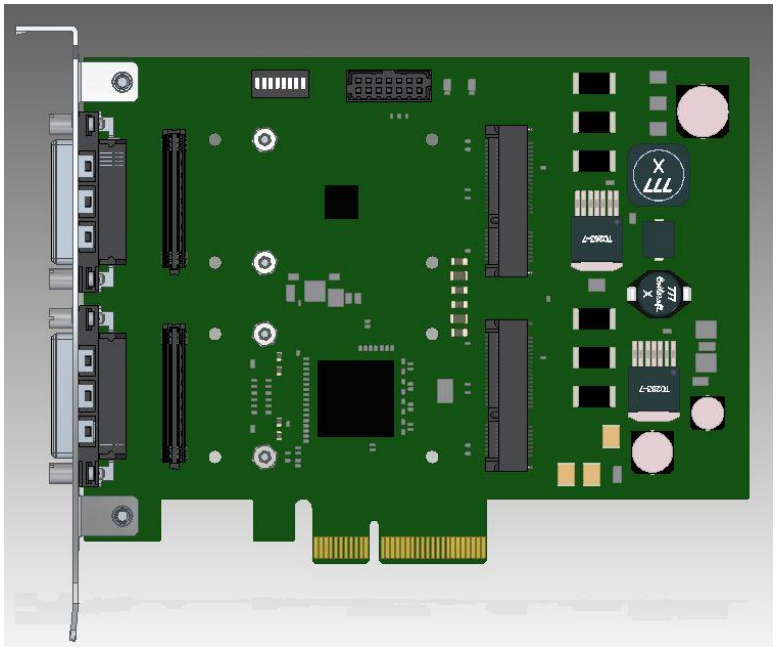
Top view



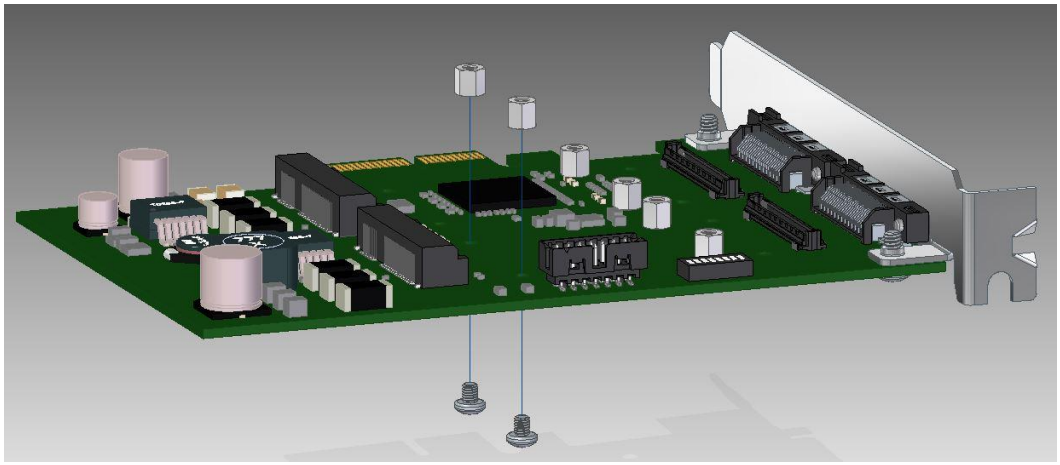
Hardware

AP-CC-01 Heat Sink Kit

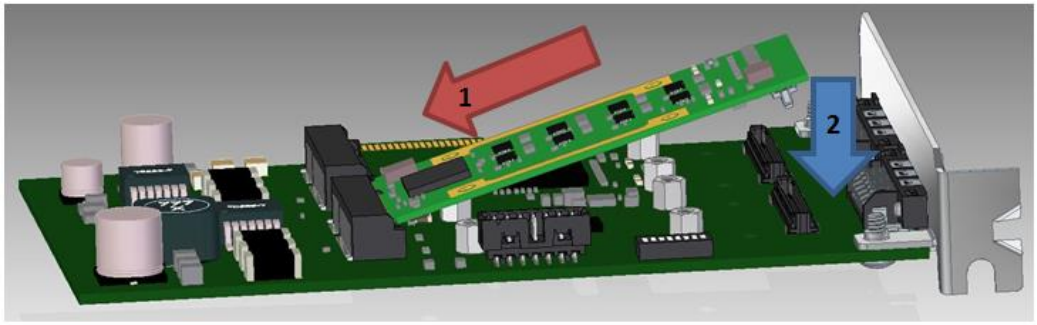
This example will show how to install the AP-CC-01 Heatsink kit with an APCe7020 carrier.



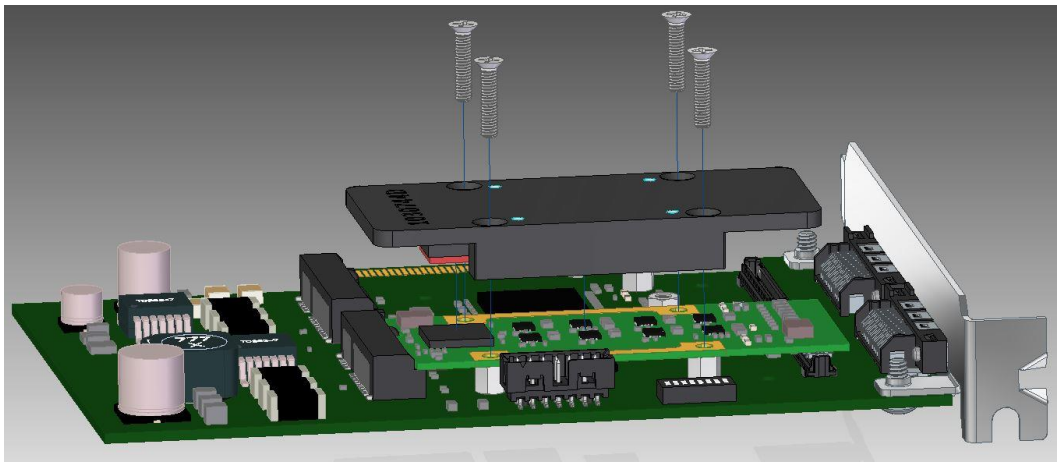
1. Install two standoffs and secure with two screws.



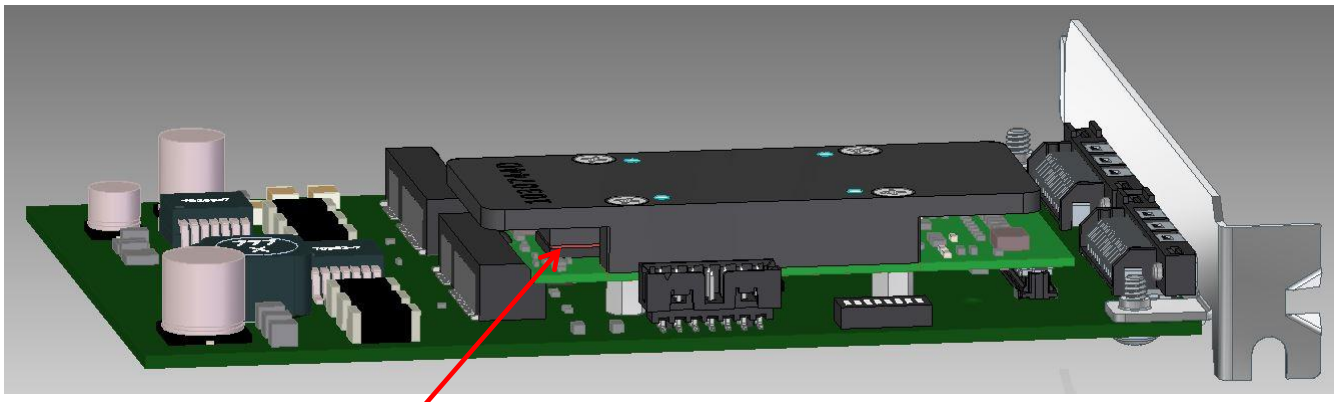
2. Install the AcroPack module.



3. Install the Heatsink and secure with 4 screws.



4. AP-CC-01 Installation is complete.



Note: Make sure the thermal pad is making contact with the FPGA IC.

Certificate of Volatility

<table>
<tr><th colspan="5">Certificate of Volatility</th></tr>
<tr><td colspan="2">Acromag Models:
AP730E-LF</td><td colspan="3">Manufacturer:
Acromag, Inc.
30765 Wixom Rd
Wixom, MI 48393</td></tr>
<tr><th colspan="5">Volatile Memory</th></tr>
<tr><td colspan="5">Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed)
■ Yes □ No</td></tr>
<tr><td>Type (SRAM, SDRAM, etc.)
FPGA based RAM</td><td>Size:
32k byte</td><td>User Modifiable
■ Yes
□ No</td><td>Function:
Data storage for FPGA</td><td>Process to Sanitize:
Power Down</td></tr>
<tr><th colspan="5">Non-Volatile Memory</th></tr>
<tr><td colspan="5">Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed)
■ Yes □ No</td></tr>
<tr><td>Type (EEPROM, Flash, etc.)
Flash</td><td>Size:
32Meg x 1bit</td><td>User Modifiable
■ Yes
□ No</td><td>Function:
Storage of Code for FPGA</td><td>Process to Sanitize:
Clear Flash memory by erasing all sectors of the Flash</td></tr>
<tr><td>Type (EEPROM, Flash, etc.)
One Time Programmable area in flash device</td><td>Size:
3 x 256-byte</td><td>User Modifiable
□ Yes
■ No</td><td>Function:
The OTP area has been disabled by writing the lock bits with logic 1</td><td>Process to Sanitize:
Not applicable</td></tr>
<tr><th colspan="5">Acromag Representative</th></tr>
<tr><td>Name:
Russ Nieves</td><td>Title:
Dir. of Sales and Marketing</td><td>Email:
solutions@acromag.com</td><td>Office Phone:
248-295-0310</td><td>Office Fax:
248-624-9234</td></tr>
</table>

REVISION HISTORY

The following table shows the revision history for this document:

Release Date	Version	EGR/DOC	Description of Revision
31 JAN 2020	A-Prelim	ENZ/ARP	Preliminary release.
27 FEB 2020	A	ENZ/ARP	Changed EMC directives "designed to comply" to "complies". Rev A release.
3 MAR 2022	B	ENZ/AMM	Added AP731E-LF model information.