IP235 & 230 BLOCK DIAGRAM

I/O INTERFACE

P2

CALIBRATION MEMORY EEPROM

Clock

Address / Data

LOGIC INTERFACE

P1

External Trigger Input or Output

FPGA

CALIBRATION MEMORY CONTROL LOGIC

DATA BUS

J1 RANGE SELECTION

ID SPACE IDENTIFICATION BYTES

Data

DIGITAL TO ANALOG CONVERTER CHANNEL 0

Channel 0 Analog Signal

CONTROL

PARALLEL TO SERIAL CONVERTER

ADDRESS BUS

INTERVAL TIMER*

ANALOG OUTPUT CHANNELS

HARDWARE TRIGGER* GENERATOR

J8 RANGE SELECTION

INTERRUPT* LOGIC & VECTOR

CONTROL BUS

DIGITAL TO ANALOG CONVERTER CHANNEL 7**

Channel 7 Analog Signal

Data

WAVEFORM MEMORY* CONTROL LOGIC

DATA

ADDRESS

Common

WAVEFORM MEMORY* 32k x 8 SRAM
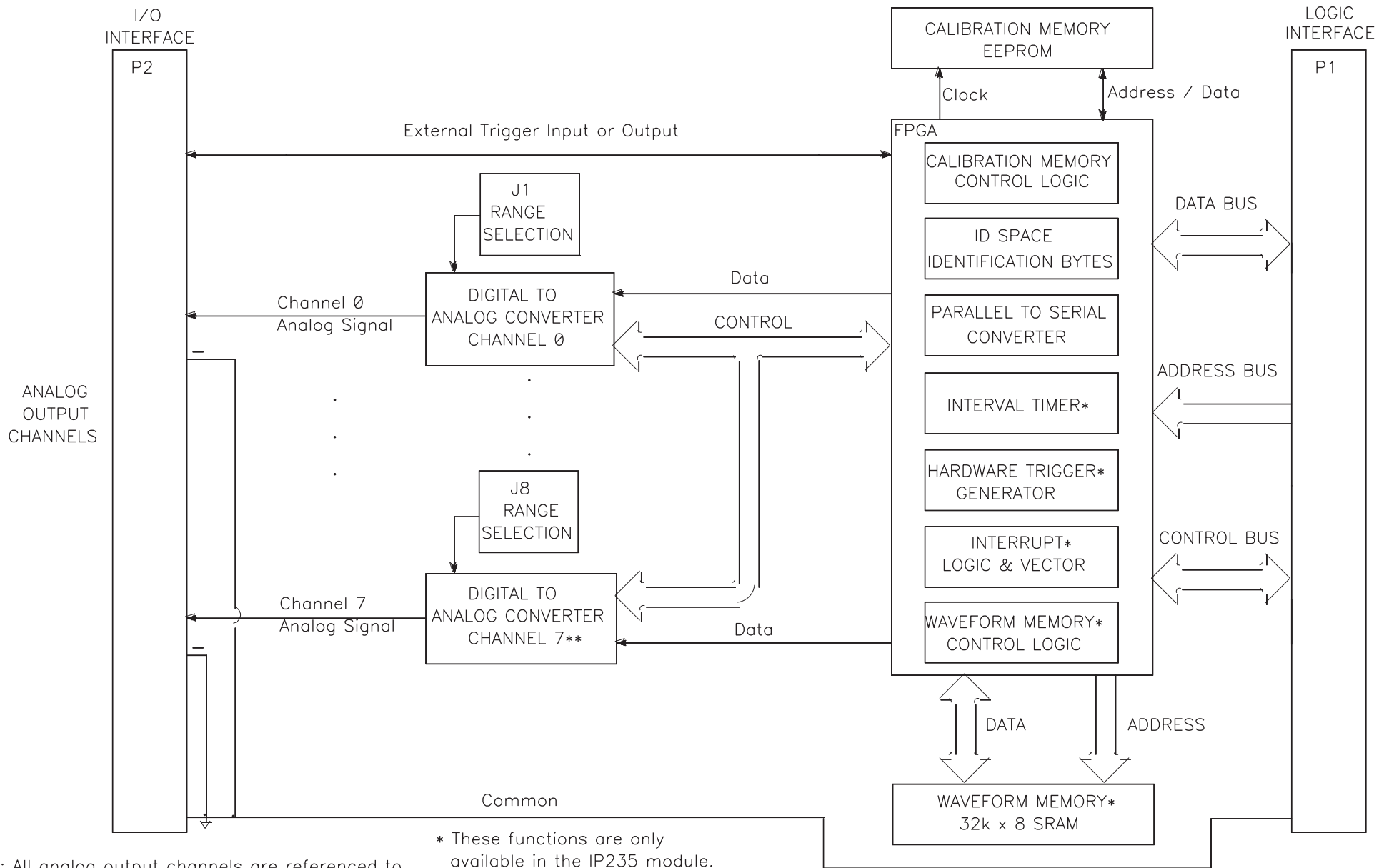
NOTE: All analog output channels are referenced to analog ground. To avoid ground loops do not connect grounded loads to the negative side of the output.

* These functions are only available in the IP235 module.

** Channels 4—7 are only available on 8—channel models

4501—621A