VPX6600

Intel® 6th Generation Core

3U VPX CPU Module

USER'S MANUAL

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1.0 GENERAL INFORMATION

1.1 Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the VPX6600 CPU. It is not intended for a general, non-technical audience that is unfamiliar with computer-on-module (COM) devices and their application.

1.2 Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag,

1.2.1 Trademark, Trade Name and Copyright Information

1.2.2 Class A Product Warning

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

1.2.3 Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, batteries, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

1.3 Product Summary

The VPX6600 is a CPU module that uses an Intel 6th Generation Core Processor (Skylake) with a 3U VPX form factor. It is available in both air and conduction-cooled varieties.

The module can support either one or two DDR4 ECC SODIMMs, for a total of up to 32GB. The SODIMMs are firmly attached to the module with screws and surrounded by heat sink material to provide a mechanically and thermally robust mechanism. Extended temperature models are available for operating in a -40°C to +85°C range.

A large amount of I/O is available, as summarized in Section 6.2 below.

The VPX6600 contains an M.2 expansion card slot to provide on-board storage capabilities. The M.2 slot supports the use of SATA III and PCIe Gen. 3 storage drives.

A two digit LED display is available for Power ON Self-Test (POST) codes, should a problem arise during the boot operation. This display is available for application software user codes after POST to aid in software debugging.

The optional VPX6600-RTM Rear-Transition Module is available to provide easy access to all of the P2 connector's I/O signals.

1.4 Related Material

The following manuals and part specifications provide the necessary information for in-depth understanding of the VPX6600 module.

- The APTIO Skylake Core BIOS Manual For Acromag Products using the Skylake Processor - Referred to hereafter as *Aptio Skylake Core BIOS Manual.*
- Intel® "6th Generation Intel® Processor Datasheet for H-Platforms – Volume 1 of 2", May 2016. http://www.intel.com/content/www/us/en/processors/core/6th-gen-core-family-mobile-h-processor-lines-datasheet-vol-1.html

1.5 Ordering Information

The VPX6600 ordering options are given in the following table.

Model Number	***Description***	***Temp Range***
VPX6600-LF	*Air-cooled 3U VPX CPU Module*	*0°C to 70°C*
VPX6601-LF	*Air-cooled 3U VPX CPU Module (No Battery)*	*0°C to 70°C*
VPX6600-CC-LF	*Conduction-cooled 3U VPX CPU Module*	*-40°C to 85°C*
VPX6601-CC-LF	*Conduction-cooled 3U VPX CPU Module (No Battery)*	*-40°C to 85°C*
VPX6600-RTM-LF	*VPX6600 Rear Transition Module*	*-40°C to 85°C*

Note: All VPX6600 CPU modules contain 32GB of DDR4 SDRAM memory.

1.6 Key Components and Features

The VPX6600 block diagram shown in Fig. 1.6.1 illustrates the key components and features that are summarized on the following pages.

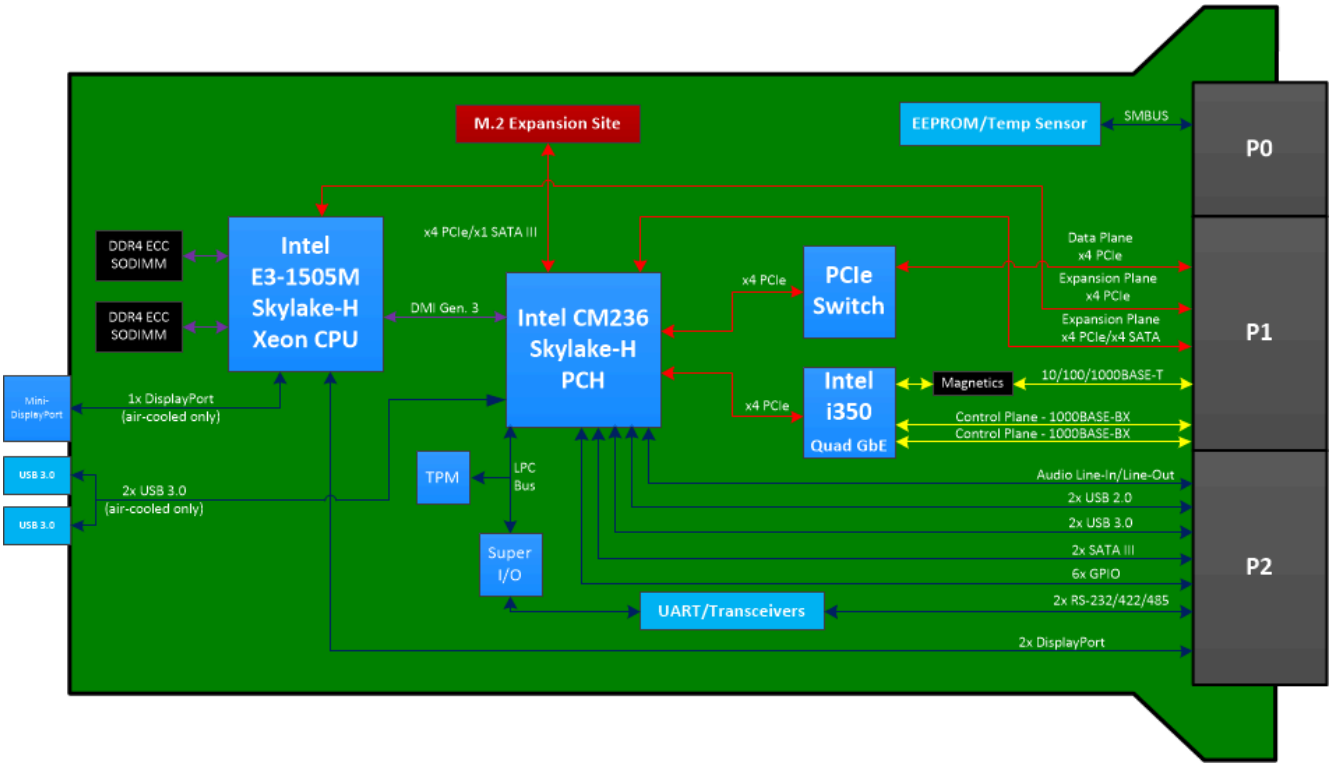


Figure 1.6.1: VPX6600 Block Diagram

1.6.1 Intel® 6th Gen (Skylake) Xeon CPU

The VPX6600 uses the 2.8GHz (3.7GHz max Turbo) quad-core Intel 6th Gen Xeon E3-1505Mv5 CPU. This is a 64-bit CPU using a 14-nanometer process with integrated GT2 graphics and contains direct interfaces for DDR4, DDI, and PCIe x16. In addition, the Direct Media Interface (DMI) is used to connect to the CM236 Platform Control Hub (PCH).

- **DDR4 SDRAM –** Two SODIMM sockets support up to 32GB of DDR4 ECC at 2133MHz. Dual-channel mode is used with the two SODIMMs. The SODIMMs are attached to the module firmly with screws and surrounded by heat sink material to provide a robust mechanism both mechanically and thermally.
- **PCIe Gen3 x4 (1) –** Traditionally used for external graphics, but supports any PCIe device(s). On the VPX6600, this x4 PCIe interface is connected to an expansion plane fat pipe on the VPX backplane allowing for direct board-to-board communication with an adjacent slot.

- **DDI (3) –** These Digital Display Interfaces can be configured to be DisplayPort 1.2, DVI, or HDMI. On the VPX6600, two display interfaces are routed to the P2 connector with the third available on a front I/O Mini-DisplayPort connector (Air-cooled only).
- **Programmable CPU power limits –** By simply programming a lower power limit in the BIOS setup, the CPU can be used in applications where less power is available or heat removal is an issue. This is accomplished by the CPU automatically underclocking its frequency to maintain a power level at the set limit.

1.6.2 Intel CM236 PCH

The Intel C230 Series CM236 PCH provides extensive I/O support, as listed below:

- **PCIe Gen3 x4 (4)** – There are four PCIe Gen3 ports of x4 width. The first is connected to the Intel I350 Quad Gigabit Ethernet Controller. The second is connected to the PEX8714 PCIe switch. The third is connected to an expansion plane fat pipe on the VPX backplane allowing for direct board-to-board communication with an adjacent slot. The fourth is connected to the M.2 expansion slot.
- **SATA Gen3 (7)** – There are seven SATA III ports on the VPX6600. All the ports are configurable as SATA ports or PCIe lanes. Two are connected to the P2 backplane connector. One is connected to the M.2 expansion site. The remaining 4 are connected to the expansion plane fat pipe on the VPX backplane.
- **USB 3.0 (4)** – There are four USB 3.0 ports on the VPX6600. Two ports are connected to the P2 backplane connector. The other two are available on front I/O USB connectors (Air-cooled only)
- **USB 2.0 (2)** – There are two additional ports that function at USB 2.0 or USB 1.1 speeds that are connected to the P2 backplane connector.
- **GPIO (6) –** There are six 3.3V general purpose inputs/outputs available on the P2 backplane connector. These have software-configurable direction control.
- **LPC** – The Low Pin Count bus is connected to the NCT6106 Super I/O for serial ports and debug port 80 connections, in addition to the AT97SC3204 TPM device.
- **Line-Level Audio In/Out** – Stereo audio input and output from onboard HDA audio codec are available on the P2 backplane connector.
- **SMBUS** – This I2C-compatible System Management Bus has connections to the memory DIMMs, the VPX backplane, the Ethernet controller, and an on-board EEPROM that can be used for module identification.

1.6.3 Intel I350 Quad Gigabit Ethernet Controller

The Intel I350 Ethernet Controller contains four ports that can be individually configured to be either a fully-integrated gigabit Ethernet media access control (MAC), physical layer (PHY) port or a SGMII/SerDes port. The VPX6600 uses three of the four ports: two ports are configured to be 1000BASE-BX connections for a board-to-board control plane interface across the VPX backplane. The third port is configured to be a 1000BASE-T Gigabit Ethernet connection available on the P1 backplane connector.

1.6.4 Nuvoton NCT6106 Super-I/O

The Nuvoton NCT6106D is an LPC device that provides temperature and voltage monitoring, Port 80 debug via 2 digit 7-segment display, and when connected to UART transceivers, two RS-232/RS-422/RS-485 (software selectable) serial ports.

1.6.5 Atmel AT97SC3204 TPM

The Atmel AT97SC3204 is a fully integrated security module that implements version 1.2 of the Trusted Computing Group (TCG) specification for Trusted Platform Modules (TPM). The TPM includes a cryptographic accelerator capable of computing a 2048-bit RSA signature in 200ms and a 1024-bit RSA signature in 40ms. Performance of the SHA-1 accelerator is 20µs per 64-byte block.

1.6.6 Avago PEX8714 PCIe Switch

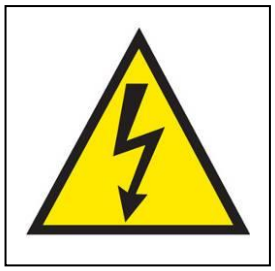
The Avago PEX8714 is a 12-lane, 5-port PCI Express Gen 3 switch. The VPX6600 uses the switch to interface with the PCIe x4 Data Plane fat pipe connection on the VPX backplane. The switch is used on the VPX6600 to allow it to be used in multi-processor systems that do not contain a dedicated PCIe switch card.

1.6.7 M.2 Expansion Site

The VPX6600 contains one M.2 expansion site that can be used as a high-speed, high-bandwidth storage interface. The M.2 site uses an M-keyed connector which, according to the M.2 PCI-SIG specification, supports storage devices that use either a SATA III interface or a PCIe x4 interface. M.2 storage modules that use the PCIe x4 interface can achieve throughput speeds over 4x faster than traditional SATA III. Module lengths of 42, 60, and 80mm can be utilized on the VPX6600.

2.0 PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.

WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

2.1 Unpacking and Inspecting

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

2.2 Installing into a VPX Backplane

The VPX6600 is a 3U, single-slot VPX module. For proper cooling, the air-cooled model must only be installed into an air-cooled VPX chassis and the conduction-cooled model must only be plugged into a conduction-cooled VPX chassis.

The VPX6600 module is designed to comply with all physical and electrical specifications of the VITA 46 VPX Base Specification and the VITA 65 OpenVPX Specification.

***WARNING:* Never install or remove any boards before turning off power to the bus and all related external power supplies.**

1. Disconnect all power supplies to the backplane and the VPX chassis. Disconnect the power cable.
2. Verify that all DIP switch settings are correct.
3. Verify that the card cage slot is clear and accessible.
4. Install the VPX6600 in the card cage by centering the unit on the guides in the slots (P0 connector facing up). Push the board slowly toward the rear of the chassis until the VPX connectors engage. The board should slide freely in the guides.

***WARNING:* Do not use excessive force or pressure to engage the connectors. If the boards do not properly connect with the backplane, remove the module and inspect all connectors and guide slots for damage or obstructions.**

1. Secure the module to the chassis by tightening the machine screws at the top and bottom of the board.

Connect all remaining peripherals by attaching each interface cable into the appropriate connector on the front of the VPX6600 board (air-cooled only), or on the VPX6600-RTM Rear Transition Module.

3.0 HARDWARE INFORMATION AND CONFIGURATION

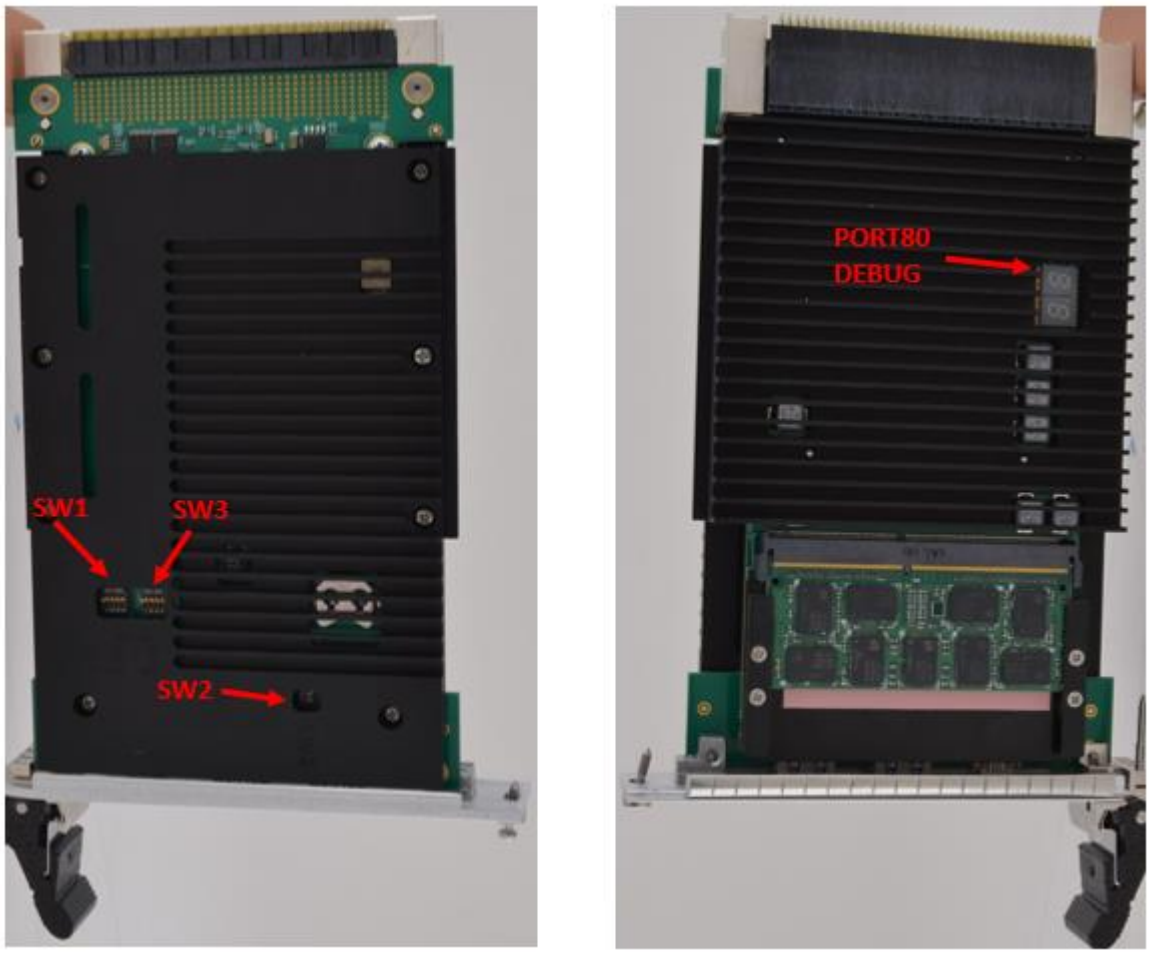


Figure 3.1.1: VPX6600 Top View (right) Bottom View (left)

3.1 Module Hardware Switch Configuration

3.1.1 Core Configuration Switch SW1

The configuration switch settings for SW1 depends on the revision of the board. If the revision of the VPX6600 product is Rev G or earlier, use the SW1 switch settings shown in Table 3.1.a. If the revision of the VPX6600 product is Rev H or later, use the SW1 switch settings shown in Table 3.1.b.

Table 3.1.a summarizes the functions, settings, and descriptions for dip switches SW1-1 thru SW1-4 for Rev G or earlier VPX6600 products.

Table 3.1.a: Core Configuration Switch SW1

Core Configuration Switch SW1			
Position	**Function**	**Switch Setting**	**Description**
1	Reserved	OFF	Reserved
		ON	Reserved
2	Expansion Plane Interface	OFF	PCIe Interface
		ON	SATA Interface
3	RTC Voltage	OFF	Coin-cell battery not used
		ON	Coin-cell battery used as RTC voltage
4	Not Used	OFF	Reserved
		ON	Reserved

SW1-1 is reserved.

SW1-2 is used to select the interface on one of the expansion planes. The expansion plane interface can either be one x4 PCIe connection or four individual SATA III interfaces.

SW1-3 is used to configure the source of the CPU's RTC voltage. With a coin-cell battery installed, the CPU will use the coin-cell battery as the RTC voltage. Turning SW1-3 on will use the VPX Battery input on Pin P1-G3 for the RTC voltage.

WARNING: ***If SW1-3 is closed with a coin-cell battery installed, it will connect the coin-cell to any voltage present on the VPX Battery pin on the VPX connector P1-G3. The coin-cell battery must be removed before closing switch SW1-3 if a voltage is supplied by the VPX backplane!***

SW1-4 is unused.

Table 3.1.b summarizes the functions, settings, and descriptions for dip switches SW1-1 thru SW1-4 for Rev H or later VPX6600 products.

Table 3.1.b: Core Configuration Switch SW1

Core Configuration Switch SW1				
Position	**Function**	**Switch Setting**		**Description**
1 - 2	NT Mode	SW1-1	SW1-2	
		ON	ON	NT Mode Disabled
		OFF	OFF	NT Mode Enabled
3	Expansion Plane Interface	OFF		PCIe Interface
		ON		SATA Interface
4	RTC Voltage	OFF		Coin-cell battery not used
		ON		Coin-cell battery used as RTC voltage

SW1-1 and SW1-2 are used to enable/disable non-transparent mode on the PEX8714 PCIe switch. Non-transparent mode provides the ability to use multiple processors in the same system.

SW1-3 is used to select the interface on one of the expansion planes. The expansion plane interface can either be one x4 PCIe connection or four individual SATA III interfaces.

SW1-4 is used to configure the source of the CPU's RTC voltage. With a coin-cell battery installed, the CPU will use the coin-cell battery as the RTC voltage. Turning SW1-4 on will use the VPX Battery input on Pin P1-G3 for the RTC voltage.

WARNING: ***If SW1-4 is closed with a coin-cell battery installed, it will connect the coin-cell to any voltage present on the VPX Battery pin on the VPX connector P1-G3. The coin-cell battery must be removed before closing switch SW1-4 if a voltage is supplied by the VPX backplane!***

3.1.2 Core Configuration Switch SW2

Table 3.1.c summarizes the functions, settings, and descriptions for dip switch SW2.

Table 3.1.c: Core Configuration Switch SW2

Core Configuration Switch SW2		
Function	**Switch Setting**	**Description**
FRU Voltage Select	1-2	FRU uses +3.3V
	2-3	FRU uses +3.3V_AUX
Not Used	4-5	Reserved
	5-6	Reserved

SW2-1 is a single-pole, dual-throw switch used to select the voltage source for the following devices:

FRU EEPROM

FRU Temperature Sensor

When configured to use the auxiliary +3.3V supply, these devices can still be operated while the rest of the system is unpowered.

3.1.3 Core Configuration Switch SW3

Table 3.1.d summarizes the functions, settings, and descriptions for dip switches SW3-1 thru SW3-4. The factory default settings for all SW3 switches is OFF.

Table 3.1.d: Core Configuration Switch SW3

Core Configuration Switch SW3			
Position	**Function**	**Switch Setting**	**Description**
1	RTC CMOS Reset	OFF	Normal Operation
		ON	Clear RTC CMOS
2	Reserved	OFF	Normal Operation
		ON	Reserved
3	Reserved	OFF	Normal Operation
		ON	Reserved
4	Reserved	OFF	Normal Operation
		ON	Reserved

SW3-1 is used to clear the Battery-backed RTC CMOS Battery-backed SRAM. To clear the CMOS SRAM, close SW3-1 momentarily and then open it again. The switch must be in the open position for normal operation.

SW3-2 is reserved and should be left in the OFF position for normal operation.

SW3-3 is reserved and should be left in the OFF position for normal operation.

SW3-4 is reserved and should be left in the OFF position for normal operation.

3.2 Power Supply and Management

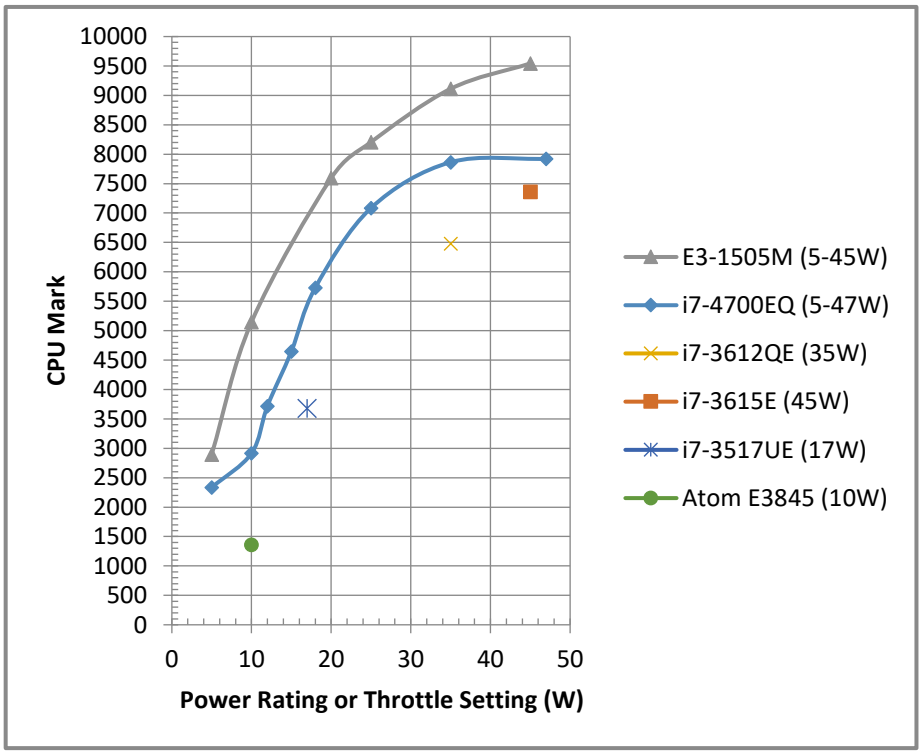
3.2.1 Power Supply Requirements

The VPX6600 must be supplied both +3.3V and 5V from the VPX backplane.

For allowed voltage ranges and expected power draw, see the specifications listed in Section 6.4.

3.2.2 Programmable CPU Power Limits

The VPX6600 features programmable power limits, allowing the user to 'dial-down' the maximum power consumption of the CPU in systems where power is a concern. The graph below shows that the E3-1505M CPU outperforms other available embedded Intel CPU's at every power point from 5W - 47W.



By simply programming a lower power limit in the BIOS setup, the CPU can be used in applications where less power is available or heat removal is an issue. This is accomplished by the CPU automatically underclocking its frequency to maintain a power level at the set limit.

Note: Once the minimum frequency of 800MHz is reached the programmed limit could be exceeded. Extremely large workloads have a realistic minimum power of around 20W. However, light to medium workloads can effectively maintain a power limit as low as 5-10W.

There are two programmable CPU limits. These are the long-term average Power Limit 1 (PL1) and the short-term Power Limit 2 (PL2). Depending on a windowed Power Limit 1 Time 'constant', the CPU can spend a short time above power level PL1 up to a maximum of PL2, allowing a significant performance boost for short workloads. If the CPU power remains above PL1 at the end of this time the power is

then limited back to PL1. The power must drop below the PL1 limit before it allowed to increase back to PL2 again. For time spent above PL1 an equivalent amount of time must be spent below PL1 in order for it to rise again to PL2. The maximum time could be as much 2.5x the value of the PL1 Time.

The default values for the CPU are as follows:

PL1: 45W
PL2: 56W
Tau: 28 seconds

PL1 and PL2 can be programmed in watts to any value below the default. Entering a value above the default will result in the default value being used. Entering 0 also results in the default value being used.

PL1 Time can be programmed to any number of seconds up to 256, however it is recommended by Intel to always use the default value of 28. This value maximizes the effectiveness of the short-term performance boost while ensuring that the life of the part is not jeopardized by spending too much time above PL1.

More details about programming these power limits using the BIOS setup utility are provided in *Aptio Skylake Core BIOS Manual*.

3.2.3 Power Management

The VPX6600 module uses the Advanced Configuration and Power Interface (ACPI) 3.0 standard to provide user-managed power via the operating system, contingent upon the carrier board selected.

The Advanced Configuration and Power Interface (ACPI) provides an open standard for device configuration and power management by the operating system. More details about this feature are provided in *Aptio Skylake Core BIOS Manual*.

3.3 CPU

The VPX6600 uses the 2.8GHz (3.7GHz max Turbo) quad-core Intel 6th Gen (Skylake) Xeon E3-1505Mv5 CPU. This is a 64-bit CPU using a 14-nanometer process with integrated GT2 graphics and contains direct interfaces for DDR4, DDI, and PCIe x16. In addition, the Direct Media Interface (DMI) is used to connect to the CM236 Platform Control Hub (PCH).

- **DDR4 ECC SDRAM –** 2 SODIMM sockets support up to 32GB of DDR4 ECC at 2133MHz. Dual-channel mode is used with 2 SODIMMs. The SODIMMs are attached to the module firmly with screws and surrounded by heat sink material to provide a robust mechanism both mechanically and thermally.
- **PCIe Gen3 x4 (1) –** Traditionally used for external graphics, but supports any PCIe device(s). On the VPX6600, this x4 PCIe interface is connected to an expansion plane fat pipe on the VPX backplane allowing for direct board-to-board communication with an adjacent slot.

- **DDI (3) –** These Digital Display Interfaces can be configured to be DisplayPort 1.2, DVI, or HDMI. On the VPX6600, two display interfaces are routed to the P2 connector with the third available on a front I/O Mini-DisplayPort connector (Air-cooled only).
- **Programmable CPU power limits –** By simply programming a lower power limit in the BIOS setup, the CPU can be used in applications where less power is available or heat removal is an issue. This is accomplished by the CPU automatically underclocking its frequency to maintain a power level at the set limit.

3.3.1 Active Processor Core Selection

All of the CPU cores should be kept active in high-performance systems requiring all available computing power. Conversely, applications having reduced power requirements can save power by disabling one or more of the CPU cores. The number of active CPU cores can be specified in the CPU configuration menu. More details about this feature are provided in *Aptio Skylake Core BIOS Manual*.

3.3.2 Turbo Boost Configuration

By default, Turbo Mode is enabled in the BIOS setup screen. Turbo Mode allows the CPU to go beyond the rated nominal clock frequency when there is headroom from the maximum Thermal Design Power of the CPU. This results in the highest available performance, but with a larger, more dynamic power draw during peak operations. More details about this feature are provided in *Aptio Skylake Core BIOS Manual*.

3.4 Platform Controller Hub (PCH)

The Intel C230 Series CM236 PCH provides extensive I/O support, as listed below:

- **PCIe Gen3 x4 (4)** – There are three PCIe Gen3 ports of x4 width. The first is connected to the Intel I350 Quad Gigabit Ethernet Controller. The second is connected to the PEX8714 PCIe switch. The third is connected to an expansion plane fat pipe on the VPX backplane allowing for direct board-to-board communication with an adjacent slot. The fourth is connected to the M.2 expansion slot.
- **SATA Gen3 (7)** – There are seven SATA III ports on the VPX6600. All the ports are configurable as SATA ports or PCIe lanes. Two are connected to the P2 backplane connector. One is connected to the M.2 expansion site. The remaining 4 are connected to the expansion plane fat pipe on the VPX backplane.
- **USB 3.0 (4)** – There are four USB 3.0 ports on the VPX6600. Two ports are connected to the P2 backplane connector. The other two are available on front I/O USB connectors (Air-cooled only)
- **USB 2.0 (2)** – There are two additional ports that function at USB 2.0 or USB 1.1 speeds that are connected to the P2 backplane connector.
- **GPIO (6) –** There are six 3.3V general purpose inputs/outputs available on the P2 backplane connector. These have software-configurable direction control.
- **LPC** – The Low Pin Count bus is connected to the NCT6106 Super I/O for serial ports and debug port 80 connections, in addition to the AT97SC3204 TPM device.
- **Line-Level Audio In/Out** – Stereo audio input and output from onboard HDA audio codec are available on the P2 backplane connector.

- **SMBUS** – This I2C-compatible System Management Bus has connections to the memory DIMMs, the VPX backplane, the Ethernet controller, and an on-board EEPROM that can be used for module identification.

3.5 System Memory

The VPX6600 CPU module has two 260-pin, right-angle SODIMM sockets to accept DDR4 ECC SDRAM modules. At least one SDRAM module is required to make the system operational.

Note: ECC (x72) SODIMM modules are required. Non-ECC SODIMM modules (x64) are not supported.

Support for the following features is provided by the system memory interface:

- DDR4 SDRAM with transfer rates of 2133 MT/s
- Up to 16GB capacity DIMMs using 4Gb or 8Gb DDR4 SDRAM densities
- 72-bit wide channels (64-bits plus 8 bits of ECC)

3.6 Video

Up to 4 displays are supported, but only three can be active at the same time. Each display type supports the following maximum resolution:

DP:	4096x2304 @ 60Hz
HDMI:	4096x2160 @ 24Hz
DVI:	1920x1200 @ 60Hz

3.6.1 Digital Display Interfaces

The Intel® Gen6 (Skylake) CPU used on the VPX6600 CPU module integrates three digital display ports (B, C, and D) that support DisplayPort, HDMI, or DVI interfaces.

DisplayPort can be configured to use 1, 2, or 4 lanes depending on the bandwidth requirements and the link data rate of the RBR (1.62 GT/s), HBR (2.7 GT/s), and HBR2 (5.4 GT/s).

All three ports support DP++, which transmits DVI/HDMI signals as well as DisplayPort. A simple passive adapter can be used to connect DVI/HDMI display devices to any of these ports. The BIOS will detect and automatically configure any of these attached devices.

When configured as HDMI, the DDIx4 port can support 2.97 GT/s link rate.

The processor supports High-bandwidth Digital Content Protection (HDCP) for high-definition content playback over digital interfaces.

The processor also integrates a dedicated Mini HD audio controller to drive audio on integrated digital display interfaces, such as HDMI and DisplayPort. The HD audio controller on the PCH would continue to support down CODECs, and so on. The processor Mini HD audio controller supports two High-Definition Audio streams simultaneously on any of the three digital ports.

The processor supports streaming any 3 independent and simultaneous display combination of DisplayPort/HDMI/DVI. In the case of three simultaneous displays, two High Definition Audio streams over the digital display interfaces are supported.

3.6.1.1 DisplayPort

DisplayPort is a digital communication interface that uses differential signaling to achieve a high-bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays.

A DisplayPort consists of a Main Link, Auxiliary channel, and a Hot-Plug Detect signal. The Main Link is a unidirectional, high-bandwidth, and low-latency channel used for transport of isochronous data streams such as uncompressed video and audio. The Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot-Plug Detect (HPD) signal serves as an interrupt request for the sink device.

The Intel 6th Gen Skylake Core CPU is designed in accordance to VESA DisplayPort Standard 1.2, VESA DisplayPort PHY Compliance Test Specification 1.2, and VESA DisplayPort Link Layer Compliance Test Specification 1.2.

3.6.1.2 HDMI

The High-Definition Multimedia Interface (HDMI) is provided for transmitting uncompressed digital audio and video signals from DVD players, set-top boxes, and other audio-visual sources to television sets, projectors, and other video displays. It can carry high-quality multi-channel audio data and all standard and high-definition consumer electronics video formats. The HDMI display interface connecting the processor and display devices uses transition minimized differential signaling (TMDS) to carry audio-visual information through the same HDMI cable.

HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control). CEC is not supported on the processor. The HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the Sink.

Audio, video, and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the PCH are AC coupled and need level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

The Intel 6th Gen Skylake Core CPU is designed in accordance with the High-Definition Multimedia Interface Specification Version 1.4.

3.6.1.3 Integrated Audio

- HDMI and DisplayPort interfaces carry audio along with video.
- The processor supports three High Definition audio streams on three digital ports simultaneously.
- The integrated audio processing (DSP) is performed by the PCH and delivered to the processor.
- The processor supports only the internal HDMI and DP CODECs.

The processor will continue to support Silent stream. Silent stream is an integrated audio feature that enables short audio streams, such as system events to be heard over the HDMI and DisplayPort monitors. The processor supports silent streams over the HDMI and DisplayPort interfaces at 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sampling rates.

3.6.2 Configuring the Primary Display

To select a specific primary display, refer to *Aptio Skylake Core BIOS Manual.*

3.6.3 Configuring the Video Memory

To configure the video memory, refer to *Aptio Skylake Core BIOS Manual.*

3.6.4 Video Display Options

The VPX6600 supports three simultaneous, independent displays.

Display mode choices when using multiple monitors include:

- Single display, in which one port is activated to display the output on one device.
- Clone mode, in which the same content, resolution, and color depth are sent to up to three display devices. Different refresh rates may be used on each display.
- Extended desktop, in which a larger Windows desktop spans up to three display devices. The displays can support different refresh rates, resolutions, and color depth.

3.6.5 Multi-Stream Transport

The VPX6600 module supports Multi-Stream Transport (MST), enabling multiple monitors to be used via a single DisplayPort connector. The max MST DP supported resolution is:

One panel display:	4096x2304 @ 60Hz
Two panel displays concurrently:	2880x1800 @ 60Hz
Three panel displays concurrently:	2304x1440 @ 60Hz

3.7 Intel® High Definition Audio

The VPX6600 uses Intel High Definition Audio through an ALC892 Audio CODEC to provide both a stereo line-level audio input and a stereo line-level audio output.

The module can also generate a separate PC speaker signal, although most CODECs intercept this signal and pipe it out through the speakers attached to the CODEC. Enabling and configuring the HDA is discussed in *Aptio Skylake Core BIOS Manual.*

3.8 Storage I/O

3.8.1 SATA

SATA (Serial Advance Technology Attachment) is the interface that connects the PCH to the supported mass storage devices (see below). Independent operation is achieved for up to 8 SATA 3.0 ports with an integrated SATA host controller on the PCH. Note that the PCH SATA controller no longer supports IDE legacy mode. Therefore, AHCI software is required.

The SATA features support:

- The SATA hard disk drives, solid state drives (SSD), and CD-ROM/DVD-ROM drives
- AHCI and RAID (0, 1, 5, and 10) modes
- Data transfer rates of up to 6.0Gbps

To configure SATA operation, refer to *Aptio Skylake Core BIOS Manual.*

3.8.2 PCIe

In addition to SATA, two of the PCIe x4 ports can use the NVMe protocol to connect to Intel PCIe Storage Devices with transfer rates of up to 32Gbps. These ports are:

- M.2 On-board Storage Expansion Site
- Expansion Plane interface on the VPX backplane allowing for direct board-to-board communication with an adjacent slot.

3.9 Flexible I/O

There are 7 lanes on the VPX6600 that can be configured as either PCIe lanes or as SATA ports. The two ports on the P2 VPX backplane connector are hard-wired to be SATA ports. The lanes going to the M.2 connector are configured by the storage module that is installed. The remaining four lanes are connected to the Expansion Plane on the VPX backplane and can be configured to be PCIe or SATA using the on-board DIP switch SW1.

3.10 General I/O

3.10.1 General Purpose I/O (GPIO)

The VPX6600 supports 6 GPIO pins which are directly connected to the PCH's GPIO pins. The direction is software configurable. The GPIO pins are available on the P2 VPX backplane connector. The GPIO pins are 3.3V level signals.

3.10.2 SMBus

The SMBus is connected directly to the PCH, as well as to other devices on the module. The SMBus is also connected to the VPX backplane as specified in VITA 46.0 VPX Base Specification.

Refer below to Table 3.10.2.a, SMBus/I2C Address Table, below for additional information.

Table 3.10.2.a: SMBus/I2C Address Table

SMBus ADDR	Function
0x32	DIMMA TEMP
0x34	DIMMA TEMP
0x5A	NCT6016 Super-I/O
0xA0	Acro-Express ID EEPROM
0xA2	DIMMA SPD
0xA4	DIMMB SPD
0x49	I350 Ethernet Controller
0x4*	PCA9500 I/O Expander
0xA*	PCA9500 EEPROM
0x9*	TMP75 Temp Sensor

Note: Slave addresses of FRU devices (PCA9500, TMP75) are slot dependent based on VPX Geographical Addressing Bits per VITA 46.

3.10.3 Low Pin Count (LPC)

The LPC interface contains the onboard NTC6106 Super I/O device, which supplies the two serial ports and also outputs the Port80 Power On Self Test (POST) codes to the dual 7-segment display.

The onboard Atmel AT97SC3204 TPM device fully integrated security module, implements version 1.2 of the Trusted Computing Group (TCG) specification for Trusted Platform Modules (TPM).

For further information regarding the system BIOS and LPC interfaces, refer to *Aptio Skylake Core BIOS Manual.*

3.10.4 Serial Ports

Two 16550-compatible serial ports are supplied by the NCT6106 Super I/O device. Both ports are software selectable between RS-232/RS-422/RS-485 and are available on the P2 VPX backplane connector.

For further information regarding BIOS serial port configuration, refer to *Aptio Skylake Core BIOS Manual.*

3.10.5 USB

The Intel® CM236 PCH has one eXensible Host Controller Interface (xHCI) controller to support the four USB 3.0 ports and the two USB 2.0 ports.

USB 3.0 ports support up to 5Gbps and USB 2.0 supports up to 480Mbps.

Note that EHCI mode is no longer supported, which may affect the installation of some operating systems.

These USB features support:

- USB hard disk drives, flash drives, floppy disk drives, and CD-ROM/DVD-ROM drives
- Super-speed, high-speed, full-speed, and low-speed USB
- USB debug capability on any USB 3.0-capable port

Two of the USB 3.0 ports are available via the front panel of the VPX6600 for air-cooled models only. The remaining 2 USB 3.0 ports and the two USB 2.0 ports are routed to the P2 VPX backplane connector.

For information on configuring specific USB ports see *Aptio Skylake Core BIOS Manual.*

3.11 Gigabit Ethernet

The VPX6600 uses the Intel i350 Quad Gigabit Ethernet Controller, which contains both the media access control (MAC) and the physical layer (PHY) for each port.

The VPX6600 provides three Gigabit Ethernet ports configured as follows:

- Two 1000BASE-BX ports connected to the P1 VPX backplane connector to be used on the board-to-board Control Plane interface as specified in VITA 65 OpenVPX specification.
- One 1000BASE-T fully-integrated port available on the P2 VPX backplane connector to be used as a standard Ethernet connection.

3.11.1 Configuring PXE Boot

For information regarding how to boot from the network, refer to *Aptio Skylake Core BIOS Manual.*

3.12 Real Time Clock (RTC)

A Motorola® MS146818B-compatible real-time clock (RTC) is included in the Intel® CM236 PCH. The RTC has 256 bytes of battery-backed RAM and runs on a 32.768 KHz crystal with a 3V battery. The RTC performs two key functions:

- It keeps track of the time of day, and
- It stores system data, even after powering down the system.

Note: After the RTC battery is removed from the board with it otherwise unpowered, the last BIOS settings will be retained for approximately 80 minutes by an onboard supercap. After that, the settings will be lost unless the module is reconnected to the RTC battery or connected to VCC_3.3VSBY.

Note: If the supercap has drained and the RTC voltage drops below 2.5V, or when a BIOS update has been done, the first time the system is powered on it may partially boot and then restart up to two times. This behavior is normal.

3.13 Security

3.13.1 Trusted Platform Support

The VPX6600 uses the Atmel AT97SC3204 fully integrated security module, which implements version 1.2 of the Trusted Computing Group (TCG) specification for Trusted Platform Modules (TPM). The TPM includes a cryptographic accelerator capable of computing a 2048-bit RSA signature in 200ms and a 1024-bit RSA signature in 40ms. Performance of the SHA-1 accelerator is 20µs per 64-byte block.

3.13.2 Password Control

You are able to specify:

- An Administrator password with full control, and
- A User password with limited access to the BIOS settings.

For further information on setting the password, refer to *Aptio Skylake Core BIOS Manual.*

3.14 System Management

3.14.1 Intel® Hyper-Threading Technology

(Note: The following information is from Intel® "6th Generation Intel® Processor Datasheet for H-Platforms– Volume 1 of 2", December 2015.)

The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology) that allows an execution core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support.

The Intel® HT Technology is enabled by default; no action by the operator is required.

For further information on disabling support for this technology, refer to *Aptio Skylake Core BIOS Manual.*

3.14.2 Enhanced Intel® SpeedStep Technology (EIST)

The Enhanced Intel® SpeedStep Technology (EIST) used by this processor enables very high performance while also meeting power-conservation needs. When EIST is enabled, the clock frequency of the CPU is dynamically changed in response to the CPU load.

The Intel® SpeedStep feature is enabled by default. For further information on disabling support for this technology, refer to *Aptio Skylake Core BIOS Manual.*

3.14.3 Intel® Virtualization Technology (Intel VT-x and VT-d)

Intel® Virtualization Technology (Intel VT) makes a single system appear as multiple independent systems to software. This allows for multiple, independent operating systems to be running simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. The first revision of this technology (Intel VT-x) added hardware support in the processor to improve the virtualization performance and robustness. The second revision of this specification (Intel VT-d) adds chipset hardware implementation to improve I/O performance and robustness.

The Intel® VT-x and VT-d features are enabled by default. For further information on disabling support for this technology, refer to *Aptio Skylake Core BIOS Manual.*

3.14.4 Intel® Trusted Execution Technology (TXT)

The featured Intel® Trusted Execution Technology attests to the authenticity of a platform and its operating system and assures that an authentic OS starts in a trusted environment and can be considered a trusted OS.

Intel® TXT works in conjunction with the TPM so that the system software may make trust decisions.

The Intel TXT feature is enabled by default. For further information on disabling support for this technology, refer to *Aptio Skylake Core BIOS Manual.*

3.14.5 Intel® Turbo Boost Technology

The number of active cores determines the maximum processor core operating frequency. See Section 3.3.1, "Active Processor Core Selection" for information and instructions.

(Note: The following information is from Intel® "6th Generation Intel® Processor Datasheet for H-Platforms– Volume 1 of 2", December 2015.)

The Intel® Turbo Boost Technology allows the processor core to opportunistically and automatically run faster than its rated operating frequency/render clock if it is operating below power, temperature, and current limits. The Intel Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads.

The processor supports a Turbo mode in which the processor can use the thermal capacity associated with the package and run at power levels higher than TDP power for short durations. This improves the system responsiveness for short, surging usage conditions. The turbo feature needs to be properly enabled by BIOS for the processor to operate with maximum performance. Since the turbo feature is configurable and dependent on many platform design limits outside of the processor control, the maximum performance cannot be ensured.

Turbo Mode availability is independent of the number of active cores; however, the Turbo Mode frequency is dynamic and dependent on the instantaneous application power load, the number of active cores, user configurable settings, operating environment, and system design.

Compared with previous generation products, Intel Turbo Boost Technology will increase the ratio of application power to TDP. Thus, thermal solutions and platform cooling that are designed to less than thermal design guidance might experience thermal and performance issues since more applications will tend to run at the maximum power limit for significant periods of time.

Refer to *Aptio Skylake Core BIOS Manual* and the appropriate processor Turbo Implementation Guide for more information.

3.14.6 Intel® Active Management Technology

Intel® Active Management Technology (Intel® AMT) is a set of advanced manageability features developed to extend the manageability capability for IT through Out Of Band (OOB). This allows asset information, remote diagnostics, recovery, and contain capabilities to be available on client systems even when they are in a low power, or "off" state, or in situations when the operating system is hung.

For further information on configuring this technology, refer to *Aptio Skylake Core BIOS Manual.*

3.14.7 Intel® Matrix Storage Technology

Intel® Matrix Storage Technology is supported by Intel's CM236 PCH, which provides:

- AHCI functionality,
- RAID 0/1/5/10 Support, and
- Intel® Rapid Storage Technology.

3.14.8 Intel® Configurable TDP Technology

Intel® Configurable TDP Technology (cTDP) allows users to reconfigure the 45W thermal design power (TDP) level of the E3-1505M CPU down to 35W in systems where a lower amount of power is available or a smaller thermal solution is required.

For further information on configuring the TDP levels, refer to Aptio Skylake Core BIOS Manual.

3.15 Thermal Management

The Intel® Skylake processor contains a digital thermal sensor for each execution core and a thermal monitor to measure the processor's temperature. A thermal sensor connected to the NCT6106 Super-I/O is used to measure the module's temperature.

The integrated graphics and memory controller (GMC) monitors its temperature and initiates thermal management with an internal digital thermal sensor. Memory loading or high GMC temperatures will result in bandwidth throttling. THERMTRIP# and Render Thermal Throttling are also supported by the internal digital thermal sensor.

The temperature of the Intel® CM236 PCH is monitored by two thermal sensors located on the PCH. The system will be shut down by the PCH when its thermal limit is reached.

3.15.1 Thermal Monitoring

The system setup utility displays the processor and board temperatures. For further information on how to check these temperatures, refer to *Aptio Skylake Core BIOS Manual.*

3.15.2 Thermal Throttling

3.15.2.1 CPU Throttling (Hardware Controlled)

The processor must not exceed the 100°C maximum junction temperature (Tj).

When the integrated thermal monitor on the processor determines that the maximum processor temperature has been reached, the CPU clock speed will be throttled back in 100MHz increments to keep Tj from exceeding the maximum junction temperature of 100° C.

If throttling is not enough to keep the processor's Tj below the catastrophic temperature limit of 105° C:

- The THERMTRIP# signal will be sent, and
- The voltage supply to the processor will be turned off within 500ms to prevent permanent silicon damage.

3.15.2.2 Thermal Management (OSPM Controlled)

The active and passive trip points are configured using the system Bios. For information on how to configure these trip points, refer to *Aptio Skylake Core BIOS Manual.*

3.15.3 Memory Throttling

The memory bandwidth can be throttled back automatically if a thermal sensor is on the DIMM. The NCT6106 will alert the memory controller via PECI when the system memory exceeds its normal operating temperature.

For further information on configuring the memory bandwidth throttling based on temperature readings from the DIMM's thermal sensor, refer to *Aptio Skylake Core BIOS Manual*.

3.16 Watchdog

The VPX6600 features a software-triggered multi-stage watchdog solution. When the watchdog timer expires the WDT# output on the VPX connector can be configured to go low and/or the module can cause a system reset.

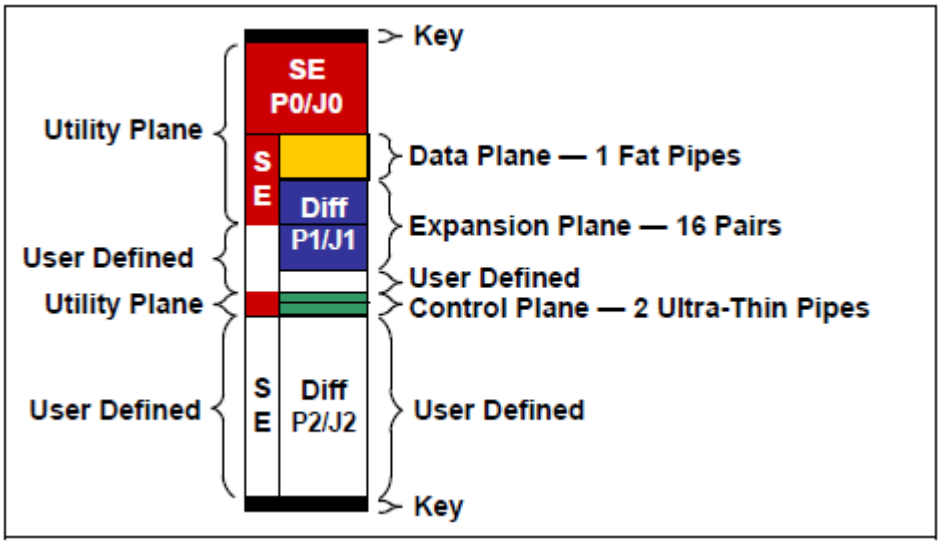
For further information on the Watchdog feature, refer to *Aptio Skylake Core BIOS Manual.*

3.17 VPX Profile

The VPX6600 is designed to be used in OpenVPX module profile MOD3-PAY-1F2F2U-16.2.2-4. This module profile complies with OpenVPX slot profile SLT3-PAY-1F2F2U-14.2.2 shown in Figure 3.17.a below.

This module profile defines one PCIe Gen 2 fat pipe connection to be used as a Data Plane, two PCIe Gen 2 fat pipes to be used as Expansion Planes, and two 1000BASE-BX Gigabit Ethernet connections to be used as Control Planes.

Fig. 3.17.a OpenVPX Slot Profile SLT3-PAY-1F2F2U-14.2.2



3.17.1 Data Plane

The VPX6600 uses the Avago PEX8714 PCIe switch for its Data Plane connection. The PCIe switch supports non-transparent bridging which allows the VPX6600 to be used in multi-processor VPX systems that do not contain a dedicated switch card.

3.17.2 Expansion Plane

The VPX6600 provides two PCIe fat pipe interfaces to be used as Expansion Plane connections to adjacent slots in the system. The first Expansion Plane connection uses PCIe lanes from the PEG interface on the CPU. The PEG interface is traditionally used for external graphics but supports any PCIe device.

The second Expansion Plane connection uses Flexible I/O from the PCH. The interface can be configured to be a x4 PCIe connection or four individual SATA III ports using switch SW1-2.

3.17.3 Control Plane

The VPX6600 uses the Intel i350 Quad Gigabit Ethernet Controller for the Control Plane interface. The i350 is configured to generate two 1000BASE-BX Gigabit Ethernet ports for the Control Plane and one 1000BASE-T port for external Internet connections.

4.0 BIOS INFORMATION AND CONFIGURATION

4.1 VPX6600 Special BIOS Features

This section contains information on configuring features specific to the VPX6600. For other, more generic BIOS setup information, refer to *Aptio Skylake Core BIOS Manual.*

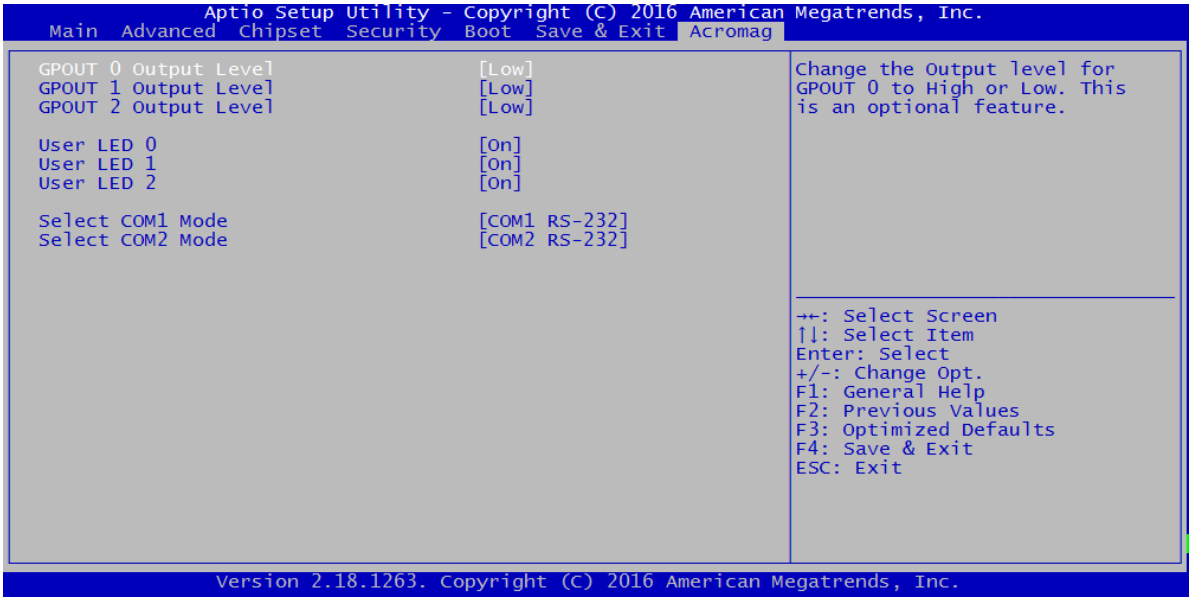


Fig. 4.1.a Acromag BIOS Setup Menu

The following hardware configuration options are available in the Acromag menu of the BIOS setup Utility:

- **GPOUT x Output Level -** Sets the corresponding General Purpose Output level to Low or High. The default is Low.
- **User LED x Output Level -** Sets the corresponding User LED output level to Low or High. The LED is on when the level is set to High. The default is High.
- **Select COMx Mode -** Sets the corresponding COM port protocol to RS-232 or RS-422/485. The default is RS-232.

4.2 Drivers and Utilities

Drivers and Utilities for the VPX6600 can be downloaded from Acromag's website at https://www.acromag.com/.

5.0 SERVICE AND REPAIR

5.1 Service and Repair Assistance

Single Board Computer (SBC) products like the VPX6600 Acro-Express module are generally difficult to repair. The module can be easily damaged unless special SBC repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. For these and other reasons, it is strongly recommended that a non-functioning SBC be returned to Acromag for repair.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts or return parts for repair.

5.2 Preliminary Service Procedure

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Before beginning repair, be sure that all of the procedures in the "Preparation for Use" section have been followed. Also, refer to the documentation for the module to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

5.3 Where to Get Help

If the problem persists, the next step should be to visit the Acromag worldwide web site at https://www.acromag.com/. Our web site contains the most up-to-date product and software information.

Go to the "Support" tab to access:

- Application Notes
- Frequently Asked Questions (FAQ's)
- Product Knowledge Base
- Tutorials
- Software Updates/Drivers

Acromag's application engineers can also be contacted directly for technical assistance via email, telephone, or FAX through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab. When needed, complete repair services are also available.

- Email: solutions@acromag.com
- Phone: 248-295-0310
- Fax: 248-624-9234

6.0 SPECIFICATIONS

6.1 Physical

The VPX6600 is a 3U VPX module that conforms to the 1" backplane spacing set forth by the VITA 48 specification (both air and conduction models).

Depth	95.0 mm (3.740 in)
Width	125.0 mm (4.921 in)
PCB Thickness	1.68 mm (0.066 in)
Unit Weight (Air-Cooled):	18.1 oz (0.514 kg)
Unit Weight (Conduction-Cooled):	17.6 oz (0.498 kg)
Unit Weight (RTM):	5.0 oz (0.143 kg)

6.2 Connector Information

6.2.1 VPX Backplane Connectors

6.2.1.1 P0 VPX Connector

P0 Wafer	A	B	C	D	E	F	G
1	+3.3 V	+3.3 V	+3.3 V	N/C	N/C	N/C	N/C
2	+3.3 V	+3.3 V	+3.3 V	N/C	N/C	N/C	N/C
3	+5 V	+5 V	+5 V	N/C	+5 V	+5 V	+5 V
4	NVRAM_LOCK	PLT_RST#	GND	N/C	GND	N/C	N/C
5	SMB_DATA	SMB_CLK	GND	+3.3V AUX	GND	N/C	N/C
6	GA0#	GA1#	GND	N/C	GND	GA2#	N/C
7	N/C	N/C	GND	N/C	N/C	GND	N/C
8	GND	AUX_CLK_P	AUX_CLK_N	GND	REF_CLK P	REF_CLK N	GND

6.2.1.2 P1 VPX Connector

P1 Wafer	A	B	C	D	E	F	G
1	PCIE_DP_RX0_P	PCIE_DP_RX0_N	GND	PCIE_DP_TX0_P	PCIE_DP_TX0_N	GND	GDISCRETE1
2	GND	PCIE_DP_RX1_P	PCIE_DP_RX1_N	GND	PCIE_DP_TX1_P	PCIE_DP_TX1_N	GND
3	PCIE_DP_RX2_P	PCIE_DP_RX2_N	GND	PCIE_DP_TX2_P	PCIE_DP_TX2_N	GND	VPX_VBAT
4	GND	PCIE_DP_RX3_P	PCIE_DP_RX3_N	GND	PCIE_DP_TX3_P	PCIE_DP_TX3_N	GND
5	SATA4_PCIE17_RX_P	SATA4_PCIE17_RX_N	GND	SATA4_PCIE17_TX_P	SATA4_PCIE17_TX_N	GND	SYS_CON#
6	GND	SATA5_PCIE18_RX_P	SATA5_PCIE18_RX_N	GND	SATA5_PCIE18_TX_P	SATA5_PCIE18_TX_N	GND
7	SATA6_PCIE19_RX_P	SATA6_PCIE19_RX_N	GND	SATA6_PCIE19_TX_P	SATA6_PCIE19_TX_N	GND	N/C
8	GND	SATA7_PCIE20_RX_P	SATA7_PCIE20_RX_N	GND	SATA7_PCIE20_TX_P	SATA7_PCIE20_TX_N	GND
9	PEG_RX8_P	PEG_RX8_N	GND	PEG_TX8_P	PEG_TX8_N	GND	LAN0_LINK/ACTIVITY
10	GND	PEG_RX9_P	PEG_RX9_N	GND	PEG_TX9_P	PEG_TX9_N	GND
11	PEG_RX10_P	PEG_RX10_N	GND	PEG_TX10_P	PEG_TX10_N	GND	LAN1_LINK/ACTIVITY
12	GND	PEG_RX11_P	PEG_RX11_N	GND	PEG_TX11_P	PEG_TX11_N	GND
13	ENET0_P0_P	ENET_P0_N	GND	ENET0_P1_P	ENET0_P1_N	GND	WDT#
14	GND	ENET0_P2_P	ENET0_P2_N	GND	ENET0_P3_P	ENET0_P3_N	GND
15	GBE_CP2_RX_P	GBE_CP2_RX_N	GND	GBE_CP2_TX_P	GBE_CP2_TX_N	GND	VPX_MASK_RESET#
16	GND	GBE_CP1_RX_P	GBE_CP1_RX_N	GND	GBE_CP1_TX_P	GBE_CP1_TX_N	GND

6.2.1.3 P2 VPX Connector

P2 Wafer	A	B	C	D	E	F	G
1	USB6_P	USB6_N	GND	USB5_P	USB5_N	GND	GPIN0
2	GND	DPC_AUX_SEL	USB_5_6_OC#	GND	DPB_AUX_SEL	USB_1_2_OC#	GND
3	USB1_SSRX_P	USB1_SSRX_N	GND	USB1_P	USB1_N	GND	GPIN1
4	GND	USB2_P	USB2_N	GND	USB1_SSTX_P	USB1_SSTX_N	GND
5	USB2_SSTX_P	USB2_SSTX_N	GND	USB2_SSRX_P	USB2_SSRX_N	GND	GPIN2
6	GND	AGND_AUDIO	LINEOUT_L	GND	AGND_AUDIO	LINEIN_L	GND
7	LINEOUT_R	AGND_AUDIO	GND	LINEIN_R	AGND_AUDIO	GND	GPOUT0
8	GND	SATA2_RX_P	SATA2_RX_N	GND	SATA2_TX_P	SATA2_TX_N	GND
9	SATA3_RX_P	SATA3_RX_N	GND	SATA3_TX_P	SATA3_TX_N	GND	GPOUT1
10	GND	DPB_TX1_P	DPB_TX1_N	GND	DPB_TX0_P	DPB_TX0_N	GND
11	DPB_TX3_P	DPB_TX3_N	GND	DPB_TX2_P	DPB_TX2_N	GND	GPOUT2
12	GND	COM1_RTS#_485_TX-	COM1_TX	GND	DPB_CTRL_AUX_P	DPB_CTRL_AUX_N	GND
13	COM1_CTS#_485_RX-	COM1_RX	GND	COM2_RTS#_485_TX-	COM2_TX	GND	DPB_HPD
14	GND	DPC_TX1_P	DPC_TX1_N	GND	DPC_TX0_P	DPC_TX0_N	GND
15	DPC_TX3_P	DPC_TX3_N	GND	DPC_TX2_P	DPC_TX2_N	GND	DPC_HPD
16	GND	COM2_CTS#_485_RX-	COM2_RX	GND	DPC_CTRL_AUX_P	DPC_CTRL_AUX_N	GND

6.2.2 I/O Connectors

There are two USB 3.0 connectors and one Mini-DisplayPort connector located on the front panel of the VPX6600. Using these connectors, along with an on-board bootable M.2 storage device, the VPX6600 can be operated without the need for a Rear Transition Module.

Note: The front I/O connectors are only available on the air-cooled VPX6600-LF model.

6.2.2.1 J6 USB 3.0 Connector

This standard 9-pin USB3.0 connector (Molex – 48394-003) brings USB Port 3 out to the front panel.

PIN	SIGNAL
1	+5V
2	USB3_N
3	USB3_P
4	GND
5	USB3_SSRX_N
6	USB3_SSRX_P
7	GND
8	USB3_SSTX_N
9	USB3_SSTX_P

6.2.2.2 J7 USB 3.0 Connector

This standard 9-pin USB3.0 connector (Molex – 48394-003) brings USB Port 4 out to the front panel.

PIN	SIGNAL
1	+5V
2	USB4_N
3	USB4_P
4	GND
5	USB4_SSRX_N
6	USB4_SSRX_P
7	GND
8	USB4_SSTX_N
9	USB4_SSTX_P

6.2.2.3 J8 Mini-DisplayPort Connector

This standard 20-pin Mini-DisplayPort connector (TE Connectivity – 2129320) brings DisplayPort D out to the front panel.

PIN	SIGNAL
1	GND
2	DPC_HPD
3	DPC_TX0_P
4	DPC_AUX_SEL
5	DPC_TX0_N
6	GND
7	GND
8	GND
9	DPC_TX1_P
10	DPC_TX3_P
11	DPC_TX1_N
12	DPC_TX3_N
13	GND
14	GND
15	DPC_TX2_P
16	DPC_CTRL_AUX_P
17	DPC_TX2_N
18	DPC_CTRL_AUX_N
19	GND
20	+3.3V

6.3 Power Requirements

The VPX6600 requires +3.3V and +5V from the VPX backplane. The +/- 12V supplies are not used.

Additionally, the switch SW2 can be used to configure certain devices to use the auxiliary +3.3V_AUX supply.

There is an optional 3.0V RTC 'coin cell' battery input voltage that is required to keep the RTC running beyond the 80 minutes supplied by the supercap when 3.3V is not powered. If no coin cell battery is used on the carrier this input should remain unconnected. The allowable range for this input is 2.5 - 3.2V.

The amount of power required to properly operate the VPX6600 module will vary depending on many variables, including the operating system, application software, and the components that the module is integrated with. See notes below for defined variables used to measure the following power values:

5V:

S0 Idle[1]:	10.5W	S0 Max[2]:	55.5/72W
S0 Typ[3]:	52W		

3.3V:

All Modes: 4.3W

[1] S0 Idle was measured with module operating at 23°C ambient with 300LFM airflow, using Windows 8.1 Operating System, idle at desktop with no active applications running. 32GB RAM. One connected SATA device, one USB keyboard, one USB mouse, VGA monitor.

[2] S0 Max was measured with module operating at 23°C ambient with 600LFM airflow, using Windows 8.1 Operating System. Prime95 Large FFT torture test stressing all CPU cores at max. 32GB RAM. 1 connected SATA device, one USB keyboard, one USB mouse, VGA monitor, DVI monitor.

Power is shown as PL1/PL2, where PL1 is the long-term power used, and PL2 is a short-term (typically <30 sec) power draw during turbo bursts. If Turbo is not used the board should not exceed the PL1 power, but performance may be impacted.

[3] S0 Typ was measured with module operating at 23°C ambient with 300LFM airflow, using Windows 8.1 Operating System. Passmark Burn-In test running the following tests: CPU, Memory, 2D Graphics, 3D Graphics, Disk, and Network. 16GB RAM. 1 connected SATA device, one USB keyboard, one USB mouse, VGA monitor, DVI monitor.

6.4 Environmental Considerations

6.4.1 Operating Temperature

0°C to 70°C (Air Cooled models) [1]
-40°C to 85°C (Conduction Cooled models) [2]

[1] Measured as Ambient Air Temperature. 300LFM minimum air-flow required. Designed to meet this temperature specification. Tested under Windows 8.1 with Passmark BurnInTest V7.1, running CPU, Memory, and 3D Graphics tests simultaneously. During application testing

CPU temp should be closely monitored for max junction temp of 100°C using a program such as Argus Monitor or Open Hardware Monitor.

[2] Measured as Ambient Air Temperature inside conduction VPX enclosure. Every board sold tested to ensure this temperature specification. Tested under Windows 8.1 with Passmark BurnInTest V7.1 running CPU, Memory, Disk, and 3D Graphics tests simultaneously. During application testing CPU temp should be closely monitored for max junction temp of 100°C using a program such as Argus Monitor or Open Hardware Monitor.

Note: CPU frequency throttling will occur if the CPU Tj temperature reaches 100°C. This is an effective mechanism to keep the unit from overheating. A small amount of intermittent throttling at high ambient temperatures is to be expected and does not greatly affect system performance. However, an inadequate final thermal solution as the result of inadequate air flow or improper conduction mounting could result in continual CPU throttling which will greatly affect system performance.

6.4.2 Relative Humidity

5% to 95% Non-condensing

6.4.3 Vibration and Shock Standards

Vibration, Sinusoidal Operating: Designed to comply with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis

Vibration, Random Operating: Designed to comply with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis

Shock, Operating: Designed to comply with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3mS half sine, 18 shocks at 6 orientations for both test levels

6.4.4 EMC Directives

The VPX6600 is designed to comply with EMC Directive 2004/108/EC.

- **Immunity per EN 61000-6-2:**
  Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2.
  Radiated Field Immunity (RFI), per IEC 61000-4-3.
  Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4.
  Surge Immunity, per IEC 61000-4-5.
  Conducted RF Immunity (CRFI), per IEC 61000-4-6.
- **Emissions per EN 61000-6-4:**
  Enclosure Port, per CISPR 16.
  Low Voltage AC Mains Port, per CISPR 16.

Note: This is a Class A product

6.5 Reliability Prediction

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled,* G_BG_C

Table 6.5.a MTBF

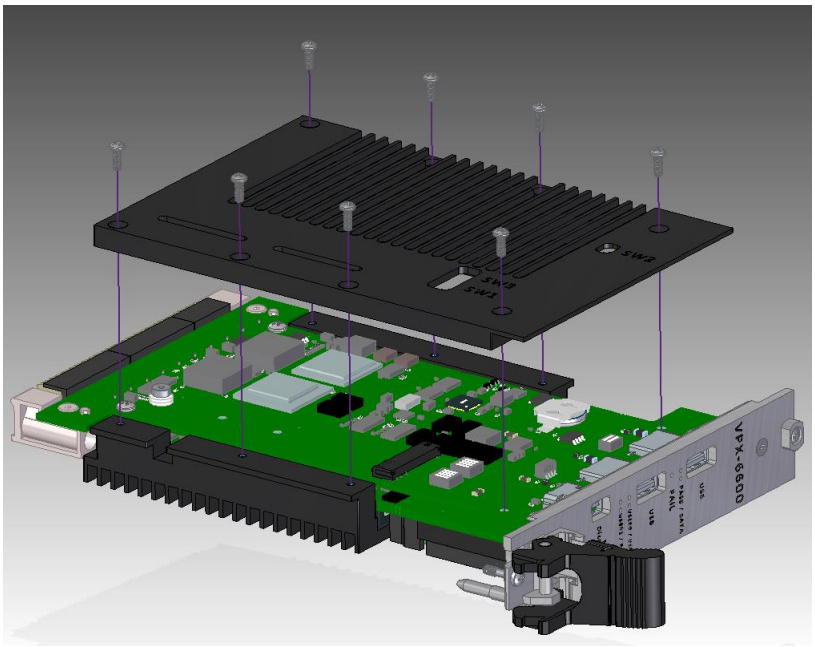
Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	187,627	21.4	5,329.7
40°C	125,853	14.4	7,945.8

[1] FIT is Failures in 10^9 hours.

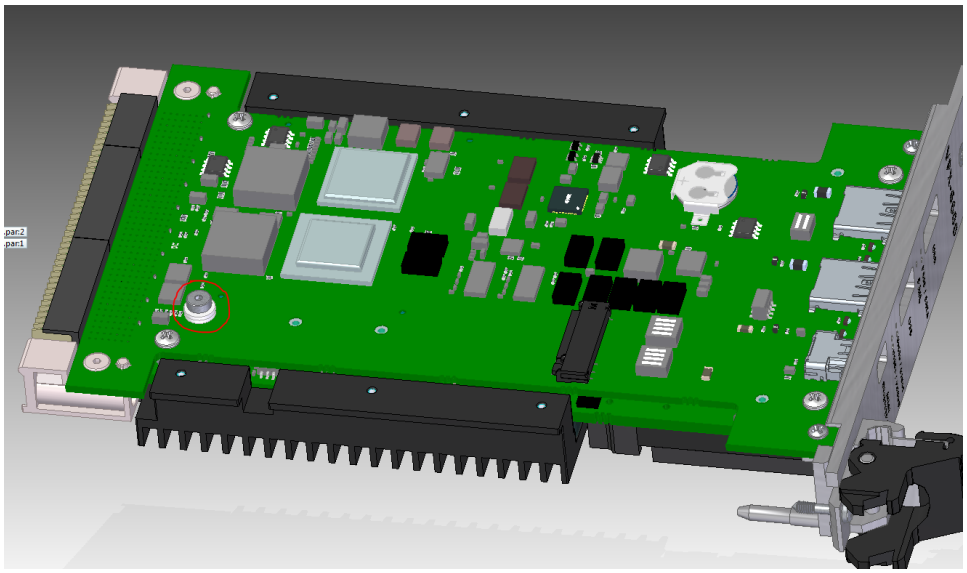
6.6 Installation of M.2 Expansion Card and Battery Replacement

6.6.1 VPX6600-LF (Air-Cooled) M.2 Expansion Card Installation

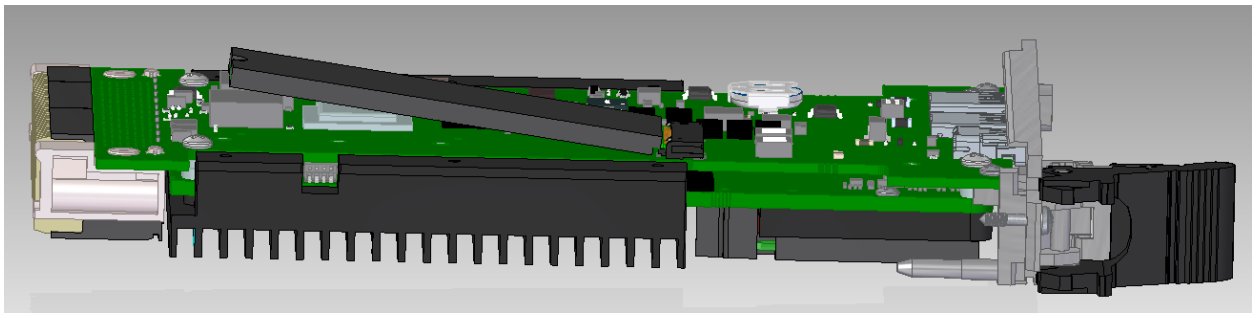
1. Remove the 8 screws (M2 x 6mm) that secure the heatsink to the board. Remove the heatsink.



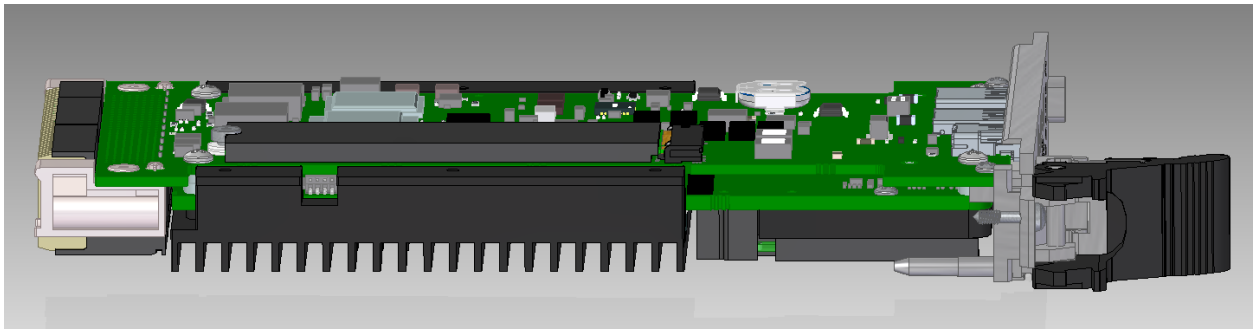
2. Remove the shoulder screw (1.5mm Hex) and washer.



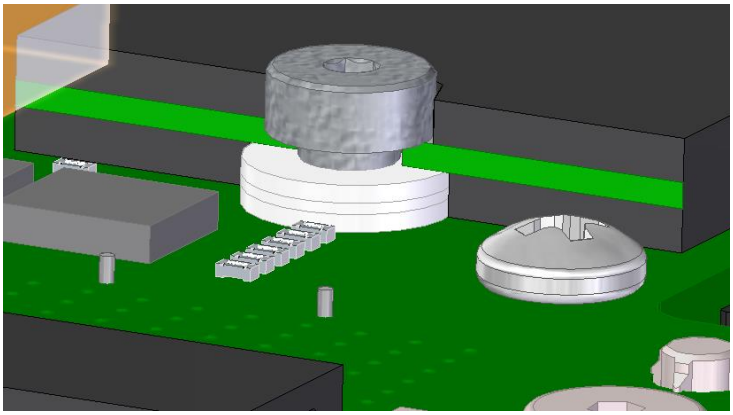
3. Install the M.2 expansion card into socket.



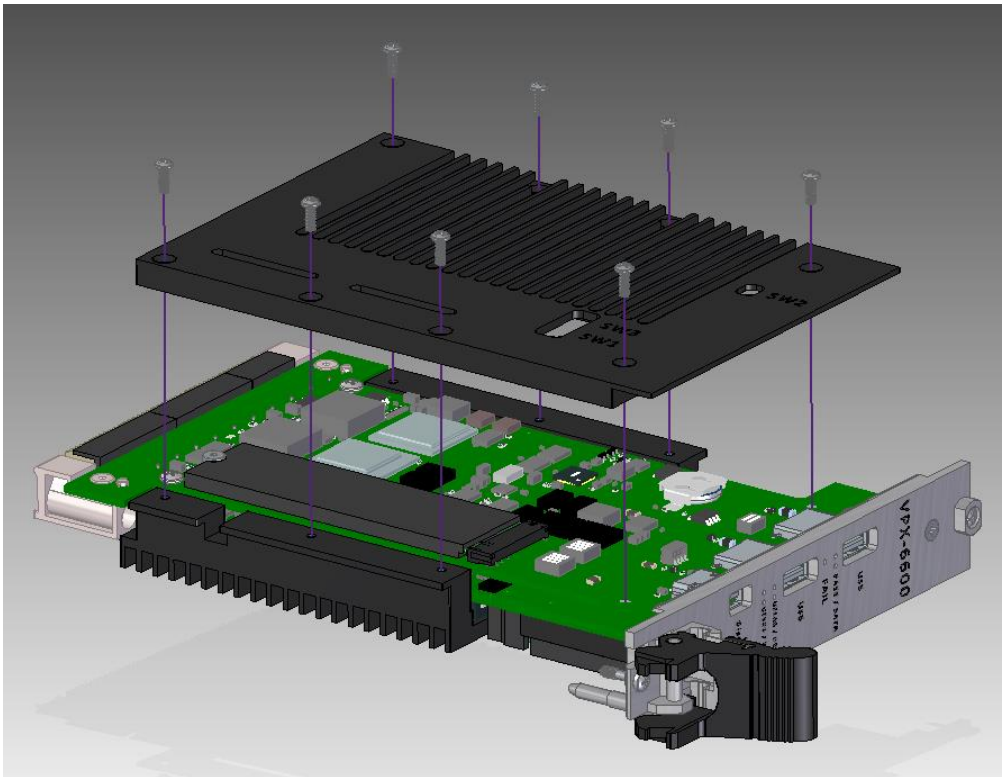
4. Place the washer on the VPX board and carefully press down the M.2 expansion card and secure with shoulder screw.



Note: The washer should be under the M.2 expansion card as shown below.



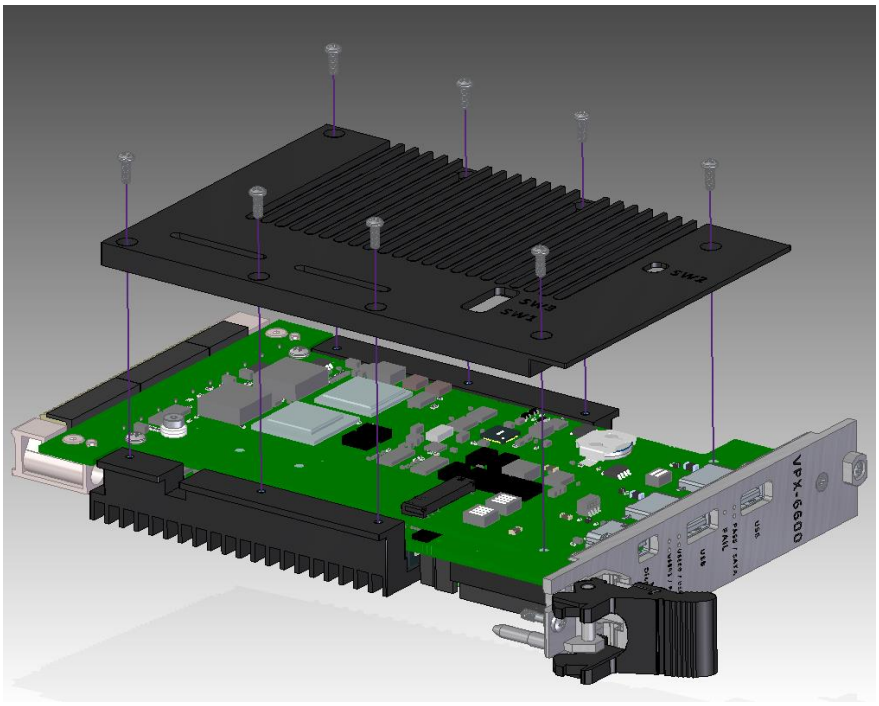
5. Re-install the heatsink and secure with 8 screws (M2 x 6mm)



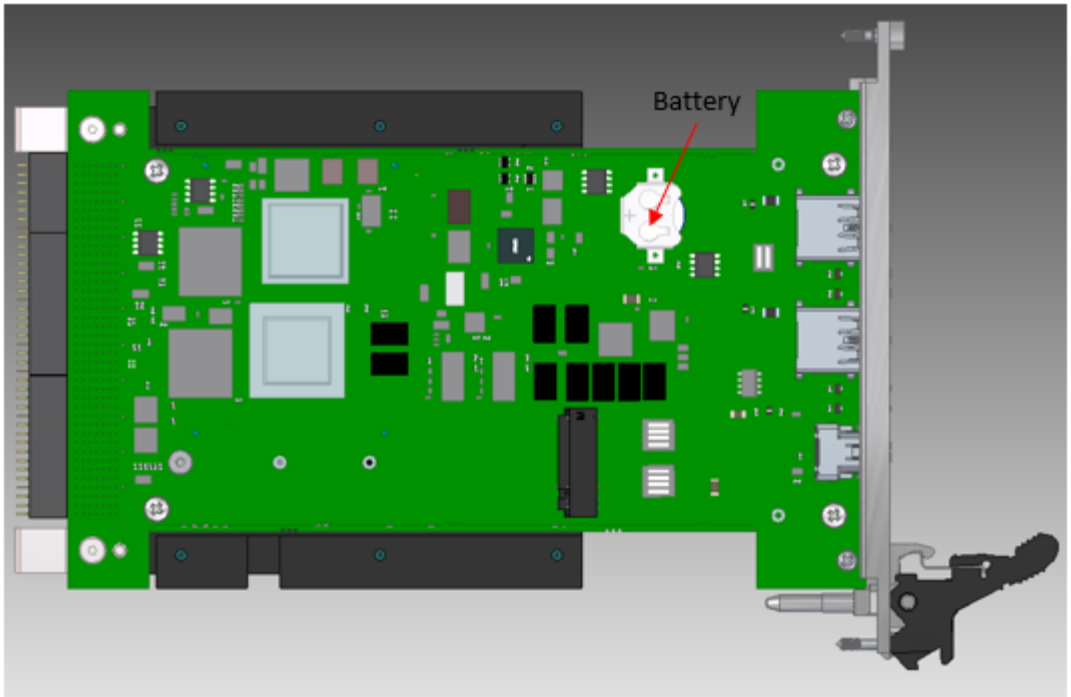
VPX6600-LF (Air-cooled) M.2 expansion card installation complete.

6.6.2 VPX6600-LF (Air-Cooled) Battery Replacement

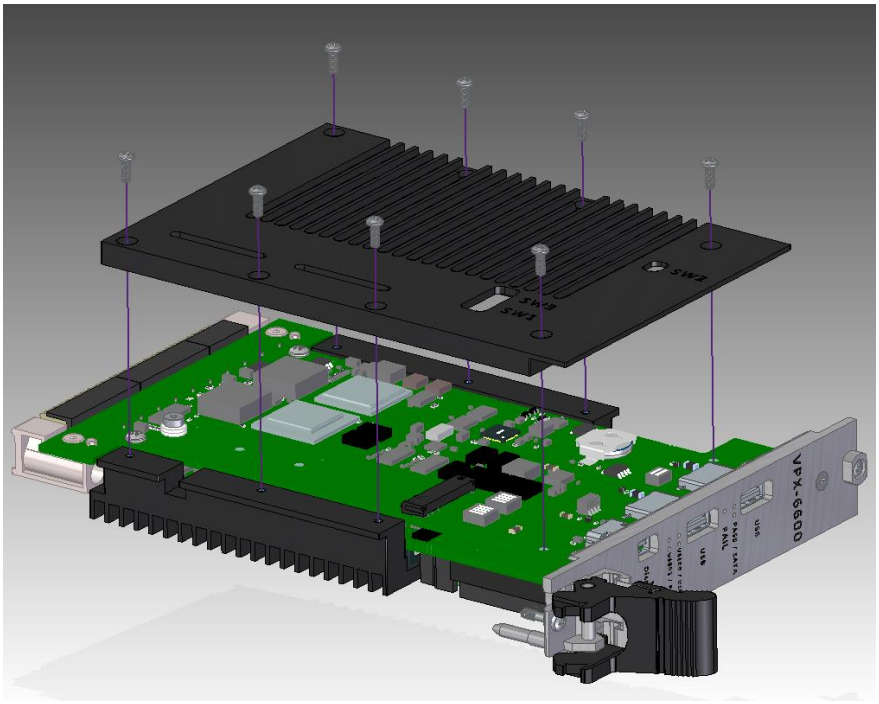
1. Remove the 8 screws (M2 x 6mm) that secure the heatsink to the board. Remove the heatsink.

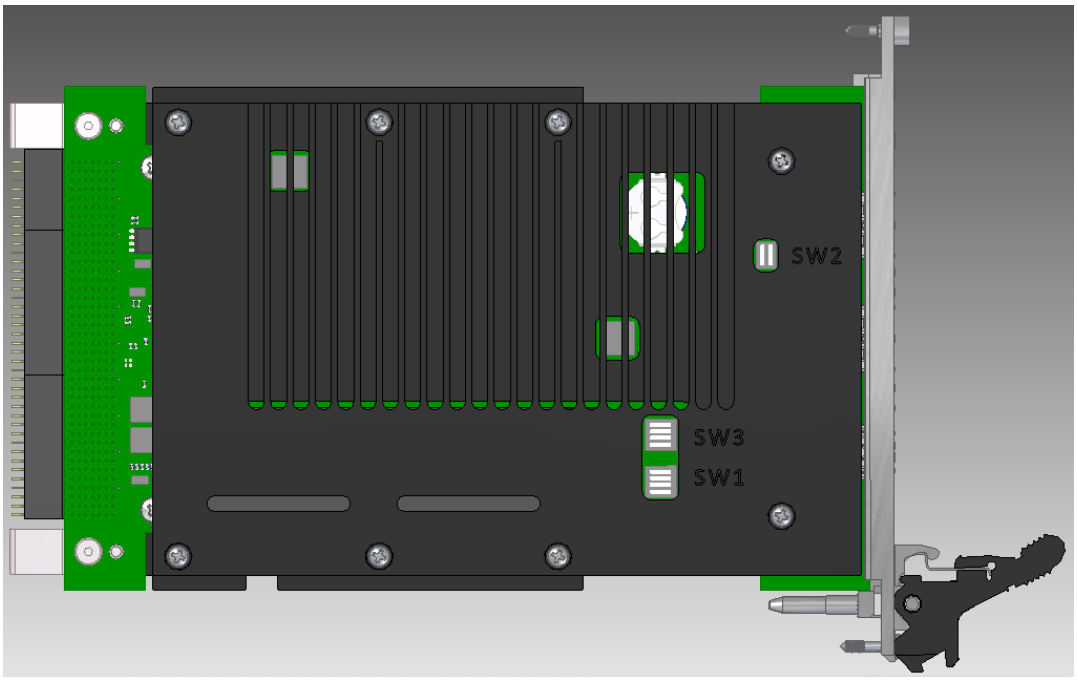


2. Install new battery with "+" face up.



3. Re-install heatsink and secure with 8 screws (M2 x 6mm)

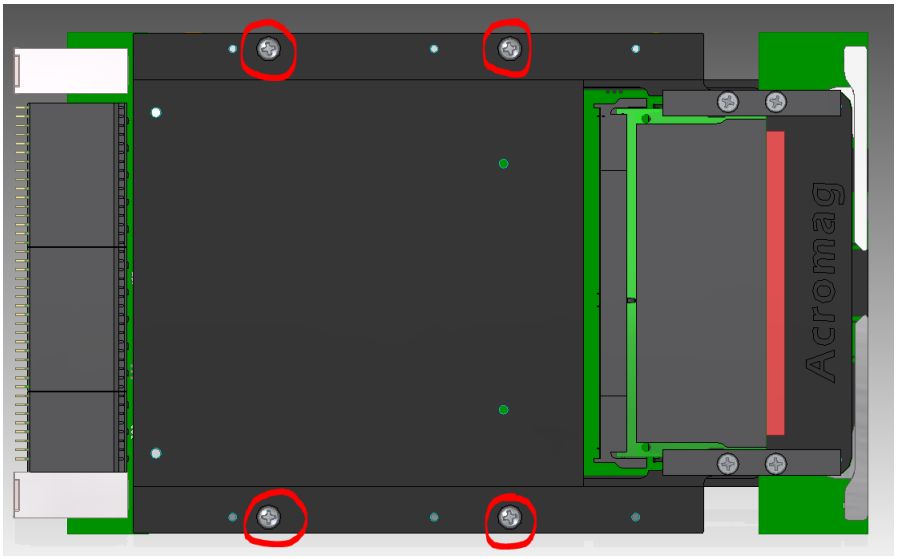


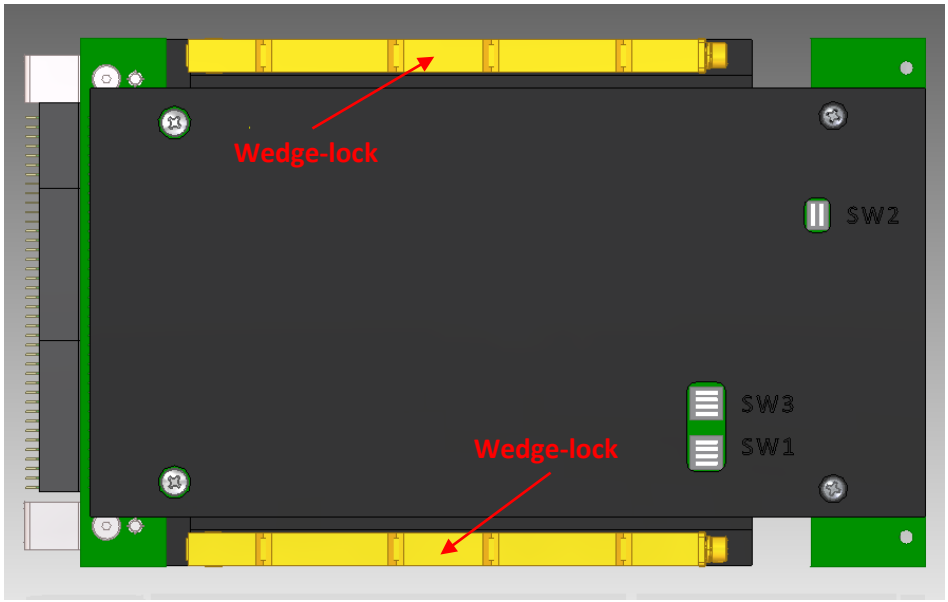


VPX6600-LF (Air-cooled) battery replacement is complete.

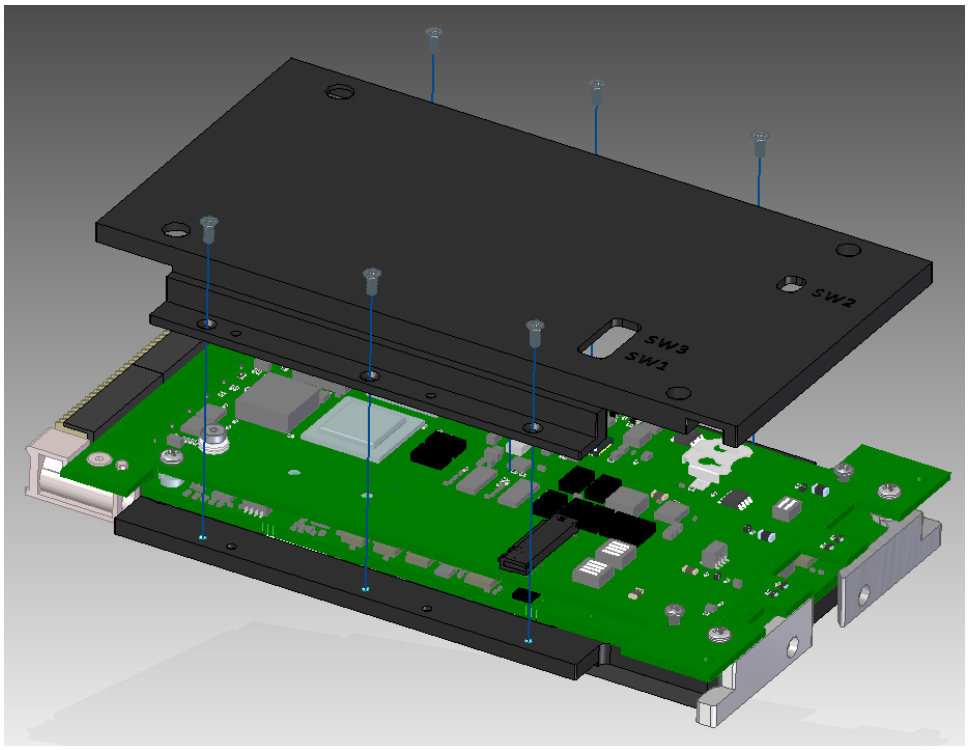
6.6.3 VPX6600-CC-LF (Conduction-Cooled) M.2 Expansion Card Installation

1. Remove the 4 screws (M2 x 6mm) that secure the two wedge-locks to the board. Remove the two wedge-locks.

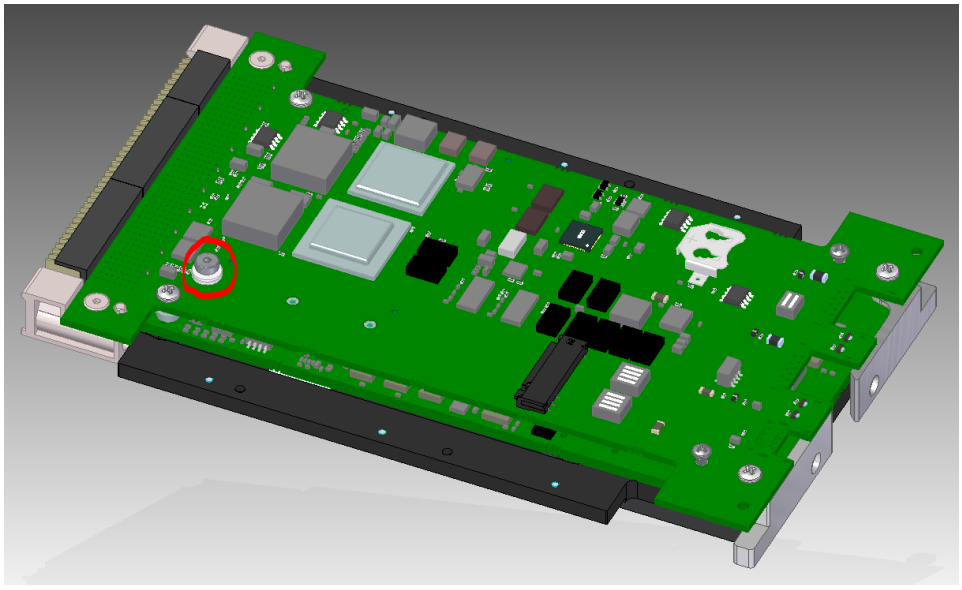




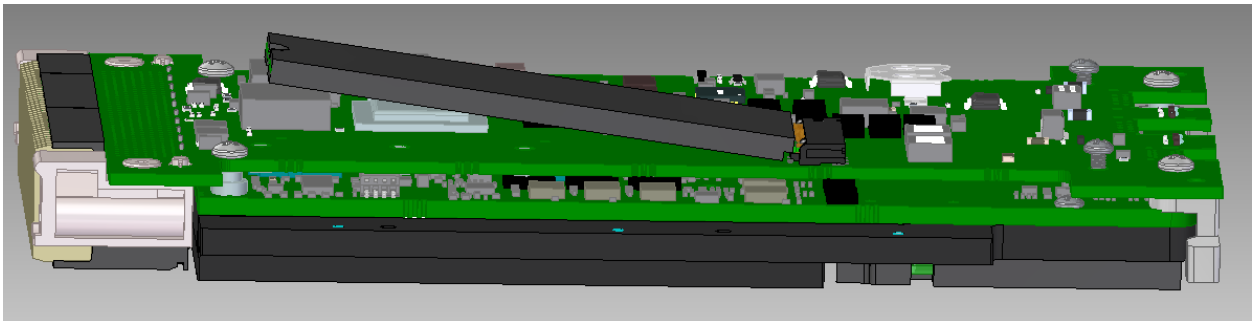
2. Remove the 6 flat-head screws (M2 x 6mm) that secure the heatsink to the board. Remove the heatsink.



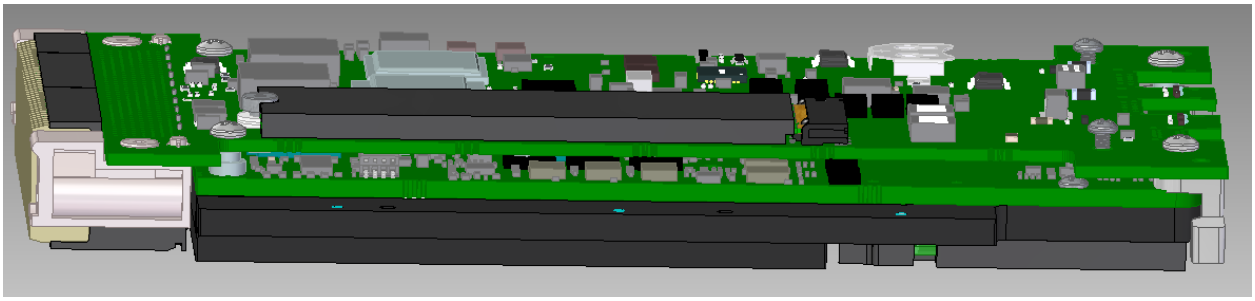
3. Remove the shoulder screw (1.5mm Hex) and washer.



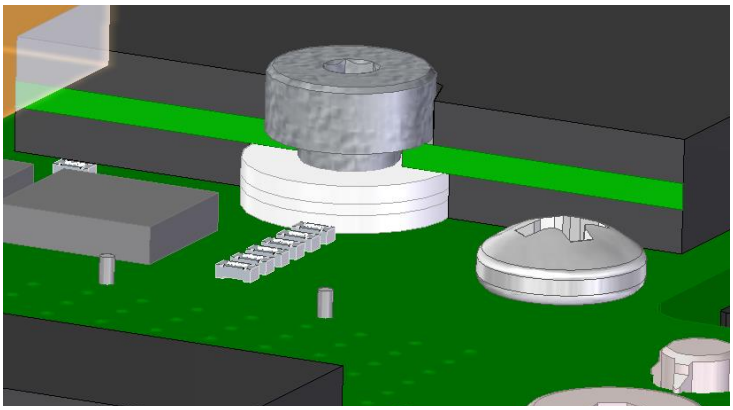
4. Install the M.2 expansion card into socket.



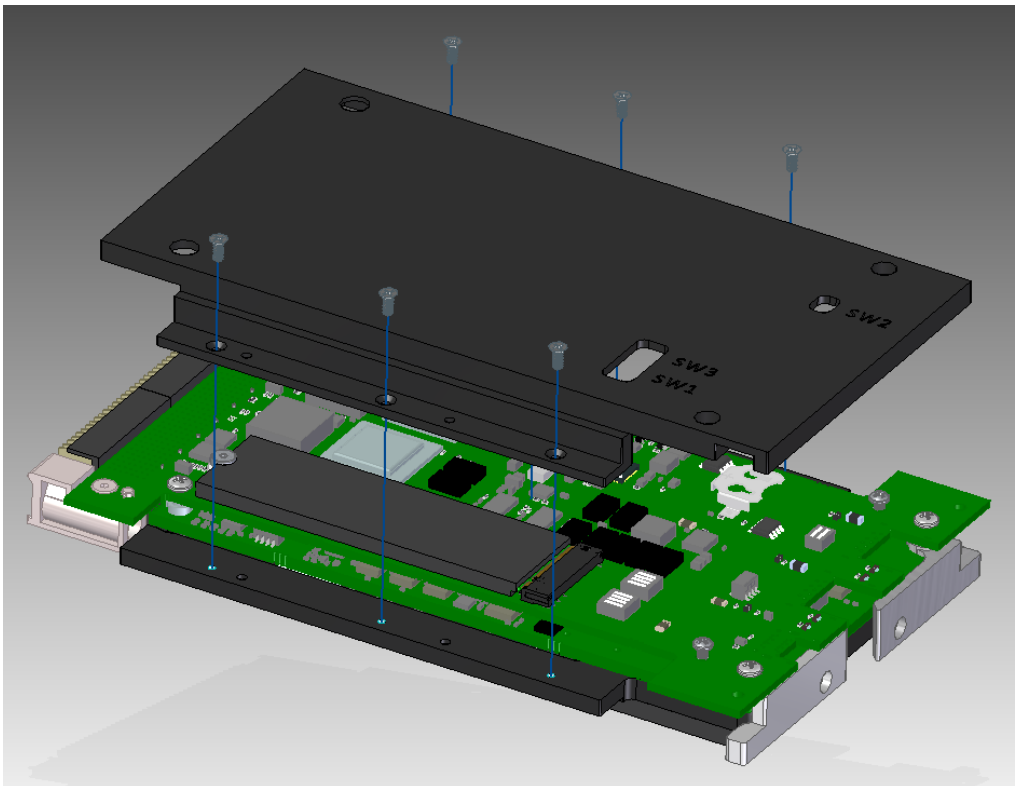
5. Place the washer on the VPX board and carefully press down the M.2 expansion card and secure with shoulder screw.



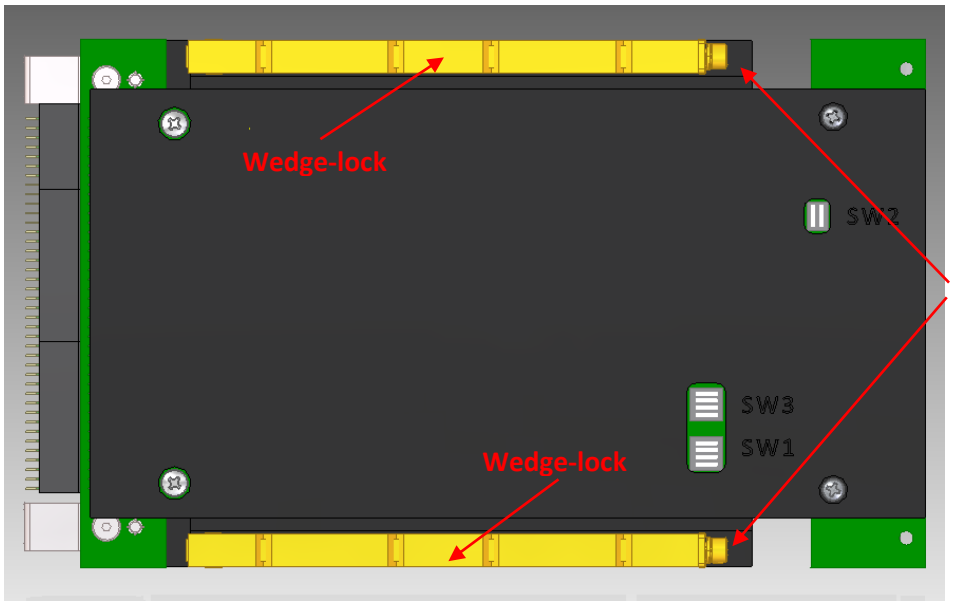
Note: The washer should be under the M.2 expansion card as shown below.

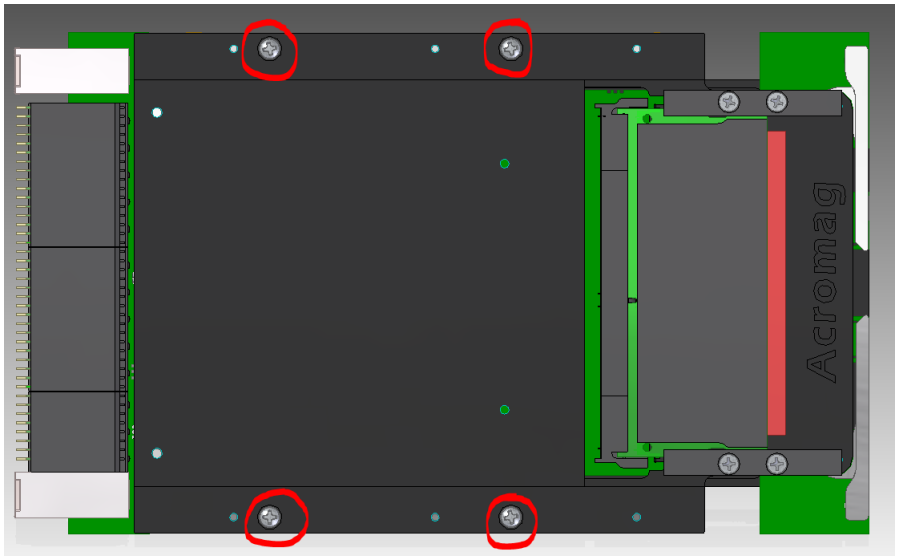


6. Re-install the heatsink and secure with 6 flat-head screws (M2 x 6mm).



7. Attach the 2 wedge-locks to the bottom and secure with 4 screws located on the top.

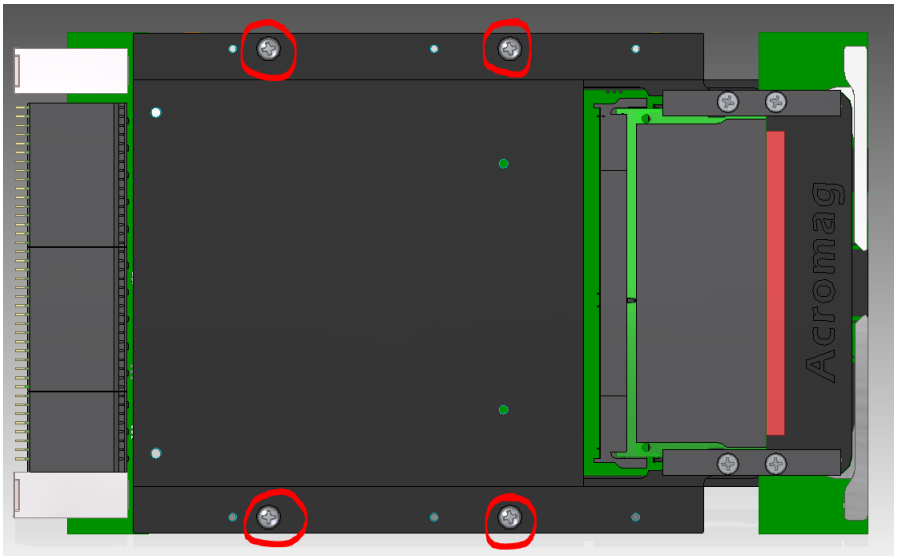


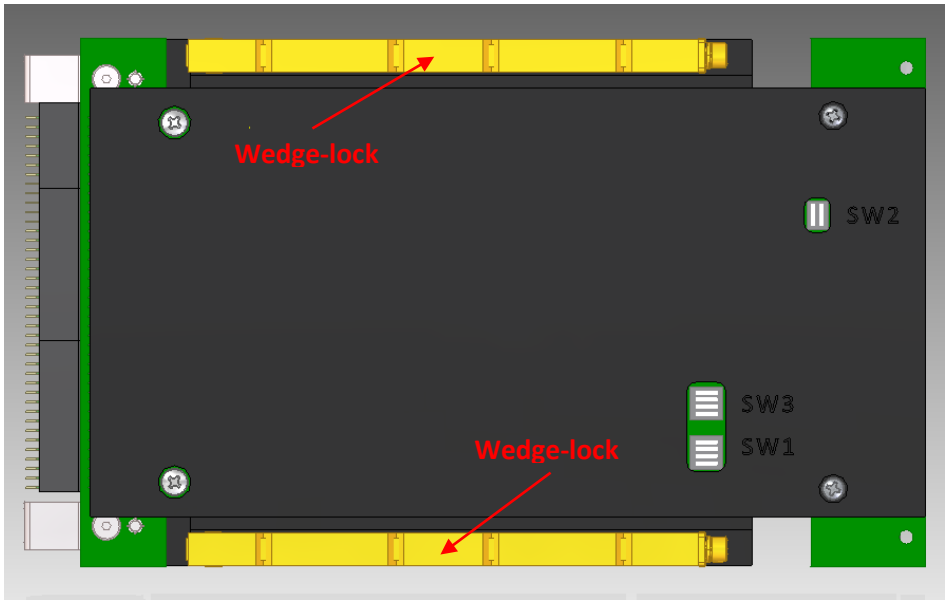


VPX6600-CC-LF (Conduction-cooled) M.2 expansion card installation complete.

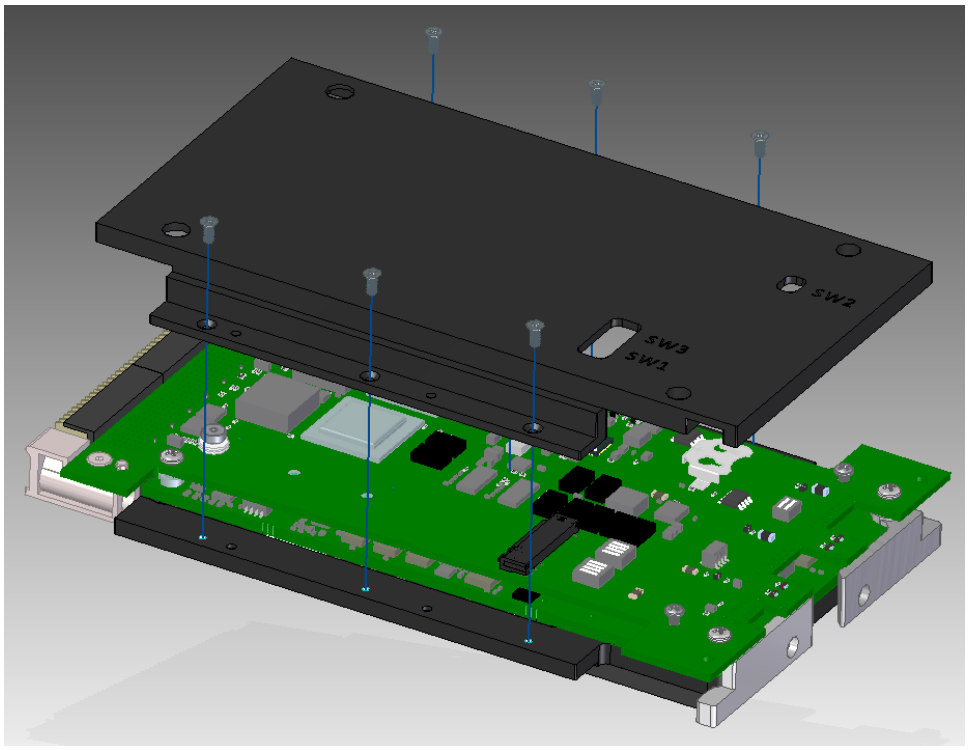
6.6.4 VPX6600-CC-LF (Conduction-Cooled) Battery Replacement

1. Remove the 4 screws (M2 x 6mm) that secure the two wedge-locks to the board. Remove the two wedge-locks.

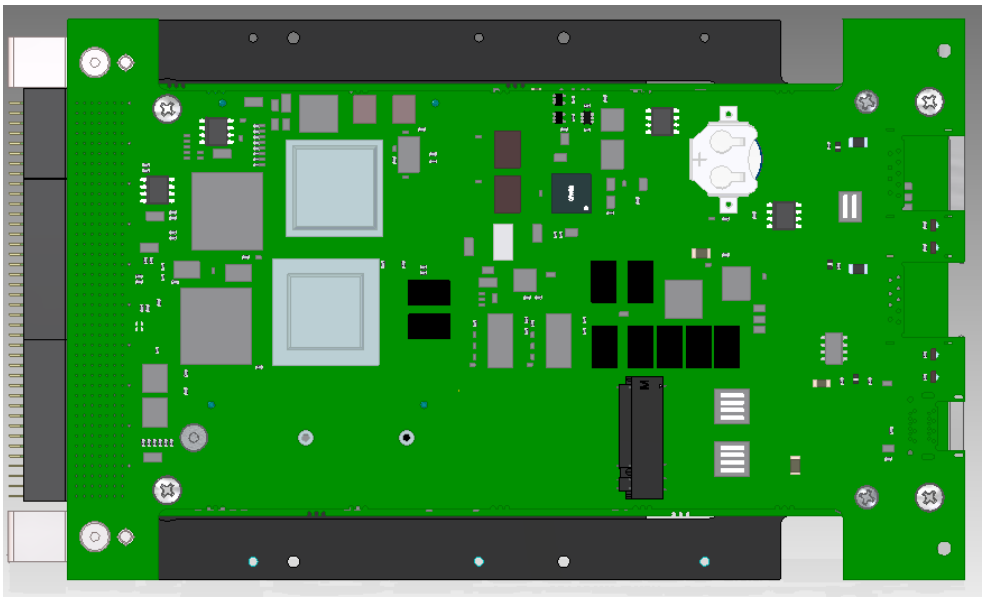




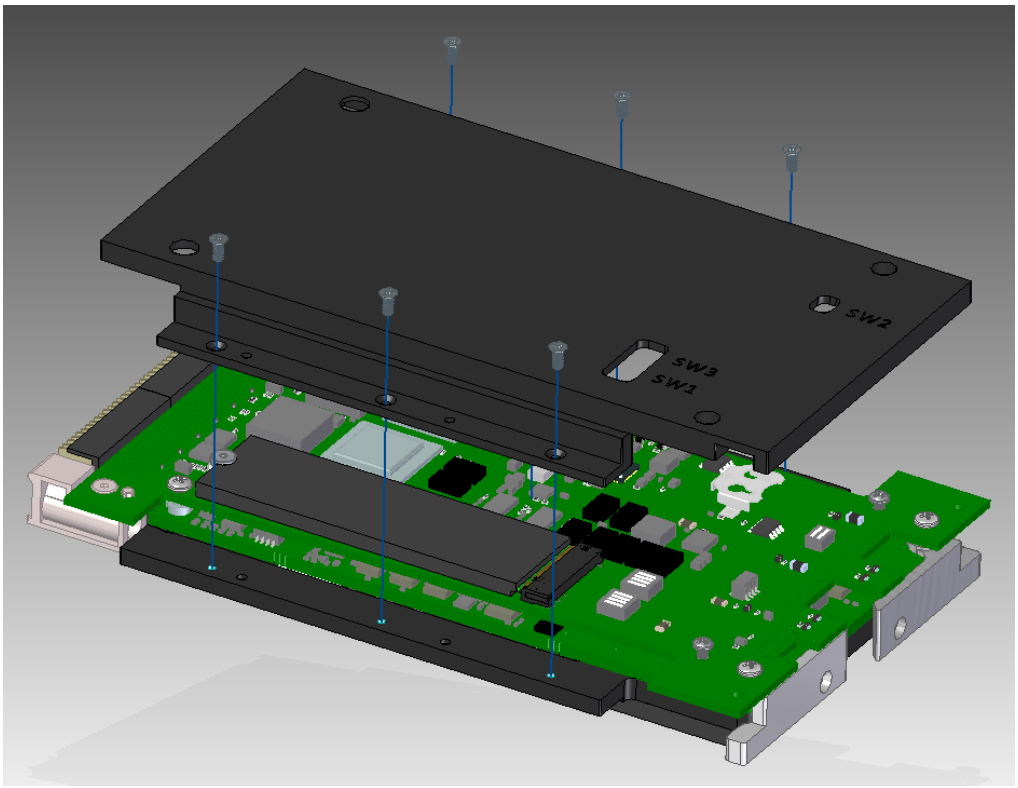
2. Remove the 6 flat-head screws (M2 x 6mm) that secure the heatsink to the board. Remove the heatsink.



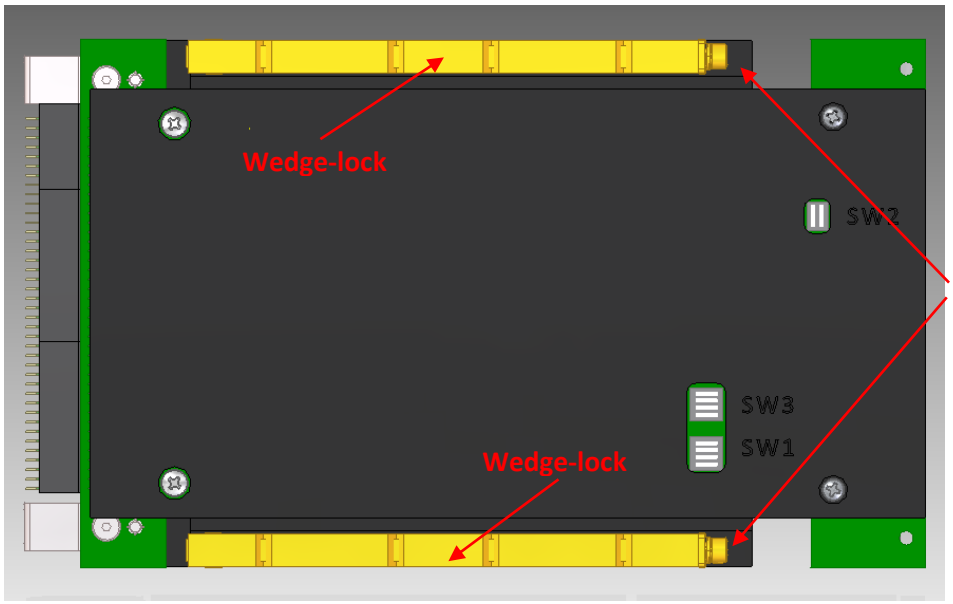
3. Install new battery with "+" face up.

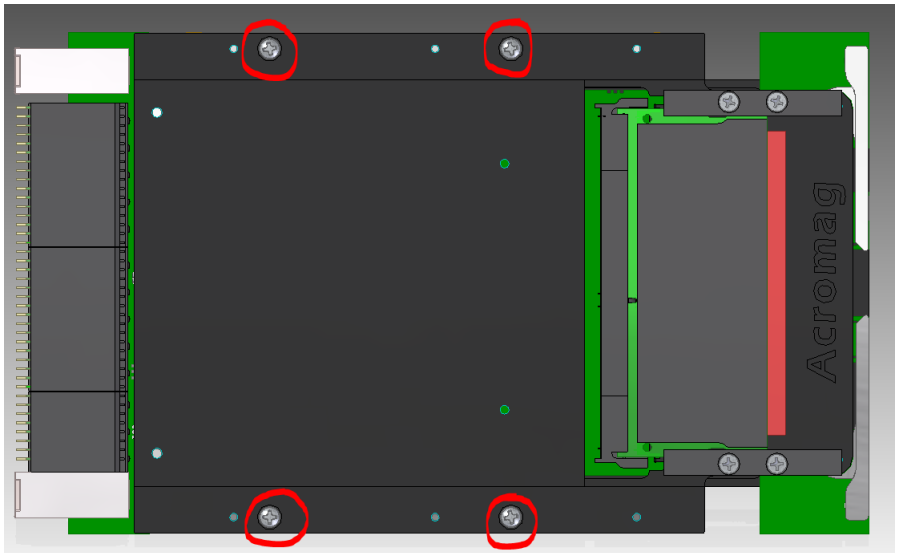


4. Re-install the heatsink and secure with 6 flat-head screws (M2 x 6mm).



5. Attach the 2 wedge-locks to the bottom and secure with 4 screws located on the top.





VPX6600-CC-LF (Conduction-cooled) battery replacement is complete.

6.7 Certificate of Volatility

Certificate of Volatility				
Acromag Model VPX6600-LF VPX6600-CC-LF	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) ■ Yes □ No				
Type (SRAM, SDRAM, etc.) SDRAM	Size: 32GB	User Modifiable ■ Yes □ No	Function: Storage of code/data for CPU	Process to Sanitize: Power Down
Type (SRAM, SDRAM, etc.) PCH internal CMOS SRAM	Size: 256 bytes	User Modifiable ■ Yes □ No	Function: Data storage for system/BIOS	Process to Sanitize: Set SW1-1 into the ON position.
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No				
Type(EEPROM, Flash, etc.) Flash	Size: 16 Mbytes	User Modifiable ■ Yes □ No	Function: Storage of Code and Data for system/BIOS	Process to Sanitize: Clear Flash memory by erasing all sectors of the Flash
Type(EEPROM, Flash, etc.) EEPROM (CPU ID EERPROM)	Size: 256 bytes	User Modifiable ■ Yes □ No	Function: Storage of CPU model and serial	Process to Sanitize: Clear EEPROM memory by erasing all bytes.
Type(EEPROM, Flash, etc.) EEPROM (VPX ID EERPROM)	Size: 2 kbytes	User Modifiable ■ Yes □ No	Function: Storage of VPX model and serial	Process to Sanitize: Clear EEPROM memory by erasing all bytes.
Acromag Representative				
Name: Russ Nieves	Title: Director of Sales and Marketing	Email: solutions@acromag.com	Office Phone: 248-295-0310	Office Fax: 248-624-9234

7.0 VPX6600-RTM Rear-Transition Accessory Module

The optional VPX6600-RTM module may be installed into the rear slot directly behind the VPX6600 to easily access all of the available I/O on P2 connector.

The following I/O is available on the front panel of the VPX6600-RTM:

- Two USB 2.0 ports via standard USB 2.0 connector.
- Two USB 3.0 ports via standard USB 3.0 connector.
- Two DisplayPort ports via standard Mini-DisplayPort connector.
- One Gigabit Ethernet port via standard RJ45 connector.

The following I/O is available via internal connectors on the VPX6600-RTM:

- Two SATA III ports via standard 7-pin SATA data connectors.
- Two software-selectable RS-232/RS-422/RS-485 Serial Ports are available via 10-pin headers.
- Stereo Audio Line-In & Line-Out via a 5-pin connector.
- Six General Purpose I/O pins via an 8-pin header.

7.1 Ordering Information

The VPX6600-RTM ordering options are given in the following table.

Model Number	***Description***	***Temp Range***
VPX6600-RTM-LF	*VPX6600 Rear Transition Module*	*-40°C to 85°C*

7.2 Connector Information

7.2.1 VPX Backplane Connectors

7.2.1.1 RP0 VPX Connector

RP0 Wafer	A	B	C	D	E	F	G
1	NC	NC	NC	NC	NC	NC	NC
2	+3.3V	+3.3V	+3.3V	NC	NC	NC	NC
3	+5V	+5V	+5V	NC	+5V	+5V	+5V
4	NC	NC	GND	NC	GND	NC	NC
5	NC	NC	GND	NC	GND	NC	NC
6	NC	NC	GND	NC	GND	NC	NC
7	NC	NC	GND	NC	NC	GND	NC
8	GND	NC	NC	GND	NC	NC	GND
9	NC	NC	GND	NC	NC	GND	NC
10	GND	NC	NC	GND	NC	NC	GND
11	NC	NC	GND	NC	NC	GND	NC
12	GND	NC	NC	GND	NC	NC	GND

13	NC	NC	GND	NC	NC	GND	NC
14	GND	NC	NC	GND	NC	NC	GND
15	NC	NC	GND	NC	NC	GND	NC
16	GND	NC	NC	GND	NC	NC	GND

7.2.1.2 RP1 VPX Connector

RP1 Wafer	A	B	C	D	E	F	G
1	NC	NC	GND	NC	NC	GND	ENET0_LINK/ACTIVITY#
2	GND	NC	NC	GND	NC	NC	GND
3	NC	NC	GND	NC	NC	GND	NC
4	GND	NC	NC	GND	NC	NC	GND
5	ENET0_P0_P	ENET0_P0_N	GND	ENET0_P1_P	ENET0_P1_N	GND	NC
6	GND	ENET0_P2_P	ENET0_P2_N	GND	ENET0_P3_P	ENET0_P3_N	GND
7	NC	NC	GND	NC	NC	GND	NC
8	GND	NC	NC	GND	NC	NC	GND
9	USB4_P	USB4_N	GND	USB3_P	USB3_N	GND	GPIN0
10	GND	DPC_AUX_SEL	USB_3_4_OC#	GND	DPB_AUX_SEL	USB_1_2_OC#	GND
11	USB1_SSRX_P	USB1_SSRX_N	GND	USB1_P	USB1_N	GND	GPIN1
12	GND	USB2_P	USB2_N	GND	USB1_SSTX_P	USB1_SSTX_N	GND
13	USB2_SSTX_P	USB2_SSTX_N	GND	USB2_SSRX_P	USB2_SSRX_N	GND	GPIN2
14	GND	AGND_AUDIO	LINEOUT_L	GND	AGND_AUDIO	LINEIN_L	GND
15	LINEOUT_R	AGND_AUDIO	GND	LINEIN_R	AGND_AUDIO	GND	GPOUT3
16	GND	SATA2_RX_P	SATA2_RX_N	GND	SATA2_TX_P	SATA2_TX_N	GND

7.2.1.3 RP2 VPX Connector

RP2 Wafer	A	B	C	D	E	F	G
1	SATA3_RX_P	SATA3_RX_N	+3.3 V	SATA3_TX_P	SATA3_TX_N	GND	GPOUT4
2	GND	DPB_TX1_P	DPB_TX1_N	GND	DPB_TX0_P	DPB_TX0_N	GND
3	DPB_TX3_P	DPB_TX3_N	+5 V	DPB_TX2_P	DPB_TX2_N	GND	GPOUT5
4	GND	COM1_TX_N	COM1_TX_P	GND	DPB_CTRL_AUX_P	DPB_CTRL_AUX_N	GND
5	COM1_RX_N	COM1_RX_P	GND	COM2_TX_N	COM2_TX_P	GND	DPB_HPD
6	GND	DPC_TX1_P	GND	GND	DPC_TX0_P	DPC_TX0_N	GND
7	DPC_TX3_P	DPC_TX3_N	GND	DPC_TX2_P	DPC_TX2_N	GND	DPC_HPD
8	GND	COM2_RX_N	COM2_RX_P	GND	DPC_CTRL_AUX_P	DPC_CTRL_AUX_N	GND

7.2.2 I/O Connectors

7.2.2.1 J3 Mini-DisplayPort Connector

This standard 20-pin Mini-DisplayPort connector (JAE Electronics – DP3R020SU32JQR400) brings DisplayPort B out to the front panel.

PIN	SIGNAL
1	GND
2	DPB_HPD
3	DPB_TX0_P
4	DPB_AUX_SEL
5	DPB_TX0_N
6	GND

7	GND
8	GND
9	DPB_TX1_P
10	DPB_TX3_P
11	DPB_TX1_N
12	DPB_TX3_N
13	GND
14	GND
15	DPB_TX2_P
16	DPB_CTRL_AUX_P
17	DPB_TX2_N
18	DPB_CTRL_AUX_N
19	GND
20	+3.3V

7.2.2.2 J4 Mini-DisplayPort Connector

This standard 20-pin Mini-DisplayPort connector (JAE Electronics – DP3R020SU32JQR400) brings DisplayPort C out to the front panel.

PIN	SIGNAL
1	GND
2	DPC_HPD
3	DPC_TX0_P
4	DPC_AUX_SEL
5	DPC_TX0_N
6	GND
7	GND
8	GND
9	DPC_TX1_P
10	DPC_TX3_P
11	DPC_TX1_N
12	DPC_TX3_N
13	GND
14	GND
15	DPC_TX2_P
16	DPC_CTRL_AUX_P
17	DPC_TX2_N
18	DPC_CTRL_AUX_N
19	GND
20	+3.3V

7.2.2.3 J5 USB 3.0 Connector

This standard 9-pin USB3.0 connector (Molex – 48404-003) brings USB Port 1 out to the front panel.

PIN	SIGNAL
1	+5V
2	USB1_N
3	USB1_P
4	GND
5	USB1_SSRX_N
6	USB1_SSRX_P
7	GND
8	USB1_SSTX_N
9	USB1_SSTX_P

7.2.2.4 J6 USB 3.0 Connector

This standard 9-pin USB3.0 connector (Molex – 48404-003) brings USB Port 2 out to the front panel.

PIN	SIGNAL
1	+5V
2	USB2_N
3	USB2_P
4	GND
5	USB2_SSRX_N
6	USB2_SSRX_P
7	GND
8	USB2_SSTX_N
9	USB2_SSTX_P

7.2.2.5 J9 SATA Connector

This standard 7-pin SATA connector (Molex – 67800-8005) brings SATA Port 2 out to an internal connector.

PIN	SIGNAL
1	GND
2	SATA2_TXP
3	SATA2_TX_N
4	GND
5	SATA2_RX_N
6	SATA2_RX_P
7	GND

7.2.2.6 J10 SATA Connector

This standard 7-pin SATA connector (Molex – 67800-8005) brings SATA Port 3 out to an internal connector.

PIN	SIGNAL
1	GND
2	SATA3_TXP
3	SATA3_TX_N
4	GND
5	SATA3_RX_N
6	SATA3_RX_P
7	GND

7.2.2.7 J11 USB 2.0 Connector

This standard 4-pin USB2.0 connector (Molex – 67329-8001) brings USB Port 3 out to the front panel.

PIN	SIGNAL
1	+5V
2	USB3_N
3	USB3_P
4	GND

7.2.2.8 J12 USB 2.0 Connector

This standard 4-pin USB2.0 connector (Molex – 67329-8001) brings USB Port 4 out to the front panel.

PIN	SIGNAL
1	+5V
2	USB4_N
3	USB4_P
4	GND

7.2.2.9 J13 Ethernet Connector

This standard 8-pin Ethernet connector (TE Connectivity – 2-406549-1) brings Ethernet Port 0 out to the front panel.

PIN	SIGNAL
1	ENET0_P0_P
2	ENET0_P0_N
3	ENET0_P1_P
4	ENET0_P2_P
5	ENET0_P2_N
6	ENET0_P1_N
7	ENET0_P3_P
8	ENET0_P3_N

7.2.2.10 P1 Serial Port Connector

This 10-pin standard 0.1" header (TE Connectivity – 5103310-1) is used for the COM1 serial port connection. These signals can be accessed through a standard DB-9 connector by using a DB9M TO IDC10 SERIAL (DTK) cable.

PIN	SIGNAL	SIGNAL	PIN
1	NC	COM1_RX-[1]	2
3	COM1_RX	NC	4
5	COM1_TX	NC	6
7	COM1_TX-[1]	NC	8
9	GND	GND	10

[1] TX- and RX- only used when serial port is in RS-422/RS-485 mode

7.2.2.11 P2 Serial Port Connector

This 10-pin standard 0.1" header (TE Connectivity – 5103310-1) is used for the COM2 serial port connection. These signals can be accessed through a standard DB-9 connector by using a DB9M TO IDC10 SERIAL (DTK) cable.

PIN	SIGNAL	SIGNAL	PIN
1	NC	COM2_RX-[1]	2
3	COM2_RX	NC	4
5	COM2_TX	NC	6
7	COM2_TX-[1]	NC	8
9	GND	GND	10

[1] TX- and RX- only used when serial port is in RS-422/RS-485 mode

7.2.2.12 P3 GPIO Connector

This 8-pin 0.1" header (Samtec – TSM-104-01-L-DV) is used to access the general purpose I/O signals.

PIN	SIGNAL	SIGNAL	PIN
1	GPIO0	GPIO3	2
3	GPIO1	GPO4	4
5	GPIO2	GPIO5	6
7	NC	NC	8

7.2.2.13 P4 Audio Connector

This 5-pin connector (Molex – 533980571) is used for the stereo audio line-in and line-out connections.

PIN	SIGNAL
1	LINEOUT_R
2	LINEOUT_L
3	AGND_AUDIO
4	LINEIN_R
5	LINEIN_L

7.3 Power Requirements

The power used by the VPX6600-RTM board is negligible.

7.4 Environmental Considerations

7.4.1 Operating Temperature

-40°C to 85°C[1]

[1] Measured as Ambient Air Temperature. 300LFM minimum air-flow required. Designed to meet this temperature specification.

7.4.2 Relative Humidity

5% to 95% Non-condensing

7.4.3 Vibration and Shock Standards

Vibration, Sinusoidal Operating: Designed to comply with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis

Vibration, Random Operating: Designed to comply with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis

Shock, Operating: Designed to comply with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3mS half sine, 18 shocks at 6 orientations for both test levels

7.4.4 EMC Directives

The VPX6600 is designed to comply with EMC Directive 2004/108/EC.

- **Immunity per EN 61000-6-2:**
  Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2.
  Radiated Field Immunity (RFI), per IEC 61000-4-3.
  Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4.
  Surge Immunity, per IEC 61000-4-5.
  Conducted RF Immunity (CRFI), per IEC 61000-4-6.
- **Emissions per EN 61000-6-4:**
  Enclosure Port, per CISPR 16.
  Low Voltage AC Mains Port, per CISPR 16.

Note: This is a Class A product

7.5 Reliability Prediction

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled,* $G_B G_C$

Table 7.5.a MTBF

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	TBD	TBD	TBD
40°C	TBD	TBD	TBD

[1] FIT is Failures in 10^9 hours.

7.6 Certificate of Volatility

<table>
<tr><th colspan="6">Certificate of Volatility</th></tr>
<tr><td colspan="2">Acromag Model
VPX6600-RTM-LF</td><td colspan="4">Manufacturer:
Acromag, Inc.
30765 Wixom Rd
Wixom, MI 48393</td></tr>
<tr><th colspan="6">Volatile Memory</th></tr>
<tr><td colspan="6">Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed)
□ Yes ■ No</td></tr>
<tr><td>Type (SRAM, SDRAM, etc.)</td><td>Size:</td><td>User Modifiable
□ Yes
□ No</td><td>Function:</td><td colspan="2">Process to Sanitize:</td></tr>
<tr><td>Type (SRAM, SDRAM, etc.)</td><td>Size:</td><td>User Modifiable
□ Yes
□ No</td><td>Function:</td><td colspan="2">Process to Sanitize:</td></tr>
<tr><th colspan="6">Non-Volatile Memory</th></tr>
<tr><td colspan="6">Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed)
□ Yes ■ No</td></tr>
<tr><td>Type(EEPROM, Flash, etc.)</td><td>Size:</td><td>User Modifiable
□ Yes
□ No</td><td>Function:</td><td colspan="2">Process to Sanitize:</td></tr>
<tr><td>Type(EEPROM, Flash, etc.)</td><td>Size:</td><td>User Modifiable
□Yes
□ No</td><td>Function:</td><td colspan="2">Process to Sanitize:
.</td></tr>
<tr><th colspan="6">Acromag Representative</th></tr>
<tr><td>Name:
Russ Nieves</td><td>Title:
Director of Sales and Marketing</td><td>Email:
solutions@acromag.com</td><td>Office Phone:
248-295-0310</td><td colspan="2">Office Fax:
248-624-9234</td></tr>
</table>

Revision History

The following table shows the revision history for this document:

Release Date	Version	EGR/DOC	Description of Revision
30 DEC 2016	Prelim	MDW/ARP	Preliminary release.
30 DEC 2016	A	MDW/MJO	Initial release.
17 FEB 2017	B	PDG/ARP	Section 6.6 Installation of M.2 Expansion Card and Battery Replacement: The two washers have been replaced with one washer; changed accordingly.
31 MAY 2019	C	JBO/ARP	Added new Batteryless products to the Ordering Information section.
7 AUG 2019	D	MDW/MJO	Added information about supported M.2 module lengths. Updated SW1 switch tables to reflect updates for Rev H or later products.
04 OCT 2019	E	MDW/MJO	Updated MTBF Table, Section 6.5 Reliability Prediction.