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Known Difference Between IP320 and the IP320A

The IP320A has been designed as a drop-in replacement for the IP320. The known differences between the models include a change in method for selecting the input range as well as enhancements in accuracy, throughput, power efficiency, and general board operation. Our testing indicates that the new IP320A should work in all current customers' applications.

Input Range Selection

The IP320A input range is now selected via a miniature DIP Switch. The original IP320 used jumpers.

Enhanced Features

➢ Increased Accuracy

The hardware on the IP320A has changed to include a new precision Analog to Digital Converter from Texas Instruments and an improved gain amplifier with decreased error. These changes have improved the accuracy of the uncalibrated error on the IP320A. For more details on the hardware changes and the resulting change in accuracy please refer to the "*IP320 vs. IP320A"* comparison section in the IP320A manual and the table below.

Hardware specification changes

	IP320	**IP320A**
A/D Converter	ADS774KE	ADS8508
Linearity Error[1]	±0.5 LSB	±0.45 LSB
Unipolar Offset Err[1]	±2 LSB	±2.05 LSB
Bipolar Offset Err[1]	±4 LSB	±0.41 LSB
F.S. Cal. Error[1]	0.25%	0.5%
PGA	PGA203KP	PGA206AU
Linearity Error[1]	±0.012%	±0.005%
RTI Error[1]	2mV +24mV/Gain	2.5mV
Gain Error[1]	0.25%	0.1%

1. Statistical Maximum values at 25°C.

➢ Increased Throughput

Additional hardware changes have reduced the settling time and conversion time on the IP320A. The increased speed allows for a maximum conversion rate of 200KHz.

	IP320	IP320A
Conversion Time[1]	8.5μs	4.5μs
Input Setting Time to 0.01% of F.S.[1]	8.5μs (10V step)	5.2μs (20 V step)

1. Statistical Maximum values at 25°C.

➢ Power Efficiency

The IP320A now only requires 90mA typical, 250mA maximum from the 5 Volt IP power supply reducing overall system load. However, the ±12 Volt (or ±15 Volt external) rails may each require 25mA maximum (an increase of 5mA).

➢ Board Operation/Reset Conditions

The new Complex Programmable Logic Device (CPLD) on the board allows for improved operation. This includes a known Reset state for all registers and a "*Data Ready*" bit in the control register to allow the end user to know when an analog conversion is complete and the resulting value is available to be read in the *ADC Data Register*. Additionally, the number of wait states for the *ADC Convert Command* has increased from zero to one and the minimum number of wait states to read the *ADC Data Register* has decreased from three to two. Wait state changes are invisible to the end user. Furthermore the storage temperature for all models is -40°C to 125°C . For more details on any of these changes please refer to the appropriate sections in the IP320A manual or the tables below.

Memory Map Changes

	IP320	IP320A
Control Register (Base Add + 0): Bit 14	Not Used.	Data Ready: Indicates if an A/D conversion is complete and valid data can be read from the ADC Data Register.
Register Reset Condition	All values undefined.	All values "0".
Not Used Address Space	R/W: Will not respond.	R/W: IP module responds w/ ACK*. All reads return "0".

*Active low signal.

Wait State Changes

	IP320	IP320A
ADC Convert Reg. Write	0 wait states	1 wait state
ADC Data Reg. Read	3 wait states min	2 wait states min
	68 wait states max	36 wait states max