

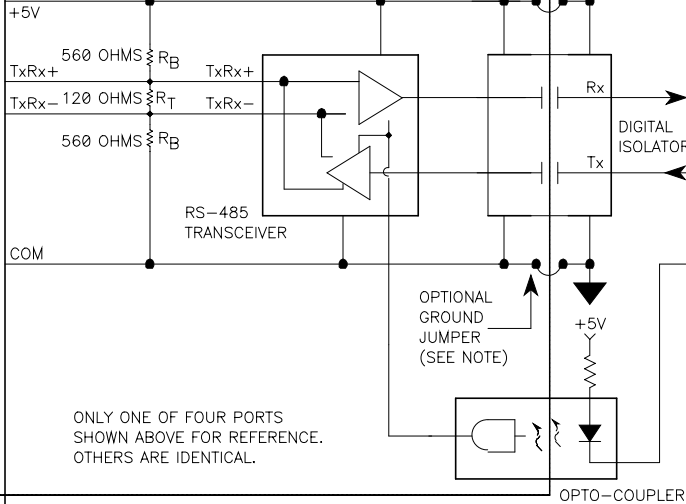
# IP512 BLOCK DIAGRAM

NOTE: THE 120 OHM RECEIVER TERMINATION RESISTOR (RT) AND 560 OHM BIAS RESISTOR (RB) SIPS ARE MOUNTED IN SOCKETS AND MAY BE REMOVED WHERE REQUIRED. SEE DRAWING 4501-587 FOR LOCATION.

EIA-485  
INTERFACE

P2

ISOLATED PORT (ONLY ONE OF FOUR SHOWN, OTHERS ARE IDENTICAL)



ONLY ONE OF FOUR PORTS SHOWN ABOVE FOR REFERENCE. OTHERS ARE IDENTICAL.

PORTS A-D

P2 PINS 19-25 & 44-50 ARE NOT CONNECTED

OPTIONAL POWER JUMPER (SEE NOTE)

+5V

Rx

Tx

DIGITAL ISOLATOR

OPTIONAL GROUND JUMPER (SEE NOTE)

+5V

OPTO-COUPLER

NOTE: PORT POWER +5V & COMMON MAY BE OPTIONALLY JUMPERED TO IP +5V & COMMON FOR NON-ISOLATED OPERATION. OTHERWISE, ISOLATED +5V POWER MUST BE PROVIDED TO THE PORT EXTERNALLY VIA P2.

+5V

Rx

Tx

UART

RTS

COMMON

CONTROL LOGIC

+5V

SUPPLY FILTERING

LOGIC  
INTERFACE

P1

DATA BUS

ADDRESS BUS

CONTROL BUS

INTERRUPT REQUEST

ACKNOWLEDGE

+5V

GND