Series IP236A Industrial I/O Pack
FIFO Buffered 16-Bit Analog Output Module

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP236A modules are precision 16-bit, high density, single size IP, analog output boards with up to eight analog voltage output channels. All channels can be independently controlled allowing unique DAC update rates if desired. Each of the output channels include generous 128-sample FIFO buffers, from which digital values are transferred to its corresponding Digital-to-Analog-Converter (DAC). In addition to the FIFO, interrupt generation is also supported for FIFO almost empty conditions, to minimize CPU interaction.

The IP236A modules interface to the VMEbus, PCIbus, or ISAbus, carrier boards. Up to five units may be mounted on the PCIbus carrier board to provide up to 40 16-bit independent DAC output channels per PCI system slot.

The IP236A utilizes state of the art Surface-Mounted Technology (SMT) to achieve its wide functionality and is an ideal choice for a wide range of industrial and scientific applications that require, high-performance analog outputs.

The IP236A modules are available with eight (IP236A-8) 16-bit analog output channels. The IP236A-8 is available in standard and extended temperature range modules as follows:

Model	Analog Output Channels	FIFO Buffer Per Channel	Temperature Range
IP236A-8	8	Yes	0 to +70°C
IP236A-8E	8	Yes	-40°C to +85°C

KEY IP236A FEATURES

- **DAC 16-Bit Resolution** - 16-bit monolithic DAC with bipolar voltage output ranges of ±10V, ±5V, and an unipolar output range of 0 to 10V. The IP236A-8 will have eight independently controlled DACs present on the board.
- **10μsec Conversion Time** - A maximum recommended conversion rate of 100KHz, for specified accuracy, is supported. The absolute maximum conversion rate of 150KHz is also supported.
- **128-Sample FIFO Buffers -** Each DAC channel provides 128-sample data buffering to reduce CPU interactions and interrupts. This allows the external processor to handle more tasks within a given time.
- **Continuous Conversion Mode -** Each of the channel's FIFOs can be filled/loaded with new data without stopping output waveform generation.
- **Single Step Mode** - On each new software or external trigger, each output channel can be independently updated with a new DAC value read from their corresponding FIFO buffer.
- **Interrupt Support -** Individually controlled FIFO almost empty interrupts may be generated. Unique interrupt thresholds can be assigned to each channel. On a FIFO almost empty interrupt, the interrupt service routine could fill the FIFO with new data while output waveform generation continues. Thus, allowing continuous conversions.
- **User Programmable Interval Timer** - Each channel has a user programmable interval timer provided to control the delay between conversions. Each channel is independently converted at the rate set by its corresponding interval timer. This feature supports a minimum interval of 6.7μsec and a maximum interval of 2.09 seconds.
- **FIFO Full and Almost Empty Flags-** Individual FIFO Full and Almost Empty flag bits are available to implement software polling schemes for FIFO buffer data control.
- **External Trigger Scan Mode** - Each channel has an external trigger which is assigned to a field I/O line. Thus, all channels can independently initiate a new conversion with each external trigger via its dedicated external trigger pin. This mode allows synchronization of conversions with external events that are often asynchronous.
- **External Trigger Output** - The external trigger may be configured as an output signal to provide a means to synchronize other channels or IP236A devices to a single IP236A channel or module.
- **Reliable Software Calibration** - Calibration coefficients stored on-board provide the means for accurate software calibration for both gain and offset correction for each of the channels of the module.
- **Reset is Failsafe For Bipolar Output Ranges -** When the module's jumpers are set for bipolar operation, the analog outputs are reset to 0 volts upon power up or receipt of a software or hardware reset. This eliminates the problem of applying random output voltages to actuators during power on sequences.
- **Hardware Jumper Setting For Selection of DAC Ranges** - Both bipolar (±5V, ±10V) and unipolar (0 to 10V) ranges are available. The ranges can be selected on a per channel basis.
- **High Density** - Provides programmable control of eight analog voltage output channels. Four units mounted on a VMEbus or ISAbus carrier board provide 32 DAC channels in a single system slot. On the PCIbus carrier, up to five units may be mounted to provide up to 40 DAC channels per PCI system slot.
- **Extended Temperature Performance Option -** Model IP236A-8E unit support operation from -40°C to +85°C.

INDUSTRIAL I/O PACK INTERFACE FEATURES

- **High density -** Single-size, industry standard, IP module footprint. Four/five units mounted on a carrier board provide up to 32/40 serial ports in a single system slot.
- **Local ID** - Each IP module has its own 8-bit ID information which is accessed via data transfers in the "ID Read" space.
- **16-bit and 8-bit I/O** - Port register Read/Write is performed through data transfer cycles in the IP module I/O space.
- **High Speed** - Access times for all data transfer cycles are described in terms of "wait" states - 0 wait state is required for reading and writing all control registers and ID values. Interrupt select cycles also require 0 wait states for reading the interrupt vector. Two wait states are typically required to write the channel data FIFO ports (see the Specifications section for detailed information).

SIGNAL INTERFACE PRODUCTS
(See Appendix for more information on compatible products)

This IP module will mate directly to any industry standard IP carrier board (including Acromag's AVME9630/9660 3U/6U VMEbus carrier boards). Additionally, PC/AT carrier boards are also supported (see the Acromag Model APC8620 PCIbus carrier board). A wide range of other Acromag IP modules are available to serve your signal conditioning and interface needs.

The cables and termination panels, described in the following paragraphs, are also available. For optimum performance with the 16-bit IP236A analog output modules, use of the shortest possible length of shielded output cable is recommended. Since all connections to field signals are made through the carrier board which passes them to the individual IP modules, you should consult the documentation of your carrier board to ensure compatibility with the following interface products.

Cables:

Model 5025-551-X (Shielded Cable), or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9630/9660, APC8610, or APC8620 carrier boards, to Model 5025-552 termination panels. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications. The "-X" suffix of the model number is used to indicate the length in feet.

Termination Panels:

Model 5025-552: A DIN-rail mountable panel that provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9630/9660, APC8610, or APC8620 carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

Transition Module:

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from a VMEbus card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. It connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within the card cage, via flat 50-pin ribbon cable (cable Model 5025-550 or 5025-551).

IP MODULE DLL CONTROL SOFTWARE

Acromag provides a software product (sold separately) to facilitate the development of Windows (98/Me/2000/XP®) applications accessing Acromag Industry Pack models installed on Acromag PCI Carrier Cards and CompactPCI Carrier Cards. This software (Model IPSW-API-WIN) consists of low-level drivers and Windows 32 Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments including Visual C++™, Visual Basic, and others. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

IP MODULE VxWORKS SOFTWARE

Acromag provides a software product (sold separately) consisting of board VxWorks® software. This software (Model IPSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all Acromag IP modules and Carriers, PCI I/O Cards, and CompactPCI I/O Cards. The software is implemented as a library of “C” functions which link with existing user code to make possible simple control of all Acromag PCI boards.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-434 and the following discussion for configuration and assembly instructions.

IMPORTANT: The leads of the large 240 pin surface mount IC are fragile. Avoid direct contact with the leads when installing and removing the module for a carrier.

The board may be configured differently, depending on the application. Jumper settings are discussed in the following sections. The jumper locations are shown in Drawing 4501-735.

Default Hardware Jumper Configuration

The board is shipped from the factory, configured as follows:

- Each analog output range is configured for a bipolar output with a 20 volt span (i.e. a DAC output range of -10 to +10 Volts).
- The default programmable software control register bits at power-up are described in section 3. The control registers must be programmed to the desired mode before starting DAC analog output conversions.

Analog Output Ranges and Corresponding Digital Codes

The IP236A is designed to accept positive-true binary two's complement (BTC) input codes which are compatible with bipolar analog output operation. Table 2.1 indicates the relationship between the data format and the ideal analog output voltage for each of the analog output ranges. Selection of an analog output range is implemented via the jumper setting given in Table 2.2.

Table 2.1: Full-Scale Ranges and Ideal Analog Output

DESCRIPTION	Digital Input Code	ANALOG OUTPUT		
Output Range		±10V	0 to 10V	±5V
LSB (Least Significant Bit) Weight		305μV	153μV	153μV
Plus Full Scale Minus One LSB	$7FFF_H$	9.999695 Volts	9.999847 Volts	4.999847 Volts
Midscale	0000_H	0V[1]	5V[1]	0V[1]
One LSB Below Midscale	$FFFF_H$	-305μV	4.999847 Volts	-153μV
Minus Full Scale	8000_H	-10V	0V	-5V

Notes (Table2.1):

1. Upon power-up or software reset the bipolar ranges will output 0 volts while the unipolar range will output 5 volts.

Analog Output Range Hardware Jumper Configuration

The output range of the DACs are individually programmed via hardware jumpers J1 to J8. Jumpers J1 to J8 are used to control channels 0 to 7, respectively. The jumpers control the output voltage span and the selection of unipolar or bipolar output ranges. J1 to J8 pins 1 and 2 control the selection of unipolar or bipolar output ranges. J1 to J8 pins 3 and 4 control the selection of output voltage span. The configuration of the jumpers for the different ranges is shown in Table 2.2. "ON" means that the pins are shorted together with a shorting clip. "OFF" means that the clip has been removed. The individual jumper locations are shown in Drawing 4501-735.

Table 2.2: Analog Output Range Selections/Jumper Settings

Desired ADC Output Range (VDC)	Output Span (Volts)	Required Output Type	J1 to J8 Pins (1&2)	J1 to J8 Pins (3&4)
-5 to +5	10	Bipolar	ON	ON
-10 to +10[1]	20	Bipolar	ON	OFF
0 to +10	10	Unipolar	OFF	ON

Notes (Table2.2):

1. The board is shipped with the default jumper setting for the ±10 volt DAC output range.

Software Configuration

Software configurable control registers are provided for control of external trigger mode, conversion mode, timer control, and interrupt mode selection. No hardware jumpers are required for control of these functions. These control registers must also be configured as desired before starting DAC analog output conversions. Refer to section 3 for programming details.

CONNECTORS

Connectors of the IP236A module consist of one IP module field I/O connector, and one IP module logic connector. These interface connectors are discussed in the following sections.

IP Field I/O Connector (P2)

P2 provides the field I/O interface connections for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly.

P2 pin assignments are unique to each IP model (see Table 2.3) and normally correspond to the pin numbers of the field I/O interface connector on the carrier board (you should verify this for your carrier board). When reading Table 2.3 note that channel designations are abbreviated to save space. For example, channel 0 is abbreviated as "+CH00" & "-CH00" for the + & - connections, respectively. Further, note that the output signals all have the same ground reference ("-CH00" and the minus leads of all other channels are connected to analog common on the module).

Table 2.3: IP236A[2] Field I/O Pin Connections (P2)

Pin Description	Number	Pin Description	Number
+CH00	1	No Connection	26
-CH00[1]	2	No Connection	27
COMMON[1]	3	No Connection	28
+CH01	4	No Connection	29
-CH01[1]	5	No Connection	30
COMMON[1]	6	No Connection	31
+CH02	7	No Connection	32
-CH02[1]	8	No Connection	33
COMMON[1]	9	No Connection	34
+CH03	10	No Connection	35
-CH03[1]	11	No Connection	36
COMMON[1]	12	No Connection	37
+CH04	13	No Connection	38
-CH04[1]	14	No Connection	39
COMMON[1]	15	No Connection	40
+CH05	16	No Connection	41
-CH05[1]	17	EXT TRIGCH0*	42
COMMON[1]	18	EXT TRIG CH1*	43
+CH06	19	EXT TRIG CH2*	44
-CH06[1]	20	EXT TRIG CH3*	45
COMMON[1]	21	EXT TRIG CH4*	46
+CH07	22	EXT TRIG CH5*	47
-CH07[1]	23	EXT TRIG CH6*	48
COMMON[1]	24	EXT TRIGCH7*	49
No Connection	25	SHIELD	50

Notes:

1. The minus leads of all channels are connected to analog common on the module.
2. Channels 04 through 07 are only present on 8 channel models.

Analog Outputs: Noise and Grounding Considerations

All output channels are referenced to analog common on the module (See Drawing 4501-737 for analog output connections), but each channel has a separate return (minus lead) to maintain accuracy and reduce noise. Still, the accuracy of the voltage output depends on the amount of current loading (impedance of the load) and the length (impedance) of the cabling. High impedance loads (e.g. loads > 100KΩ) provide the best accuracy. For low impedance loads, the IP236A can source up to 5mA, but the effects of source and cabling resistance should be considered.

Output common is electrically connected to the IP module analog ground which connects to logic ground of the module at the DAC's. As such, the IP236A is non-isolated between the logic and field I/O grounds. Consequently, the field I/O connections are not isolated from the carrier board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections. This is particularly important for analog outputs when a high level of accuracy/resolution is needed. Refer to Drawing 4501-737 for example output and grounding connections.

External Trigger Input/Output Signals

The external trigger signals on pins 42 to 49 of the P2 connector can be programmed to accept a TTL compatible external trigger input signal, or output hardware timer generated triggers to allow synchronization of multiple IP236A modules.

As an input, the external trigger must be a 5 Volt logic, TTL-compatible, debounced signal referenced to analog common. The trigger pulse must be low for a minimum of 250n seconds to guarantee acquisition. The actual conversion is triggered within 6.25μ seconds of the falling edge of the external trigger signal. This type of conversion triggering can be used to synchronize generation of analog output signals to external events.

As an output an active-low TTL signal can be driven to additional IP236A modules, thus providing a means to synchronize conversions. The additional IP236A modules must be programmed for external trigger input and convert on external trigger only mode. The trigger pulse generated is low for 500n seconds, typically. See section 3.0 for programming details to make use of this signal.

IP Logic Interface Connector (P1)

P1 of the IP module provides the logic interface to the mating connector on the carrier board. This connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly. The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.4).

Table 2.4: Standard Logic Interface Connections (P1)

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSEL*	29
D01	5	***DMAReq0****	30
D02	6	MEMSEL*	31
D03	7	***DMAReq1****	32
D04	8	IntSel*	33
D05	9	***DMAck0****	34
D06	10	IOSEL*	35
D07	11	***RESERVED***	36
D08	12	A1	37
D09	13	***DMAEnd****	38
D10	14	A2	39
D11	15	***ERROR****	40
D12	16	A3	41
D13	17	INTReq0*	42
D14	18	A4	43
D15	19	***INTReq1****	44
BS0*	20	A5	45
BS1*	21	***STROBE****	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	***RESERVED***	49
GND	25	GND	50

An Asterisk (*) is used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by this IP Model.

3.0 PROGRAMMING INFORMATION

ADDRESS MAPS

This manual is presented using the "Big Endian" byte ordering format. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses. Thus, byte accesses are done on odd address locations. The Intel x86 family of microprocessors use the opposite convention, or "Little Endian" byte ordering. Little Endian uses even-byte addresses to store the low-order byte. As such, use of this module on a PC carrier board will require the use of the even address locations to access the 8-bit data, while a VMEbus carrier requires the use of odd address locations.

IDENTIFICATION SPACE - (Read Only, 32 Odd-Byte Addresses)

Each IP module contains identification (ID) information that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID space. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP236A ID information space does not contain any variable (e.g. unique calibration) information. ID space bytes are addressed using only the odd addresses in a 64 byte block (on the "Big Endian" VMEbus). Even addresses are used on the "Little Endian" PC ISA bus and PCI bus. The IP236A ID space contents are shown in Table 3.1. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID space. Execution of an ID space read requires 0 wait states.

Table 3.1: IP236A ID Space Identification (Format I)

Hex Offset From ID Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All IP's have 'IPAC'
03	P	50	
05	A	41	
07	C	43	
09		A3	Acromag ID Code
0B		(26 IP236A-8)	IP Model Code[1]
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		0C	Total Number of ID PROM Bytes
17		(93 IP236A-8)	CRC
19 to 3F		yy	Not Used

Notes (Table 3.1):

1. The IP model number is represented by a two-digit code within the ID space (for example the IP236A-8 model is represented by 26 Hex).

I/O SPACE ADDRESS MAP

This board is addressable in the Industrial Pack I/O space to control the conversion of analog outputs to the field. As such, three types of information are stored in the I/O space: control, status, and data.

The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1 to A6, but the IP236A uses only a portion of this space. The I/O space address map for the IP236A is shown in Table 3.2. Note that the base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space.

Table 3.2: IP236A I/O Space Address Memory Map[2]

Hex Base Adr+	MSB D15 D08	LSB D07 D00	Hex Base Adr+
00	Channel Software Reset	Start Convert & FIFO Full Status	01
02	Interrupt Status	Interrupt Vector	03
04	Rd Wr~ / Calibration Coefficient Address	Calibration Coefficient Write Data	05
06	Calibration Coefficient Read Data	Wr Busy / Rd Comp	07
08	Timer Prescaler Channel 0	Control/Status Channel 0	09
0A	Conversion Timer Channel 0		0B
0C	FIFO Port Channel 0		0D
0E	Timer Prescaler Channel 1	Control/Status Channel 1	0F
10	Conversion Timer Channel 1		11
12	FIFO Port Channel1		13
14	Timer Prescaler Channel 2	Control/Status Channel 2	15
16	Conversion Timer Channel 2		17
18	FIFO Port Channel 2		19
1A	Timer Prescaler Channel 3	Control/Status Channel 3	1B
1C	Conversion Timer Channel 3		1D
1E	FIFO Port Channel 3		1F
20	Timer Prescaler[3] Channel 4	Control/Status Channel 4	21
22	Conversion Timer[3] Channel 4		23
24	FIFO Port Channel 4[3]		25

Hex Base Adr+	MSB D15 D08	LSB D07 D00	Hex Base Adr+
26	Timer Prescaler[3] Channel 5	Control/Status Channel 5	27
28	Conversion Timer[3] Channel 5		29
2A	FIFO Port Channel 5[3]		2B
2C	Timer Prescaler[3] Channel 6	Control/Status Channel 6	2D
2E	Conversion Timer[3] Channel 6		2F
30	FIFO Port Channel 6[3]		31
32	Timer Prescaler[3] Channel 7	Control/Status Channel 7	33
34	Conversion Timer[3] Channel 7		35
36	FIFO Port Channel 7[3]		37
38	Reserved[4]	Not Used[1]	39
3A	Not Used[1] ⇓		3B
7E	Not Used[1]		7F

Notes (Table 3.2):

1. The IP will not respond to addresses that are "Not Used".
2. All Reads and writes are 0 wait states (except write to FIFO ports which require 2 wait states typically).
3. Channels 4-7 are only present on 8 channel models.
4. This byte is reserved for use at the factory to enable writing of the calibration coefficients.

Channel Software Reset Register (Write Only, 00H)

This is a write only register that allows software reset on an individual channel basis. Setting data bits 8 to 15 will issue a software reset to the individual channels per the table below. The software reset will clear the individual channel's control register, counters, and FIFO buffer.

Channel Software Reset Register							
MSB							LSB
15	14	13	12	11	10	09	08
Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0

Start Convert & FIFO Full Status Register (Read/Write, 01H)

The Start Convert register (bits-7 to 0) is used to start the conversions of the individual channels. When the channel's corresponding bit is set high, per the table below, conversions are initiated for that channel. The desired mode of conversion must first be configured by setting the channel's: Control, Timer Prescaler, Conversion Timer, and FIFO buffer. Note, if interrupts are used the interrupt vector must also be set prior to issue of a software start convert.

When External Trigger Only mode is selected via bits 2 and 1 of the channel's control register (set to "11"), the channel Software Start Convert bit is disabled from starting data conversions.

This register can be written with either a 16-bit or 8-bit data value. The channel's actual conversion will be initiated 6.625µ seconds after setting its corresponding Start Convert Bit.

Start Convert & FIFO Full Status Register							
MSB							LSB
07	06	05	04	03	02	01	00
Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0

When read this register is used to reflect the FIFO full status of the individual channel FIFO buffers. The individual bits used to indicate FIFO Full status for each of the channel FIFOs is shown in the previous table. A set bit indicates that the channel's FIFO is full. No additional writes to the FIFO buffer should be implemented after the FIFO is full since data transfer will not be acknowledged and can result in a system bus error.

This register can be read as either a 16-bit or 8-bit data read. FIFO Full status will be cleared upon software or hardware reset.

Interrupt Status Register (Read Only, 02H)

The Interrupt Status register (bits 15 to 8) represents the interrupt status of each of the analog output channels. A set bit represents an active interrupt request for the corresponding channel. Disabling a channel interrupt enable bit will clear its interrupt status bit. The interrupt status bit corresponding to each of the analog output channels is shown in the following table. The interrupt status bits are read only bits and can be read as either 8 or 16-bit values.

Interrupt Status Register							
MSB							LSB
15	14	13	12	11	10	09	08
Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0

Interrupt Vector Register (Read/Write, 03H)

The Vector Register can be written with an 8-bit interrupt vector. This vector is provided to the carrier and system bus upon an active INTSEL* cycle. Reading or writing to this register is possible via 16-bit or 8-bit data transfers.

Interrupt Vector Register							
MSB							LSB
07	06	05	04	03	02	01	00

The IP236A Interrupt Vector register can be used as a pointer to an interrupt handling routine. The vector is an 8-bit value and can be used to point to any one of 256 possible locations to access the interrupt handling routine.

An interrupt can be enabled for generation when the number of samples in the FIFO is equal to or less than the set threshold (see the Channel Control register section). Interrupts generated by the IP236A use interrupt request line INTREQ0* (Interrupt Request 0). The IP236A will release the INTREQ0* signal after the FIFO buffer has more samples than the set threshold or if interrupts are disabled.

Issue of a hardware reset will clear the contents of this register to 0. A software reset has no effect on this register.

Calibration Coefficient Access Register (Write, 04H)

This register is used to access the calibration coefficient memory. Calibration data is provided so that software can adjust and improve the accuracy of the analog output voltage over the uncalibrated state. Each channel's unique offset and gain calibration coefficients are stored in coefficient memory which is accessed through this register.

The Calibration Coefficient Access Register is a write-only register and is used to configure and initiate a read cycle to the calibration coefficient memory. Setting bit-15 of this register high, to a "1'', initiates a read cycle.

The address of the calibration coefficient to be read must be specified on bits 14 to 8 of Calibration Coefficient Access register. The address location of each of the gain and offset coefficient is given in table 3.3.

Most Significant Byte of Calibration Coefficient Access Reg	
Read or Write~	Calibration Coefficient Address
15	14, 13, 12, 11, 10, 9, 8

The address corresponding to each of the offset and gain coefficients is given in hex. The coefficients are 16-bit values with the most significant byte at the even addresses and the least significant bytes at the odd addresses for big endian systems. The calibration coefficients are stored as 1/4 LSB's. For additional details on the use of the calibration coefficients, refer to the "Use of Calibration Data" section.

Table 3.3: Offset and Gain Address Memory Map

Channel		Offset Coefficient Address (Hex)		Gain Coefficient Address (Hex)	
		MSB	LSB	MSB	LSB
±10 Volt Range	0	00	01	02	03
	1	04	05	06	07
	2	08	09	0A	0B
	3	0C	0D	0E	0F
	4	10	11	12	13
	5	14	15	16	17
	6	18	19	1A	1B
	7	1C	1D	1E	1F
±5 Volt Range	0	20	21	22	23
	1	24	25	26	27
	2	28	29	2A	2B
	3	2C	2D	2E	2F
	4	30	31	32	33
	5	34	35	36	37
	6	38	39	3A	3B
	7	3C	3D	3E	3F
0 to 10 Volt Range	0	40	41	42	43
	1	44	45	46	47
	2	48	49	4A	4B
	3	4C	4D	4E	4F
	4	50	51	52	53
	5	54	55	56	57
	6	58	59	5A	5B
	7	5C	5D	5E	5F

Write accesses to the Calibration Coefficient Access register require zero wait states and are possible via 16-bit data transfers only. Writes to the coefficient memory are normally only performed at the factory.

A software or hardware reset has no affect on this register.

Calibration Coefficient Status Register (Read, 06H)

The Calibration Coefficient Status register is a read-only register and is used to access the calibration coefficient read data and determine the status of a read cycle initiated by the Calibration Coefficient Access register. In addition, this register is used to determine the status of a write cycle to the coefficient memory. When set bit-1 of this register indicates the coefficient memory is busy completing a write cycle.

All read accesses to this Calibration Coefficient Status register initiate an approximately 1millisecond access to the coefficient memory. **Thus, you must wait 1 millisecond after reading this status register before a new read or write cycle to the coefficient memory can be initiated, (an EEPROM latency limitation).**

A read request of the coefficient memory, initiated through the Calibration Coefficient Access register, will provide the addressed byte of the calibration coefficient on data bits 15 to 8 of the Calibration Coefficient Status register. Although the read request via the Calibration Coefficient Access register is accomplished in less then 800n seconds, typically, the calibration coefficient will not be available in the Calibration Coefficient Status register for approximately 2.5 milliseconds.

Bit-0 of the Calibration Coefficient Status register is the read complete status bit. This bit will be set high to indicate that the requested calibration coefficient is available on data bits 15 to 8 of the status register. This bit is cleared upon initiation of a new read access of the coefficient memory or upon issue of a hardware reset.

Writes to calibration coefficient memory require a special enable code. Writes to coefficient memory are normally only performed at the factory. The module should be returned to Acromag if recalibration is needed.

A write operation to the calibration coefficient memory, initiated via the Calibration Coefficient Access register, will take approximately 5 milliseconds. Bit-1 of the Calibration Coefficient Status register serves as a write operation busy status indicator. Bit-1 will be set high upon initiation of a write operation and will remain high until the requested write operation has completed. New read or write accesses to the coefficient memory, via the Calibration Coefficient Access register, should not be initiated unless the write busy status bit-1 is clear (set low to 0). A hardware reset of the IP module will also clear this bit.

Read accesses to Calibration Coefficient Status register require zero wait states and are possible via 16-bit data transfers only. A software or hardware reset will clear all bits to 0.

CHANNEL REGISTERS

Each channel has it own control/status, counters, and FIFO Buffer registers. This allows each channel to function independently of all others in the module. These registers include a control/status register, 8-bit Timer Prescaler, 16-bit Conversion Timer, and FIFO Port register. Each of these registers are described in the following sections.

Channel Control & Status Register (Read/Write)

This 8-bit read/write register is used to: enable single or continuous conversions, control external trigger mode, enable interrupts, set the FIFO interrupt threshold, and identify a FIFO almost empty condition.

The function of each of the control register bits are described in Table 3.4. This register can be read or written with either 8-bit or 16-bit data transfers. A power-up or software channel reset sets all control register bits to 0.

Table 3.4: Channel Control/Status Register

BIT	FUNCTION
0 Status Bit	0 = FIFO is not almost empty 1 = FIFO is almost empty. This bit is set to a logic 1 when the channel's FIFO contains less than or equal to the number of data samples set by the threshold bits (6 and 5).
2, 1	00 = Conversions are disabled. 01 = Enable Single Conversion Mode. A single conversion is initiated per software start convert or external trigger. The internal channel timer has no function in this mode of operation. 10 = Enable Continuous Conversion Mode. Conversions are initiated by a software start convert or external trigger and continued by internal hardware triggers generated at the frequency set by the interval timer registers. 11 = External Trigger Input Mode. Conversions are initiated only by external triggers in this mode of operation. The software start convert and internal hardware generated triggers do not initiate conversions in this mode of operation.
3	0 = External Trigger Set as Input 1 = External Trigger Set as Output. As an output Internal Timer triggers are driven on the External trigger pin of the field I/O connector. It is possible to synchronize the conversion of multiple IP236A modules. A single master IP236A must be selected to output the external trigger signal while all other modules are selected to input the external trigger signal. The external trigger signals (pins 49 to 42 of the field I/O connector) of all modules must be wired together for all channels/modules to be synchronized. The External Trigger input can be sensitive to external EMI noise which can cause erroneous external triggers. If External Trigger Inputs are not required, the External Trigger should be configured as an output.
4	0 = Disable Interrupt 1 = Enable Interrupt An interrupt request from the IP236A will be issued to the system if enabled via this bit and the FIFO has equal to or less than the threshold number of bytes selected via bits 6 and 5. The interrupt request will remain active until the interrupt condition is removed by writing new data to the FIFO buffer (thus moving the number of values above the set threshold) or by disabling interrupts via this bit.
6, 5	FIFO Interrupt Threshold 00 = Disabled no Threshold Set 01 = Threshold of 4 samples selected. 10 = Threshold of 16 samples selected. 11 = Threshold of 64 samples selected. When the data samples in the corresponding FIFO is equal to or falls below the selected threshold an interrupt request can be issued and the FIFO Almost Empty bit-0 of this register will be set. Note: Interrupts must also be enabled on the carrier and via bit 4 of this register.
7	Not Used

Channel Timer Prescaler Register (Read/Write)

The Channel Timer Prescaler register is an 8-bit register that can be written with an 8-bit or 16-bit data transfer to control the interval time between conversions.

Timer Prescaler Register							
MSB			Data Bus				LSB
15	14	13	12	11	10	09	08
MSB			Timer Prescaler Value				LSB
07	06	05	04	03	02	01	00

This 8-bit number divides the 8 MHz clock signal. The clock signal is further divided by the number held in the Conversion Timer Register. The resulting frequency can be used to generate periodic triggers for precisely timed intervals between conversions.

The Timer Prescaler has a minimum allowed value restriction of 35 hex or 53 decimal. A Timer Prescaler value of less then 53 (decimal) will result in unpredictable operation. This minimum value corresponds to a conversion interval of 6.625μ seconds which translates to the maximum conversion rate of about 150KHz. Although the board will operate at the 150KHz conversion rate, conversion accuracy will be sacrificed. To achieve specified conversion accuracy a maximum conversion rate of 100KHz is recommended (see the specification chapter for details regarding accuracy).

The formula used to calculate and determine the desired Timer Prescaler value is given in the Conversion Timer section which immediately follows.

Reading or writing to this register is possible via 16-bit or 8-bit data transfers. The Timer Prescaler register contents are cleared upon reset.

Channel Conversion Timer Register (Read/Write)

Each channel has its own dedicated Timer Prescaler and Conversion Timer pair. The value stored in the Conversion Timer Register controls the interval time between conversions in conjunction with the value stored in the Timer Prescaler register. Read or writing the Conversion Timer register is possible with either 16-bit or 8-bit data transfers. This register's contents are cleared upon reset.

Conversion Timer Register	
MSB	LSB
15 14 13 12 11 10 09 08	07 06 05 04 03 02 01 00

This 16-bit number is the second divisor of the 8MHz clock signal and is used together with the Timer Prescaler Register to derive the frequency of periodic triggers for precisely timed intervals between conversions.

The interval time between conversion triggers is generated by cascading two counters. The first counter, the Timer Prescaler, is clocked by the 8MHz clock signal. The output of this clock is input to the second counter, the Conversion Timer, whose output is used to generate periodic trigger pulses. The time period between trigger pulses is described by the following equation:

$$\frac{\text{Timer Prescaler} * \text{Conversion Timer}}{8} = \text{T in } \mu \text{ seconds}$$

Where: **T** = time period between trigger pulses in microseconds.
Timer Prescaler can be any value between 53 and 255 decimal.
Conversion Timer can be any value between 1 and 65,535 decimal.

The maximum period of time which can be programmed to occur between conversions is (255 * 65,535) ÷ 8 = 2.0889 seconds. The minimum time interval which can be programmed to occur is (53 * 1) ÷ 8 = 6.625μ seconds. This minimum of 6.625μ seconds is defined by the minimum conversion time of the hardware but does sacrifice conversion accuracy. To achieve specified conversion accuracy a minimum conversion time of 10μ seconds is recommended (see the specification chapter for details regarding accuracy).

Channel FIFO Buffer Port (Write Only)

Each channel has its own dedicated 128 sample deep FIFO buffer. The FIFO samples are 16-bit data values. Writing to the FIFO is possible via 16-bit data transfers only.

Care should be taken when writing data to the FIFO buffer to insure the FIFO is not full when a new write is initiated. The IP236A will not acknowledge data written to the FIFO after it contains the maximum of 128 samples. In some systems this will result in a system bus error. The FIFO Full flag bit can be read prior to writing the FIFO to avoid this error.

New FIFO locations are available after data transfers to its corresponding DAC are initiated. In addition, the FIFO can be cleared by implementing a software or hardware reset.

It is recommended that interrupts be enabled for a FIFO almost empty condition (64, 16, or 4 samples or less left in the FIFO). .Upon this interrupt no more then 128 samples minus the threshold value (64, 16, or 4) should be written to the FIFO.

Write accesses to this register typically require two wait states and can be a maximum of 4 wait states when the write overlaps with a FIFO read for DAC update. The FIFO read operation will wait for a previously started FIFO write operation without causing the FIFO write to take more than the typical two wait states. The FIFO read will commence immediately after the write has completed. If a new write is required immediately after the previous write then this new write will be implemented with 4 wait states.

A software or hardware reset will clear the FIFO contents.

DAC MODES OF CONVERSION

The IP236A provides three methods of analog output operation for maximum flexibility with different applications. The following sections describe the features of each method and how to best use them.

Single Conversion from FIFO Buffer

In Single Conversion mode of operation, one value is moved from its corresponding FIFO buffer to its corresponding DAC. With each conversion, initiated by a software or external trigger, a new data value is read from the FIFO and is used to update the DAC analog output.

To select this mode of operation bits 2 and 1 of the Channel Control register must be set to digital code "01". Then, issuing a software start convert or external trigger will initiate the read of the FIFO buffer for update of the corresponding channel's DAC. The interval timer is not used in this mode of operation.

Continuous Conversions from FIFO Buffer

In the Continuous Conversion mode of operation, the hardware controls the continuous shifting through the FIFO buffer for the given channel. Digital data from the given channel's corresponding FIFO buffer is output to the converter at the rate specified by the interval timer (Timer Prescaler and Conversion Counter). This mode of operation is ideal for waveform generation.

To initiate this mode of operation bits 2 and 1 of the Channel Control register must be set to digital code "10". Then, issuing a software start convert or external trigger will initiate the continuous update of the selected channel.

The interrupt capability of the IP236A can be employed as a means to indicate to the system that the 128 sample FIFO is reduced down to 64, 16, or 4 samples (depending on the threshold selected) and must be loaded with additional values.

Alternatively, a polling method could be used. The FIFO almost empty bit in the channel's Status register is polled and when set the FIFO can be reloaded with new data.

Convert On External Trigger Only

When bit-2 and 1 of the control register are set to digital code "11", each conversion is initiated by an external trigger only (logic low pulse) input to the EXT TRIGGER* signal of the P2

connector. Conversions are performed for the corresponding channel, independent of all other channels, with each external trigger pulse. The interval between conversions is controlled by the period between external triggers. The interval timer has no functionality in this mode of operation.

Note that the external trigger signal must be configured as an input for this mode of operation. Bit-3 of the Channel Control register must be set to a logic "0".

External Trigger Only mode of operation can be used to synchronize multiple IP236A modules to a single module running in a continuous conversion mode. The external trigger, of the IP236A "master", must be programmed as an output. The external trigger signal of that IP236A must then be connected to the external trigger signal of all other IP236A modules, programmed for external trigger input, that are to be synchronized. These other IP236A modules must be programmed for External Trigger Input only mode. Data conversion can then be started by writing high to the Start Convert bit of the master IP236A configured for continuous conversion mode.

PROGRAMMING CONSIDERATIONS

The IP236A provides different methods of analog output generation to give the user maximum flexibility for each application. Examples are presented in the following sections to illustrate programming the different modes of operation.

Single Conversion Mode Example

This example will enable channel 0 for the single conversion mode of operation. The conversion can be initiated via software or external trigger.

1. Execute Write of 0002H to the Control Register at Base Address + 08H.
   a) Single Conversion from FIFO buffer is enabled.
   b) External, and Software generated triggers are enabled.
2. Execute Write of 7FFFH to the FIFO buffer port at Base Address + 0CH. This will drive channel zero's analog output to plus full scale minus one least significant bit.
3. Execute Write 0001H to the Start Convert Bit at Base Address + 00H. This starts the transfer of the digital data in channel zero's FIFO buffer to its corresponding converter for analog conversion.

Continuous Conversion Mode with Interrupt Example

This example will enable channel 7 for continuous conversion mode of operation. Interrupts are enabled and an interrupt threshold of 16 samples is enabled. The interval timer will be set for an 80μ second interval. The conversions can be initiated via software or external trigger.

This example assumes that the IP236A is installed onto an Acromag AVME9630/60 carrier board (consult your carrier board documentation for compatibility details).

1. Clear the global interrupt enable bit in the carrier board status register by writing a "0" to bit 3.

2. Write the interrupt vector to the IP236A Module at base address + 03H.

3. Write to the carrier board interrupt Level Register to program the desired interrupt level per bits 2,1, & 0.

4. Write "1" to the carrier board IP Interrupt Clear Register corresponding to the desired IP interrupt request being configured.

5. Write "1" to the carrier board IP Interrupt Enable Register bit corresponding to the IP interrupt request to be enabled.

6. Enable interrupts for the carrier board by writing a "1" to bit 3 (the Global Interrupt Enable Bit) of the carrier board's Status Register.

7. Execute Write of 54H to the Channel Control Register at Base Address + 33H.
   a) Continuous Conversion mode is selected.
   b) External, Software, and Hardware timer generated triggers are all enabled.
   c) Interrupts are enabled.
   d) Interrupt when 16 or less values remain in the FIFO buffer.

8. Execute Write of 50H to Timer Prescaler Register at Base Address + 32H.
   a) This sets the Timer Prescaler to 80 decimal.

9. Execute Write of 0008H to the Conversion Timer Register at Base Address + 34H. The conversion timer in conjunction with the Timer Prescaler sets the interval time between conversions to $(80 * 8) \div 8 = 80\mu$ seconds.

10. Execute Write of 8000H to the FIFO buffer port at Base Address + 36H. Channel 7's first FIFO location is written with digital value 8000H. This digital value will provide a minus full scale analog output when converted. Continue to fill the FIFO with 127 additional values.

11. Execute Write of 0080H to the Start Convert Bit at Base Address + 00H. This starts the transfer of data from channel seven's FIFO buffer to its corresponding DAC for analog conversions. Conversions will continue with interrupt request when 16 or fewer samples reside in the FIFO buffer.

General Sequence of Events for Processing an Interrupt

1. The IP236A asserts the Interrupt Request 0 Line (INTREQ0*) in response to an interrupt condition.
2. The AVME9630/60 carrier board acts as an interrupter in making the VMEbus interrupt request (IRQx*) corresponding to the IP interrupt request.
3. The VMEbus host (interrupt handler) asserts IACK* and the level of the interrupt it is seeking on A01-A03.
4. When the asserted VMEbus IACKIN* signal (daisy-chained) is passed to the AVME9630/60, the carrier board will check if the level requested matches that specified by the host. If it matches, the carrier board will assert the INTSEL* line to the appropriate IP together with (carrier board generated) address bit A1 to select which interrupt request is being processed (A1 low corresponds to INTREQ0*).
5. The IP236A puts the interrupt vector on the local data bus (D00-D07 for the D08 [O] interrupter) and asserts ACK* to the carrier board. The carrier board passes this along to the VMEbus (D08[O]) and asserts DTACK*.

6. The host uses the vector to form a pointer to an interrupt service routine for the interrupt handler to begin execution.
7. Example of Generic Interrupt Handler Actions:
   a) Disable the interrupting IP by writing “0” to the appropriate bit in the AVME9630/60 IP Interrupt Enable Register.
   b) Service the interrupt.
   c) Clear the interrupting IP by writing a “1” to the appropriate bit in the AVME9630/60 IP Interrupt Clear register.
   d) Enable the interrupting IP by writing “1” to the appropriate bit in the AVME9630/60 IP Interrupt Enable Register.

USE OF CALIBRATION DATA

Calibration data is provided in the form of calibration coefficients, so the user can adjust and improve the accuracy of the analog output voltage over the uncalibrated state. Each channel's unique offset and gain calibration coefficients are stored in memory. The use of software calibration allows the elimination of hardware calibration potentiometers traditionally used in producing precision analog outputs.

Software calibration uses some fairly complex equations. **Acromag provides you with the Industrial I/O Pack Software Library diskette to make communication with the board and calibration easy. It relieves you from having to turn the equations of the following sections into debugged software calibration code.** The functions are written in the “C” programming language and can be linked into your application. Refer to the “README.TXT” file in the root directory and the “INFO236.TXT” file in the “IP236A” subdirectory on the diskette for details.

Uncalibrated Performance

The uncalibrated performance is affected by two primary error sources. These are the channel's offset and gain errors. The use of channel specific calibration coefficients to accurately adjust offset and gain is important because the worst case uncalibrated error can be significant (although the typical uncalibrated errors observed may be much less). See the specification chapter for details regarding maximum uncalibrated error.

Calibrated Performance

Accurate calibration of the IP236A can be accomplished through software control by using calibration coefficients to adjust the analog output voltage. Unique calibration coefficients are stored in memory as (1/4 LSB’s) for each channel. Once retrieved, the channel's unique offset and gain coefficients can be used to correct the data value sent to the DAC channel to accurately generate the desired output voltage. See the specification chapter for details regarding maximum calibrated error.

Data is corrected using a couple of formulas. Equation (1) expresses the ideal relationship between the value (Ideal_count) written to the 16-bit DAC to achieve a specified voltage within the selected output range.

Equation (1):

$$\text{Ideal\_Count} = \left[\frac{\text{Count\_Span} * \text{Desired\_Voltage}}{\text{Ideal\_Volt\_Span}} \right]$$

where,
Count_Span = 65,536 (a 16-bit converter has 2^{16} possible levels)
Ideal_Volt_Span = 20 Volts (for the bipolar ±10 Volt range)
= 10 Volts (for the bipolar ±5 or unipolar 0 to 10 volt ranges).

Using equation (1), one can determine the ideal count for any desired voltage within the range. For example, if it is desired to output a voltage of +5 Volts for the bipolar ±10 volt range, the Ideal_Count of 16,384 results. If this value is used to program the DAC output, the output value will approach +5 Volts to within the uncalibrated error. This will be acceptable for some applications.

For applications needing better accuracy, the software calibration coefficients should be used to correct the Ideal_Count into the Corrected_Count required to accurately produce the output voltage. This is illustrated in the next equation.

Equation (2):

$$\text{Corrected\_Count} = \text{Ideal\_Count} * \left[1 + \text{Gain\_Correction} \right] + \text{Offset\_Correction} + \text{Ideal\_Zero\_Count}$$

where,
Gain_Correction = Stored_Gain_Error / (4*65,536)
Offset_Correction = Stored_Offset_Error / 4
Ideal_Zero_Count = 0 for bipolar ±5 and ±10 volt ranges
32,768 for unipolar 0 to 10 volt range

Ideal_Count is determined from equation (1) given above. Stored_Gain_Error and Stored_Offset_Error are written at the factory and are obtained from memory on the IP236A on a per channel basis. The Stored_Gain_Error and Stored_Offset_Error are stored in memory as two’s complement numbers. Refer to the “Calibration Coefficient Access Register” section for details on how to read the coefficients from memory.

Using equation (2), you can determine the corrected count from the ideal count. For the previous example, equation (1) returned a result 16,384 for the Ideal_Count to produce an output of +5 Volts. Assuming that a gain error of -185 and an offset error of -43 are read from memory on the IP236A for the desired channel, substitution into equation (2) yields:

$$\text{Corrected\_Count} = 16{,}384 * \left[1 + \frac{-185}{4*65536} \right] - \frac{43}{4} = 16{,}361.6875$$

If this value (rounded to 16,362) is used to program the DAC output, the output value will approach +5 Volts to within the calibrated error (see the specification chapter for details regarding maximum calibrated error).

Calibration Programming Example

Assume it is necessary to program channel 0 with an output of -2.5 Volts. Also assume the bipolar range centered around 0 Volts is -10 to +10 Volts.

The Single Conversion mode of operation is used in this example.

1. Execute Write of 02H to Channel Control Register at Base Address + 09H.
   a) External, and Software triggers are enabled.
   b) Single Conversion mode is enabled.

2. Read the calibration memory to retrieve channel 0's unique offset coefficient. To obtain the 16-bit offset coefficient, two read accesses of the coefficient memory are required. To initiate a read of channel 0's most significant byte of the offset coefficient, the Calibration Coefficient Access register must be written with data value 8000H at Base Address + 04H. The offset coefficient can be read by polling the Calibration Coefficient Status register. When bit 0 of the Calibration Coefficient Status register is set to logic high, then the data on bits 15 to 8 contain the most significant byte of the offset coefficient.

To initiate a read of channel 0's least significant byte of the offset coefficient, the Calibration Coefficient Access register must be written with data value 8100H at Base Address + 04H. When bit 0 of the Calibration Coefficient Status register is set to logic high, then the data on bits 15 to 8 of this register contains the least significant byte of the offset coefficient.

3. Read the calibration memory to retrieve channel 0's unique 16-bit gain coefficient. To obtain the 16-bit gain coefficient, two read accesses of the coefficient memory are required. To initiate a read of channel 0's most significant byte of the gain coefficient, the Calibration Coefficient Access register must be written with data value 8200H at Base Address + 04H. The gain coefficient can be read by polling the Calibration Coefficient Status register. When bit 0 of the Calibration Coefficient Status register is set to logic high, then the data on bits 15 to 8 contains the most significant byte of the gain coefficient.

To initiate a read of channel 0's least significant byte of the gain coefficient, the Calibration Coefficient Access register must be written with data value 8300H at Base Address + 04H. When bit 0 of the Calibration Coefficient Status register is set to logic high, then the data on bits 15 to 8 of this register contains the least significant byte of the gain coefficient.

4. Calculate the Ideal_Count required to provide an uncorrected output of the desired value (-2.5 Volts) by using equation (1). **Ideal_Count =** [65,536×(-2.5)]/20 = -8,192.0

5. Calculate the Corrected_Count required to provide an accurate output of the desired value (-2.5 Volts) by using equation (2). Assume the offset and gain coefficients are -43 and -185 respectively.
   Corrected_Count = -8,192.0×[1 + -185/(4×65,536)] - 43/4 = -8,196.9687. This value is rounded to -8,197 and is equivalent to DFFB hex as a 2's complement value.

6. Execute Write of DFFB hex to the Channel 0's FIFO Buffer port at Base Address + 0CH.

7. Execute Write of 0001H to the Start Convert Bit at Base Address + 00H. This starts the transfer of the digital data in Channel 0's FIFO buffer to its corresponding DAC for analog conversions. This will drive channel 0's analog output to -2.5 volts.

8. (OPTIONAL) Observe or monitor that the specific DAC channel (0) reflects the results of the digital data converted to an analog output voltage at the field connector.

Error checking should be performed on the calculated count values to insure that calculated values below 0 or above 65535 decimal are restricted to those end points. Note that the software calibration cannot generate outputs near the endpoints of the range which are clipped off due to hardware limitations(i.e. the DAC).

4.0 THEORY OF OPERATION

This section contains information regarding the hardware of the IP236A. A description of the basic functionality of the circuitry used on the board is also provided. Refer to the Block Diagram shown in Drawing 4501-736 as you review this material.

FIELD ANALOG OUTPUTS

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.3). **Field I/O signals are NON-ISOLATED.** This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring ground loops may cause operation errors, and with extreme abuse, possible circuit damage. Refer to Drawing 4501-737 for example wiring and grounding connections.

Jumpers on the board control the range selection for the DACs (-5 to +5, -10 to +10, and 0 to 10 Volts) as detailed in chapter 2. Jumper selection should be made prior to powering the unit. Channels may use different ranges.

LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1 (refer to Table 2.4). The P1 interface also provides +5V and ±12V power to the module. Note that the DMA control, INTREQ1∗, ERROR∗, and STROBE∗ signals are not used.

A Field Programmable Gate-Array (FPGA) installed on the IP Module provides an interface to the carrier board per IP Module specification ANSI/VITA 4 1995. The interface to the carrier board allows complete control of all IP236A functions.

IP INTERFACE LOGIC

IP interface logic of the IP236A is imbedded within the FPGA. This logic includes: address decoding, I/O and ID read/write control circuitry, and ID storage implementation.

Address decoding of the six IP address signals A(1:6) is implemented in the FPGA, in conjunction with the IP select signals, to identify access to the IP module's ID or I/O space. In addition, the byte strobes BS0∗ and BS1∗ are decoded to identify low byte, high byte, or double byte data transfers.

The carrier to IP module interface implements access to both ID and I/O space via 16 or 8-bit data transfers. Read only access

to ID space provides the identification for the individual module (as given in Table 3.1) per the IP specification. Read and write accesses to the I/O space provide a means to control the IP236A.

Access to both ID and I/O spaces are implemented with zero wait states read or write data transfers, except for write access to the FIFO buffers. Write cycles to the FIFO buffers requires two wait states typically and four wait states worst case.

Four wait state writes to the FIFO buffers will only be implemented when the write overlaps with a FIFO read for DAC update. The FIFO read operation will wait for a previously started FIFO write operation without causing the FIFO write to take more than the typical two wait states. The FIFO read will commence immediately after the write has completed. If a new write is required immediately after the previous write then this new write will be implemented with 4 wait states.

CONVERSION CONTROL LOGIC

All logic to control data conversions is imbedded in the IP module's FPGA. The control logic of the IP236A is responsible for controlling the user specified mode of operation. Once the IP module has been configured, the control logic performs the following:

- Controls serial transfer of data from the FPGA to the corresponding DAC register based on the selected mode of operation.
- Provides external or internal trigger control.
- Controls read and write access to calibration memory.
- Controls issue of interrupt requests to the carrier.
- Provides status on FIFO Full or Almost Empty conditions.

DATA TRANSFER FROM FPGA TO DACs

A 16-bit serial shift register is implemented in the IP module's FPGA for each of the supported channels. Internal FPGA counters are used to synchronize the transfer of FIFO data to the corresponding serial shift register for output to its converter.

INTERVAL TIMER

Each channel of the IP236A has its own dedicated interval timer logic. The DAC update interval maybe controlled by the interval timer, which is a 24-bit counter implemented in the FPGA. The timer is implemented via two programmable counters: an 8-bit Timer Prescaler and a 16-bit Conversion Timer. The Timer Prescaler is clocked by the 8MHz board clock. The output of the Timer Prescaler is then used to clock the Conversion Timer. In this way, the two counters are cascaded to provide variable time periods anywhere from 6.6μ seconds to 2.0889 seconds. The output of this interval counter is used to trigger the start of new conversions. Triggers generated by the interval counter are also referenced as hardware timer generated triggers in chapter 3 of this manual.

EXTERNAL TRIGGER

The external trigger connections are made via pins 42 to 49 of the P2 Field I/O Connector. For all modes of operation, when the external trigger input is enabled via bit 3 of the channel's control register, the falling edge of the external trigger will initiate conversions for the corresponding channel. For External Trigger Input mode (bit 3 set to digital value "0"), each falling edge of the external trigger causes a conversion at the DAC. Once the external trigger signal has been driven low, it should remain low for a minimum of 250n seconds for proper external trigger operation. The external trigger input signals must be TTL compatible. The IP236A uses a diode clamping circuit to protect the board from external trigger signals that violate the 5 volt logic (TTL) requirement.

As an output, an active-low TTL signal is driven from the IP236A. The trigger pulse generated is low for 500n seconds typically. See section 3.0 for programming details to make use of this signal.

INTERRUPT CONTROL LOGIC

The IP236A can be configured to generate an interrupt on a programmable FIFO Almost Empty status. When the FIFO has 64, 16, or 4 samples or less left (user programmable) the IP interrupt signal INTREQ0* is issued to the carrier to request an interrupt. An 8-bit interrupt service routine vector is provided during an interrupt acknowledge cycle on data lines D0 to D7. The interrupt is released when the FIFO is no longer almost empty or if interrupts are disabled.

CALIBRATION MEMORY CONTROL LOGIC

The FPGA of the IP236A module contains control logic that implements read and write access to calibration memory. The calibration memory (EEPROM) contains offset and gain coefficients for each of the ranges and channels. Calibration of the individual DACs is implemented via software to avoid the mechanical drawbacks of hardware potentiometers.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Application Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

PHYSICAL

Physical Configuration……..Single Industrial Pack Module.
Length.....3.880 in. (98.5 mm).
Width.....1.780 in. (45.2 mm).
Board Thickness.....0.062 in. (1.59 mm).
Max Component Height.....0.290 in. (7.37 mm).
Connectors:
P1 (IP Logic Interface).....50-pin female receptacle header (AMP 173279-3 or equivalent).
P2 (Field I/O).....50-pin female receptacle header (AMP 173279-3 or equivalent).

Power: Maximum VCC rise time ……..100m Seconds

Power Requirements		IP236A -8/8E
5V (±5%)	Typical	92mA
	Max.	120mA
+12V (±5%)	Typical	130mA
	Max.	170mA
-12V (±5%)	Typical	160mA
	Max.	210mA

ENVIRONMENTAL

Operating Temperature.....Standard Unit 0 to +70°C.
"E" suffixed units -40°C to +85°C.

Note: The extended temperature grade version of the DAC714 is no longer available from the manufacturer. Acromag has performed operational tests of sampled commercial grade components over the extended temperature range without failure. All DAC714s' used on the -E version of the IP236A have been functionally tested by an independent third party laboratory for use in extended temperature applications, except for verification of analog output specifications.

Relative Humidity.....5-95% Non-Condensing.
Storage Temperature.....-55°C to 125°C.

Non-Isolated.....Logic and field commons have a direct electrical connection.

Radiated Field Immunity (RFI)..Designed to comply with IEC1000-4-3 Level 3 (10V/m, 80 to 1000MHz AM & 900MHz. keyed) and European Norm EN50082-1 with error less than ±0.25% of FSR.

Electromagnetic Interference Immunity (EMI)…….Error is less than ±0.25% of FSR under the influence of EMI from switching solenoids, commutator motors, and drill motors.

Electrostatic Discharge (ESD) Immunity……..Complies with IEC1000-4-2, Level 3 (8KV/4KV air/direct discharge) to the enclosure port and European Norm EN50082-1.

Surge Immunity……Not required for signal I/O per European Norm EN50082-1.

Electric Fast Transient Immunity EFT…….. Complies with IEC1000-4-4 Level 2 (0.5KV at field input and output terminals) and European Norm EN50082-1.

Radiated Emissions……..... Meets or exceeds European Norm EN50081-1 for class A equipment.

Warning: This is a class A product. In a domestic environment this product may cause radio interference in which the user may be required to take adequate measures.

Note:
1. Reference Test Conditions: All output ranges, Temperature 25°C, 100K conversions/second, using Acromag's AVME9660 VMEbus IP carrier with a 1 meter shielded cable length connection to the field analog output signals unloaded.

ANALOG OUTPUTS

Output Channels……. IP236A-8 Eight Independent Single Ended Channels

Output Signal Type..... Voltage (Non-isolated).
Output Ranges[2]…….. Bipolar -5 to +5 Volts
(Jumper Selected) Bipolar -10 to +10 Volts
Unipolar 0 to +10 Volts

Note:
2. The actual outputs may fall short of the range endpoints due to hardware offset and gain errors. The software calibration corrects for these across the output range, but cannot extend the output beyond that achievable with the hardware.

Output Current……. -5mA to +5mA (Maximum); this corresponds to a minimum load resistance of 2KΩ with a 10V output.
DAC Data Format…… Positive-true binary two's complement (BTC) input codes.
DAC Programming..... Independent; Input registers and FIFOs are directly loaded
Resolution..... 16-bits.
Monotonicity 14-bits (IP236A)
13-bits (IP236AE)
Linearity Error..... ± 4 LSB (Maximum).@ 25°C.
Differential Linearity Error..... ± 4 LSB (Maximum).@ 25°C.

Maximum Overall Calibrated Error[3].@ 25°C

Max. Linearity Error LSB	Max. Offset Error LSB	Max. Gain Error LSB	Max. Total Error LSB (%)
± 4	± 1	± 1	± 6 (0.0091)

Note:
3. Offset and gain calibration coefficients stored in the coefficient memory must be used to perform software calibration in order to achieve the specified accuracy. Specified accuracy does not include quantization error and are with outputs unloaded. Follow the output connection recommendations of Chapter 2, to keep non-ideal grounds from degrading overall system accuracy.

The maximum uncalibrated error combining the linearity, offset and gain errors is ± 0.461%.

DAC714P @ Tmin to Tmax:
Linearity Error is ± 0.011% maximum (i.e. ± 8 LSB).
Bipolar Offset Error is ± 0.2% FSR (i.e. 20V SPAN) max.
Gain Error is ± 0.25% maximum.

Settling Time..... 10uS to within 0.003% of FSR for a 20V step change (load of 5KΩ in parallel with 500pF).
Conversion Rate (per channel). 150KHz Maximum, 100KHz recommended for specified accuracy.
Output Noise……... 120 nV/√Hz typical
Output at Reset..... Bipolar Zero Volts.
Unipolar 5 Volts (See Note 5)
Board Warm-up Time..... 10 minutes minimum

Note:
5. The hardware reset function resets the DAC analog output and the FPGA's internal DAC FIFO buffer. The software reset will only clear the FPGA's internal DAC FIFO buffer. A software reset has no affect on the DAC analog output.

Output Impedence..... 0.1Ω Typical at 25°C
Short Circuit Protection ..... Indefinite at 25°C.
FIFO Buffer…….. 128 Samples per Channel
Interrupt……. Vectored interrupt on Almost Empty Condition.

External Trigger Input/Output

As An Input:.....…..…. Negative edge triggered. Must be an active low 5 volt logic TTL compatible, debounced signal referenced to digital common. Conversions are triggered within 6.4u seconds of the falling edge. Minimum pulse width is 250n seconds.
As An Output……..... Active low 5 volt logic TTL compatible output is generated. The trigger pulse is low for typically 500n seconds.

INDUSTRIAL I/O PACK COMPLIANCE

Specification……. This device meets or exceeds all written Industrial I/O Pack specifications per ANSI/VITA 4 1995 for 8MHz operation for Format I Modules.

Electrical/Mechanical
Interface……... Single-Size IP Module.

I/O Space Read/Write…..…... 16-bit, 8-bit:
ID Space Read.....…..…. 16-bit, 8-bit (low byte) Supports Type 1, 32 bytes per IP (consecutive odd byte addresses).
Memory Space..... Not Used.
Interrupts……..…… 8-bits (low byte) Generates INTREQ0* interrupt request per IP and interrupt acknowledge cycles via access to IP INT space.
Access Times (8MHz Clock):
ID Space Read.....……..…. 0 wait state (250ns cycle).
FIFO Buffer Write…..…….. 2 wait states typical (500ns), 5-wait states maximum (875ns)
Registers Read/Write…….. 0 wait state (250ns cycle).
Interrupt Read/Write…..…….. 0 wait states (250ns cycle).

APPENDIX

CABLE: MODEL 5025-550-x (Non-Shielded)
MODEL 5025-551-x (Shielded)

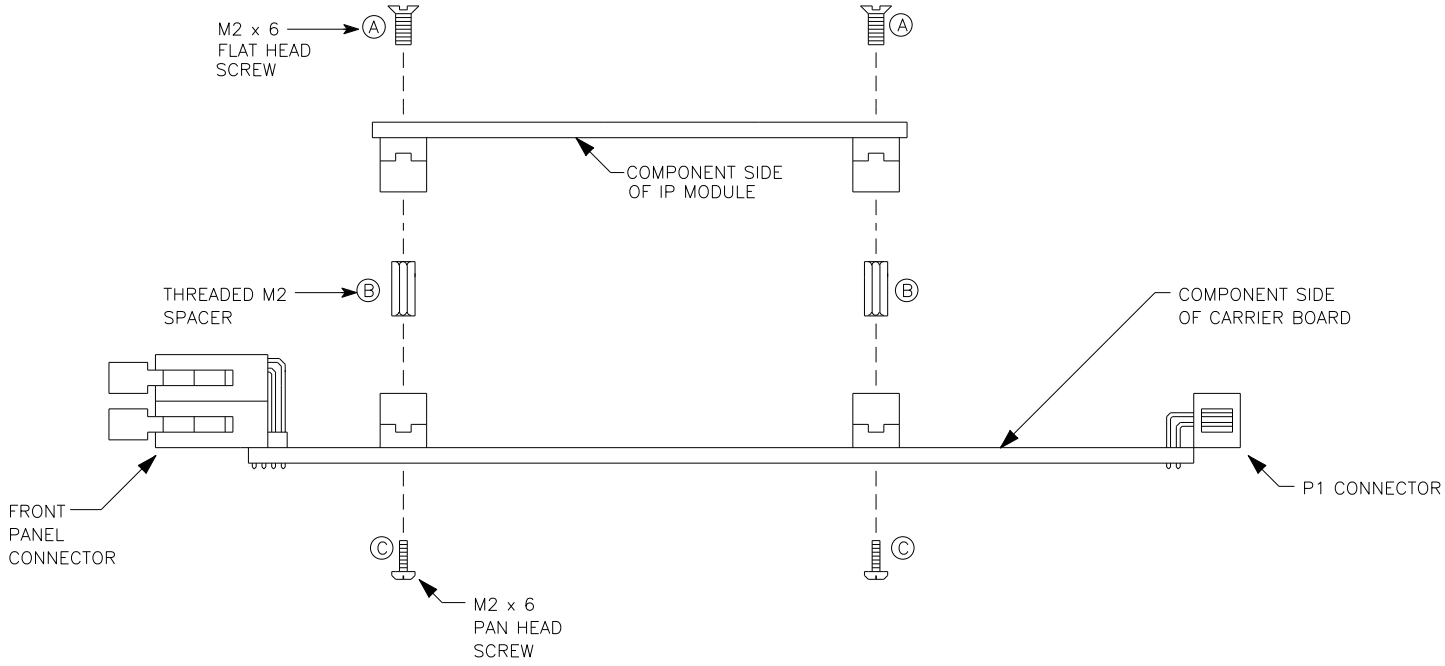
Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet (12 feet maximum). Choose shielded or unshielded cable according to model number. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.
Application: Used to connect a Model 5025-552 termination panel to the AVME9630/9660 non-intelligent carrier board A-D connectors (both have 50-pin connectors).
Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50-wire flat ribbon cable, 28 gage. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent). Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).
Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).
Keying: Headers at both ends have polarizing key to prevent improper installation.
Schematic and Physical Attributes: For Non-Shielded cable model, see Drawing 4501-462. For Shielded cable model, see Drawing 4501-463.
Shipping Weight: 1.0 pound (0.5Kg) packaged.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For AVME9630/9660, APC8610, or APC8620 Boards
Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660 3U/6U, APC8610, or APC8620 non-intelligent carrier boards (field connectors only) via a flat ribbon cable (Model 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Connections to AVME9630/9660, APC8610, or APC8620: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight : 1.25 pounds (0.6kg) packaged.

TRANSITION MODULE: MODEL TRANS-GP

Type: Transition module for AVME9630/9660 boards.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Schematic and Physical Attributes: See Drawing 4501-465.
Field Wiring: 100-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Printed Circuit Board: Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40 to +85°C.
Storage Temperature: -55°C to +105°C.
Shipping Weight: 1.25 pounds (0.6Kg) packaged.

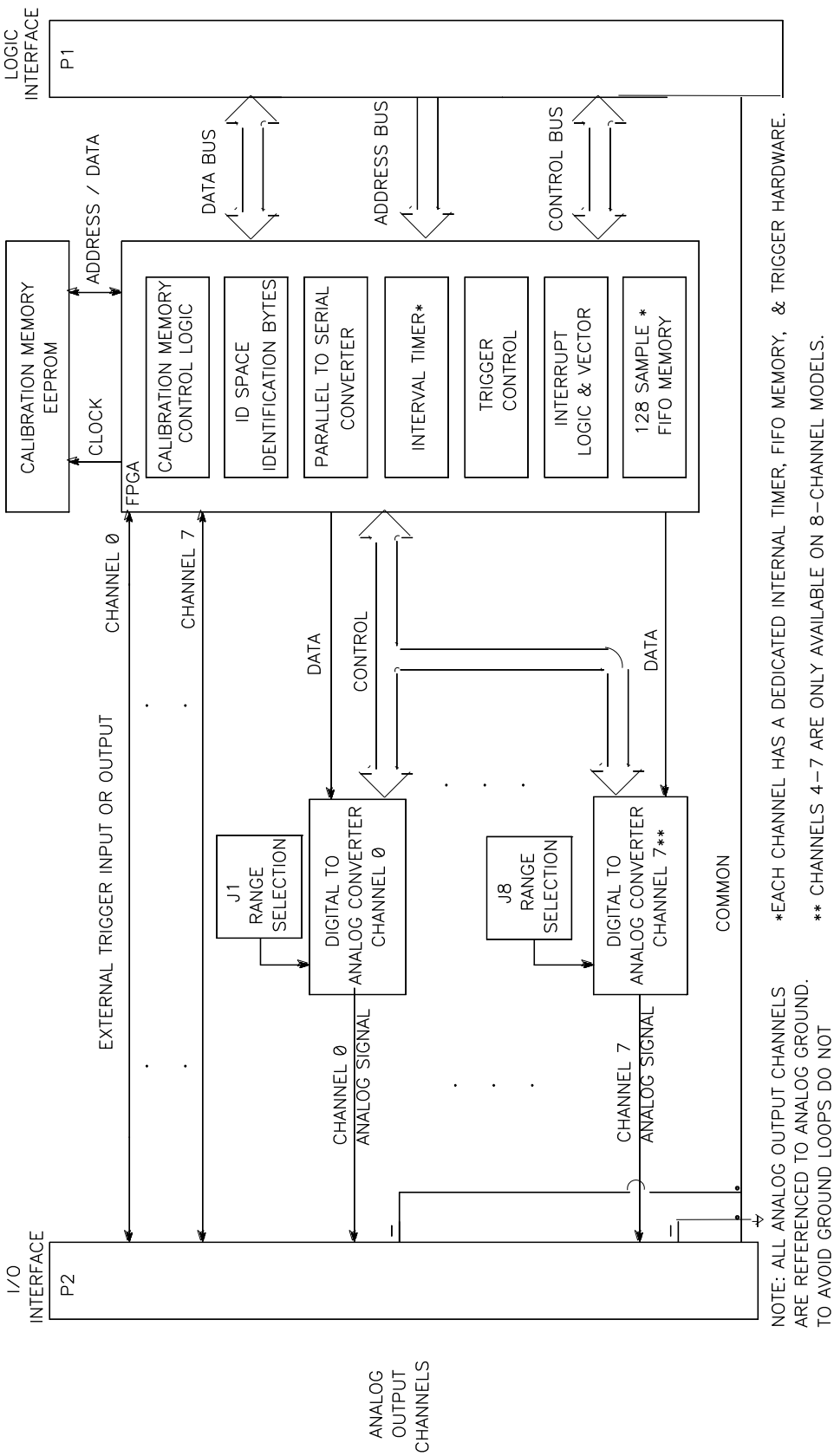


ASSEMBLY PROCEDURE:

1. THREADED SPACERS ARE PROVIDED FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED. THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES). THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.

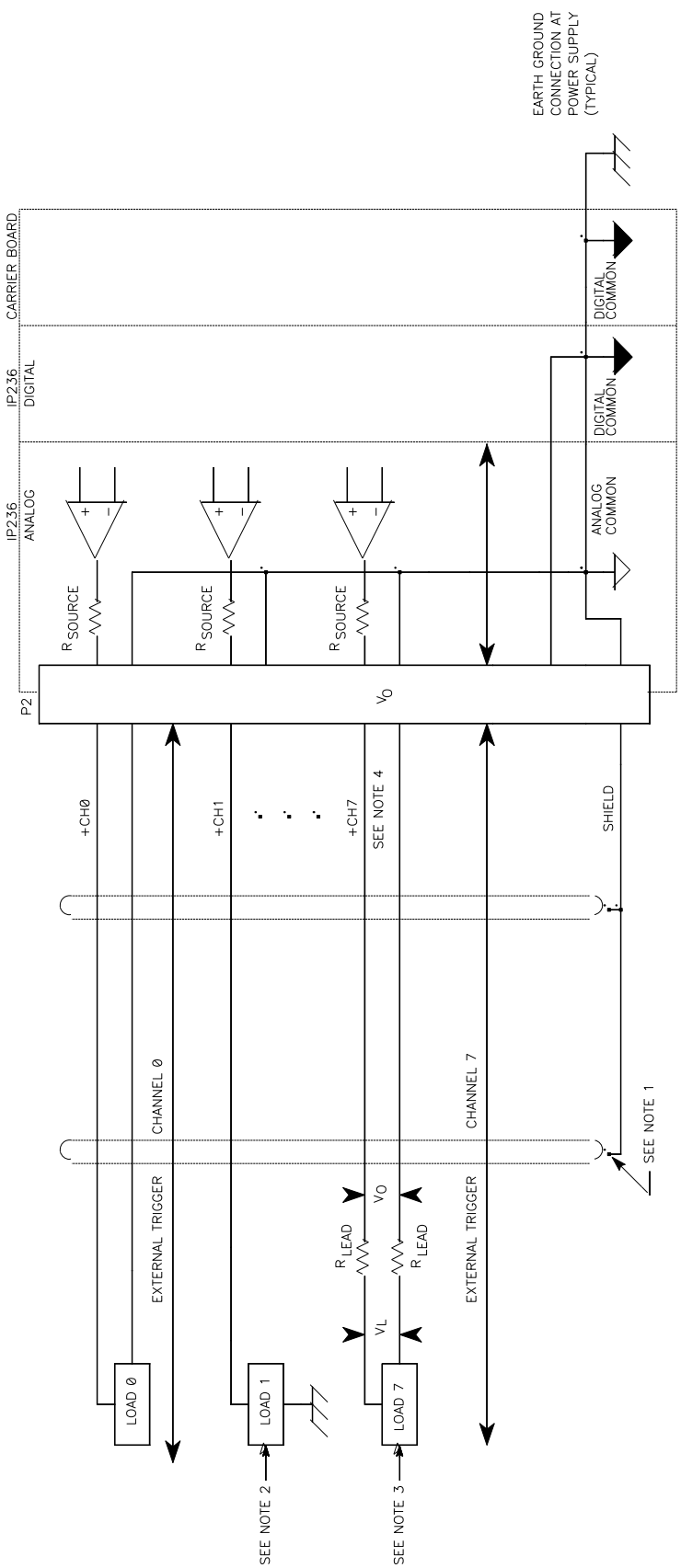
IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY

4501-434C



IP236 BLOCK DIAGRAM

4501-736A

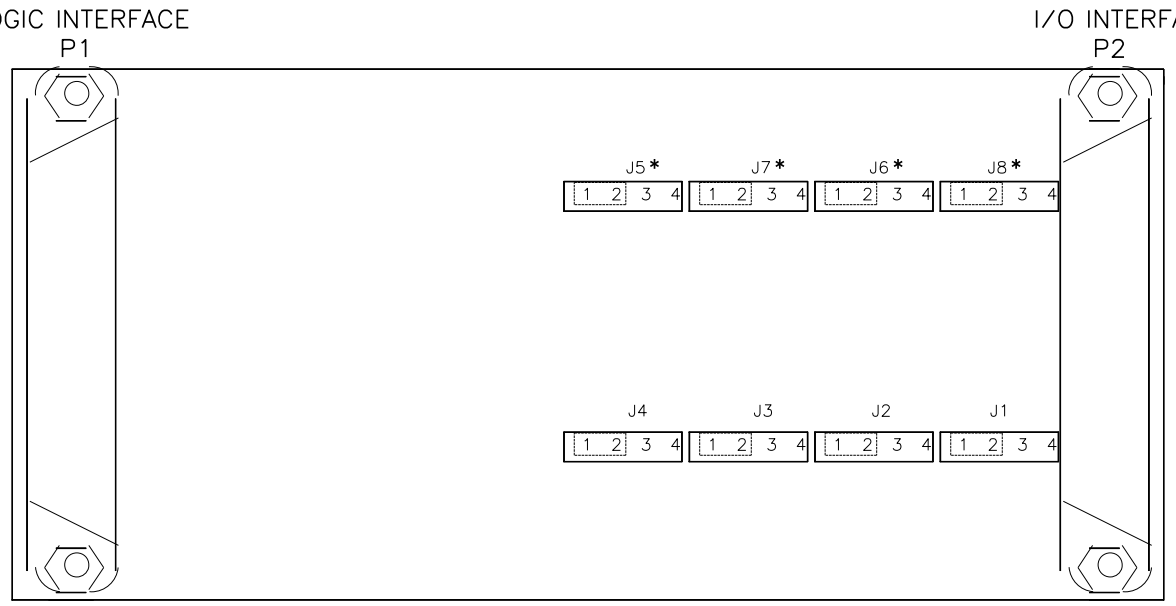


NOTES:

1. SHIELDED CABLE IS RECOMMENDED FOR LOWEST NOISE. SHIELD IS CONNECTED TO GROUND REFERENCE AT ONLY ONE END TO PROVIDE SHIELDING WITHOUT GROUND LOOPS.
2. ALL 8 CHANNELS ARE REFERENCED TO ANALOG COMMON AT THE IP236. TO AVOID GROUND LOOPS, DO NOT CONNECT GROUNDED CHANNELS TO THE NEGATIVE SIDE OF THE OUTPUT.
3. VL < VO DUE TO VOLTAGE DROPS ACROSS THE LEAD RESISTANCE OF THE WIRE. IT IS RECOMMENDED THAT A HIGH RESISTANCE LOAD WITH A SHORT WIRE RUN BE CONNECTED AT THE OUTPUT TO REDUCE THE EFFECTS OF LEAD AND SOURCE RESISTANCE VOLTAGE DROPS IN THE WIRE.
4. CHANNELS 4–7 ARE ONLY AVAILABLE ON 8–CHANNEL MODELS.

IP236 ANALOG OUTPUT CONNECTION DIAGRAM

4501–737A



COMPONENT SIDE VIEW

NOTE: DASHED LINES INSIDE JUMPER BLOCKS REPRESENT INSTALLED JUMPERS.

ANALOG OUTPUT RANGE SELECTION (JUMPER SETTINGS)

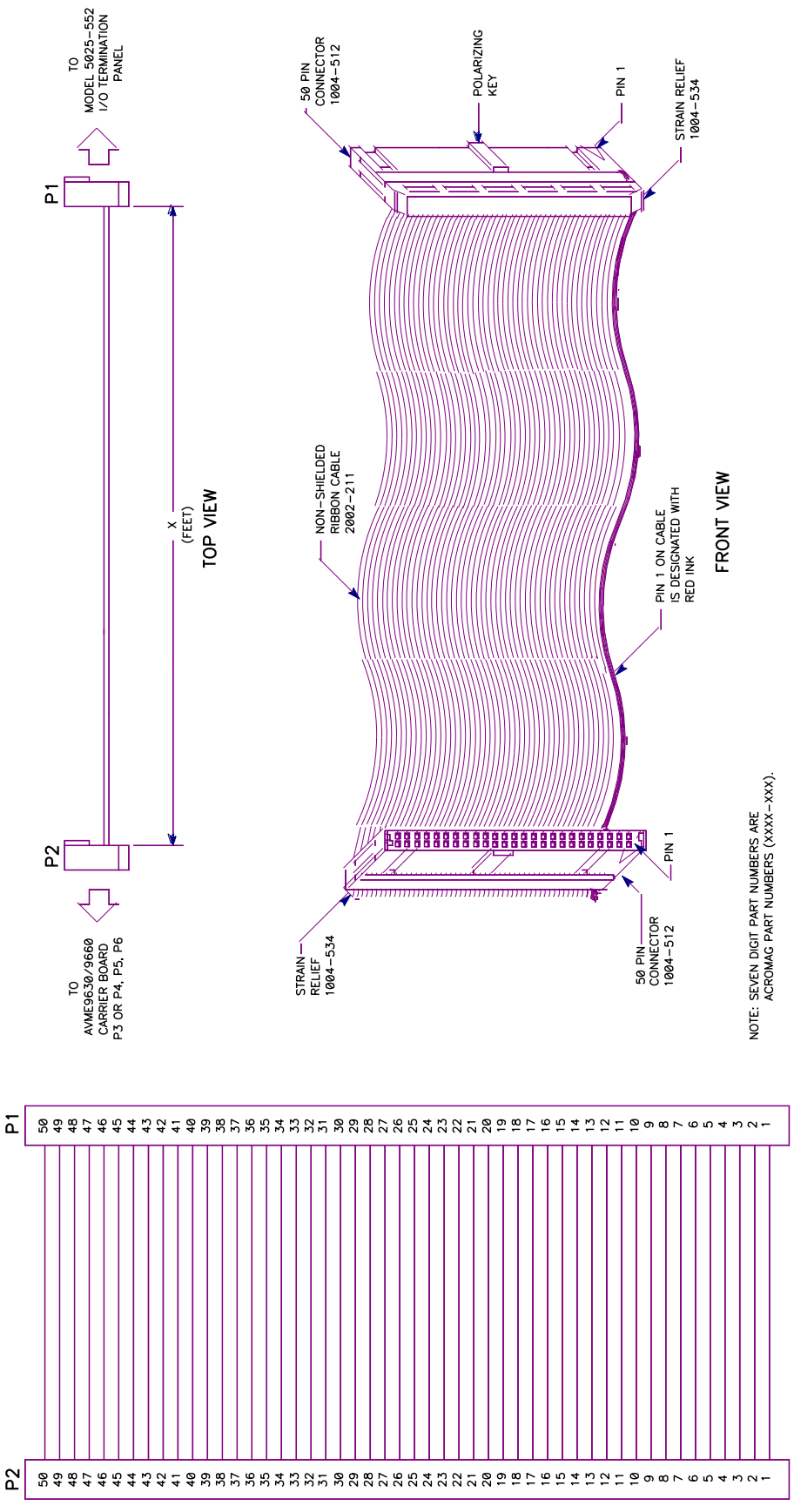
DESIRED ADC OUTPUT RANGE (VDC)	OUTPUT SPAN (VOLTS)	OUTPUT TYPE	J1 to J8 PINS (1&2)	J1 to J8 PINS (3&4)
−5 TO +5	10	Bipolar	ON	ON
−10 TO +10**	20	Bipolar	ON	OFF
0 TO +10	10	Unipolar	OFF	ON

* JUMPER BLOCKS NOT PRESENT ON THE IP236−4 MODEL.

** THE BOARD IS SHIPPED WITH THE DEFAULT JUMPER SETTING FOR THE −10 TO +10 VOLT DAC OUTPUT RANGE AS SHOWN IN THE ABOVE DIAGRAM.

4501−735A

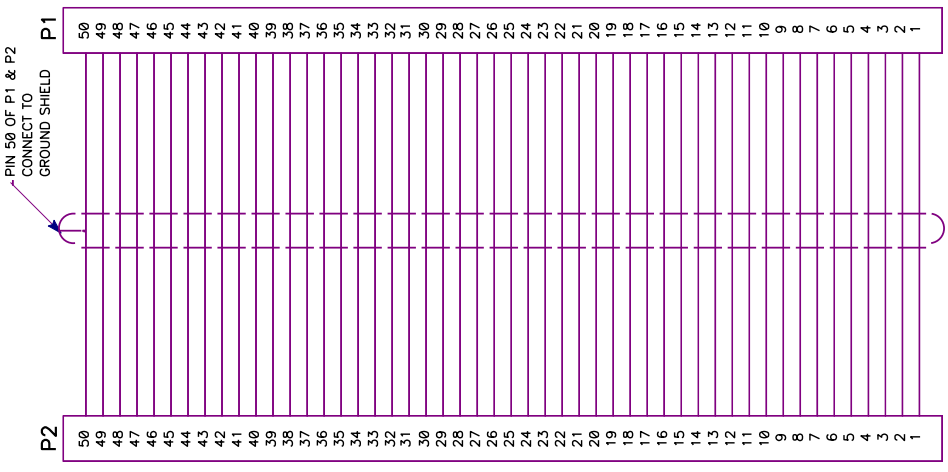
IP236 JUMPER LOCATIONS



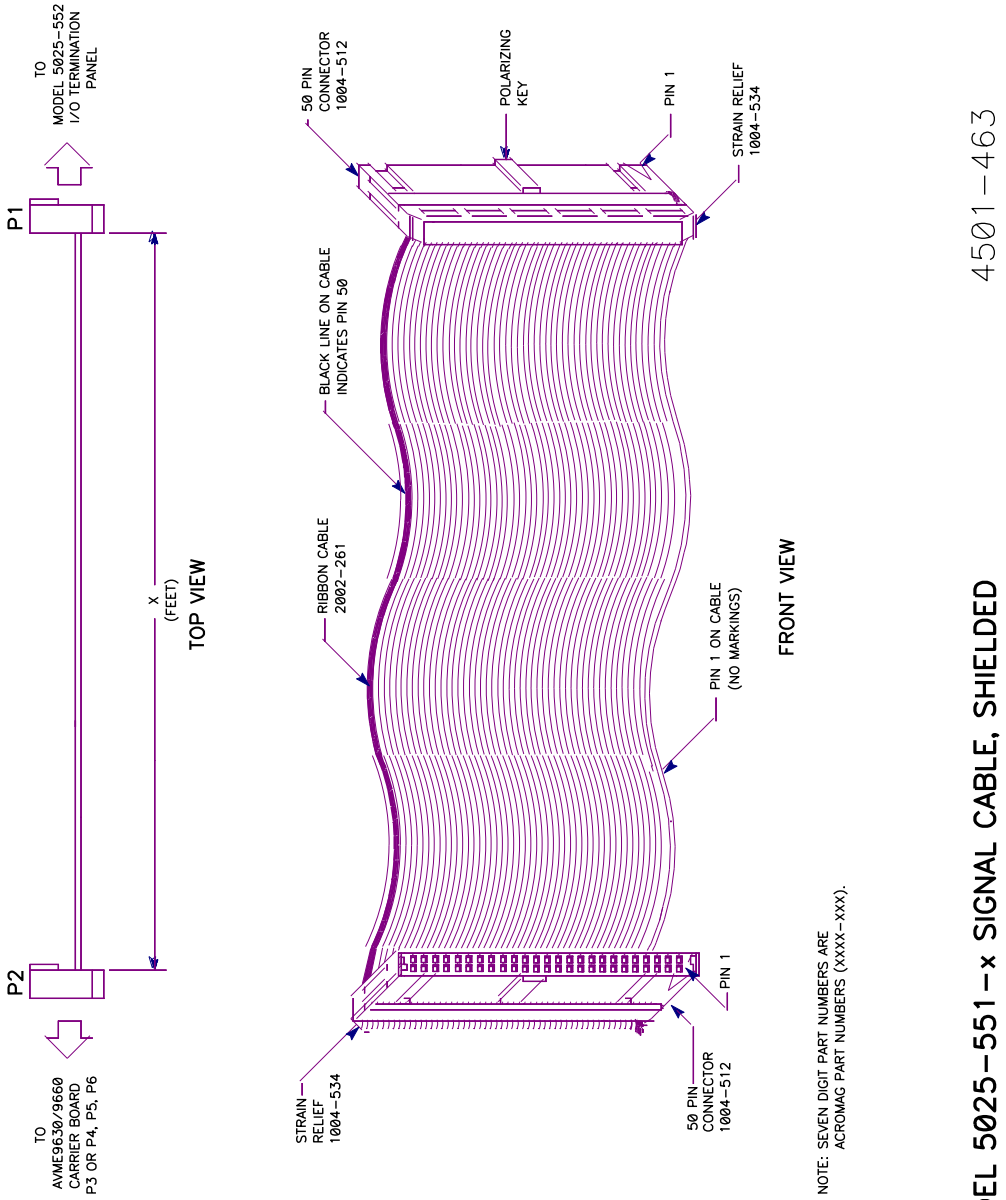
MODEL 5025-550-x SCHEMATIC

MODEL 5025-550-x SIGNAL CABLE, NON-SHIELDED

4501-462

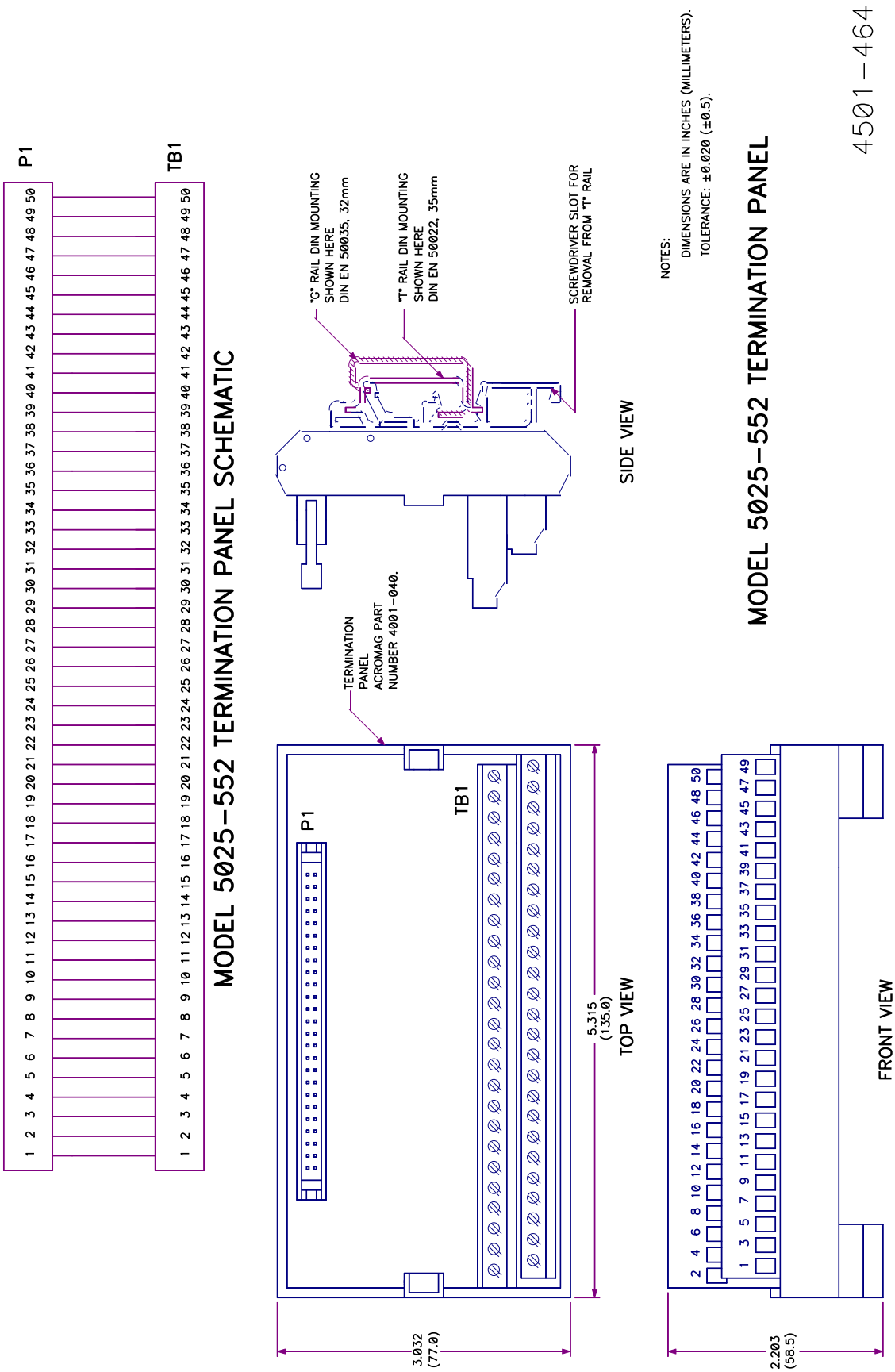


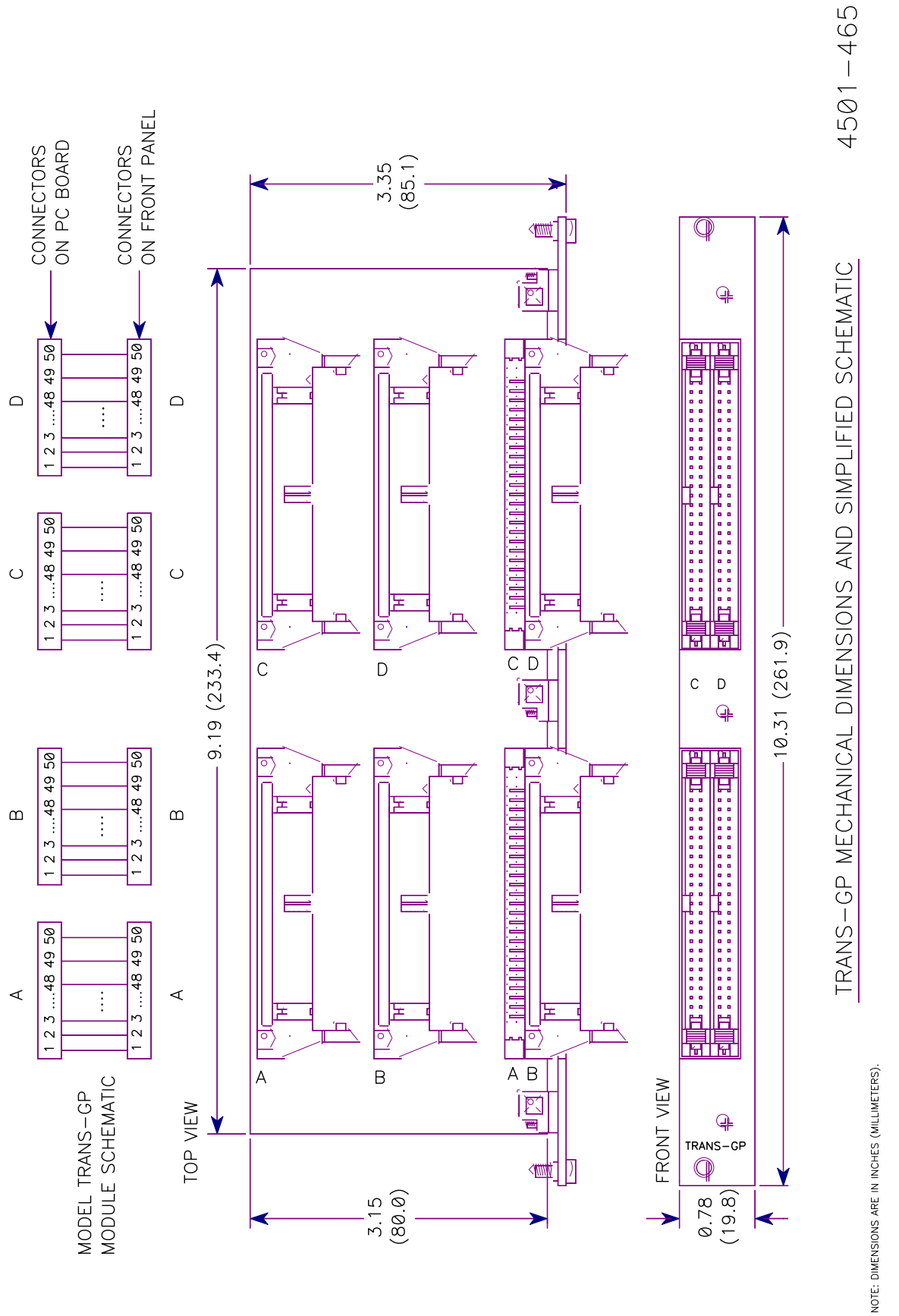
MODEL 5025-551-x SCHEMATIC



MODEL 5025-551-x SIGNAL CABLE, SHIELDED

4501-463


P1
TB1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
MODEL 5025-552 TERMINATION PANEL SCHEMATIC
"G" RAIL DIN MOUNTING SHOWN HERE DIN EN 50035, 32mm
"T" RAIL DIN MOUNTING SHOWN HERE DIN EN 50022, 35mm
SCREWDRIVER SLOT FOR REMOVAL FROM "T" RAIL
SIDE VIEW
NOTES:
DIMENSIONS ARE IN INCHES (MILLIMETERS).
TOLERANCE: ±0.020 (±0.5).
MODEL 5025-552 TERMINATION PANEL
4501-464
TERMINATION PANEL ACROMAG PART NUMBER 4001-040.
P1
TB1
5.315 (135.0)
TOP VIEW
3.032 (77.0)
2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48 50
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 41 43 45 47 49
FRONT VIEW
2.203 (58.5)


4501-465
TRANS-GP MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC
CONNECTORS ON PC BOARD
CONNECTORS ON FRONT PANEL
MODEL TRANS-GP MODULE SCHEMATIC
TOP VIEW
FRONT VIEW
TRANS-GP
9.19 (233.4)
3.35 (85.1)
3.15 (80.0)
10.31 (261.9)
0.78 (19.8)
NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).