Acromag®

Series AVME9675 Industrial I/O Pack
VME64x Bus 6U Non-Intelligent Carrier Board

RETIRED

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The AVME9675 VME64x bus card is a carrier for the Industrial I/O Pack (IP) mezzanine board field I/O modules. The Industrial I/O Packs field I/O exits the carrier via the rear panel per the VME64 Extensions (ANSI/VITA 1.1-1997). The carrier boards facilitate a modular approach to system assembly, since each carrier can be populated with any combination of analog input/output and digital input/output IP modules. Thus, the user can create a board which is customized to the application which saves money and space - a single carrier board populated with IP modules may replace several dedicated function VMEbus boards. The AVME9675 non-intelligent carrier boards provide impressive functionality at low cost.

Model is available in one standard VME64x bus 6U size, with support for up to four IP modules.

MODEL	VME64x Board Size	Supported IP Slots	Operating Temperature Range
AVME9675-4	6U	4 (A,B,C,D)	0 to +70 °C
AMVE9675-4E	6U	4 (A,B,C,D)	-40 to +85 °C
AVME9675-2	6U	2 (A,B)	0 to +70 °C
AVME9675-2E	6U	2 (A,B)	-40 to +85 °C

KEY AVME9675 FEATURES

- **Supports Four IP Modules** - Provides an electrical and mechanical interface for up to four industry standard IP modules. IP Modules are available from Acromag and other vendors in a wide variety of Input/Output configurations to meet the needs of varied applications.
- **Provides Full IP Data Access** - Supports accesses to IP input/output, memory, identification data, and interrupt spaces.
- **Full IP Register Access** - Makes maximum use of logically organized programmable registers on the carrier boards to provide for easy configuration and control of IP modules.
- **VME64 & VME64x CR/CSR Space** – Configuration ROM / Control & Status Register (CR/CSR) space provides additional carrier board identification & programming capabilities. These include software selection of the base address and address modifier of the carrier card in the short I/O space.
- **VME64x Geographical Addressing –** Supports the six Geographical Addressing signals provided by VME64x backplanes. These signals control the base address of the CR/CSR space of each installed carrier. This provides unambiguous identification of each carrier's location within the VME64x chassis.
- **No Hardware Jumpers or Switches –** The board is fully configurable via control registers.
- **LED Indicators Simplify Debugging** - Front panel LED's are dedicated to each IP module to give a visual indication of successful IP accesses.
- **Rear Backplane Connectors Access I/O** - Rear backplane connector P2 & P0 access to field I/O signals mapped per the VME64x IP I/O (ANSI/VITA 4.1-1996) specification.
- **Memory Space Access Support** - IP memory space accesses are supported and software configurable from 1Mbyte to 8Mbytes in the VME64x bus standard address space.
- **Supports Two Interrupt Channels per IP** - Up to two interrupt requests are supported for each IP. The VME64x bus interrupt level is software programmable. Additional registers are associated with each interrupt request for control and status monitoring.
- **Interrupt Priority Control** - Interrupts use a proirity shifting scheme based on the last interrupt serviced. This prevents the continuous interrupts of one IP module interrupt request from blocking the interrupts of other IP modules.
- **Supervisory Circuit for Reset Generation** - A microprocessor supervisor circuit provides power-on, power-off, and low power detection reset signals to the IP modules per the IP specification.
- **Individually Filtered Power** - Filtered +5V, +12V, and -12V DC power is provided to the IP modules via passive filters present on each supply line serving each IP. This provides optimum filtering and isolation between the IP modules and the carrier board and allows analog signals to be accurately measured or reproduced on IP modules without signal degradation from the carrier board logic signal noise.
- **ESD Strip** - The AVME9675 board has been designed to provide electrostatic discharge (ESD) capability by using an ESD strip on the board per ANSI/VITA 1.1-1997 and IEEE1101.10.
- **Injector/Ejector Handles** - The AVME9675 uses modern injector/ejector handles, which push the board into the rack during installation and pull the board out of the rack for removal or replacement. These handles are needed to give you leverage to install and remove the board.

VME64x bus INTERFACE FEATURES

- **Slave Module**-

CR/CSR Registers	A24, D16/D08(O)
Carrier Register Short I/O Access	A16, D16/D08(O)
IP Module ID Space	A16, D16/D08(O)
IP Module I/O Space	A16, D16/D08(EO)
IP Module Memory Space	A24, D16/D08(EO)

- **Supports Short I/O Address Modifiers** - Supports short I/O (A16) address modifiers 29H, 2DH (H = Hex). Short I/O space is used for carrier registers and IP module I/O and ID spaces. The carrier board base addresss and short I/O address modifier is set within the Function 0 Address DEcoder CompaRe register (ADER) in CR/CSR space and decoded on 1K byte boundaries.
- **Supports CR/CSR Space Address Modifier** – Supports address modifier 2FH (H = Hex). CR/CSR space is used to establish initial module communication, identification, location (via geographic address), module base address, address modifier and additional configuration parameters.
- **Supports Standard I/O Address Modifiers** - Supports standard (A24) address modifiers 39H, 3DH (H = Hex). Standard address space is used when an IP supports memory space. The carrier board is configured using programmable registers to set the IP starting address and size (1Mbyte to 8Mbytes).
- **Supports Read-Modify-Write Cycles** - Carrier board supports VME64x bus read-modify-write cycles.
- **Interrupt Support** - I(1-7) interrupter D16/D08 (O). Up to two interrupt requests are supported for each IP module. The VME64x bus interrupt level is software programmable. Carrier board software programmable registers are utilized as interrupt request control and status monitors. Interrupt release mechanism is Release On Register Access (RORA) type.

SIGNAL INTERFACE PRODUCTS

(See Appendix for more information on compatible products)

This IP carrier board will mate directly to all industry standard 8 MHz IP modules. Acromag provides the following interface products (all connections to field signals are made through the carrier board and transition module which passes them to the individual IP modules):

Cables:

Model 5028-187 (SCSI-2 to Flat Ribbon Cable, Shielded): A round 50 conductor shielded cable with a male SCSI-2 connector at one end and a flat female ribbon connector at the other end. The cable is used for connecting AVME9670 or AVME9675 with the TRANS-200, or other compatible carrier boards, to Model 5025-552 termination panels.

Termination Panel:

Model 5025-552: DIN-rail mountable panel provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9670 or AVME9675 with the TRANS-200, or other compatible carrier boards, via SCSI-2 to Flat Ribbon Cable, Shielded (Model 5028-187).

VME64x Transition Module :
Model TRANS-200: This module plugs into the rear backplane directly behind the carrier board. The field I/O connections are made through the backplane to P0 (AVME9670 & AVME9675-4) and P2 (AVME9670, AVME9675-2 & AVME9675-4) connectors of the carrier board and then routed to four (two AVME9675-2) SCSI-2 connectors on the transition module (marked IP module slots “A through D”) or (“A through B” for AVME9675-2) for rear exit from the card cage. It is available for use in VME64x bus card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VME64x bus mechanical dimensions and IEEE Standard (1101.11-1998), with a printed circuit board depth of 80mm, which is a standard transition module depth. The transition module connects to Acromag Termination Panel (Model 5025-552) using SCSI-2 to Flat Ribbon Cable, Shielded (Model 5028-187) to the rear of the card cage, and to AVME9670, AVME9675-2 & AVME9675-4 boards within the card cage.

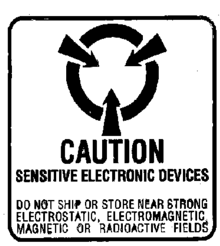
2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.



The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

The carrier board may be configured for different applications. Configuration options will be discussed in the following Sections. The IP module positions are shown in Drawing 4501-800. Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-801 and your IP module documentation for specific configuration and assembly instructions.

VME64x INTERFACE CONFIGURATION

The carrier board is shipped from the factory configured as follows:

- Carrier board will respond to address modifier 2FH for CR/CSR standard (A24) address space access. Base address of the CR/CSR space is located in the CR/CSR Base Address Register (BAR). Geographic addressing (per the VME64x specification) is used to set the CR/CSR base address and also to determine the active CR/CSR card locations within the VME64x chassis.
- Carrier board must be programmed with the Short I/O base address and address modifier within the Function 0 Address DEcoder CompaRe (ADER) Register in CR/CSR space to define the base address of the AVME9675 carrier & IP module registers.
- Programmable Bit Set Register in the CR/CSR defaults to Short I/O accesses disabled. Once enabled via the Bit Set Register the board will respond to address modifier 29H or 2DH, as programmed in the ADER. Registers on the carrier board plus the I/O and ID spaces on any installed IP modules will then become accessible.
- Programmable software registers default to IP memory space (VME64x bus standard address space) accesses disabled.
- Programmable software registers default to IP interrupt requests-disabled and VME64x bus interrupt level-none.

Address Decode Configuration

There are no address jumpers or switches on this board. All configuration takes place via control registers. Initial communication with the carrier must be made to the CR/CSR space using geographic addressing per the VME64x specification. The VME64x backplane applies six geographic address signal lines to the P1 connector as listed in Table 2.1:

Table 2.1: Geographical Address Pin Assignments

Slot No.	GAP* Pin	GA4* Pin	GA3* Pin	GA2* Pin	GA1* Pin	GA0* Pin
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21	Open	GND	Open	GND	Open	GND

The AVME9675 board has pull-up resistors tied to each of the six geographic address inputs, so that their state (Open = "high" or GND = "low") can be interpreted by logic on the carrier board. This logic uses the geographic addressing inputs to encode the base address of the CR/CSR space into the CR/CSR Base Address Register (BAR). The host computer can locate the AVME9675 by scanning the A24 CR/CSR space using address modifier 2FH (refer to section 3 for CR/CSR space programming details).

Once located, additional characteristics of the AVME9675 may be read from the Configuration ROM (CR) portion of the space. Following power up, accesses to the card's Short I/O (A16) space are disabled. The base address of the carrier in the Short I/O space and the desired address modifier must be programmed using the Function 0 Address DEcoder CompaRe (ADER) Register in the Control/Status Register (CSR) portion of the CR/CSR space. Then, accesses to the Short I/O space can be enabled by writing to the Bit Set Register in the CSR. Each carrier board implements a 1K byte block of addresses in the Short I/O space.

- Consult your host CPU manual for detailed information about addressing the VME64x bus short I/O (A16, 16-bit) space. In many cases, CPU's utilizing 24-bit addressing will start the 16-bit address at FF0000 (Hex), and 32-bit CPU's at FFFF0000 (Hex).

VME64x bus Address Modifiers

No hardware jumper configuration is needed. The carrier board initially responds to address modifier 2FH in the standard (A24) CR/CSR space.

Following configuration within the CR/CSR space the carrier board will respond to either address modifier 29H or 2DH in the VME64x bus Short (A16) I/O space. This means that both short supervisory and short non-privileged accesses are supported.

The carrier board will also respond to both address modifiers 39H and 3DH in the VME64x bus standard (A24) address space, when standard address space accesses to IP memory are enabled via programmable registers on the carrier board (refer to Section 3 for programming details).

Interrupt Configuration

No hardware jumper configuration is required. All interrupt enabling, status, and VME64x bus interrupt level selections are configured via programmable registers on the carrier board (see Section 3 for programming details). The carrier board passes interrupt requests from the IP modules to the VME64x bus -- It does not originate interrupt requests. Refer to the IP modules for their specific configuration requirements.

CONNECTORS

Carrier Field I/O Connectors (IP modules A through D)

Field I/O connections are made through the rear via transition module (TRANS-200) connectors A-D for IP modules in positions A-D, respectively. IP module assignment is marked on the transition module for easy identification (see IP location drawing 4501-800 for physical locations of the IP modules). SCSI-2 Round cable assemblies and Acromag termination panels (or user defined terminations) can be quickly mated to the transition module connectors. Pin assignments are defined by the IP I/O Mapping to VME64x Standard (ANSI/VITA 4.1-1996).

Connectors A-D are 50-pin SCSI-2 right angle (female) connectors (AMP). Connectors are high-density, and there is one connector for each IP module marked with A-D on the transition module panel. These connectors include spring latch hardware and 30 microns of gold in the mating area for excellent connection.

The TRANS-200 was originally designed for use with the AVME9670 product which supports four IP modules A-D. It also may be used for the four IP slot AVME9675-4 or the two slot AVME9675-2.

IP Field I/O Connectors (IP modules A through D)

The field side connectors of IP modules A-D mate to connectors P3, P5, P7 and P9, respectively, on the carrier board. IP location is silk-screened on the board for easy identification. Field and logic side connectors are keyed to avoid incorrect assembly.

P3, P5, P7, and P9 are 50-pin male plug header connectors. These AMP 173280-3 connectors mate to AMP 173279-3 connectors (or similar) on the IP modules. This provides excellent connection integrity and utilizes gold plating in the mating area. Threaded metric M2 screws and spacers (supplied with Acromag IP modules) provide additional stability for harsh environments (see Drawing 4501-801 for assembly details).

Pin assignments for these connectors are made by the specific IP model used and correspond identically to the pin numbers of the transition module panel connectors.

IP Logic Interface Connectors (IP modules A through D)

The logic interface sides of IP modules A-D mate to connectors P4, P6, P8, and P10, respectively, on the carrier board. IP location is silk-screened on the board for easy identification. Field and logic side connectors are keyed to avoid incorrect assembly.

P4, P6, P8, and P10 are 50-pin male plug header connectors. These AMP 173280-3 connectors mate to AMP 173279-3 connectors (or similar) on the IP modules. This provides excellent connection integrity and utilizes gold plating in the mating area. Threaded metric M2 screws and spacers (supplied with Acromag IP modules) provide additional stability for harsh environments (see Drawing 4501-801 for assembly details).

Pin assignments for these connectors are defined by the IP module specification and are shown in Table 2.2:

Table 2.2: Standard IP Logic Interface Connections (P4,6,8,10)

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSEL*	29
D01	5	**_DMAReq0*_**	30
D02	6	MEMSEL*	31
D03	7	**_DMAReq1*_**	32
D04	8	IntSel*	33
D05	9	**_DMAck0*_**	34
D06	10	IOSEL*	35
D07	11	**_RESERVED_**	36
D08	12	A1	37
D09	13	**_DMAEnd*_**	38
D10	14	A2	39
D11	15	ERROR*	40
D12	16	A3	41
D13	17	INTReq0*	42
D14	18	A4	43
D15	19	INTReq1*	44
BS0*	20	A5	45
BS1*	21	**_STROBE*_**	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	**_RESERVED_**	49
GND	25	GND	50

Asterisk (*) is used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by the carrier board.

VME64x bus Connections for P1

Table 2.3 indicates the pin assignments for the VME64x bus signals at the P1 connector. The P1 connector is the upper rear connector on the AVME9675 board, as viewed from the front. The connector consists of 32 rows of five pins labeled A, B, C, D and Z. Pin Z1 is located at the upper right hand corner of the connector if the board is viewed from the front component side.

Refer to the VME64x bus specification for additional information on the VME64x bus signals.

TABLE 2.3: VME64x bus P1 CONNECTIONS

Pin	Row Z	Row A	Row B	Row C	Row D
1	**_MPR_**	D00	**_BBSY*_**	D08	**_VPCϕ_**
2	GND	D01	**_BCLR*_**	D09	GNDϕ
3	**_MCLK_**	D02	**_ACFAIL*_**	D10	**_+V1_**
4	GND	D03	BG0IN*	D11	**_+V2_**
5	**_MSD_**	D04	BG0OUT*	D12	**_RsvU_**
6	GND	D05	BG1IN*	D13	**_-V1_**
7	**_MMD_**	D06	BG1OUT*	D14	**_-V2_**
8	GND	D07	BG2IN*	D15	**_RsvU_**
9	**_MCTL_**	GND	BG2OUT*	GND	GAP*
10	GND	SYSCLK	BG3IN*	**_SYSFAIL*_**	GA0*
11	**_RESP*_**	GND	BG3OUT*	**_BERR*_**	GA1*
12	GND	DS1*	**_BR0*_**	SYSRESET*	**_+3.3V_**
13	**_RsvBus_**	DS0*	**_BR1*_**	LWORD*	GA2*
14	GND	WRITE*	**_BR2*_**	AM5	**_+3.3V_**
15	**_RsvBus_**	GND	**_BR3*_**	A23	GA3*
16	GND	DTACK*	AM0	A22	**_+3.3V_**
17	**_RsvBus_**	GND	AM1	A21	GA4*
18	GND	AS*	AM2	A20	**_+3.3V_**
19	**_RsvBus_**	GND	AM3	A19	**_RsvBus_**
20	GND	IACK*	GND	A18	**_+3.3V_**
21	**_RsvBus_**	IACKIN*	**_SERA_**	A17	**_RsvBus_**
22	GND	IACKOUT*	**_SERB_**	A16	**_+3.3V_**
23	**_RsvBus_**	AM4	GND	A15	**_RsvBus_**
24	GND	A07	IRQ7*	A14	**_+3.3V_**
25	**_RsvBus_**	A06	IRQ6*	A13	**_RsvBus_**
26	GND	A05	IRQ5*	A12	**_+3.3V_**
27	**_RsvBus_**	A04	IRQ4*	A11	**_LI/I*_**
28	GND	A03	IRQ3*	A10	**_+3.3V_**
29	**_RsvBus_**	A02	IRQ2*	A09	**_LI/O*_**
30	GND	A01	IRQ1*	A08	**_+3.3V_**
31	**_RsvBus_**	-12V	**_+5VSTDBY_**	+12V	GNDϕ
32	GND	+5V	+5V	+5V	**_VPCϕ_**

Asterisk (*) is used to indicate an active-low signal.
Shaded area are pins defined under the VME64 bus specification.
BOLD ITALIC Logic Lines are NOT USED by the carrier board.
(ϕ) = Elongated (mate first, break last) connector contact.

VME64x bus Connections for P2

Table 2.4 indicates the pin assignments for the VME64x bus signals at the P2 connector. The P2 connector is the lower rear connector on the AVME9675 board, as viewed from the front. The connector consists of 32 rows of five pins labeled A, B, C, D and Z. Pin Z32 is located at the lower right hand corner of the connector if the board is viewed from the front component side.

TABLE 2.4: VME64x bus P2 CONNECTIONS

Pin	Row Z	Row A	Row B	Row C	Row D
1	C46	B41	**_Not Used_**	B42	C47ϕ
2	GND	B43	**_Not Used_**	B44	C48ϕ
3	C49	B45	**_Not Used_**	B46	C50
4	GND	B47	**_Not Used_**	B48	B1
5	B2	B49	**_Not Used_**	B50	B3
6	GND	A1	**_Not Used_**	A2	B4
7	B5	A3	**_Not Used_**	A4	B6
8	GND	A5	**_Not Used_**	A6	B7
9	B8	A7	**_Not Used_**	A8	B9
10	GND	A9	**_Not Used_**	A10	B10
11	B11	A11	**_Not Used_**	A12	B12
12	GND	A13	**_Not Used_**	A14	B13
13	B14	A15	**_Not Used_**	A16	B15
14	GND	A17	**_Not Used_**	A18	B16
15	B17	A19	**_Not Used_**	A20	B18
16	GND	A21	**_Not Used_**	A22	B19
17	B20	A23	**_Not Used_**	A24	B21
18	GND	A25	**_Not Used_**	A26	B22
19	B23	A27	**_Not Used_**	A28	B24
20	GND	A29	**_Not Used_**	A30	B25
21	B26	A31	**_Not Used_**	A32	B27
22	GND	A33	**_Not Used_**	A34	B28
23	B29	A35	**_Not Used_**	A36	B30
24	GND	A37	**_Not Used_**	A38	B31
25	B32	A39	**_Not Used_**	A40	B33
26	GND	A41	**_Not Used_**	A42	B34

27	B35	A43	***Not Used***	A44	B36
28	GND	A45	***Not Used***	A46	B37
29	B38	A47	***Not Used***	A48	B39
30	GND	A49	***Not Used***	A50	B40
31	***Not Used***	***Not Used***	***Not Used***	***Not Used***	***Not Used*ϕ**
32	GND	***Not Used***	***Not Used***	***Not Used***	***Not Used*ϕ**

Note: The letter in front of the number indentifies the IP Module Slot. The number indentifies the I/O pin number of that IP Module.
Example: A46 A = IP Module in Slot "A"
46 = I/O Pin number "46"
(This pin on the IP Module connects to P2, Pin 28, Row C.)
Shaded area are pins defined under the VME64x bus specification.
BOLD ITALIC Logic Lines are NOT USED by the carrier board.
(ϕ) = Elongated (mate first, break last) connector contact.

The I/O signals for the P2 connector are mapped per the IP Module I/O to VME64x bus Standard (ANSI/VITA 4.1-1996). Refer to this standard for additional information on the VME64x bus signals.

VME64x bus Connections for P0

Table 2.5 lists the pin assignments for the VME64x bus signals at the P0 connector. The P0 connector is the center connector on the AVME9675 board, as viewed from the front. The connector consists of 6 rows of 19 pins labeled A, B, C, D, E, and F. Pin A1 is located at the upper right hand corner of the connector near the center of the board, viewed from the front component side.

The I/O signals for the P0 connector are mapped per the IP Module I/O to VME64Xbus Standard (ANSI/VITA 4.1-1996). Refer to this standard for additional information on the VME64x bus signals.

TABLE 2.5: VME64x bus P0 CONNECTIONS

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	D1	D2	D3	D4	D5	GND
2	D6	D7	D8	D9	D10	NP
3	D11	D12	D13	D14	D15	GND
4	D16	D17	D18	D19	D20	NP
5	D21	D22	D23	D24	D25	GND
6	D26	D27	D28	D29	D30	NP
7	D31	D32	D33	D34	D35	GND
8	D36	D37	D38	D39	D40	NP
9	D41	D42	D43	D44	D45	GND
10	D46	D47	D48	D49	D50	NP
11	C1	C2	C3	C4	C5	GND
12	C6	C7	C8	C9	C10	NP
13	C11	C12	C13	C14	C15	GND
14	C16	C17	C18	C19	C20	NP
15	C21	C22	C23	C24	C25	GND
16	C26	C27	C28	C29	C30	NP
17	C31	C32	C33	C34	C35	GND
18	C36	C37	C38	C39	C40	NP
19	C41	C42	C43	C44	C45	GND

Note: The letter in front of the number indentifies the IP Module Slot. The number indentifies the I/O pin number of that IP Module.
Example: D1 D = IP Module in Slot "D"
1 = I/O Pin number "1"
(This pin on the IP Module connects to P0, Pin 1, Row A.)
(NP) = No Pin for PO connector (Row F is for upper ground shield).

- The P0 connector will not be present on AVME9675-2 models.

POWER-UP TIMING AND LOADING

The AVME9675 board uses a Field Programmable Gate-Array (FPGA) to handle the bus interface and control logic timing. Upon power-up, the FPGA automatically clocks in configuration vectors from a local PROM to initialize the logic circuitry for normal operation. This time is measured as the first 145mS (typical) after the +5 Volt supply rises to +2.5 Volts at power-up. The VME64x bus specification requires that the bus master drive the system reset for the first 200mS after power-up, thus inhibiting any data transfers from taking place.

IP control registers are also reset following a power-up sequence, disabling interrupts, etc. (see Section 3 for details).

DATA TRANSFER TIMING

VME64x bus data transfer time is measured from the falling edge of DSx* to the falling edge of DTACK* during a normal data transfer cycle. Typical transfer times are given in the following table.

Register	Data Transfer Time
All Carrier Registers	450 nS, Typical.
IP Registers	450 nS, Typical, If No Wait States*

* See IP module specifications for information on wait states. IP module register access time will increase by the number of wait states multiplied by 125nS (the period of the 8 MHz clock).

FIELD GROUNDING CONSIDERATIONS

Carrier boards are designed with passive filters on each supply line to each IP module. This provides maximum filtering and signal isolation between the IP modules and the carrier board. However, the boards are considered non-isolated, since there is electrical continuity between the VME64x bus and the IP grounds. Therefore, unless isolation is provided on the IP module itself, the field I/O connections are not isolated from the VME64x bus. Care should be taken in designing installations without isolation to avoid ground loops and noise pickup. This is particularly important for analog I/O applications when a high level of accuracy/resolution is needed (12-bits or more). Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the IP input/output modules.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to operate the AVME9675 non-intelligent carrier board.

The AVME9675 implements Geographical Addressing and the Configuration ROM / Control and Status Register (CR/CSR) space as they are defined in the VME64x Standard.

The AVME9675's CR/CSR Space is 512 KB in size (0x00000 to 0x7FFFF). The AVME9675's position in the CR/CSR Space array is determined by the CR/CSR Base Address Register (CR/CSR BAR). The AVME9675 uses the VME64x Geographical Addressing method to automatically provide the CR/CSR BAR value.

GEOGRAPHICAL ADDRESSING

Geographical address capability allows the AVME9675 CR/CSR space to be addressed upon system initialization and configured without setting address switches. The CR/CSR Base Address Register value is derived from the geographical address pins (see Table 2.3 Row D). The geographical address pins are set by the system backplane with unique slot addresses and are routed via the P1 connector to the AVME9675's FPGA. The FPGA hardware automatically writes the geographic address into the CR/CSR BAR upon system power-up. **The implementation of geographical addressing requires the use of a VME64x backplane or a proprietary design which provides the same capability**.

The combination of geographical addressing and the AVME9675 Configuration ROM (CR) board identification values allow system software to automatically identify into which VME64x backplane slot the AVME9675 is plugged. With the CR/CSR BAR defined by geographical addressing, the AVME9675 CR and CSR registers can then be addressed by system software to define a base address for the AVME9675 carrier and IP module registers.

CONFIGURATION ROM (CR) ASSIGNMENTS

Table 3.1 defines the CR address space from 0x0 through 0xFFF. The addresses within the CR are given as offset addresses. They are relative to the CR/CSR BAR (given by geographical addressing). An absolute address in the CR is created, by adding the offset address to the CR/CSR BAR. The CR area is "read-only" and cannot be changed by system software. Access to the CR is compatible with the D16 or D08(0) access method and utilizes only every fourth byte. All unimplemented locations in the defined CR Area will be read as 0x0.

Table 3.1: CONFIGURATION ROM (CR) Memory Map

CR Offset Address [MSB ………LSB]	Content Description	ROM Data [MSB …LSB]
1 byte 0x03	Checksum	0xAD
3 bytes 0x07,0x0B,0x0F	Length of ROM	0xFFF
1 byte 0x13	Configuration ROM data access width: Use D16 or D08(EO), every fourth byte	0x83
1 byte 0x17	CSR Data access width Use D16 or D08(EO), every fourth byte	0x83
1 byte 0x1B	CR/CSR Space Specification ID Specifies the VME64x CR/CSR version	0x02
1 byte 0x1F	ASCII "C" Used to identify a valid CR	0x43
1 byte 0x23	ASCII "R" Used to identify a valid CR	0x52
3 bytes 0x27, 0x2B, 0x2F	Manufacturer's ID assigned by IEEE	0x00,01,C3
4 bytes 0x33,0x37,0x3B,0x3F	AVME9675 Board ID supplied by Acromag	0x00,00,00,01
4 bytes 0x43,0x47,0x4B,0x4F	AVME9675 Revision ID supplied by Acromag	0x00,…,00
3 bytes 0x53, 0x57 ,0x5B	Pointer to a null terminated ASCII printable string or 0x000000	0x00,00,00
8 bytes 0x5F to 0x7B	RESERVED	0x00,…,00
1 byte 0x7F	Program ID code	0x00
24 bytes 0x83 to 0xDF	Unimplemented	0x00,…,00
1 byte 0xE3	Slave Characteristics Parameter: Supports Read-Modify-Write (RMW) and Implements a P2 connector	0x44
4 bytes 0xE7 to 0xF3	Unimplemented	0x00
1 byte 0xF7	Interrupt Capabilities Interrupt Levels 7 to 1 can be selected	0xFE
2 bytes 0xFB, 0xFF	Unimplemented	0x00,00
1 byte 0x103	Function 0 Data Access Width (DAWPR) Supports Data transfer access width of D16 or D08(EO)	0x83
7 bytes 0x107 to 0x11F	Unimplemented	0x00,…,00
8 bytes 0x123 to 0x13F	Function 0 AM Code Mask (AMCAP) Supports Address Modifers 45 (0x2D), and 41 (0x29)	0x00,00,22,00, 00,00,00,00
312 bytes 0x143 to 0x61F	Unimplemented	0x00,…,00
4 bytes 0x623 to 0x62F	Function 0 Address Decoder Mask (ADEM) Address bits A15 to A10 are decoded for access of the AVME9675 carrier and IP module registers (that is, a 1Kbyte address space size is specified).	0x00,00,FC,00
627 bytes 0x633 to 0xFFF	Unimplemented or Reserved	0x00,…,00

The mapping of the AVME9675 carrier and IP module registers into 1KB of A16/D16 or D08(EO) short I/O space is selected by the Function 0 address relocation CR values as described in this paragraph. The Function 0 Data Access Width

(DAWPR) specifies support for data transfer access widths of D16 or D08(EO). Bits 15 to 10 of the Address DEcoder Mask (ADEM) are set and indicate that address bits A15, A14, A13, A12, A11, and A10 are compared for decoding purposes. This corresponds with the support of A16 short I/O space addressing as selected in the Function 0 AM Code Mask (AMCAP). The values read from the DAWPR, ADEM, and AMCAP are fixed and are not programmable.

CONTROL/STATUS REGISTER (CSR) ASSIGNMENTS

The AVME9675 CSR is used to store the CR/CSR BAR and the CSR Function 0 Address DEcoder CompaRe (ADER) register. As indicated above, the CR/CSR BAR contains the base address for the CR/CSR space registers (as defined by geographical addressing). The CSR Function 0 ADER register is set by system software with the base address of the AVME9675 carrier and IP module registers. Once the CSR Function 0 ADER register has been programmed, the “Module Enable” bit defined within the Bit Set / Bit Clear CSRs is used to enable the AVME9675. The AVME9675 will then respond to its defined address space as initialized by software.

The defined Control/Status Register (CSR) area is specified from 0x7FC00 through 0x7FFFF for a total of 256 usable locations. The locations from 0x7FC00 to 0x7FFFF are specified in Table 3.2.

Table 3.2: Control/Status Register (CSR) Memory Map

CSR Address [MSB ………LSB]	Content Description	Example Data [MSB …LSB]
1 byte 0x7FFFF	CR/CSR (BAR) Base Address Register The address is set by Geographical Addressing and is the base address which provides access to the CR/CSR space.	Board is Slot 3 0x18
1 byte 0x7FFFB	Bit Set Register Bit-4 (when set) is used to enable the AVME9675 to respond to data accesses starting from the base address (programmed in the CSR Function 0 ADER). Upon read, bit-4 will indicate the current status (0 for disabled, 1 for enabled). All other bits of this register have no effect.	AVME9675 Enabled 0x10
1 byte 0x7FFF7	Bit Clear Register Bit-4 (when set) is used to disable the module from responding to data accesses starting from the base address (programmed in the CSR Function 0 ADER). Upon read, bit-4 will indicate the current status (0 for disabled, 1 for enabled). All other bits of this register have no effect.	0x00
33 bytes 0x7FFF3 to 0x7FF73	Unimplemented or Reserved	0x00,…,0x00
4 bytes 0x7FF63 to 0x7FF6F	Function 0 Address Decoder Compare (ADER) Register. This register contains the base address of the AVME9675 carrier and IP module registers and the address modifier code 0x29 or 0x2D.	Short I/O Address set to FC00 and Address Modifier 0x29 0x00,00,FC,A4
216 bytes 0x7FC00 to 0x7FF5F	Reserved	0x00,…,0x00

The CSR locations can be modified after the module goes “on-line.” Access to the CSR is compatible with the D16 or D08(0) access method and utilizes only every fourth byte. All unimplemented locations in the defined CSR area will be read as 0x0.

The CR/CSR Base Address Register (BAR) will be set to the address corresponding to the geographic address (slot) the card is plugged into. For example, if the card resides in slot 3 then the BAR will automatically be set to 0x18 which corresponds to the geographic address of slot 3 per section 3.2.11 of the VME64x standard. The AVME9675 will parity check the geographical address. If bad parity is detected, the local address will be set to decimal 30 (0x1E) as recommended by the VME64x standard.

The base address of the AVME9675 carrier and IP module registers is defined by system software and is written into the CSR Function 0 Address Decoder Compare (ADER) register along with the address modifier. Address modifiers 0x29 (A16 non-privileged access) and 0x2D (A16 supervisory access) are supported. After the base address is written, the AVME9675 can be enabled for data transfers by setting enable bit-4 of the Bit Set register to a logic “1”. The AVME9675 cannot be addressed until the CSR Function 0 ADER register has been programmed.

Some IP modules require mapping into VMEbus A24 standard address space to support IP modules with up to 8Mbytes of IP module memory. Mapping of an IP module into A24 standard address is not implemented via the CR/CSR registers. However, the AVME9675 can be enabled for A24 standard access via the AVME9675 control registers as is decribed in IP Memory Enable Register section of this chapter. When properly enabled for IP module memory space, the AVME9675 will then respond to both address modifiers 0x3D and 0x39.

AVME9675 CARRIER AND IP MODULE REGISTERS

The AVME9675 carrier and IP module register space is addressable on 1K byte boundaries in the Short I/O (A16) Address Space. The 1K byte of memory consumed by the board is composed of blocks of memory for the I/O and ID spaces of up to four IP modules. The rest of the 1K byte address space is unused, or contains registers or memory specific to the function of the carrier board.

- IP module slots C & D are not supported, in the AVME9675-2 model because their mounting and field I/O access (P0) connectors are not present. However, the address space of IP module slots C and D is still allocated in the following memory maps.

The base address of the AVME9675 carrier and IP module registers is defined by system software and is written into the CSR Function 0 Address Decoder Compare (ADER) register as described in the CSR section. The memory map for the AVME9675 is shown in Table 3.3A. The addresses given in Table 3.3A are given as offset addresses. They are relative to the ADER register. An absolute address in the AVME9675 carrier and IP module space is created, by adding the offset address to the ADER base address.

Table 3.3A: AVME9675 6U Carrier Bd Short I/O Memory Map

Base Address + (Hex)	EVEN Byte D15 D08	ODD Byte D07 D00	Base Address + (Hex)
0000 ↓ 007E	IP A I/O Space High Byte	IP A I/O Space Low Byte	**0001 ↓ 007F**
0080 ↓ 00BE	Not Used	IP A ID Space Low Byte	**0081 ↓ 00BF**
00C0 ↓ 00FE	Not Used	Carrier Board Registers (See Table 3.3B)	**00C1 ↓ 00FF**
0100 ↓ 017E	IP B I/O Space High Byte	IP B I/O Space Low Byte	**0101 ↓ 017F**
0180 ↓ 01BE	Not Used	IP B ID Space Low Byte	**0181 ↓ 01BF**
01C0 ↓ 01FE	Not Used	Not Used	**01C1 ↓ 01FF**
0200 ↓ 027E	IP C I/O Space High Byte	IP C I/O Space Low Byte	**0201 ↓ 027F**
0280 ↓ 02BE	Not Used	IP C ID Space Low Byte	**0281 ↓ 02BF**
02C0 ↓ 02FE	Not Used	Not Used	**02C1 ↓ 02FF**
0300 ↓ 037E	IP D I/O Space High Byte	IP D I/O Space Low Byte	**0301 ↓ 037F**
0380 ↓ 03BE	Not Used	IP D ID Space Low Byte	**0381 ↓ 03BF**
03C0 ↓ 03FE	Not Used	Not Used	**03C1 ↓ 03FF**

The Input/Output (IO) and Identification (ID) spaces of each IP are accessible via the VME64x bus Short I/O space as shown in Table 3.3A. The carrier board may optionally occupy memory in the VME64x bus standard (A24) address space, if needed for IP modules containing Memory space. IP memory will only be mapped into the standard memory space if it is enabled for a particular IP per the user programmable IP Memory Enable Register (see Table 3.3B and subsequent description). The starting memory address for each enabled IP and the memory size for each enabled IP module is user-programmable via its associated IP Memory Base Address & Size Register (see Table 3.3B and subsequent description).

Table 3.3B: AVME9675 Carrier Board Registers

Base Address + (Hex)	EVEN Byte D15 D08	ODD Byte D07 D00	Base Address + (Hex)
00C0	Not Used	Carrier Board Status Register	00C1
00C2	Not Used	Interrupt Level Register	00C3
00C4	Not Used	IP Error Register	00C5
00C6	Not Used	IP Memory Enable Register	00C7
00C8 ↓ 00CE	Not Used	Not Used	00C9 ↓ 00CF
00D0	Not Used	IP_A Memory Base Address & Size Register	00D1
00D2	Not Used	IP_B Memory Base Address & Size Register	00D3
00D4	Not Used	IP_C Memory Base Address & Size Register	00D5
00D6	Not Used	IP_D Memory Base Address & Size Register	00D7
00D8 ↓ 00DE	Not Used	Not Used	00D9 ↓ 00DF
00E0	Not Used	IP Interrupt Enable Register	00E1
00E2	Not Used	IP Interrupt Pending Register	00E3
00E4	Not Used	IP Interrupt Clear Register	00E5
00E6 ↓ 00FE	Not Used	Not Used	00E7 ↓ 00FF

Identification ROM - (Read Only, 32 Odd-Byte Addresses)

Each IP contains identification information (ID) that resides in the ID space per the IP specification. This area of memory contains 32 bytes of information at most (ID ROM Format I). Both fixed and variable information may be present within the ID ROM. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information may include unique information required for the module. The identification Section for each IP module is located in the carrier board memory map per Table 3.3A. ID bytes are addressed using only the odd addresses in a 64-byte block. The ID contents are shown in Table 3.4 for a generic IP. Refer to the documentation of your IP module for specific information.

Table 3.4: Generic IP Module ID Space Identification (ID) ROM

Hex Offset From ID PROM Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All IP modules have ‘IPAC’
03	P	50	
05	A	41	
07	C	43	
09		A3	Acromag ID Code
0B		mm	IP Model Code[1]
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		nn	Total Number of ID PROM Bytes
17		cc	CRC
19 to (2*nn - 1)		xx	IP Specific Space
(2*nn + 1) to 3F		yy	Not Used

Notes (Table 3.4):
1. The IP model number is represented by a two-digit code within the ID ROM (e.g. the IP405 model is represented by 01 Hex).

Carrier Board Status Register - (Read/Write, Base + C1H)

The Carrier Board Status Register reflects and controls functions globally on the carrier board.

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
ACE[1]	AAD[2]	TOA[3]	Soft Reset	GIE[4]	GIP[5]	Not Used	Not Used

Notes:
1. ACE – this bit is Auto Clear Interrupt Enable.
2. AAD - this bit is Auto Acknowledge Disable.
3. TOA - this bit is Time Out Access Enable.

4. GIE - this bit is Global Interrupt Enable.
5. GIP - this bit is Global Interrupt Pending.

Where:

Bits 1, 0	Not used - equal "0" if read
Bit 7	Writing a “1” to this bit will enable automatic clear of pending interrupts on the carrier. When this bit is set, pending interrupts will not be latched or registered on the carrier. An interrupt will only remain set as pending on the carrier if its corresponding IP module has an active interrupt request.
Bit 6 Auto Acknowledge Disable	When this bit is set to “1” automatic acknowledge of the IP module access is disabled. Thus an access to an empty IP module slot can result in a bus error due to time out. When this bit is set to “0” automatic acknowledgement is enabled. The carrier will acknowledge the access even if the IP module does not or if there is no IP module present. Bit 5 of this register will be set to indicate that the last IP module access has timed out.
Bit 5 Timed Out Access	This bit when set to “1” indicates that the last IP module has timed out (The IP did not acknowledge the access.) This bit will be “0” on power-up. Reading the carrier board status register will clear this bit to “0”.
Bit 4 Software Reset (Write)	Writing a "1" to this bit causes a software reset. Writing "0" or reading the bit has no effect. When set the software reset bit will have a duration of 1us. The effect of software reset on the various registers is noted in the description of each register. Reset Condition: Set to "0".
Bit 3 Global Interrupt Enable (GIE) (Read/Write)	Writing a "1" to this bit enables interrupts to be serviced, provided that interrupts are supported and configured. A "0" disables servicing interrupts. Reset Condition: Set to "0", interrupts disabled.
Bit 2 Global Interrupt Pending (GIP) (Read)	This bit will be "1" when there is an interrupt pending. This bit will be "0" when there is no interrupt pending. Polling this bit will reflect the board's pending interrupt status, even if the Global Interrupt Enable bit is set to "0". Reset condition: Set to "0".

Interrupt Level Register - (Read/Write, Base + C3H)

The carrier board passes interrupt requests from the IP modules to the VME64x bus. It does not originate interrupt requests. The Interrupt Level Register allows the user to control the mapping of IP interrupt requests to the desired VME64x bus interrupt level. Note that the “Global Interrupt Enable” bit in the Carrier Board Status Register must be set for interrupts to be enabled from the carrier board. Also, the specific IP interrupt request must be enabled via its corresponding bit in the Interrupt Enable Register, described subsequently.

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
Not Used	Not Used	Not Used	Not Used	Not Used	IL2	IL1	IL0

Where:

Bits 7,6,5,4,3	Not used - equal "0" if read
Bits 2,1,0 IL2-IL0 (Read/Write)	These bits control the VME64x bus interrupt request level associated with IP interrupt requests as illustrated in the following table. Reset Condition: Set to "0", no interrupt request.

VME64x bus Interrupt Level	IL2	IL1	IL0
None	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

IP Error Register - (Read, Base + C5H)

The IP Error Register allows the user to monitor the Error signals of IP modules A through D. The Industrial I/O Pack specification states that the error signals indicate a non-recoverable error from the IP (such as a component failure or hard-wired configuration error). Refer to your IP specific documentation to see if the error signal is supported and what it indicates.

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	IP Error

Where:

Bits 7, 6, 5, 4, 3, 2, 1	Not used - equal "0" if read
Bit 0 IP Error (Read)	This bit will be a "1" when any IP module asserts its Error signal. This bit will be “0” when there is no error. Reset Condition: Bit will be “0” (no error) unless driven by IP.

IP Memory Enable Register - (Read/Write, Base + C7H)

The IP Memory Enable Register allows the user to program which IP modules will be accessible in the standard (A24) memory space. An enable bit is associated with each IP A through D. This register must be used in conjunction with the IP Memory Base Address & Size Registers to fully define the addressable memory space of the IP modules. Enabling IP memory has no effect on the I/O and ID spaces of the module.

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0

Not Used	Not Used	Not Used	Not Used	IP-D Mem Ena	IP-C Mem Ena	IP-B Mem Ena	IP-A Mem Ena

Where:

Bits 7, 6, 5, 4	Not used - equal "0" if read.
Bit 3 IP-D Memory Enable (Read/Write)	Writing a "1" to this bit enables the memory space for IP D. A zero disables memory space accesses. Reset Condition: Set to "0", memory space accesses disabled for IP D.
Bit 2 IP-C Memory Enable (Read/Write)	Writing a "1" to this bit enables the memory space for IP C. A zero disables memory space accesses. Reset Condition: Set to "0", memory space accesses disabled for IP C.
Bit 1 IP-B Memory Enable (Read/Write)	Writing a "1" to this bit enables the memory space for IP B. A zero disables memory space accesses. Reset Condition: Set to "0", memory space accesses disabled for IP B.
Bit 0 IP-A Memory Enable (Read/Write)	Writing a "1" to this bit enables the memory space for IP A. A zero disables memory space accesses. Reset Condition: Set to "0", memory space accesses disabled for IP A.

IP Memory Base Address & Size Registers - (Read/Write)
IP_A (Base + D1H)
IP_B (Base + D3H)
IP_C (Base + D5H)
IP_D (Base + D7H)

The IP Memory Base Address & Size Registers are user programmable to define the starting address of standard (A24) memory space and the size of that memory space corresponding to IP modules A through D. The memory size for each enabled IP module is user-programmable from 1MByte to 8MByte in multiples of two. Note that memory on IP modules can only be accessed if enabled within the IP Memory Enable Register, and that the memory bases for enabled IP modules must not be programmed to overlap with each other. The size selected by these registers should be matched to that required by the associated IP.

Base Address				Not Used		Memory Size		
MSB D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**LSB D0**	
A23	A22	A21	A20	Not Used	Not Used	0	0	**1M**
A23	A22	A21	Not Used	Not Used	Not Used	0	1	**2M**
A23	A22	Not Used	Not Used	Not Used	Not Used	1	0	**4M**
A23	Not Used	Not Used	Not Used	Not Used	Not Used	1	1	**8M**

Where:

Bit 7, 6, 5, 4 IP Memory Base Address (Read/Write)	These bits define the memory base address. Read and write operations are implemented on all bits even if labeled unused. Thus, a read operation will return the last value written. Reset Condition: Set to "0", memory base address 0.
Bit 3, 2	Not used - equal "0" if read.
Bit 1, 0 IP Memory Size (Read/Write)	These bits define the memory size selected 1MB, 2MB, 4MB, or 8MB as shown in the previous table. Reset Condition: Set to "0", 1MB memory size.

IP Interrupt Enable Register - (Read/Write, Base + E1H)

The IP Interrupt Enable Register is used to individually enable/disable IP interrupts. Each IP A through D may have up to two requests. Note that the "Global Interrupt Enable" bit in the Carrier Board Status Register must be set for interrupts to be enabled from the carrier board. The user must also configure the VME64x bus interrupt level using the Interrupt Level Register.

MSB D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**LSB D0**
IP D Int1 Ena	IP D Int0 Ena	IP C Int1 Ena	IP C Int0 Ena	IP B Int1 Ena	IP B Int0 Ena	IP A Int1 Ena	IP A Int0 Ena

Where:

All Bits IP Interrupt Enable (Read/Write)	Writing a "1" to a bit enables interrupts for the corresponding IP module and interrupt level. A zero disables the corresponding interrupt. Reset Condition: Set to "0", IP interrupts disabled.

IP Interrupt Pending Register - (Read, Base + E3H)

The IP Interrupt Pending Register is used to individually identify pending IP interrupts. If multiple IP interrupts are pending, they will be serviced with the lowest priority given to the last IP interrupt and the highest priority is given to all other pending interrupts. This prevents the continuous interrrupts of one IP module from blocking the interrupts of other modules.

MSB D7 Low Prior.	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**LSB D0 High Prior.**
IP D Int1 Pend	IP D Int0 Pend	IP C Int1 Pend	IP C Int0 Pend	IP B Int1 Pend	IP B Int0 Pend	IP A Int1 Pen d	IP A Int0 Pen d

Where:

All Bits IP Interrupt Pending (Read)	A bit will be a “1” when the corresponding IP interrupt is pending. A bit will be a “0” when its corresponding interrupt is not pending. Polling this bit will reflect the IP modules pending interrupt status, even if the IP interrupt enable bit is set to “0”. Reset Condition: Set to "0".

IP Interrupt Clear Register - (Write, Base + E5H)

The IP Interrupt Clear Register is used to individually clear the IP interrupt Pending bits set in the IP Interrupt Pending register.

MSB D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**LSB D0**
IP D Int1 Clear	IP D Int0 Clear	IP C Int1 Clear	IP C Int0 Clear	IP B Int1 Clear	IP B Int0 Clear	IP A Int1 Clear	IP A Int0 Clear

Where:

All Bits IP Interrupt Clear (Write)	Writing a “1” to a bit causes the corresponding IP interrupt Pending bit to clear. Writing “0” or reading has no effect. Reset Condition: Set to "0".

GENERAL PROGRAMMING CONSIDERATIONS

The carrier board register architecture makes the configuration fast and easy. With the AVME9675’s supported geographical addressing and the Configuration ROM board identification values system software can automatically identify into which VME64x backplane slot the AVME9675 is plugged. By the means of the geographic address set into the CR/CSR BAR, the base address of the AVME9675 CR/CSR space is fixed. The AVME9675 CR and CSR registers are then addressed by system software to define a base address for the AVME9675 carrier and IP module registers.

Once the carrier board is mapped to the desired base address, communication with its registers and the I/O and ID spaces of the IP modules is straightforward. The carrier board is easily configured to communicate with IP memory space, if present, through two configuration registers. Interrupt configuration/control, if supported by IP modules, is also easily done through registers.

Board Diagnostics

The board is a non-intelligent slave and does not perform self diagnostics. It does, however, provide front panel LED's to indicate successful communication with each of up to four IP modules, A-D. These LED's are driven by the corresponding IP acknowledge signal which is lengthened by the logic in the FPGA on the carrier board to make the access visible to the user. This means that frequent accesses to an IP will result in constant LED illumination. The LED's indicate I/O, memory, interrupt acknowledge, and ID space accesses. Note that the LED's will not illuminate during accesses of carrier board registers, or accesses to IP modules which are not physically present, or to unsupported memory space. Additional information about the error status of the IP modules can be obtained by reading the IP Error Register.

GENERATING INTERRUPTS

Interrupt requests do not originate from the carrier board, but rather, from the IP modules. Each IP may support 0, 1, or 2 interrupt requests. The carrier board processes the request from the IP and uses the Interrupt Level Register data to map the request to the desired VME64x bus interrupt level (if locally enabled within the Interrupt Enable Register and globally enabled within the Carrier Board Status Register). The carrier board then waits for an interrupt acknowledge from the VME64x bus host after asserting the appropriate VME64x bus interrupt request.

When the carrier board recognizes an interrupt acknowledge cycle on the VME64x bus, it checks for a match of the IP interrupt requests. If none is pending or the interrupt level does not match, it will pass the acknowledgment signal along, without consuming it. If there is a match, the carrier board will initiate an acknowledgment cycle with the requesting IP, which must supply the interrupt vector during the cycle. The VME64x bus interrupt acknowledge signal is consumed by the carrier board during a valid cycle. Note that if multiple IP interrupt requests are pending, then the carrier board will prioritize the requests based on the last interrupt serviced. Lowest proirity will be given to the last interrupt serviced.

Interrupt Configuration Example

1. Clear the global interrupt enable bit in the Carrier Board Status Register by writing a "0" to bit 3.
2. Write interrupt vector to the location specified on the IP and perform any other IP specific configuration required - do for each supported IP interrupt request.
3. Write to the Interrupt Level Register to program the desired interrupt level per bits 2,1,0.
4. Write “1” to the IP Interrupt Clear Register corresponding to the desired IP interrupt request(s) being configured.
5. Write “1” to the IP Interrupt Enable Register bits corresponding to the IP interrupt request to be enabled.
6. Enable interrupts from the carrier board by writing a "1" to bit 3 (global interrupt enable bit) in the Carrier Board Status Register.

Sequence of Events For an Interrupt

1. The IP asserts an interrupt request to the carrier board (asserts IntReq0* or IntReq1*).
2. The AVME9675 carrier board acts as an interrupter in making the VME64x bus interrupt request (asserts IRQx*) corresponding to the IP interrupt request.
3. The VME64x bus host (interrupt handler) asserts IACK* and the level of the interrupt it is seeking on A01-A03.
4. When the asserted VME64x bus IACKIN* signal (daisy-chained) is passed to the AVME9675, the carrier board will check if the level requested matches that specified by the host. If so, the carrier board will assert the IntSel* line to the appropriate IP together with (carrier board generated) address bit A1 to select which interrupt request is being processed (A1 low corresponds to IntReq0*; A1 high corresponds to IntReq1*).
5. The IP puts the appropriate interrupt vector on the local data bus (D00-D07 if an D08 (O) interrupter or D00-D15 if a D16 interrupter), and asserts Ack* to the carrier board. The carrier board passes this along to the VME64x bus (D08 [O] or D16) and asserts DTACK*.
6. The host uses the vector to point at which interrupt handler to execute and begins its execution.
7. Example of Generic Interrupt Handler Actions:
   A. Disable the interrupting IP by writing a "0" to the appropriate bit in the IP Interrupt Enable Register.
   B. Take any IP specific action required to remove the interrupt request at its source.
   C. Clear the interrupting IP by writing a "1" to the appropriate bit in the IP Interrupt Clear Register.
   D. Enable the interrupting IP by writing a "1" to the appropriate bit in the IP Interrupt Enable Register.
8. If the IP interrupt stimulus has been removed and no other IP modules have interrupts pending, the interrupt cycle is completed (i.e. the carrier board negates its interrupt request).
   A. If the IP interrupt stimulus remains, a new interrupt request will immediately follow. If the stimulus cannot be removed, then the IP should be disabled or reconfigured.
   B. If other IP modules have interrupts pending, then the interrupt request (IRQx*) will remain asserted. This will start a new interrupt cycle.

4.0 THEORY OF OPERATION

This section describes the basic functionality of the circuitry used on the carrier board. Refer to the Block Diagram shown in the Drawing 4501-802 as you review this material.

CARRIER BOARD OVERVIEW

The carrier board is a VME64x bus slave board providing up to four industry standard IP module interfaces for the AVME9675. The carrier board's VME64x bus interface allows an intelligent single board computer (VME64x bus Master) to control and communicate with electronic devices that are external to the VME64x bus card cage. The external electronic hardware may linked to the carrier board rear access via a transition module (TRANS-200) or proprietary interface. The electronic link from the field I/O connections to the carrier board is made via the IP module selected for your specific application.

To facilitate easy connection of external devices to the IP field I/O pins of the carrier board, optional Termination Panels are available. SCSI-2 cables connect a 50 pin IP field I/O connector on the transition module (TRANS-200) to the Termination Panel. At the Termination Panel field I/O signals are connected to a 50 position terminal block via screw clamps. The AVME9675 contains up to four IP modules, and thus 200 I/O connections may be provided via the transition module through SCSI-2 connectors marked A-D.

- The TRANS-200 was originally designed for use with the AVME9670 product which supports four IP modules A-D. It is also compatible with the AVME9675-4 (IP slots A-D) and AVME9675-2 (IP slots A & B).

The VME64x bus and IP module logic commons have a direct electrical connection (i.e., they are not electrically isolated). However, the field I/O connections can be isolated from the VME64x bus if an IP module that provides this isolation (between the logic and field side) is utilized. A wide variety of IP modules are currently available (from Acromag and other vendors) that allow interface to many external devices for both digital and analog I/O applications.

VME64x bus Interface

The carrier board's VME64x bus interface is used to program and monitor the carrier board's registers for configuration and control of the board's documented modes of operation (see section 3). In addition, the VME64x bus interface is also used to communicate with and control external devices that are connected to an IP module's field I/O signals (assuming an IP module is present on the carrier board).

The VME64x bus interface is implemented in the logic of the carrier board's Field Programmable Gate-Array (FPGA). The FPGA implements VME64x bus specification ANSI/VITA 1-1994 (VME64) & ANSI/VITA 1.1-1997 (VME64x) as an interrupting slave including the following data transfer types.

* A24, D16/D08(O) CR/CSR Register Space
* A16, D16/D08(O) Carrier Register Short I/O Access
* A16, D16/D08(O) IP Module ID Space
* A16, D16/D08(EO) IP Module I/O Space
* A24, D16/D08(EO) IP Module Memory Space

The carrier board's VME64x bus data transfer rates are typically:

- 450ns for accesses to the carrier board registers.
- 450ns for data transfers to the IP modules (assuming 0 wait states on IP).

The carrier board's FPGA monitors the six geographical address signal inputs supplied by the VME64x backplane on the P1 connector. These signals determine the base address of the carrier in the standard (A24) Configuration ROM / Control & Status Register (CR/CSR) address space. The host computer must scan the CR/CSR space to determine active card locations within the VME64x chassis. When the CR/CSR address matches the card's, the FPGA controls and implements the required bus transfer allowing communication with the card's CR/CSR space.

Carrier Board Registers

The carrier board registers (presented in section 3) are implemented in the logic of the carrier board's FPGA. An outline of the functions provided by the carrier board registers includes:

- **Configuration ROM (CR within CR/CSR space)** registers provide carrier board identification and capabilities information.

- **Control & Status Registers (CSR within CR/CSR space)** allow the base address of the Short (A16) I/O carrier space to be relocated on 1K byte boundaries as desired by the host computer using the **Function 0 Address DEcoder CompaRe (ADER)** register and accesses to this space to be enabled or disabled using the **Bit Set or Bit Clear Registers**.

The following registers are located in the carrier's Short (A16) I/O space:

- Software reset can be issued to reset the FPGA Logic and all IP modules present on the carrier board via the **Status Register**.
- Monitoring the error signal received from each IP module is possible via the **IP Error Register**.
- Configuration of VME64x bus A24 standard address space for optional Memory Space on each IP module is possible. Memory Space access to the IP modules can be individually enabled via the **IP Memory Enable Register**. The base address and address range (size) is programmed via carrier registers **IP_A and IP_B Memory Base Address & Size Registers**. The address size can be selected from 1M, 2M, 4M, or 8M bytes.
- Enabling of VME64x bus interrupt requests from each IP module via the **IP Interrupt Enable Register** is possible. The desired VME64x bus interrupt level desired can be set (via the **Interrupt Level Register**), and pending interrupts can be monitored and cleared via carrier registers **IP Interrupt Pending and IP Interrupt Clear Registers**.
- Lastly, pending interrupts can be globally monitored and released to the VME64x bus via the **Status Register**.

IP Logic Interface

The IP logic interface is also implemented within the carrier board's FPGA. The carrier board implements ANSI/VITA 4 1995 for 8 MHz operation only. Industrial I/O Pack logic interface specification includes four IP logic interfaces on an AVME9675. The VME64x bus address and data lines are linked to the address and data of the IP logic interface. This link is implemented and controlled by the carrier board's FPGA.

The VME64x bus to IP logic interface link allows a VME64x bus master to :

- Access up to 32 ID Space bytes for IP module identification (ID ROM Data Format I) via D08(O) data transfers using VME64x bus A16 short address space.
- Access up to 128 I/O Space bytes of IP data via D16/D08(EO) data transfers using VME64x bus A16 short address space.
- Access up to 8Mbytes of IP data mapped to Memory Space via D16 or D08(EO) transfers using VME64x bus A24 standard address space.
- Respond to two IP module interrupt requests per IP with software programmable VME64x bus interrupt levels.

Carrier Board Clock Circuitry

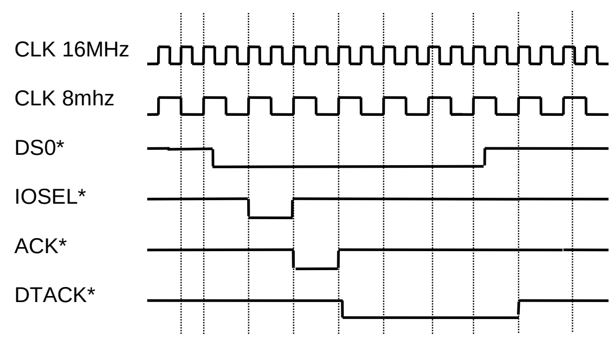
Separate 8MHz IP clocks are driven to each IP module. All clock lines include series damping resistors to reduce clock overshoot and undershoot, and similar length PC board trace lengths are employed to minimize clock skew between the IP modules.

IP Read and Write Cycle Timing

An IP read or write cycle is carried out via a VME64x bus A24 or A16 data transfer. The data transfer starts when the VME64x bus Data Strobe 0 (DS0*) goes active and ends when the carrier board drives Data Transfer Acknowledge (DTACK*) active back to the VME64x bus master. The carrier board typically has a 450ns IP module data transfer cycle time.

A typical IP module data transfer cycle is described here, starting with DS0* going active. DS0* is sampled on the rising edge of the system 16MHz clock edge after it goes active. All operations are then synchronized to the IP 8MHz clock as required by the IP module specification. Thus, typically one 8MHz clock cycle later, an IP select line goes active (IOSEL*, IDSEL*, MEMSEL*, or INTSEL*) and is held active for one clock cycle. With no IP wait states, an active IP Acknowledge (ACK*) signal is driven by the IP on the next rising edge of the 8MHz clock. The carrier board samples ACK* one clock cycle later and then asserts DTACK* ending the VME64x bus data transfer.

Timing Diagram



A Time-out error will result for the following condition if Auto Acknowledge is disabled in the carrier status register.

If a select line (IOSEL*, IDSEL*, INTSEL*, or MEMSEL*) is driven active to an IP module and the IP module does not return ACK* active, then DTACK* will also not be generated by the carrier board. This will cause a bus transfer time-out error and the VME64x bus system may need to be reset. In addition, the carrier board will remain in a state waiting for ACK* from the IP. To take it out of this state, a software reset can be issued.

When an IP module places data on the bus, for all data read cycles, any undriven data lines are read by the VME64x bus as high because of pull-up resisters on the carrier board's data bus.

VME64x bus Interrupter

Interrupts are initiated from an interrupting IP module. However, the carrier board will only pass an interrupt generated by an IP module to the VME64x bus if the carrier board has been first enabled for interrupts. Each IP module can initiate two interrupts which can be individually enabled on the carrier board. After interrupts are enabled on the carrier board via the Interrupt Enable Register (see section 3 for programming details), an IP generated interrupt is recognized by the carrier board and is recorded in the carrier board's Interrupt Pending Register.

A carrier board pending interrupt will cause the board to release the interrupt to the VME64x bus provided the Global Interrupt Enable bit of the carrier's Status Register has been enabled (see section 3 for programming details).

The carrier board releases the interrupt to the VME64x bus by asserting the interrupt request level as pre-programmed in the carrier's Interrupt Level Register. The carrier board's interrupt logic then monitors the VME64x bus Interrupt Acknowledge Input (IACKIN*) signal.

An active IACKIN* signal, detected by the carrier board, is either passed to Interrupt Acknowledge Output (IACKOUT*) or consumed by the carrier board. IACKIN* is passed to IACKOUT* if the VME64x bus interrupt level does not match that programmed into the carrier's Interrupt Level Register. If a match is detected, the carrier board responds to the interrupt by consuming IACKIN*.

The carrier board also responds to an interrupt by driving IP Interrupt Select (INTSEL*) active to the IP that generated the interrupt, provided only one interrupt has been issued. If two or more interrupts occur at the same time, then INTSEL* is driven active to the IP with the highest priority. The carrier board will prioritize the requests based on the last interrupt serviced. The last interrupt serviced will be given the lowest priority. See section 3 for more detail. The IP module responds by placing the interrupt vector on the data bus and asserts ACK*. The carrier then asserts DTACK* active, and the VME64x bus master responds by executing the code at the address of the interrupt vector.

The user written interrupt routine should include code to clear the carrier board's pending interrupt via the carrier's Interrupt Clear Register (see section 3) since the interrupt release mechanism is Release on Register Access (RORA) type. In addition, the IP module may need similar attention (see your IP module documentation).

Power Failure Monitor

The carrier board contains a 5 volts undervoltage monitoring circuit which provides a reset to the IP modules when the 5 volt power drops below 4.27 volts, typical / 4.15 volts minimum. This circuitry is implemented per the Industrial I/O Pack specification.

Access LEDs and Pulse Stretcher Circuitry

An LED display and pulse stretcher circuit is dedicated to each IP module for indication of a data transfer to/from the corresponding IP module. An IP acknowledged data transfer activates the pulse stretcher circuit. The pulse stretcher's circuit is programmed to illuminate the LED for a duration of 0.125 seconds, typical.

Power Supply Filters

Power line filters are dedicated to each IP module for filtering of the +5, +12, and -12 volt supplies. The power line filters are a T type filter circuit comprising ferrite bead inductors and a feed-thru capacitor. The filters provide improved noise performance as is required on precision analog IP modules. Specifically, the filters are typically capable of over 40dB of insertion loss for undesirable noise and oscillations in the 100MHz frequency range and over 20dB of insertion loss for noise and oscillations in the 10MHz frequency range.

Power Supply Fuses

Power line fuses are dedicated to each IP module for fusing of the +5, +12, and -12 volt supplies. The +5 volt supply uses a 2 Amp fuse and the +/- 12 volt supplies use a 1 Amp fuse. These fuses are needed to protect the power suppy in the VME64x bus cage system.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your IP module to verify that it is correctly configured. Replacement of the carrier and/or IP with one that is known to work correctly is a good technique to isolate a faulty board.

In order to perform accesses to the carrier and IP module in the A16 short space, the A16 base address must be configured first within the CR/CSR space, and the module enabled. The CR/CSR space's base address is derived from geographical addressing signals supplied by the VME64x backplane. If there is a problem with the geographical addressing signals, the carrier should detect "bad parity". In this case, the CR/CSR base address will be set to decimal 30 (0x1E) as recommended by the VME64x standard.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

PHYSICAL

Physical Configuration...................... AVME9675 (6U)
Length.. 9.187 inches (233.3 mm)
Width... 6.299 inches (160.0 mm)
Board Thickness........................ 0.062 inches (1.59 mm)
Max Component Height.............. 0.550 inches (13.97 mm)
Recommended Card Spacing..... 0.800 inches, (20.32mm)

Connectors:
P1 & P2 (VME64x bus)............. DIN 41612 160-pin Type C, Level II.
P0 (VME64x bus)...................... J3 Type B, Right-Angle Female 95-contacts, with upper ground shield.
P3,5,7,9 (IP Field I/O)................ 50-pin male plug header (AMP 173280-3 or equivalent).
P4,6,8,10 (IP Logic Interface)... 50-pin male plug header (AMP 173280-3 or equivalent).

Power:
Board power requirements are a function of the installed IP modules. This specification lists currents for the carrier boards only. The carrier boards individually filter and provide +5V, +12V and -12V power to each IP from the VME64x bus. Note that the VME64x bus standard does not support +15V and -15V supplies, but the carrier boards are designed to handle these if needed for unique situations.

The power supply filters are typically capable of over 40dB of insertion loss for undesirable noise and oscillations in the 100MHz frequency range and over 20dB of insertion loss for noise and oscillations in the 10MHz frequency range.

Power line fuses are dedicated to each IP module for fusing of the +5, +12, and -12 volt supplies. These fuses are used to protect the power suppy in the VME64x bus cage system.

The power failure monitor circuit provides a reset to IP modules when the 5 volt power drops below 4.27 volts, typically / 4.15 volts minimum.

Currents specified are for the <u>carrier board only</u>, add the IP module currents for the total current required from each supply.

+5 Volts (±5%).................... AVME9675-X 350 mA, Typical
525 mA, Maximum.
Maximum rise time of 100 m Seconds.
+12 Volts (±5%) or
+15 Volts (±5%).................. 0mA (Not Used).
-12 Volts (±5%) or
-15 Volts (±5%)................... 0mA (Not Used).

VME64x bus COMPLIANCE

Specification.............................. This device meets written VME specifications per VME64 ANSI/VITA 1-1994, VME64 Extensions ANSI/VITA 1.1-1997, and IP I/O Mapping to VME64x ANSI/VITA 4.1-1996.
Data Transfer Bus..................... A24/A16:D16/D08 (EO) DTB slave; supports Read-Modify-Write cycles.
VME64x bus Access Time......... 450nS Typical (all carrier board registers); measured from the falling edge of DSx* to the falling edge of

DTACK*. 450nS Typical IP registers with no wait states).
See IP specifications for information on wait states. IP register access time will increase by the number of wait states multiplied by 125nS (the period of the 8 Mhz clock).

VME64x bus Address Modifier Codes:

Short I/O (A16) Space................ Base address is relocatible with selection in CR/CSR space. Occupies 1K byte. Responds to either address modifier 29H or 2DH in the VME64x bus short I/O space for carrier board registers and IP I/O and ID spaces.

Standard Address (A24) Space.. Responds to address modifier 2FH in the VME64x bus standard address space to provide access to CR/CSR space locations. Base address of this space is determined by geographical address signals provided by the VME64x backplane.

Also responds to both address modifiers 39H & 3DH in the VME64x bus standard address space when such accesses to IP memory are enabled via programmable registers on the carrier board. Base addresses and sizes of IP memory are programmable from 1M to 8M bytes.

Interrupts................................... Creates I(1-7) programmable request levels (up to two requests sourced from each IP). D16/D08(O) interrupter (interrupt vectors come from IP modules). Carrier registers for control & status monitoring. Interrupt release mechanism is Release On Register Access (RORA) type.

INDUSTRIAL I/O PACK COMPLIANCE

Specification................................This device meets or exceeds all written Industrial I/O Pack specifications per ANSI/VITA 4 1995 (For 8 Mhz operation only) and IP I/O Mapping to VME64x (ANSI/VITA 4.1-1996).

Electrical/Mechanical Interface... AVME9675 supports up to four single-size IP modules (A-D), or two double-size. 32-bit IP modules are Not Supported.

I/O Space................................... A16/D16 or D08(EO); supports 128 byte values per IP.

ID Space.................................... A16/D08(O); supports 32 bytes per IP (consecutive odd-byte addresses) ID Data Format I. D16 is also supported with pull-ups on the carrier board holding the upper 8-bits high.

Memory Space........................... A24/D16 or D08(EO); supports 1M to 8M bytes per IP module.

Interrupts.................................... Supports two interrupt requests per IP and interrupt acknowledge cycles, D16/D08(O).

Access LED (Illuminate duration).................... 0.125 second, typical

ENVIRONMENTAL

Operating Temperature............... 0 to +70°C. -40 to +85°C (E versions) Note that visual LED performance May be degraded below -20°C.

Relative Humidity........................ 5-95% non-condensing

Storage Temperature.................. -55 to +100°C.

Non-Isolated............................... VME64x bus and IP module logic commons have a direct electrical connection. As such, unless the IP module provides isolation between the logic and field side, the field I/O connections are not isolated from the VME64x bus.

Radiated Field Immunity (RFI).... Designed to comply with IEC1000-4-3 Level 3 (10V/m at frequencies 27MHz to 500MHz) and European Norm EN50082-1.

Electromagnetic Interference Immunity (EMI)........................... No digital upset under the influence of EMI from switching solenoids, commutator motors, and drill motors.

Electrostatic Discharge Immunity (ESD).......................... Complies with IEC1000-4-2 Level 1 (2KV direct contact discharge) at field input/output terminals and European Norm EN50082-1.

Electric Fast Transient Immunity EFT............................. Complies with IEC1000-4-4 Level 2 (0.5KV at field input and output terminals) and European Norm EN50082-1.

Radiated Emissions.................... Meets or exceeds European Norm EN50081-1 for class B equipment.

APPENDIX

CABLE: MODEL 5028-187 (SCSI-2 to Flat Ribbon, Shielded)

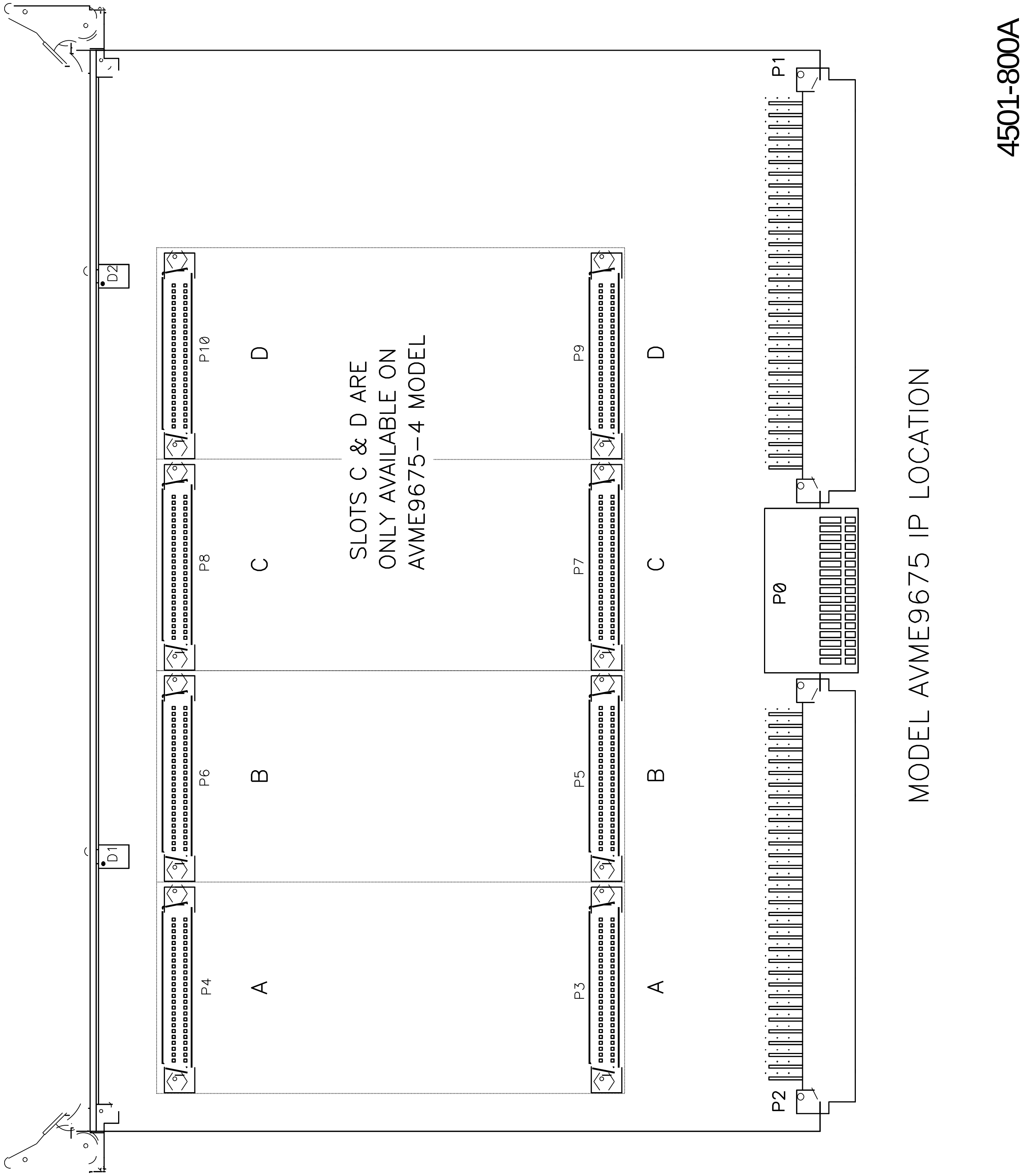
Type: Round shielded cable, 50-wires (SCSI-2 male connector at one end and a flat female ribbon connector at the other end). The cable length is 2 meters (6.56 feet). This shielded cable is recommended for all I/O applications (both digital I/O and precision analog I/O).
Application: Used to connect Model 5025-552 termination panel to the TRANS-200 Transition Module. The transition module then connects to all four IP module slots to the rear of the AVME9670 or AVME9675-4 (Slots A-D). The AVME9675-2 uses IP slots A-B.
Length: Standard lenght is 2 meters (6.56 feet). Consult factory for other lenghts. It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50 conductors, 28 AWG on 0.050 inch centers (permits mass termination for IDC connectors), foil/braided shield inside a PVC jacket.
Connectors: (One End): SCSI-2, 50-pin male connector with backshell and spring latch hardware.
(Other End): IDC, 50-pin female connector with strain relief.
Keying: The SCSI-2 connector has a “D Shell” and the IDC connector has a polarizing key to prevent improper installation.
Schematic and Physical Attributes: See Drawing 4501-758.
Electrical Specifications: 30 VAC per UL and CSA (SCSI-2 connector spec.’s). 1 Amp maximum at 50% energized (SCSI-2 connector spec.’s).
Operating Temperature: -20°C to +80°C.
Storage Temperature: -40°C to +85°C.
Shipping Weight: 1.0 pound (0.5Kg), packed.

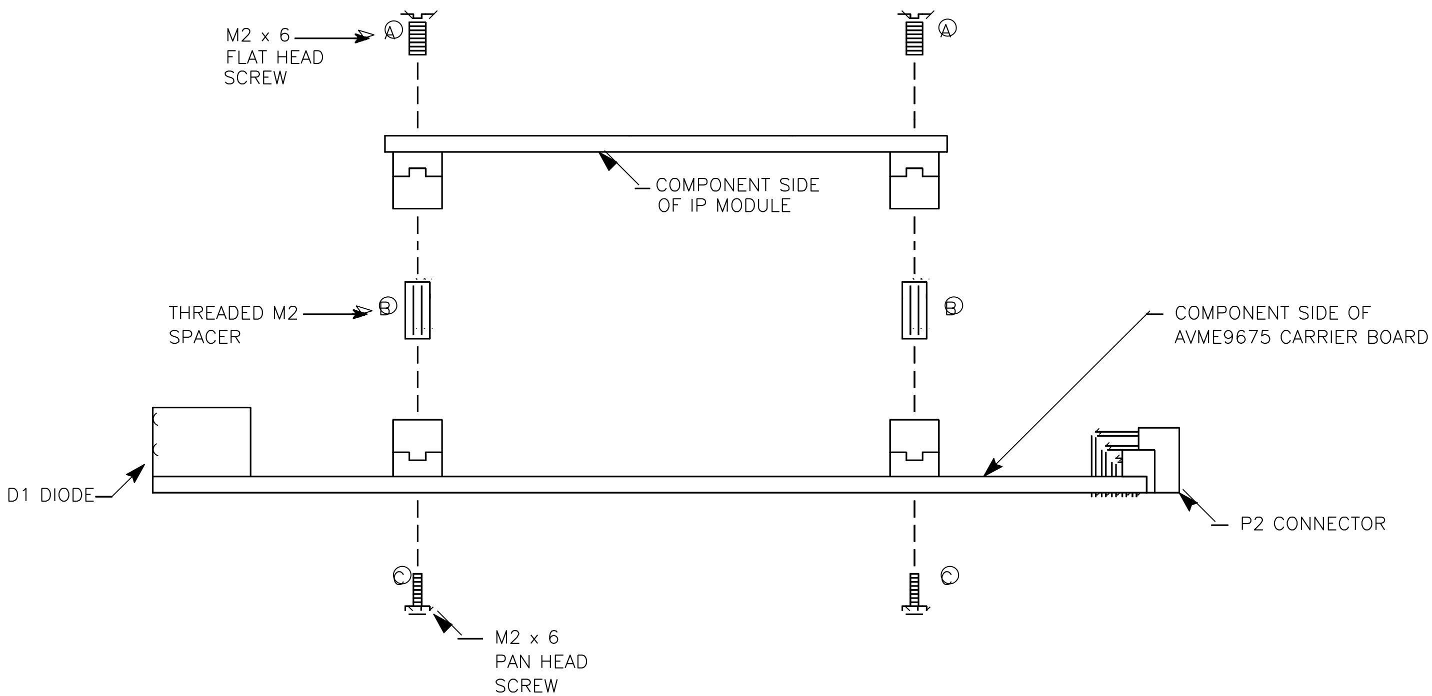
TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For Carrier Boards
Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the TRANS-200 transition module via a cable (Model 5028-187). Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Connections to TRANS-200 Transition Module: P1, 50-pin male header with strain relief ejectors. Use Acromag 5028-187 cable to connect panel to TRANS-200 transition module. Keep cable as short as possible to reduce noise and power loss.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight : 1.25 pounds (0.6kg) packed.

VME64x TRANSITION MODULE: MODEL TRANS-200

Type: Transition module for AVME9670, AVME9675-4, and AVME9675-2 boards.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME64x card cages. This module is available for use in card cages which provide rear exit for I/O connections via 80 mm wide transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VME64x bus mechanical dimensions and IEEE Standard (1101.11-1998), for 80 mm depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9670 & AVME9675 boards within card cage, via connectors RP0 and RP2.
Schematic and Physical Attributes: See Drawing 4501-760.
Electrical Specifications: 30 VAC per UL and CSA (SCSI-2 connector spec.’s). 1 Amp maximum at 50% energized (SCSI-2 connector spec.’s).
Field Wiring: Four SCSI-2, 50-pin female connectors (AMP 787082-5 or equivalent) employing latch blocks and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via round shielded cable (Model 5028-187).
Connections to AVME9670 & AVME9675: Connections are made though the PC board connectors RP0 (95 pin female with upper ground shield) and RP2 (160 pin female). The transition module plugs directly behind the AVME9670 or AVME9675 board into the VME64x bus backplane within the card cage system.
Mounting: Transition module is inserted into a 6U-size, 80 mm width slot at the rear of the VME64Xbus card cage. (Directly behind AVME9670 or AVME9675 board).
Printed Circuit Board: Eight-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +85°C.
Storage Temperature: -40°C to +85°C.
Shipping Weight: 1.25 pounds (0.6Kg) packed.


4501-800A
MODEL AVME9675 IP LOCATION
SLOTS C & D ARE
ONLY AVAILABLE ON
AVME9675-4 MODEL
P1
P0
P2
P10
P9
P8
P7
P6
P5
P4
P3
D
C
B
A
D2
D1

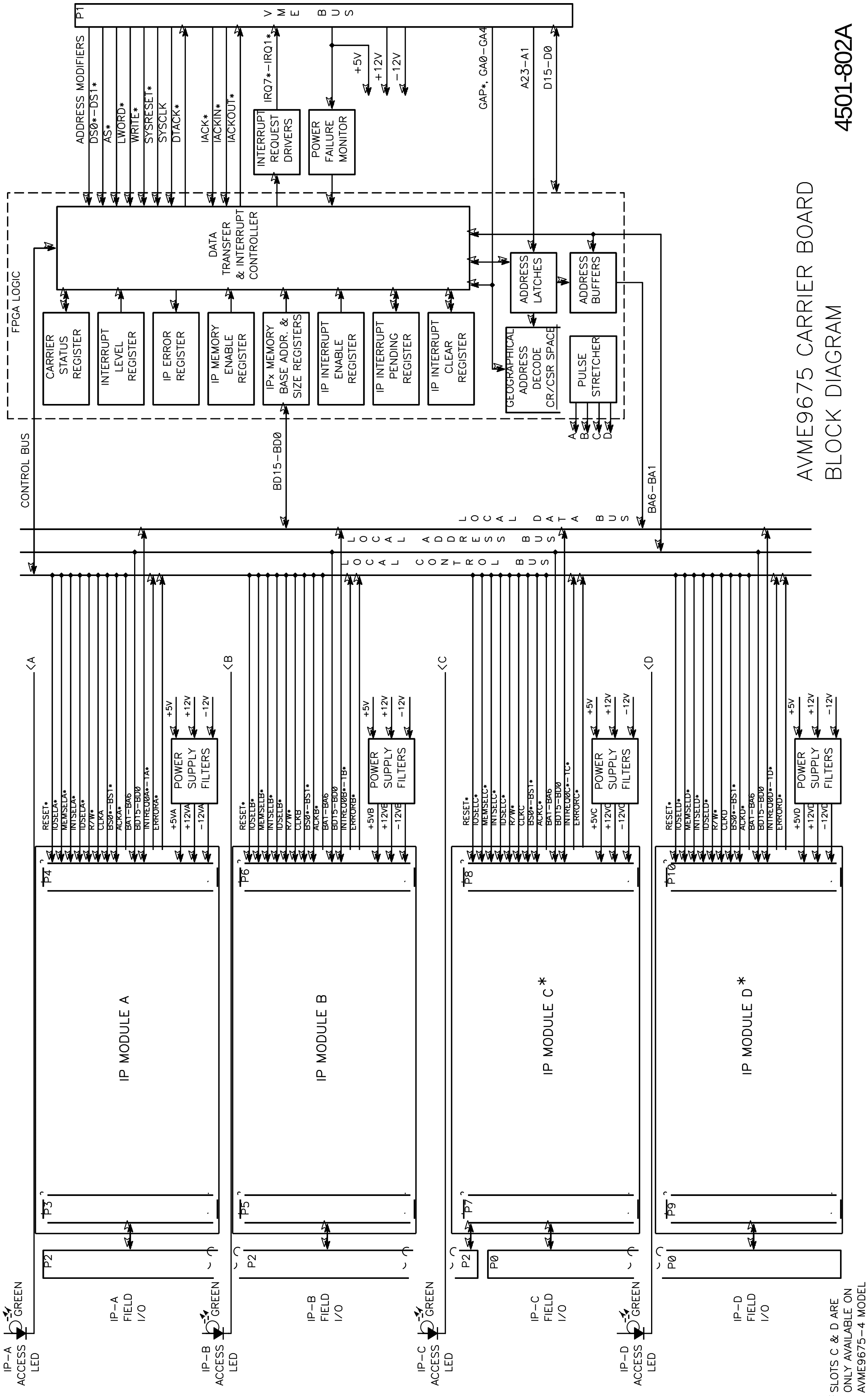


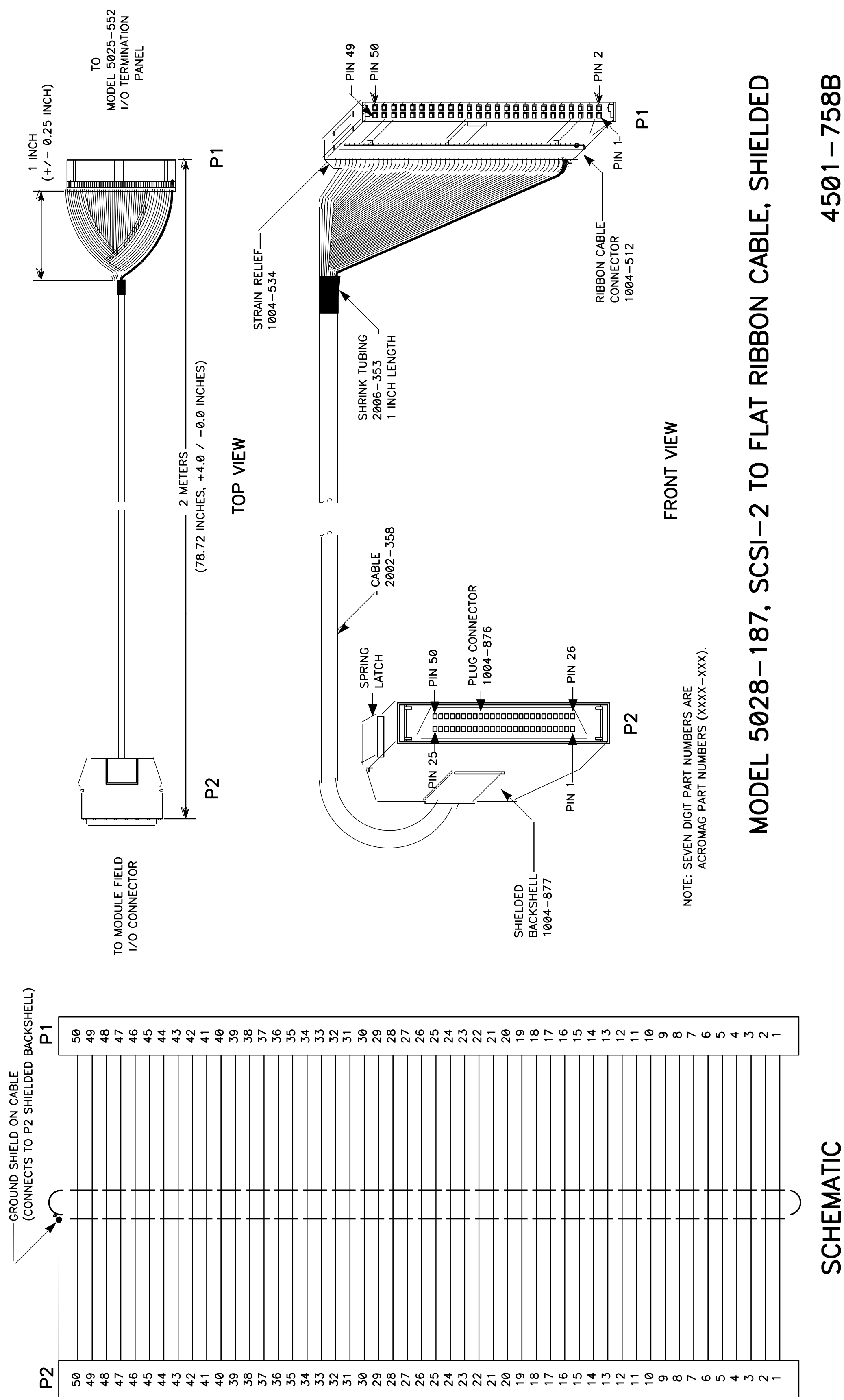
ASSEMBLY PROCEDURE:

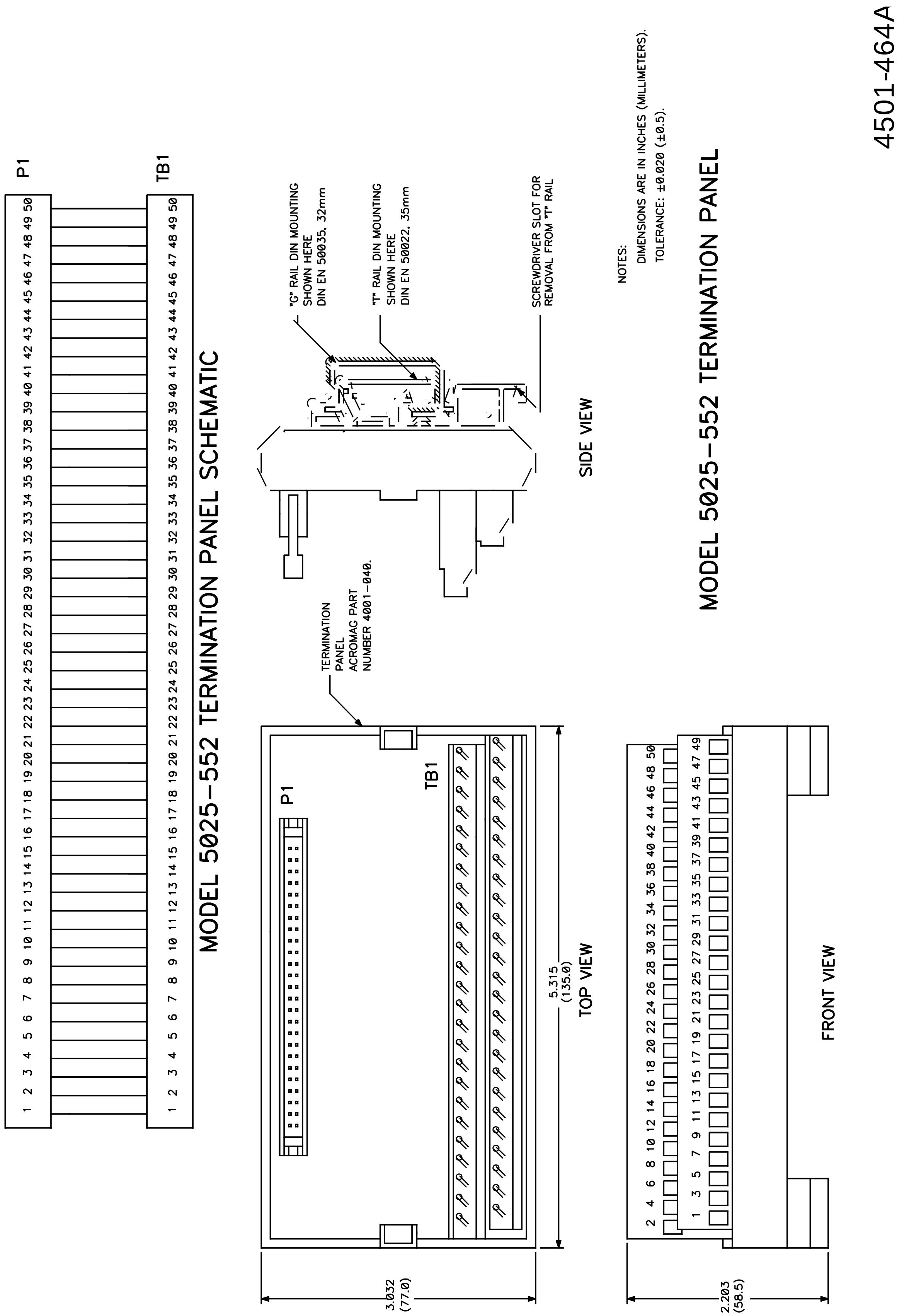
1. THREADED SPACERS ARE PROVIDED IN TWO DIFFERENT LENGTHS. THE SHORTER LENGTH IS FOR USE WITH AVME9675 CARRIER BOARD (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES).

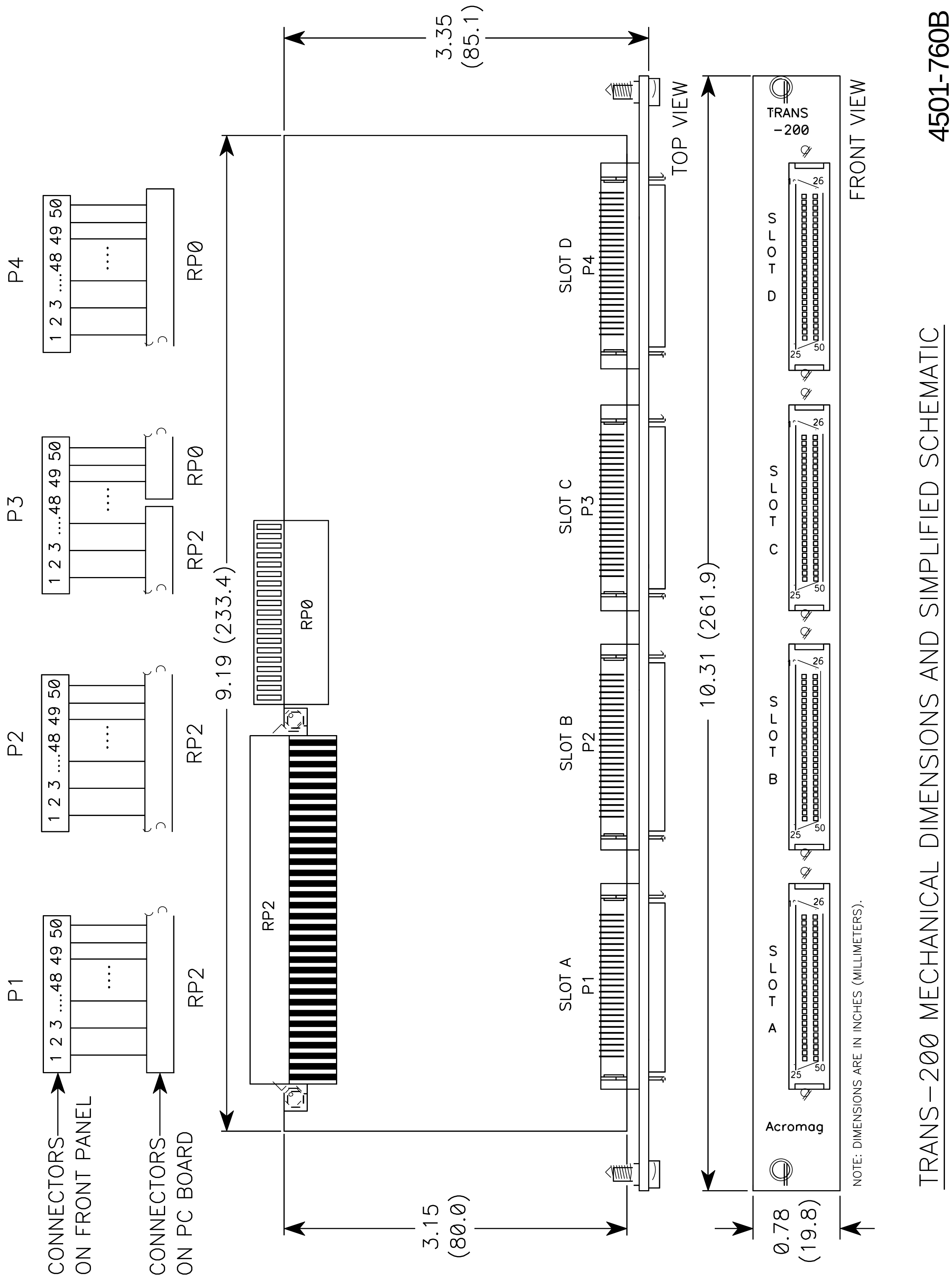
IP MODULE TO AVME9675 CARRIER BOARD MECHANICAL ASSEMBLY

4501-801A


P1
VME BUS
ADDRESS MODIFIERS
DS0*-DS1*
AS*
LWORD*
WRITE*
SYSRESET*
SYSCLK
DTACK*
IACK*
IACKIN*
IACKOUT*
IRQ7*-IRQ1*
+5V
+12V
-12V
GAP*, GA0-GA4
A23-A1
D15-D0
INTERRUPT REQUEST DRIVERS
POWER FAILURE MONITOR
FPGA LOGIC
DATA TRANSFER & INTERRUPT CONTROLLER
CARRIER STATUS REGISTER
INTERRUPT LEVEL REGISTER
IP ERROR REGISTER
IP MEMORY ENABLE REGISTER
IPx MEMORY BASE ADDR. & SIZE REGISTERS
IP INTERRUPT ENABLE REGISTER
IP INTERRUPT PENDING REGISTER
IP INTERRUPT CLEAR REGISTER
ADDRESS LATCHES
ADDRESS BUFFERS
GEOGRAPHICAL ADDRESS DECODE CR/CSR SPACE
PULSE STRETCHER
CONTROL BUS
BD15-BD0
BA6-BA1
LOCAL DATA BUS
LOCAL ADDRESS BUS
LOCAL CONTROL BUS
POWER SUPPLY FILTERS
IP MODULE A
IP MODULE B
IP MODULE C*
IP MODULE D*
IP-A FIELD I/O
IP-B FIELD I/O
IP-C FIELD I/O
IP-D FIELD I/O
IP-A ACCESS LED
IP-B ACCESS LED
IP-C ACCESS LED
IP-D ACCESS LED
GREEN
AVME9675 CARRIER BOARD BLOCK DIAGRAM
4501-802A
* SLOTS C & D ARE ONLY AVAILABLE ON AVME9675-4 MODEL


TO MODEL 5025-552 I/O TERMINATION PANEL
1 INCH (+/- 0.25 INCH)
P1
2 METERS (78.72 INCHES, +4.0 / -0.0 INCHES)
TOP VIEW
P2
TO MODULE FIELD I/O CONNECTOR
PIN 49
PIN 50
PIN 2
P1
PIN 1
STRAIN RELIEF 1004-534
SHRINK TUBING 2006-353 1 INCH LENGTH
RIBBON CABLE CONNECTOR 1004-512
FRONT VIEW
CABLE 2002-358
SPRING LATCH
PIN 50
PLUG CONNECTOR 1004-876
PIN 26
P2
PIN 25
PIN 1
SHIELDED BACKSHELL 1004-877
NOTE: SEVEN DIGIT PART NUMBERS ARE ACROMAG PART NUMBERS (XXXX-XXX).
MODEL 5028-187, SCSI-2 TO FLAT RIBBON CABLE, SHIELDED
4501-758B
GROUND SHIELD ON CABLE (CONNECTS TO P2 SHIELDED BACKSHELL)
P1
50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
P2
50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
SCHEMATIC


P1
TB1
MODEL 5025-552 TERMINATION PANEL SCHEMATIC
"G" RAIL DIN MOUNTING SHOWN HERE DIN EN 50035, 32mm
"T" RAIL DIN MOUNTING SHOWN HERE DIN EN 50022, 35mm
SCREWDRIVER SLOT FOR REMOVAL FROM "T" RAIL
NOTES:
DIMENSIONS ARE IN INCHES (MILLIMETERS).
TOLERANCE: ±0.020 (±0.5).
SIDE VIEW
MODEL 5025-552 TERMINATION PANEL
4501-464A
TERMINATION PANEL ACROMAG PART NUMBER 4001-040.
TOP VIEW
5.315 (135.0)
3.032 (77.0)
FRONT VIEW
2.203 (58.5)


TRANS–200 MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC
4501-760B
NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).
3.35 (85.1)
3.15 (80.0)
9.19 (233.4)
10.31 (261.9)
0.78 (19.8)
TOP VIEW
FRONT VIEW
TRANS -200
SLOT A P1
SLOT B P2
SLOT C P3
SLOT D P4
RP0
RP2
Acromag
P1
P2
P3
P4
1 2 3 ....48 49 50
CONNECTORS ON FRONT PANEL
CONNECTORS ON PC BOARD

Notes:

Notes:

Revision History

The following table shows the revision history for this document:

Release Date	Version	EGR/DOC	Description of Revision
28 NOV 2018	D	LMP/ARP	Removed Industrial I/O Pack Software Library information.