AP500/AP520/AP521 AcroPack
Serial Communication Module

USER'S MANUAL

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1.0 GENERAL INFORMATION

1.1 Intended Audience

This user's manual was written for technically qualified personnel who will be working with I/O devices using the AcroPack module. It is not intended for a general, non-technical audience that is unfamiliar with AcroPack devices and their application.

1.2 Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag.

1.2.1 Trademark, Trade Name and Copyright Information

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1.2.2 Class A Product Warning

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

1.2.3 Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

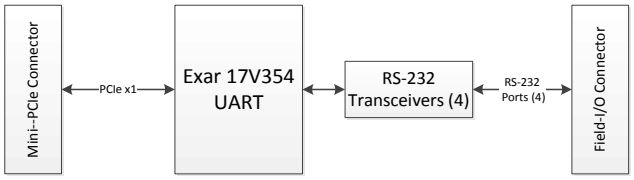
1.3 AcroPack Information – All Models

The AcroPack IO modules are based on the PCI Express Mini Card Electromechanical specification and are 70mm in length with an additional 100 pin field I/O connector.

The AcroPack is 19.05mm longer than the full length mini PCIe card at 50.95mm. It has the same mPCIe board width of 30mm and uses the same mPCIe standard board hold down standoff and screw keep out areas.

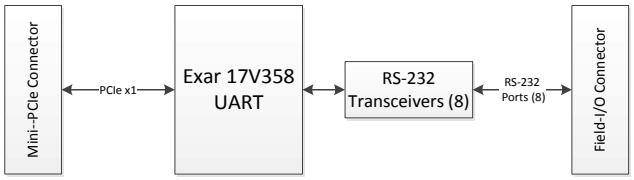
The AP500 uses the 16550-compatible Exar 17v354 UART and contains four RS-232 serial communication ports that provide full EIA/TIA-232E modem line support, including RTS, CTS, DTR, DSR, DCD, and RI.

Figure 1.1 - AP500 Block Diagram



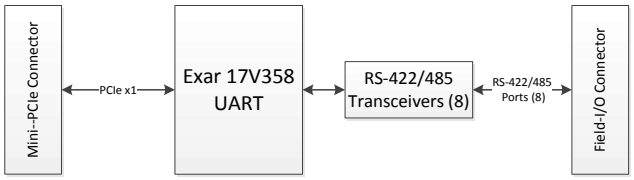
The AP520 uses the 16550-compatible Exar 17v358 UART and contains eight RS-232 serial communication ports that provide EIA/TIA-232E modem line support, including RTS, and CTS.

Figure 1.2 - AP520 Block Diagram



The AP521 uses the 16550-compatible Exar 17v358 UART and contains eight RS-422/485 serial communication ports that provide EIA-TIA-422B or full duplex EIA-485 line support. Termination and biasing resistors are installed by default. For non-terminated ports please consult the factory.

Figure 1.3 - AP521 Block Diagram



1.3.1 Ordering Information

The AcroPack ordering options are given in the following table.

Table 1.1 Ordering Options

Model Number	*#/Type of Serial Ports*	*Operational Temperature Range*
AP500E-LF[1,2]	4x RS-232	-40°C to 85°C[1,2]
AP520-64E-LF[1,2]	8x RS-232	-40°C to 85°C[1,2]
AP521-64E-LF[1,2]	8x RS-422/485	-40°C to 85°C[1,2]

Note 1: For all models *listed - all standoffs and screws required for an air cooled application are provided with the carrier.*

Note 2: *A conduction cooled application will require purchase of AcroPack Accessory **AP-CC-01** (Conduction Cool Kit).*

1.3.2 Key Features

- **High Density** – Provides 4 (AP500) or 8 (AP520/521) serial ports on each module.
- **16550 compatible** – Exar Quad or Octal UART with 16550-compatible register set.
- **256-Byte FIFO Buffers** – 256-byte TX and RX FIFOs with programmable trigger levels.
- **Programmable Baud Rate** – Each individual channel has its own programmable baud rate generator with fractional divisor. While the UART supports data rates up to 31.25Mbps, the serial transceivers only support data rates up to 500kbps (AP500/520) or 20Mbps (AP521).
- **Interrupt Support** – Individually controlled transmit, receive, line status, and data set interrupts may be generated.
- **General Purpose Timer/Counter** – This 16-bit timer/counter uses an internal 125MHz clock as the clock source and can be set to be a single-shot or re-triggerable and is capable of generating an interrupt.
- **Individual Modem Control Signals** – The AP500 module provides all modem control signals: RTS, CTS, DTR, DSR, CD, and RI. The AP520 only provides RTS and CTS.
- **PCIe Bus** – The AP module includes a PCI Express Generation 1 interface operating at a bus speed of 2.5 Gbps with one lane in each direction.

- **Compatibility** – PCI Express Base Specification v2.0 compliant PCI Express Endpoint.

1.4 Signal Interface Products

This AcroPack module will mate directly to all Acromag AP carriers. Once connected, the module is accessed via a front panel connector.

The cables and termination panels are also available. For optimum performance with the AP5XX communication modules, use of the shortest possible length of shielded I/O cable is recommended.

1.5 Software Support

The AcroPack series products require support drivers specific to your operating system. Supported operating systems include: Linux, Windows, and VxWorks.

Windows®

Acromag provides software products (sold separately) to facilitate the development of Windows® applications interfacing with AcroPack modules, VPX I/O board products, and PCIe I/O Cards. This software (model APSW-API-WIN) consists of low-level drivers and Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

VxWorks®

Acromag provides a software product (sold separately) consisting of VxWorks® software. This software (Model APSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

Linux®

Acromag provides a software product consisting of Linux® software. This software (Model APSW-API-LNX) is composed of Linux® libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

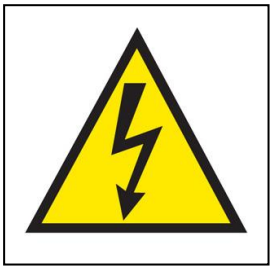
1.6 References

The following resources regarding AcroPack modules are available for download on Acromag's website or by contacting your sales representative.

- PCI Express MINI Card Electromechanical Specification, REV 1.2 http://www.pcisig.com
- Exar 17v354 High Performance Quad PCI Express UART datasheet
- Exar 17v358 High Performance Octal PCI Express UART datasheet

2.0 PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.

WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

2.1 Unpacking and Inspecting

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static-sensitive components and should only be handled at a static-safe workstation.

2.2 Installation Considerations

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

Refer to the specifications section for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

In an air cooled assembly, adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

In a conduction cooled assembly, adequate thermal conduction must be provided to prevent a temperature rise above the maximum operating temperature.

2.3 Board Configuration

Power should be removed from the board when installing AP modules, cables, termination panels, and field wiring. Model AP500/520/521 UART communication boards have no hardware jumpers or switches to configure.

2.4 Field I/O Connector

A field I/O interface connector provides a mating interface between the AP modules and the carrier board. The 100 pin ST5-50-1.50-L-D-P-TR Samtec connector is used on the AcroPack module as board to board interconnect. This connector will mate with the 100 pin SS5-50-3.00-L-D-K-TR Samtec connector on the carrier. The stack height is 4.5mm.

Threaded metric M2.5 screws and spacers are supplied with the module to provide additional stability for harsh environments.

Pin assignments are unique to each AP5XX model. Table 2.1 lists signal pin assignments for the 100-pin module/carrier field I/O connectors, as well as the 50-pin and 68-pin CHAMP and ribbon I/O connectors on the carrier.

Table 2.1 Field I/O Connector Pin Assignments

Module/Carrier Field I/O Connector Pin #	Generic Field I/O Connector Pin Name	Carrier 50-pin Ribbon I/O Connector Pin#	Carrier 50-pin CHAMP I/O Connector Pin#	AP500 Module Function	AP520 Module Function	AP521 Module Function
2	Field I/O 1	1	1	GND	GND	GND
1	Field I/O 2	2	26	RI_A*	TXD_A	TXD-_A
4	RSVD/ISOL					
3	RSVD/ISOL					
6	Field I/O 3	3	2	DTR_A*	RXD_A	TXD+_A
5	Field I/O 4	4	27	CTS_A*	RTS_A*	RXD-_A
8	RSVD/ISOL					
7	RSVD/ISOL					
10	Field I/O 5	5	3	TXD_A	CTS_A*	RXD+_A
9	Field I/O 6	6	28	RTS_A*	GND	GND
12	RSVD/ISOL					
11	RSVD/ISOL					
14	Field I/O 7	7	4	RXD_A	TXD_B	TXD-_B
13	Field I/O 8	8	29	DSR_A*	RXD_B	TXD+_B
16	RSVD/ISOL					
15	RSVD/ISOL					
18	Field I/O 9	9	5	DCD_A*	RTS_B*	RXD-_B
17	Field I/O 10	10	30	GND	CTS_B*	RXD+_B
20	RSVD/ISOL					
19	RSVD/ISOL					
22	Field I/O 11	11	6	RI_B*	GND	GND
21	Field I/O 12	12	31	DTR_B*	TXD_C	TXD-_C
24	RSVD/ISOL					
23	RSVD/ISOL					
26	Field I/O 13	13	7	CTS_B*	RXD_C	TXD+_C
25	Field I/O 14	14	32	TXD_B	RTS_C*	RXD-_C
28	RSVD/ISOL					
27	RSVD/ISOL					
30	Field I/O 15	15	8	RTS_B*	CTS_C*	RXD+_C
29	Field I/O 16	16	33	RXD_B	GND	GND
32	RSVD/ISOL					
31	RSVD/ISOL					
34	Field I/O 17	17	9	DSR_B*	TXD_D	TXD-_D
33	Field I/O 18	18	34	DCD_B*	RXD_D	TXD+_D
36	RSVD/ISOL					

Module/Carrier Field I/O Connector Pin #	Generic Field I/O Connector Pin Name	Carrier 50-pin Ribbon I/O Connector Pin#	Carrier 50-pin CHAMP I/O Connector Pin#	**AP500** Module Function	**AP520** Module Function	**AP521** Module Function
35	RSVD/ISOL					
38	Field I/O 19	19	10	GND	RTS_D*	RXD-_D
37	Field I/O 20	20	35	GND	CTS_D*	RXD+_D
40	RSVD/ISOL					
39	RSVD/ISOL					
42	Field I/O 21	21	11	GND	GND	GND
41	Field I/O 22	22	36	GND	TXD_E	TXD-_E
44	RSVD/ISOL					
43	RSVD/ISOL					
46	Field I/O 23	23	12	GND	RXD_E	TXD+_E
45	Field I/O 24	24	37	GND	RTS_E*	RXD-_E
48	RSVD/ISOL					
47	RSVD/ISOL					
50	Field I/O 25	25	13	GND	CTS_E*	RXD+_E
49	Field I/O 26	26	38	GND	GND	GND
52	RSVD/ISOL					
51	RSVD/ISOL					
54	Field I/O 27	27	14	RI_C*	TXD_F	TXD-_F
53	Field I/O 28	28	39	DTR_C*	RXD_F	TXD+_F
56	RSVD/ISOL					
55	RSVD/ISOL					
58	Field I/O 29	29	15	CTS_C*	RTS_F*	RXD-_F
57	Field I/O 30	30	40	TXD_C	CTS_F*	RXD+_F
60	RSVD/ISOL					
59	RSVD/ISOL					
62	Field I/O 31	31	16	RTS_C*	GND	GND
61	Field I/O 32	32	41	RXD_C	TXD_G	TXD-_G
64	RSVD/ISOL					
63	RSVD/ISOL					
66	Field I/O 33	33	17	DSR_C*	RXD_G	TXD+_G
65	Field I/O 34	34	42	DCD_C*	RTS_G*	RXD-_G
68	RSVD/ISOL					
67	RSVD/ISOL					
70	Field I/O 35	35	18	GND	CTS_G*	RXD+_G
69	Field I/O 36	36	43	RI_D*	GND	GND

Module/Carrier Field I/O Connector Pin #	Generic Field I/O Connector Pin Name	Carrier 50-pin Ribbon I/O Connector Pin#	Carrier 50-pin CHAMP I/O Connector Pin#	AP500 Module Function	AP520 Module Function	AP521 Module Function
72	RSVD/ISOL					
71	RSVD/ISOL					
74	Field I/O 37	37	19	DTR_D*	TXD_H	TXD-_H
73	Field I/O 38	38	44	CTS_D*	RXD_H	TXD+_H
76	RSVD/ISOL					
75	RSVD/ISOL					
78	Field I/O 39	39	20	TXD_D	RTS_H*	RXD-_H
77	Field I/O 40	40	45	RTS_D*	CTS_H*	RXD+_H
80	RSVD/ISOL					
79	RSVD/ISOL					
82	Field I/O 41	41	21	RXD_D	GND	GND
81	Field I/O 42	42	46	DSR_D*	GND	No Connect
84	RSVD/ISOL					
83	RSVD/ISOL					
86	Field I/O 43	43	22	DCD_D*	GND	No Connect
85	Field I/O 44	44	47	GND	GND	No Connect
88	RSVD/ISOL					
87	RSVD/ISOL					
90	Field I/O 45	45	23	GND	GND	No Connect
89	Field I/O 46	46	48	GND	GND	No Connect
92	RSVD/ISOL					
91	RSVD/ISOL					
94	Field I/O 47	47	24	GND	GND	No Connect
93	Field I/O 48	48	49	GND	GND	No Connect
96	RSVD/ISOL					
95	RSVD/ISOL					
98	Field I/O 49	49	25	GND	GND	No Connect
97	Field I/O 50	50	50	GND	GND	No Connect
100	RSVD/ISOL					
99	RSVD/ISOL					

Note: An Asterisk (*) is used to indicate an active-low signal.

Table 2.2 Field I/O 68 PinConnector Assignments

Module/Carrier Field I/O Connector Pin #	Generic Field I/O Connector Pin Name	Carrier 68-pin CHAMP I/O Connector Pin#	AP500 Module Function	AP520 Module Function	AP521 Module Function
2	Field I/O 1	1	GND	GND	GND
1	Field I/O 2	35	RI_A*	TXD_A	TXD-_A
4	RSVD/ISOL				
3	RSVD/ISOL				
6	Field I/O 3	2	DTR_A*	RXD_A	TXD+_A
5	Field I/O 4	36	CTS_A*	RTS_A*	RXD-_A
8	RSVD/ISOL				
7	RSVD/ISOL				
10	Field I/O 5	3	TXD_A	CTS_A*	RXD+_A
9	Field I/O 6	37	RTS_A*	GND	GND
12	RSVD/ISOL				
11	RSVD/ISOL				
14	Field I/O 7	4	RXD_A	TXD_B	TXD-_B
13	Field I/O 8	38	DSR_A*	RXD_B	TXD+_B
16	RSVD/ISOL				
15	RSVD/ISOL				
18	Field I/O 9	5	DCD_A*	RTS_B*	RXD-_B
17	Field I/O 10	39	GND	CTS_B*	RXD+_B
20	RSVD/ISOL				
19	RSVD/ISOL				
22	Field I/O 11	6	RI_B*	GND	GND
21	Field I/O 12	40	DTR_B*	TXD_C	TXD-_C
24	RSVD/ISOL				
23	RSVD/ISOL				
26	Field I/O 13	7	CTS_B*	RXD_C	TXD+_C
25	Field I/O 14	41	TXD_B	RTS_C*	RXD-_C
28	RSVD/ISOL				
27	RSVD/ISOL				
30	Field I/O 15	8	RTS_B*	CTS_C*	RXD+_C
29	Field I/O 16	42	RXD_B	GND	GND
32	RSVD/ISOL				
31	RSVD/ISOL				
34	Field I/O 17	9	DSR_B*	TXD_D	TXD-_D
33	Field I/O 18	43	DCD_B*	RXD_D	TXD+_D

Module/Carrier Field I/O Connector Pin #	Generic Field I/O Connector Pin Name	Carrier 68-pin CHAMP I/O Connector Pin#	AP500 Module Function	AP520 Module Function	AP521 Module Function
36	RSVD/ISOL				
35	RSVD/ISOL				
38	Field I/O 19	10	GND	RTS_D*	RXD-_D
37	Field I/O 20	44	GND	CTS_D*	RXD+_D
40	RSVD/ISOL				
39	RSVD/ISOL				
42	Field I/O 21	11	GND	GND	GND
41	Field I/O 22	45	GND	TXD_E	TXD-_E
44	RSVD/ISOL				
43	RSVD/ISOL				
46	Field I/O 23	12	GND	RXD_E	TXD+_E
45	Field I/O 24	46	GND	RTS_E*	RXD-_E
48	RSVD/ISOL				
47	RSVD/ISOL				
50	Field I/O 25	13	GND	CTS_E*	RXD+_E
49	Field I/O 26	47	GND	GND	GND
52	RSVD/ISOL				
51	RSVD/ISOL				
54	Field I/O 27	14	RI_C*	TXD_F	TXD-_F
53	Field I/O 28	48	DTR_C*	RXD_F	TXD+_F
56	RSVD/ISOL				
55	RSVD/ISOL				
58	Field I/O 29	15	CTS_C*	RTS_F*	RXD-_F
57	Field I/O 30	49	TXD_C	CTS_F*	RXD+_F
60	RSVD/ISOL				
59	RSVD/ISOL				
62	Field I/O 31	16	RTS_C*	GND	GND
61	Field I/O 32	50	RXD_C	TXD_G	TXD-_G
64	RSVD/ISOL				
63	RSVD/ISOL				
66	Field I/O 33	17	DSR_C*	RXD_G	TXD+_G
65	Field I/O 34	51	DCD_C*	RTS_G*	RXD-_G
68	RSVD/ISOL				
67	RSVD/ISOL				
70	Field I/O 35	18	GND	CTS_G*	RXD+_G

Module/Carrier Field I/O Connector Pin #	Generic Field I/O Connector Pin Name	Carrier 68-pin CHAMP I/O Connector Pin#	AP500 Module Function	AP520 Module Function	AP521 Module Function
69	Field I/O 36	52	RI_D*	GND	GND
72	RSVD/ISOL				
71	RSVD/ISOL				
74	Field I/O 37	19	DTR_D*	TXD_H	TXD-_H
73	Field I/O 38	53	CTS_D*	RXD_H	TXD+_H
76	RSVD/ISOL				
75	RSVD/ISOL				
78	Field I/O 39	20	TXD_D	RTS_H*	RXD-_H
77	Field I/O 40	54	RTS_D*	CTS_H*	RXD+_H
80	RSVD/ISOL				
79	RSVD/ISOL				
82	Field I/O 41	21	RXD_D	GND	GND
81	Field I/O 42	55	DSR_D*	GND	No Connect
84	RSVD/ISOL				
83	RSVD/ISOL				
86	Field I/O 43	22	DCD_D*	GND	No Connect
85	Field I/O 44	56	GND	GND	No Connect
88	RSVD/ISOL				
87	RSVD/ISOL				
90	Field I/O 45	23	GND	GND	No Connect
89	Field I/O 46	57	GND	GND	No Connect
92	RSVD/ISOL				
91	RSVD/ISOL				
94	Field I/O 47	24	GND	GND	No Connect
93	Field I/O 48	58	GND	GND	No Connect
96	RSVD/ISOL				
95	RSVD/ISOL				
98	Field I/O 49	25	GND	GND	No Connect
97	Field I/O 50	59	GND	GND	No Connect
100	RSVD/ISOL				
99	RSVD/ISOL				

Note: An Asterisk (*) is used to indicate an active-low signal.

2.5 RS-422/485 Termination (AP521 Only)

The standard AP521 modules have 120ohm termination resistors installed on both line drivers and receivers, as well as 560ohm biasing resistors installed on the line drivers. For modules without termination please consult the factory.

2.6 Noise and Grounding Considerations

The board is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

2.7 Logic Interface Connector

The AP module logic edge connector interfaces to the mating connector on the carrier board. The pin assignments of this connector are standard for all AP modules according to the PCI Express MINI Card Electromechanical Specification, REV 1.2 (with exceptions shown in Table 2.3 and noted below).

Threaded metric M2.5 screws and spacers are supplied with the AP module to provide additional stability for harsh environments (see carrier documentation for assembly details).

Table 2.3 Logic Interface Connections

Pin #	Name	Pin #	Name
51	**+5V**[3]	52	+3.3V[4]
49	N.C. **(+12V)**[3]	50	GND
47	N.C. **(-12V)**[3]	48	N.C.(+1.5V)
45	**Present**[3]	46	N.C. (LED_WPAN#)[1]
43	GND	44	N.C. (LED_WLAN#)[1]
41	+3.3V[4]	42	N.C. (LED_WWAN#)[1]
39	+3.3V[4]	40	GND
37	GND	38	N.C. (USB_D+)[1]
35	GND	36	N.C. (USB_D-)[1]
33	PETp0	34	GND
31	PETn0	32	SMB_DATA[5]
29	GND	30	SMB_CLK[5]
27	GND	28	N.C. (+1.5V)
25	PERp0	26	GND
23	PERn0	24	+3.3V[4]
21	GND	22	PERST#
19	**TDI** (UIM_C4)[1,6]	20	N.C. (W_DISABLE#)[1]
17	**TDO** (UIM_C8)[1,6]	18	GND
15	GND	16	N.C. (UIM_VPP)[2]
13	RECLK+	14	N.C. (UIM_RESET)[2]

11	REFCLK-	12	N.C. (UIM_CLK)[2]
9	GND	10	N.C. (UIM_DATA)[2]
7	N.C. (CLKREQ#)	8	N.C. (UIM_PWR)[2]
5	N.C. **(TCK)** [COEX2][1]	6	N.C. (+1.5V)
3	N.C. **(TMS)** [COEX1][1]	4	GND
1	N.C. (WAKE#)[1]	2	+3.3V[4]

Note 1: The following mini-PCIe signals are not supported: USB_D+, USB_D-, WAKE#, LED_WPAN#, LED_WLAN#, LED_WWAN#, W_DISABLE#, COEX1, COEX2, UIM_C4, UIM_C8.

Note 2: UIM_PWR, UIM_RESET, UIM_CLK, UIM_VPP, UIM_DATA – SIM card for cell signals may be available on some AcroPack carriers. See carrier documentation for more information.

Note 3: +5, +12, and -12 Volt power supplies have been assigned to pins that are reserved in the mini-PCIe specification. Use of fuses on these power supplies, along with new Present signal on pin 45, to allow support of mini-PCIe cards from other vendors that cannot tolerate power applied to these reserved pins. The Present signal must be grounded on the AP modules. The +12V, -12V, and +5V voltages are needed to power the proposed Analog AcroPack modules.

Note 4: All +3.3Vaux power pins are changed to system +3.3V power.

Note 5: The SM bus signals SMB_CLK and SMB_DATA will be used to clock a carrier location serial stream from the carrier, however this is not supported on the AP500/520/521 modules.

Note 6: TDI is tied to TDO on the AP500/520/521 modules as they do not use JTAG.

3.0 PROGRAMMING INFORMATION

This section provides an overview of the AP5XX module's registers. Once the driver is loaded the modules will be identified by the operating system as a standard serial port so low-level programming is not required for normal operation in a supported operating system.

More detailed register information can be found in Section 1.0 of the Exar17v35x UART datasheets, referenced in Section 1.6.

3.1 PCIe Configuration Registers

The PCIe bus is defined to address three distinct address spaces: I/O, memory, and configuration space. The AcroPack module can be accessed via the PCIe bus memory space and configuration spaces only.

The AcroPack configuration registers are initialized by system software at power-up to configure the card. The AcroPack module is a Plug-and-Play PCIe card. As a Plug-and-Play card the board's base address and system interrupt request are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCIe bus configuration access is used to access the AcroPack's configuration registers.

When the computer is first powered-up, the computer's system configuration software scans the PCIe bus to determine what PCIe devices are present. The software also determines the configuration requirements of the PCIe card.

The system software accesses the configuration registers to determine how many blocks of memory space the module requires. It then programs the board's configuration registers with the unique memory base address.

Since this board is not fixed in address space, its device driver must use the mapping information stored in the board's Configuration Space registers to determine where the board is mapped in memory space.

The configuration registers are also used to indicate that the board requires an interrupt request. The system software then programs the configuration registers with the interrupt request for the board.

The PCIe specification requires software driven initialization and configuration via the Configuration Address space. This board provides 512 bytes of configuration registers for this purpose. It contains the configuration registers shown in the following table to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers and the Interrupt Register which must be read to

determine the base address assigned to the board and the interrupt request that goes active on a board interrupt request.

Table 3.1 PCI Configuration Registers

Address Offset	D31 D24	D23 D16	D15 D8	D7 D0
0x00	**Device ID** 0x0354 AP500 0x0358 AP520/521		**Vendor ID** 0x13A8	
0x04	Status		Command	
0x08	Class Code=0x070002			Rev ID= Current REV
0x0C	BIST	Header	Latency	Cache
0x10	Memory Base Address for Memory Accesses to PCIe interrupt and I/O registers 16K Space **(BAR0)**			
0x14-0x28	Not Used			
0x2C	**Subsystem ID** 0x0000		**Subsystem Vendor ID** 0x0000	
0x30	Not Used			
0x34-0x38	Reserved			
0x3C	Max_Lat	Min_Gnt	Inter. Pin	Inter. Line

This board is allocated a 16K byte block of memory (BAR0), to access UART and device configuration registers. Only 8K is used, as the upper 8K is for a second 'slave' UART' connected to the master that does not exist on the AP5XX module.

3.2 UART and Device Configuration Registers

The Device Configuration Registers and the four or eight individual UART Configuration Registers occupy 4K/8K of PCI bus memory address space. These registers are offset from the BAR0 address as identified in the PCI Configuration Registers in the previous section.

Each UART Configuration Register occupies 1K byte of memory space that include the 16550 compatible registers.

The Device Configuration Registers are accessible from all UART channels, however not all bits can be controlled by all channels. The control of the 8XMODE, 4XMODE, RESET, and SLEEP bits are only available for that particular channel.

Table 3.2 UART and Device Configuration Registers

Address Offset	Register Function	Comment
0x0000-0x000F	UART 0 Registers	See Table 3.8
0x0010-0x007F	Reserved	
0x0080-0x009A	Device Configuration Registers	See Table 3.3
0x009B-0x00FF	Reserved	Reserved
0x0100-0x01FF	UART 0 FIFOs	256 bytes of FIFO data
0x0200-0x03FF	UART 0 Read FIFO with errors	256 bytes of RX FIFO data + LSR
0x0400-0x07FF	Repeat above registers for UART 1	
0x0800-0x0BFF	Repeat above registers for UART 2	
0x0C00-0x0FFF	Repeat above registers for UART 3	
0x1000-0x13FF	Repeat above registers for UART 4	
0x1400-0x17FF	Repeat above registers for UART 5	
0x1800-0x1BFF	Repeat above registers for UART 6	
0x1C00-0x1FFF	Repeat above registers for UART 7	

Table 3.3 Device Configuration Registers in Byte Alignment

Address Offset	Register	Read/Write Comments	Reset State
0x0080	INT0 [7:0]	Read-only Interrupt	0x00
0x0081	INT1[15:8]	Read-only	0x00
0x0082	INT2[23:16]	Read-only	0x00
0x0083	INT3[31:24]	Read-only	0x00
0x0084	TIMERCNTL	Read/Write Timer Control	0x00
0x0085	REGA	Reserved	0x00
0x0086	TIMERLSB	Read/Write Timer LSB	0x00
0x0087	TIMERMSB	Read/Write Timer MSB	0x00
Individual UART channels can only control the bit pertaining to that channel in the registers at address offset 0x088-0x08B			
0X088	8XMODE	Read/Write	0x00
0x089	4XMODE	Read/Write	0x00
0x08A	RESET	Write-only Self clear bits after executing Reset	0x00
0x08B	SLEEP	Read/Write Sleep mode	0x00
0x08C	DREV	Read-only Device revision	Current Rev.
0x08D	DVID	Read-only Device identification	0x88
0x08E	REGB	Read/Write EEPROM control	0x00
0x08F	MPIOINT[7:0]	Not Used.	0x00
0x090	MPIOLVL[7:0]	Read/Write MPIO[7:0] level control	0x00
0x091	MPIO3T[7:0]	Not Used.	0x00
0x092	MPIOINV[7:0]	Not Used.	0x00

0x093	MPIOSEL[7:0]	Not Used.	0XFF
0x094	MPIOOD[7:0]	Not Used.	0x00
0x095	MPIOINT[15:8]	Not Used.	0x00
0x096	MPIOLVL[15:8]	Read/Write MPIO[15:8] level control	0x00
0x097	MPIO3T[15:8]	Not Used.	0x00
0X098	MPIOINV[15:8]	Not Used.	0x00
0x099	MPIOSEL[15:8]	Not Used.	0xFF
0x09A	MPIOOD[15:8]	Not Used.	0x00
0x09B	Reserved		0x00

Table 3.4 Device Configuration Registers in DWORD Alignment

Address Offset	Register	BYTE 3 [31:24]	BYTE 2 [32:16]	BYTE 1 [15:8]	BYTE 0 [7:0]
0x0080–0x0083	INTERRUPT (read only)	INT3	INT2	INT1	INT0
0x0084–0x0087	TIMER (read/write)	TIMERMSB	TIMERLSB	Reserved	TIMERCTL
0x0088–0x008B	ANCILLARY1 (read/write)	SLEEP	RESET	4XMODE	8XMODE
0x008C–0x008F	ANCILLARY2 (read only)	Not used.	REGB	DVID	DREV
0x0090–0x0093	MPIO1 (read/write)	Not Used.	Not Used.	Not Used.	MPIOLVL [7:0]
0x0094–0x0097	MPIO2 (read/write)	Not Used.	MPIOLVL [15:8]	Not Used.	Not Used.
0x0098–0x009B	MPIO3 (read/write)	Reserved	Not Used.	Not Used.	Not Used.

3.2.1 The Global Interrupt Registers – INT0, INT1, INT2 and INT3

The XR17V35x can support two different interrupt schemes with a 32-bit wide register [INT3, INT2, INT1 and INT0]. The first scheme uses INT0 (bits [7:0]) along with the Interrupt Status Register (ISR) of the individual UART channels. Each bit gives an indication of the channel that has requested for service. Bit [0] represents channel 0 and bit [7] indicates channel 7. Logic 1 is an indication that the corresponding channel has called for service. The interrupt bit clears after reading the appropriate register of the interrupting channel register, see Interrupt Clearing section.

The second interrupt scheme uses INT3 – INT1 to provide details about the source of the interrupts for each UART channel. Interrupts are encoded into a 3-bit code where bits [10:8] represent channel 0 and bits [31:29] represent channel 7, respectively. Using this scheme, the highest pending interrupt for all 8 channels are available with a single DWORD read operation without having to read the ISR register of the individual UART channels. The 3-bit encoding and their priority order are shown in the table below. If there is a global interrupt such as the wake-up interrupt, timer/counter interrupt or MPIO interrupt, then they would be reported in the 3-bit code for channel 0 in INT1 bits [10:8]. However, since the UART interrupts have a higher priority, all UART channel 0 interrupts must first be cleared before any of the global interrupts can be reported in INT1 bits [10:8].

All bits start up zero. A special interrupt condition is generated by the XR17V35x upon awakening from sleep after all channels were put to sleep mode earlier. This wake-up interrupt is cleared by a read to the INT0 register.

Table 3.5 UART Channel Interrupt Source Encoding

Priority	BIT[N+2]	BIT[N+1]	BIT[N]	Interrupt Source(s)
X	0	0	0	None or wake-up indicator (wake up indicator is reported in channel 0 only)
1	0	0	1	RXRDY and RX Line Status (logic OR of LSR[4:1])
2	0	1	0	RXRDY Time-out
3	0	1	1	TXRDY, THR or TSR (auto RS485 mode) empty
4	1	0	0	MSR, RTS/CTS or DTR/DSR delta or Xoff/Xon detected or special char. detected
5	1	0	1	Reserved
6	1	1	0	MPIO pin(s). Reported in channel 0 only.
7	1	1	1	Timer/Counter. Reported in channel 0 only.

3.2.1.1 Interrupt Clearing

- Wake-up Indicator is cleared by reading the INT0 register.
- RXRDY and RXRDY Time-out is cleared by reading data in the Rx FIFO.
- Rx Line Status Interrupt clears after reading the LSR register that is in the UART channel register set.
- TXRDY interrupt clears after reading the ISR register that is in the UART channel register set.
- Modem Status Register interrupt clears after reading the MSR register that is in the UART channel register set.
- RTS/CTS or DTR/DSR delta interrupt clears after reading the MSR register that in the UART channel register set.
- Xoff/Xon delta and special character detect interrupt clears after reading the ISR that is in the UART channel register set.
- TIMER Time-out interrupt clears after reading the TIMERCNTL register that is in the Device Configuration register set.
- MPIO interrupt clears after reading the MPIOLVL register that is in the Device Configuration register set.

3.2.2 General Purpose 16-bit Timer/Counter [TimerMSB, TimerLSB, TIMER, TIMECNTL]

The XR17V35x has a general purpose 16-bit timer/counter. The internal 125 MHz clock is used for the timer/counter. The timer can be set to be a single-shot for a one-time event or re-triggerable for a periodic signal. An interrupt may be generated when the timer times out and will show up as a Channel 0 interrupt. It is controlled through 4 configuration registers [TIMERCNTL, TIMER, TIMELSB, TIMERMSB]. The TIMERCNTL register provides the Timer commands such as start/stop.

3.2.2.1 TIMERMSB[31:24] and TIMERLSB[23:16]

The concatenation of the 8-bit registers TIMERMSB and TIMERLSB forms a 16-bit value which decides the time-out period of the Timer, per the following equation:

Timer output frequency = Timer input clock / 16-bit Timer value

The least-significant bit of the timer is being bit [0] of the TIMERLSB with most-significant-bit being bit [7] in TIMERMSB. Notice that these registers do not hold the current counter value when read. Default value is zero (timer disabled) upon powerup and reset. The 'Reset Timer' command does not have any effect on this register.

3.2.2.2 TIMERCNTL[7:0] Register

The bits [3:0] of this register are used to issue commands. The commands are self-clearing, so reading this register does not show the last written command. Reading this register returns a value of 0x01 when the Timer

interrupt is enabled and there is a pending Timer interrupt. It returns a value of 0x00 at all other times. The default settings of the Timer, upon power-up, a hardware reset or upon the issue of a 'Timer Reset' command are:

- Timer Interrupt Disabled
- Re-triggerable mode selected
- Internal 125MHz clock selected as clock source
- Timer output not routed to MPIO[0]
- Timer stopped

Table 3.6 Timer Control Register

TIMERCNTL[7:4]	Reserved
TIMERCNTL[3:0]	These bits are used to invoke a series of commands that control the function of the Timer/Counter. The commands 1100 to 1111 are reserved. 0001: Enable Timer Interrupt 0010: Disable Timer Interrupt 0011: Select One-shot mode 0100: Select Re-triggerable mode 0101: 125MHz clock as clock input for Timer 0110: not supported 0111: not supported 1000: De-route Timer output from MPIO[0] 1001: Start Timer 1010: Stop Timer 1011: Reset Timer

3.2.2.3 Timer Operation

The following paragraphs describe the operation of the 16-bit Timer/Counter. The following conventions will be used in this discussion:

- 'N' is the 16-bit value programmed in the TIMER MSB, LSB registers
- P +Q = N, where 'P' and 'Q' are approximately half of 'N'.
- If N is even, P = Q = N/2.
- If N is odd, P = (N – 1)/2 and Q = (N + 1)/2.
- 'N' can take any value from 0x0002 to 0xFFFF

Timer Operation in One-Shot Mode:
In the one-shot mode, the Timer output will stay HIGH when started (default state) and will continue to stay HIGH until it times out (reaches the terminal count of 'N' clocks), at which time it will become LOW and stay LOW. If the Timer is re-started before the Timer times out, the counter is reset and the Timer will wait for another time-out period before setting its output LOW. If the Timer times out, re-starting the Timer does not have any effect and a 'Stop Timer' command needs to be issued first which will set the Timer output to its default HIGH state. The Timer must be programmed while it is stopped since the following operations are blocked after the Timer has been started:

- Any write to TIMER MSB, LSB registers
- Issue of any command other than 'Start Timer', 'Stop Timer' and 'Reset Timer'

Timer Operation in Re-triggerable Mode:
In the re-triggerable mode, when the Timer is started, the Timer output will stay HIGH until it reaches half of the terminal count N (= P clocks) and toggle LOW and stay LOW for a similar amount of time (Q clocks). The above step will keep repeating until the Timer is stopped at which time the output will become HIGH (default state). Also, after the Timer is started, re-starting the Timer does not have any effect in re-triggerable mode. The Timer must be programmed while it is stopped since the following operations are blocked when the Timer is running:

- Any write to TIMER MSB, LSB registers
- Issue of any command other than 'Stop Timer' and 'Reset Timer' ('Start Timer' is not allowed)

Timer Interrupt:
In the one-shot mode, the Timer will issue an interrupt upon timing out which is 'N' clocks after the Timer is started. In the re-triggerable mode, the Timer will keep issuing an interrupt every 'N' clocks which is on every rising edge of the Timer output. The Timer interrupt can be cleared by reading the TIMERCNTL register or when a Timer Reset command is issued which brings the Timer back to its default settings. The TIMERCNTL will read a value of 0x01 when the Timer interrupt is enabled and there is a pending interrupt. It reads a value of 0x00 at all other times. Stopping the Timer does not clear the interrupt and neither does subsequent restarting.

3.2.3 8XMODE[7:0] (default 0x00)

Each bit selects 8X or 16X sampling rate for that UART channel. The 8XMODE register is accessible from the Device Configuration Registers in all UART channels but the UART channel can only control the bit for that channel. For example, bit [0] is for channel 0 and can only be controlled by channel 0. All other bits are read-only in channel 0. Logic 0 (default) selects normal 16X sampling (with 4XMODE = 0x00) and logic one selects 8X sampling rate. Transmit and receive data rates will double by selecting 8X. If using the 4XMODE, the corresponding bit in this register should be logic 0.

3.2.4 4XMODE[15:8] (default 0x00)

Each bit selects 4X or 16X sampling rate for that UART channel. The 4XMODE register is accessible from the Device Configuration Registers in all UART channels but the UART channel can only control the bit for that channel. For example, bit [0] is channel 0 and can only be controlled by channel 0. All other bits are read-only in channel 0. Logic 0 (default) selects normal 16X sampling (with 8XMODE = 0x00) and logic one selects 4X sampling rate. Transmit and receive data rates will quadruple by selecting 4X. If using the 8XMODE, the corresponding bit in this register should be logic 0.

3.2.5 RESET[23:16] (default 0x00)

The 8-bit RESET register provides the software with the ability to reset the UART(s) when there is a need. The RESET register is accessible from the Device Configuration Registers in all UART channels but the UART channel can only control the bit for that channel. For example, writing 0xFF to the RESET register in channel 0 will only reset channel 0. Each bit is self-clearing after it is written a logic 1 to perform a reset to that channel. All registers in that channel will be reset to the default condition.

3.2.6 SLEEP[31:24] (default 0x00)

The 8-bit SLEEP register enables each UART separately to enter Sleep mode. The SLEEP register is accessible from the Device Configuration Registers in all UART channels but the UART channel can only control the bit for that channel. For example, writing 0xFF to the SLEEP register in channel 0 will only enable the sleep mode for channel 0. Sleep mode reduces power consumption when the system needs to put the UART(s) to idle. The UART enters sleep mode when the following conditions are satisfied after the sleep mode is enabled (Logic 0 (default) is to disable and logic 1 is to enable sleep mode):

- Transmitter and Receiver are empty (LSR[6]=1, LSR[0]=0)
- RX pin is idling at a HIGH in normal mode
- The modem input (CTS#, DSR#, CD# and RI#) is steady at either HIGH or LOW (MSR bits [3:0] = 0x0)

The XR17V35x is awakened by any of the following events occurring at any of the UART channels:

- A receive data start bit transition (HIGH to LOW in normal mode)

- A data byte is loaded into the transmitter
- A change of logic state on any of the modem inputs so that any of the delta bits (MSR bits[3:0]) is set (RI# delta bit is only set on the rising edge)

A receive data start bit transition will not wake up the UART if the Multidrop mode is disabled (DLD[6] = 0) and the receiver is disabled (MSR[2] = 1, MSR[0] = 0).

A special interrupt is generated with an indication of no pending interrupt. The XR17V35x will return to sleep mode automatically after all interrupting conditions have been serviced and cleared. It will stay in the sleep mode of operation until it is disabled by resetting the SLEEP register bits.

3.2.7 DVID[15:8]

Device identification for the type of UART. The Device ID of the XR17V354 is 0x84 and XR17V358 is 0x88.

3.2.8 DREV[7:0]

Revision number of the XR17V35x. A 0x01 represents "revision-A" with 0x02 for rev-B and so on.

3.2.9 REGB[23:16] (default 0x00)

REGB register provides a control for simultaneous write to all UARTs configuration register or individually. This is very useful for device initialization in the power up and reset routines.

Table 3.7 REGB Register

REGB[23:19]	Not Used.
REGB[18]	Global Interrupt Disable: 0 = Global interrupt enabled. Interrupts to PCIe host are enabled (default). 1 = Global interrupt disabled. Interrupts to PCIe host are disabled.
REGB[17]	Wake-up Interrupt Disable: 0 = Wake-up interrupt is generated when UART exits sleep mode (default). 1 = No wake-up interrupt is generated when UART exits sleep mode.
REGB[16]	Enable Simultaneous Configuration: 0 = write to each UART configuration registers individually (default). 1 = Enable simultaneous write to all 4 UART configuration registers.

3.2.10 MPIO Registers

The MPIO pins of the Exar device are reserved for device identification. As inputs, MPIO[15:0] on the AP500 and AP520 module will read 0x0000 through the MPIOLVL registers, the AP521 will read 0x0001. This can be used in conjunction with the DVID to identify an AcroPack module.

3.3 Transmit and Receive Data

There are two methods to load transmit data and unload receive data from each UART channel. First, there is a transmit data register and receive data register for each UART channel as shown in Table 3.2 set to ease programming. These registers support 8, 16, 24 and 32-bit wide format. In the 32-bit format, it increases the data transfer rate on the PCI bus. Additionally, a special register location provides receive data byte with its associated error flags. This is a 16-bit or 32-bit read operation where the Line Status Register (LSR) content in the UART channel register is paired along with the data byte. This operation further facilitates data unloading with the error flags without having to read the LSR register separately. Furthermore, the XR17V35x supports 32-bit read/write operation of up to 256 bytes of data.

The second method is through each UART channel's transmit holding register (THR) and receive holding register (RHR). The THR and RHR registers are 16550 compatible so their access is limited to 8-bit format. The software driver must separately read the LSR content for the associated error flags before reading the data byte.

3.3.1 FIFO Data Loading and Unloading in 32-bit Format

The XR17V35x supports 32-bit Read and 32-bit Write transactions anywhere in the mapped memory region (except reserved areas). In addition, to utilize this feature fully, the device provides a separate memory location (apart from the individual channel's register set) where the RX and the TX FIFO can be read from/written to, as shown in Table 3.2. The following is an extract from the table showing the memory locations that support 32-bit transactions:

Channel N: (for channels 0 through 7) where M = 4N + 1.

RX FIFO: 0xM00 – 0xMFF (256 bytes)

TX FIFO: 0xM00 – 0xMFF (256 bytes)

RX FIFO + status: 0x(M+1)00 – 0x(M+2)FF (256 bytes data+256 bytes status)

For example, the locations for channel 2 are:

RX FIFO: 0x0900 – 0x09FF (256 bytes)

TX FIFO: 0x0900 – 0x09FF (256 bytes)

RX FIFO + status: 0x0A00 – 0x0BFF (256 bytes data+256 bytes status)

Normal Rx/Tx FIFO Data Unloading/Loading at Locations 0x0100, 0x0500, 0x0900, 0x0D00, 0x1100, 0x1500, 0x1900 and 0x1D00:

The RX FIFO data can be read out 32-bits at a time at memory locations 0x0100 (channel 0), 0x0500 (channel 1), 0x0900 (channel 2), 0x0D00 (channel 3), 0x1100 (channel 4), 0x1500 (channel 5), 0x1900 (channel 6), 0x1D00 (channel 7). This operation is 4 times faster than reading the data in 256 separate 8-bit memory reads of RHR register (0x0000 for channel 0, 0x0400 for channel 1, 0x0800 for channel 2, 0x0C00 for channel 3, 0x1000 for channel 4, 0x1400 for channel 5, 0x1800 for channel 6 and 0x1C00 for channel 7).

The TX FIFO data can be loaded 32-bit (4 bytes) at a time at memory locations 0x0100 (channel 0), 0x0500 (channel 1), 0x0900 (channel 2), 0x0D00 (channel 3), 0x1100 (channel 4), 0x1500 (channel 5), 0x1900 (channel 6) and 0x1D00 (channel 7).

Special Rx FIFO Data Unloading at Locations 0x0200, 0x0600, 0x0A00, 0x0E00, 0x1200, 0x1600, 0x1A00 and 0x1E00:

The XR17V35x also provides the same RX FIFO data along with the LSR status information of each byte side-by-side, at locations 0x0200 (channel 0), 0x0600 (channel 1), 0x0A00 (channel 2) 0x0E00 (channel 3), 0x1200 (channel 4), 0x1600 (channel 5), 0x1A00 (channel 6) and 0x1E00 (channel 7). The Status and Data bytes must be read in 16 or 32-bit format to maintain data integrity.

3.3.2 FIFO Data Loading/Unloading Through the UART Channel Registers, THR and RHR, in 8-Bit Format

The THR and RHR for each channel 0 to 7 are located sequentially at address 0x0000, 0x0400, 0x0800, 0x0C00, 0x1000, 0x1400, 0x1800 and 0x1C00. Transmit data byte is loaded to the THR when writing to that address and receive data is unloaded from the RHR register when reading that address. Both THR and RHR registers are 16C550 compatible in 8-bit format, so each bus operation can only write or read in bytes.

3.4 UART Channel Configuration Registers

There are 4 UARTs channel [3:0] in the XR17V354 and 8 UARTs channel[7:0] in the XR17V358. Each has its own 256-byte of transmit and receive FIFO, a set of 16550 compatible control and status registers, and a baud rate generator for individual channel data rate setting. Eight additional registers per UART were added for the EXAR enhanced features.

Address lines A0 to A3 select the 16 registers in each channel. The first 8 registers are 16550 compatible with EXAR enhanced feature registers located on the upper 8 addresses.

Table 3.8 UART Channel Configuration Registers

A[3:0]	Registers	Read/Write	Comments

16550 COMPATIBLE			
0 0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7]=0
0 0 0 0	DLL - Divisor LSB	Read/Write	LCR[7]=1
0 0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7]=0
0 0 0 1	DLM - Divisor MSB	Read/Write	LCR[7]=1
0 0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	LCR[7]=0
0 0 1 0	DLD - Divisor Fractional	Read/Write	LCR[7]=1
0 0 1 1	LCR - Line Control Register	Read/Write	
0 1 0 0	MCR - Modem Control Register	Read/Write	
0 1 0 1	LSR - Line Status Register	Read-only	
0 1 1 0	MSR - Modem Status Register -Auto RS485 Delay	Read-only Write-only	EFR bit-4=1
0 1 1 1	SPR- Scratch Pad Register	Read/Write	
ENHANCED REGISTER			
1 0 0 0	FCTR - Feature Control Register	Read/Write	
1 0 0 1	EFR - Enhanced Function Register	Read/Write	
1 0 1 0	TXCNT - Tx FIFO Level Counter TXTRG - Tx FIFO Trigger Level	Read-only Write-only	
1 0 1 1	RXCNT- Rx FIFO Level Counter RXTRG – Rx FIFO Trigger Level	Read-only Write-only	
1 1 0 0	Xoff-1 - Xoff Character 1 Xchar	Write-only Read-only	Xon,Xoff Rcvd. Flags
1 1 0 1	Xoff-2 - Xoff Character 2	Write-only	
1 1 1 0	Xon-1 - Xon Character 1	Write-only	
1 1 1 1	Xon-2 - Xon Character 2	Write-only	

3.4.1 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and Receive Holding Register (RHR). The RSR uses the 16X, 8X or 4X clock for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X, 8X or 4X clock rate. After 8 or 4 or 2 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits [4:1]. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error flags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out function when receive data does not reach the receive FIFO trigger level. This time-out

delay is 4 word lengths as defined by LCR bits [1:0] plus 12 bits time. The RHR interrupt is enabled by IER bit [0].

3.4.2 Transmitter

The transmitter section comprises of a 256 byte FIFO, a byte-wide Transmit Holding Register (THR) and an 8-bit Transmit Shift Register (TSR). THR receives a data byte from the host (non-FIFO mode) or a data byte from the FIFO when the FIFO is enabled by FCR bit [0]. TSR shifts out every data bit with the 16X or 8X internal clock. A bit time is 16 or 8 clock periods. The transmitter sends the start bit followed by the number of data bits, inserts the proper parity bit if enable, and adds the stop bit(s). The status of the THR and TSR are reported in the Line Status Register (LSR bit [6:5]).

3.4.2.1 Transmit Holding Register (THR)

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (bit [0]) becomes first data bit to go out. The THR is also the input register to the transmit FIFO of 256 bytes when FIFO operation is enabled by FCR bit[0]. A THR empty interrupt can be generated when it is enabled in IER bit [1].

3.4.2.2 Transmitter Operation in non-FIFO mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit [5]) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit [1]) when it is enabled by IER bit [1]. The TSR flag (LSR bit [6]) is set when TSR becomes completely empty.

3.4.2.3 Transmitter Operation in FIFO mode

The host may fill the transmit FIFO with up to 256 bytes of transmit data. The THR empty flag (LSR bit [5]) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit [1]) when the amount of data in the FIFO falls below its programmed trigger level (see TXTRG register). The transmit empty interrupt is enabled by IER bit [1]. The TSR flag (LSR bit [6]) is set when TSR becomes completely empty. Furthermore, with the RS485 half-duplex direction control enabled (FCTR bit [5]=1) the source of the transmit empty interrupt changes to TSR empty instead of THR empty. This is to ensure the RTS# output is not changed until the last stop bit of the last character is shifted out.

3.4.2.4 Auto RS485 Operation (AP521 Only)

The auto RS485 half-duplex direction control changes the behavior of the transmitter when enabled by FCTR bit [5]. It de-asserts RTS# or DTR# after a specified delay indicated in MSR[7:4] following the last stop bit of the last character that has been transmitted. This helps in turning around the transceiver to receive the remote station's response. The delay optimizes the

time needed for the last transmission to reach the farthest station on a long cable network before switching off the line driver. This delay prevents undesirable line signal disturbance that causes signal degradation. It also changes the transmitter empty interrupt to TSR empty instead of THR empty.

3.4.3 Baud Rate Generator Divisors (DLM, DLL and DLD)

Each UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter and receiver. The prescaler is controlled by a software bit in the MCR register. The MCR register bit [7] sets the prescaler to divide the internal 125 MHz clock by 1 or 4. The output of the prescaler clocks to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (2^{16} - 0.0625) in increments of 0.0625 (1/16) to obtain a 16X, 8X or 4X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling.

3.4.3.1 DLM[7:0], DLL[7:0] and DLD[3:0]

The Baud Rate Generator (BRG) generates the data rate for the transmitter and receiver. The rate is programmed through registers DLM, DLL and DLD which are only accessible when LCR bit [7] is set to logic 1.

The BRG divisor (DLL, DLM and DLD registers) defaults to 1 (DLL = 0x01, DLM = 0x00, DLD = 0x00). The DLL and DLM registers provide the integer part of the divisor and the DLD register provides the fractional part of the divisor. Only the four lower bits of the DLD are implemented and they are used to select a value from 0 (for setting 0000) to 0.9375 or 15/16 (for setting 1111). Programming the Baud Rate Generator Registers DLL, DLM and DLD provides the capability for selecting the operating data rate. Table 3.5 shows the divisor for some standard and non-standard data rates when using the internal 125 MHz clock at 16X clock rate. If the pre-scaler is used (MCR bit [7] = 1), the output data rate will be 4 times less than that shown in Table 3.5. At 8X sampling rate, these data rates would double. At 4X sampling rate, these data rates would quadruple. Also, when using 8X or 4X sampling mode, note that the bit-time will have a jitter (+/- 1/16) whenever the DLD is an odd number. For data rates not listed in Table 3.5, the divisor value can be calculated with the following equation(s):

Calculated Divisor (decimal) = (125 MHz clock frequency / prescaler) / (desired data rate x 16), **WHEN 8XMODE = 0 AND 4XMODE = 0**

Calculated Divisor (decimal) = (125 MHz clock frequency / prescaler / (desired data rate x 8), **WHEN 8XMODE = 1 AND 4XMODE = 0**

Calculated Divisor (decimal) = (125 MHz clock frequency / prescaler / (desired data rate x 4), **WHEN 8XMODE = 0 AND 4XMODE = 1**

The closest actual divisor that is obtainable in the XR17V35x can be calculated using the following formula:

Actual Divisor (decimal) = ROUND((Calculated Divisor - TRUNC (Calculated

Divisor))*16)/16 + TRUNC (Calculated Divisor),

DLM = TRUNC (Actual Divisor in hex) >> 8

DLL = TRUNC (Actual Divisor in hex) & 0xFF

DLD = ROUND ((Calculated Divisor - TRUNC (Calculated Divisor))*16)

In the formulas above, please note that: TRUNC (N) = Integer Part of N. For example, TRUNC (5.6) = 5. ROUND (N) = N rounded towards the closest integer. For example, ROUND (7.3) = 7 and ROUND (9.9) = 10.

Table 3.9 Typical Data Rates with Internal 125MHz Clock at 16X Sampling

Required Output Data Rate	Divisor for 16X Clock (decimal)	Divisor Obtainable in XR17V35x	DLM Program Value (HEX)	DLL Program Value (HEX)	DLD Program Value (HEX)	Data Error Rate (%)
9600	813.80	813 12/16	03	2D	D	0
19200	406.90	406 14/16	01	96	E	0.01
38400	203.45	203 7/16	00	CB	7	0.01
57600	135.63	135 10/16	00	87	A	0.01
115200	67.82	67 13/16	00	43	D	0.01

Note that there is a more extensive list of possible data rates in the Exar datasheet.

3.4.3.2 DLD[7:4]

Table 3.10 DLD Register[7:4]

DLD BIT	INTERRUPT ACTION
4	Not Used.
5	Multi-drop Mode: 0 = Normal mode. 1 = Enable Multi-drop mode.
6	XON/XOFF Parity Check: 0 = XON/XOFF characters are valid flow control characters even if they have parity errors. 1 = XON/XOFF characters are not valid flow control characters if they have parity errors.

7	RS-485 Polarity: Must be set to logic 0 on the AP521 (default). N/A on the AP500 and AP520.

3.4.4 Interrupt Enable Register (IER) – Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR) and also encoded in INT (INT0-INT3) register in the Device Configuration Registers.

3.4.4.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR bit [0] = logic 1) and receive interrupts (IER bit [0] = logic 1) are enabled, the RHR interrupts (see ISR bits [4:3]) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR bit [0]) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

3.4.4.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR bit [0] equals a logic 1 for FIFO enable; resetting IER bits [3:0] enables the XR17V35x in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in RHR (non-FIFO mode) or RX FIFO (FIFO mode).

B. LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

C. LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR BIT-5 indicates THR (non-FIFO mode) or TX FIFO (FIFO mode) is empty.

E. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

F. LSR BIT-7 indicates a data error in at least one character in the RX FIFO

Table 3.11 Interrupt Enable Register

IER BIT	INTERRUPT ACTION

0	RX Interrupt Enable: 0 = Disable receive data ready interrupt (default). 1 = Enable receive data ready interrupt. In non-FIFO mode an interrupt will be issued when RHR has a data character. In FIFO mode an interrupt will be issued when the FIFO has reached the programmed trigger level and is cleared when the FIFO drops below the trigger level. Note that the receive FIFO must also be enabled via bit-0 of the FCR in FIFO mode.
1	TX Ready Interrupt Enable: 0 = Disable transmit ready interrupt (default). 1 = Enable transmit ready interrupt. In non-FIFO mode, an interrupt is issued whenever the THR is empty. In FIFO mode, an interrupt is issued when the number of bytes in the TX FIFO fall below the programmed trigger level and again when the TX FIFO is empty. When auto RS485 mode is enabled (FCTR bit [5] = 1 on the AP521), the second interrupt is delayed until the transmitter (both the TX FIFO and the TX Shift Register) is empty.
2	Receive Line Status Interrupt Enable: 0 = Disable the receiver line status interrupt (default). 1 = Enable the receiver line status interrupt. An Overrun Error, Framing Error, Parity Error or detection of a break character will result in an LSR interrupt. An interrupt will be issued immediately after receiving a character with an error and again when the character with the error is on top of the FIFO.
3	Modem Status Interrupt Enable: 0 = Disable modem status register interrupt (default). 1 = Enable modem status register interrupt. An interrupt will be issued whenever any of the delta bits of the MSR register is set.
4	Reserved.
5[1]	Xoff Interrupt Enable:

	0 = Disable the receive Xoff interrupt, software flow control (default). 1 = Enable the receive Xoff interrupt, software flow control. When software flow control in enabled, and one or two sequential receive data characters match the preprogrammed Xoff 1-2 values an interrupt will be issued.
6[1]	RTS# Output Interrupt Enable: 0 = Disable RTS# interrupt (default). 1 = Enable RTS# interrupt. This Interrupt is generated when the RTS pin transitions from a logic 0 to a logic 1.
7[1]	CTS# Input Interrupt Enable: 0 = Disable CTS# interrupt (default). 1 = Enable CTS# interrupt. This interrupt will be issued when the CTS pin transitions from a logic 0 to a logic 1.

[1]Bits 5-7 are only programmable when the EFR bit 4 is set to "1".

3.4.5 Interrupt Status Register (ISR) – Read Only

The Interrupt Status Register is used to indicate that a prioritized interrupt is pending and the type of interrupt that is pending. Six levels of prioritized interrupts are provided to minimize software interaction. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. Note, only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after re-reading the interrupt status bits.

The following interrupt source table shows the data values (bit 0-5) for the six prioritized interrupt levels and the interrupt sources associated with each of these interrupts.

3.4.5.1 Interrupt Generation

- LSR is by any of the LSR bits [4:1]. See IER bit [2] description on the previous page. • RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char plus 12 bits delay timer.
- TXRDY is by TX trigger level or TX FIFO empty (or transmitter empty

in auto RS-485 control).

- MSR is by any of the MSR bits [3:0].
- Receive Xoff/Xon/Special character is by detection of a Xoff, Xon or Special character.
- CTS#/DSR# is when its transmitter toggles the input pin (from LOW to HIGH) during auto CTS/RTS flow control enabled by EFR bit [7] and selection on MCR bit [2].
- RTS#/DTR# is when its receiver toggles the output pin (from LOW to HIGH) during auto RTS/DTR flow control enabled by EFR bit [6] and selection on MCR bit [2].
- Wake-up indicator is when the UART wakes up from the sleep mode.

3.4.5.2 Interrupt Clearing

- LSR interrupt is cleared by a read to the LSR register.
- RXRDY interrupt is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading RHR.
- TXRDY interrupt is cleared by a read to the ISR register or writing to THR.
- MSR interrupt is cleared by a read to the MSR register.
- Xoff/Xon interrupt is cleared by reading ISR.
- Special character interrupt is cleared by a read to ISR.
- RTS# and CTS# status change interrupts are cleared by a read to the MSR register.
- Wake-up indicator is cleared by a read to the INT0 register.

Table 3.12 Interrupt Source and Priority Level

PRIORITY LEVEL	ISR BITS Bit5 to Bit0	Source of the Interrupt
1	000110	Receiver Line Status (see LSR bits 1-4)
2	000100	Received Data Ready or Trigger Level reached.
2	001100	Receive Data Time Out.
3	000010	Transmitter Holding Register Empty
4	000000	MSR (Modem Status Register)
5	010000	Received Xoff signal special character
6	100000	CTS#/DSR#, RTS#/DTR# change of state

X	000001	None (default)

Note that ISR bit 0 can be used to indicate whether an interrupt is pending (bit 0 low when interrupt is pending).

Bits 6 and 7 are set when bit 0 of the FIFO Control Register is set to 1. A power-up or system reset sets ISR bit 0 to logic "1", and bits 1 to 7 to logic "0".

3.4.6 FIFO Control Register (FCR) – Write Only

This write-only register is used to enable and clear the FIFO buffers, set the transmit/receive FIFO trigger levels, and select the type of DMA signaling.

Table 3.13 FIFO Control Register

FCR BIT	FUNCTION
0	Tx and Rx FIFO Enable: 0 = disable the transmit and receive FIFO (default). 1 = enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.
1	Rx FIFO Reset: 0 = no receive FIFO reset (default). 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to logic 0 after resetting the FIFO.
2	Tx FIFO Reset: 0 = No transmit FIFO reset (default). 1 = Reset the transmit FIFO pointers and FIFO level counter logic (the transmit shift register is not cleared or altered). This bit will return to logic 0 after resetting the FIFO.
3	DMA Mode Select: 0 = Set DMA mode to 0 (default). 1 = Set DMA mode to 1. This bit has no effect and is provided for legacy software compatibility.
5,4[1]	Transmit FIFO Trigger Select: These two bits set the trigger level for the transmit FIFO interrupt. The UART will issue a transmit interrupt when the

	number of characters in the FIFO falls below the selected trigger level, or when it gets empty in case that FIFO did not get filled over the trigger level on last reload. Refer to Table 3.10 for selections. The FCTR[7:6] are associated with these 2 bits.
7,6	Receive FIFO Trigger Select: These two bits set the trigger level for the receive FIFO. The UART will issue a receive interrupt when the number of characters in the FIFO crosses the trigger level. Refer to Table 3.10 for selections. The FCTR[7:6] are associated with these 2 bits. Note that the receiver and transmitter cannot use different trigger tables. Whichever selection is made applies to both the Rx and Tx side.

[1]Bits 4 and 5 are only programmable when the EFR bit 4 is set to "1". A power-up or system reset sets all FCR bits to 0.

Table 3.14 Transmit and Receive FIFO Trigger Table and Level Selection

Trigger Table	FCTR [7:6]	FCR [7:6]	FCR [5:4]	Rx Trigger Level	Tx Trigger Level	Compatibility
A	0 0	0 0 0 1 1 0 1 1	0 0	1 4 8 14	1	16C550, 16C2550, 16C2552, 16C554, 16C580, 16L580
B	0 1	0 0 0 1 1 0 1 1	0 0 0 1 1 0 1 1	8 16 24 28	16 8 24 30	16C650A, 16L651
C	1 0		0 0 0 1		8 16	16C654

		0 0 0 1 1 0 1 1	1 0 1 1	8 16 56 60	32 56	
D	1 1	X X	X X	Prog. via RXTRIG reg.	Prog. via TXTRIG reg.	16L2752, 16L2750, 16C2852, 16C850, 16C854, 16C864

3.4.7 Line Control Register (LCR) – Read/Write

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register. The individual bits of this register control the format of the data character as follows:

Table 3.15 Line Control Register

LCR Bit	FUNCTION	PROGRAMMING
1,0	Word Length Select	0 0 = 5 Data Bits 0 1 = 6 Data Bits 1 0 = 7 Data Bits 1 1 = 8 Data Bits
2	Stop Bit Select	0 = 1 Stop Bit 1 = 1.5 Stop Bits if 5 data bits; 2 Stop Bits if 6, 7, or 8 data bits selected.
3	Parity Enable	0 = Parity Disabled, 1 = Parity Enabled A parity bit is generated and checked for between the last data word bit and the stop bit.
4	Even-Parity Select	0 = Odd Parity 1 = Even Parity
5	Stick Parity	0 = Disabled, 1 = Enabled When parity is enabled, stick parity causes the transmission and reception of a parity bit to be in the opposite state from the value selected via bit 4. This is used as a diagnostic tool to force parity

		to a known state and allow the receiver to check the parity bit in a known state.
6	Transmit Break Enable	0 = Break Disabled, 1 = Break Enabled When break is enabled, the serial output line (TxD) is forced to the space state (low). This bit acts only on the serial output and does not affect transmitter logic. For example, if the following sequence is used, no invalid characters are transmitted due to the presence of the break. 1. Load a zero byte in response to the Transmitter Holding Register Empty (THRE) status indication. 2. Set the break in response to the next THRE status indication. 3. Wait for the transmitter to become idle when the Transmitter Empty status signal is set high (TEMT=1); then clear the break when normal transmission has to be restored.
7	Baud Rate Divisors Enable (DLL, DLM and DLD)	0 = Data registers are selected (default). 1 = Divisor latch registers (DLL, DLM and DLD) are selected.

Note that bit 7 must be set high to access the divisor latch registers DLL & DLM of the baud rate generator or access the Enhanced Feature Register (EFR). Bit 7 must be low to access the Receiver Holding Register (RHR), the Transmitter Holding Register (THR), or the Interrupt Enable Register (IER). A power-up or system reset sets all LCR bits to 0.

3.4.8 Modem Control Register (MCR) – Read/Write

The Modem Control register controls the interface with the modem or data set as described below.

Table 3.16 Modem Control Register

MCR Bit	FUNCTION	PROGRAMMING
0	Data Terminal Ready Output Signal (DTR)	0= DTR* Not Asserted (Inactive) 1= DTR* Asserted (Active) Only supported on the AP500.

1	Ready to Send Output Signal (RTS)	0 = RTS* Not Asserted (Inactive) 1 = RTS* Asserted (Active) Supported on the AP500 and AP520.
2	DTR# or RTS# for Auto Flow Control	0 = Uses RTS# and CTS# pins for auto hardware flow control. (supported on the AP500 and AP520) 1 = Uses DTR# and DSR# for auto hardware flow control (only supported by the AP500).
3	Send Char Immediate	0 = Send char immediate disabled (default). 1 = Send char immediate enabled.
4	Loop-back	0 = Loop-back Disabled 1 = Loop-back Enabled
5[1]	Xon Control	0 = Disable Xon 1 = Enable any Xon function. In this mode any RX character received will enable Xon.
6[1]	Not Used	Must be logic 0
7[1]	Divide by Four	0 = Divide by one. The internal 125MHz clock is fed directly to the Programmable Baud Rate Generator without further modification. 1 = Divide by four. 125MHz divided by 4, or 31.25MHz, is fed to the Programmable Baud Rate Generator.

[1]Bits 5-7 are only programmable when the EFR bit 4 is set to "1". The programmed values for these bits are latched when EFR bit 4 is cleared, preventing existing software from inadvertently overwriting the extended functions. A power-up or system reset sets all MCR bits to 0.

3.4.9 Line Status Register (LSR) – Read Only

The Line Status Register (LSR) provides status indication corresponding to the data transfer. LSR bits 1-4 are the error conditions that produce receiver line-status interrupts (a priority 1 interrupt in the Interrupt Identification Register).

Table 3.17 Line Status Register

LSR Bit	FUNCTION	PROGRAMMING
0	Receive	0 = No data in the RHR or FIFO (default).

	Data Ready	1 = Data has been received and is saved in the RHR or FIFO.
1	Receiver Overrun Error	0 = No Error (default). 1 = Indicates that data in the RHR is not being read before the next character is transferred into the RHR, overwriting the previous character. In the FIFO mode, it is set after the FIFO is filled and the next character is received. The overrun error is detected by the CPU on the first LSR read after it happens. The character in the shift register is not transferred into the FIFO, but is overwritten. This bit is reset low when the CPU reads the LSR.
2	Receive Data Parity Error	0 = No Error (default). 1 = Parity Error – the received character does not have the correct parity as configured via LCR bits 3 & 4. This bit is set high on detection of a parity error and reset low when the host CPU reads the contents of the LSR. In the FIFO mode, the parity error is associated with the character at the top of the FIFO.
3	Receive Data Framing Error	0 = No Error 1 = Framing Error – Indicates that the received character does not have a valid stop bit (stop bit following last data bit or parity bit detected as a zero/space bit). This bit is reset low when the CPU reads the contents of the LSR. In FIFO mode, the framing error is associated the character at the top of the FIFO.
4	Receive Break Flag	0 = No Break 1 = Break – the received data input has been held in the space (logic 0) state for more than a full-word transmission time (start bits+ data+ parity bit+ stop bits). Reset upon read of LSR. In FIFO mode, this bit is associated with the break character at the top of the FIFO. It is detected by the host CPU during the first LSR read. Only one "0" character is loaded into the FIFO when the break occurs.
5	Transmit FIFO Empty	0 = Not Empty 1 = Empty – indicates that the transmitter is

		ready to accept a new character for transmission. The last data byte has been transferred from the transmit FIFO to the transmit shift register.
6	Transmitter Empty	0 = Not Empty 1 = Transmitter Empty – set when both the transmit FIFO (or THR, in non-FIFO mode) and the Transmit Shift Register (TSR) are both empty.
7	Receiver FIFO Error	0 = No Error in FIFO (default). 1 = Error in FIFO – An indicator for the sum of all error bits in the Rx FIFO. At least one parity error, framing error or break indication is in the FIFO data. Cleared when there are no more errors in the FIFO.

Note that LSR Bits 1-4 are the error conditions that produce a receiver-line-status interrupt (a priority 1 interrupt in the ISR register when any one of these conditions are detected). This interrupt is enabled by setting IER bit 2 to "1".

A power-up or system reset sets all LSR bits to 0, except bits 5 and 6 which are high.

3.4.10 Modem Status Register (MSR) – Read Only

The Modem Status Register (MSR) provides the host CPU with an indication on the status of the modem input line from a modem or other peripheral device. This register allows the current state of CTS, DSR, RI and CD to be read and provides indication on whether the states of the lines has changed since the last read of the MSR (bit is set high when the corresponding control input changes state and is reset low when the CPU reads the MSR).

Table 3.18 Modem Status Register

MSR BIT	FUNCTION
0	ΔCTS - Set if CTS# has changed states since last read of MSR. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit[3]).
1	ΔDSR - Set if DSR# has changed states since last read of MSR. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit[3]).
2	ΔRI - Set if RI# has changed states since last read of MSR. A modem status interrupt will be generated if MSR interrupt is

	enabled (IER bit[3]).
3	ΔCD - Set if CD# has changed states since last read of MSR. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit[3]).
4	CTS - If the channel is in the loopback mode (MCR bit 4 = 1), then the state of RTS# in the MCR is reflected.
5	DSR - If the channel is in the loopback mode (MCR bit 4 = 1), then the state of DTR# in the MCR is reflected.
6	RI - In the loopback mode this bit is equivalent to bit [2] in the MCR register.
7	CD - In the loopback mode this bit is equivalent to bit [3] in the MCR register.

Note that reading MSR clears the delta-modem status indication but has no effect on the status bit. For both the LSR & MSR, the setting of the status bits during a status register read operation is inhibited (the status bit will not be set until the trailing edge of the read). However, if the same status condition occurs during a read operation, that status bit is cleared on the trailing edge of the read instead of being set again.

Note that not all UART signal paths are used by the all models and their corresponding UART pins are tied high (+3.3). This includes, RI (Ring Indicator), DSR (Data Set Ready), and CD (Carrier Detect) on the AP520 and AP521.

A power-up or system reset sets the MSR to 0x00.

3.4.11 Modem Status Register (MSR) – Write Only

The upper four bits [7:4] of this register set the delay in number of bits time for the auto RS-485 turnaround from transmit to receive.

MSR [7:4]: Auto RS485 Turn-Around Delay (requires EFR bit [4]=1) (For use on the AP521 only)

When Auto RS485 feature is enabled (FCTR bit [5]=1) and RTS# output is connected to the enable input of a RS-485 transceiver. These 4 bits select from 0 to 15 bit-time delay after the end of the last stop-bit of the last transmitted character. This delay controls when to change the state of RTS# output. This delay is very useful in long-cable networks. The table below shows the selection. The bits are enabled by EFR bit-4.

Table 3.19 Auto RS485 Half-Duplex Direction Control Delay from Transmit to Receive

MSR[7:4]	DELAY IN BIT TIMES
0000	0

0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	10
1011	11
1100	12
1101	13
1110	14
1111	15

MSR[3:0]

Table 3.20 MSR[3:0]

MSR Bit	FUNCTION	PROGRAMMING
0	Receiver Disable Modes	This is only applicable when MSR[2] = 1. 0 = All RX data and Xon/Xoff flow control characters are ignored. 1 = All RX data is ignored. Xon/xoff flow control characters are detected and acted upon.
1	Transmitter Disable Modes	This bit is only applicable when MSR[3] = 1. 0 = No Xon/Xoff software flow control characters will be transmitted when the transmitter is disabled. If there is a pending xon/xoff character to be sent while the transmitter is disabled, it will be transmitted. No additional xon/xoff characters will be sent.

		1 = Xon/xoff software flow control characters will be transmitted even though the transmitter is disabled.
2	Receiver Disable	0 = Enable Receiver (default). 1 = Disable Receiver This bit can be used to disable the receiver by halting the RSR. When this bit is set to a logic 1, the receiver will operate in one of the following ways: • If a character is being received at the time of setting this bit, that character will be correctly received. No more characters will be received. • If the receiver is idle at the time of setting this bit, no more characters will be received. The receiver can be enabled and will start receiving characters by resetting this bit to a logic 0. The receiver will operate in one of the following ways: • If the receiver is idle (RX pin is HIGH) at the time of setting this bit, the next character will be received normally. It is recommended that the receiver be idle when resetting this bit to a logic 0. • If the receiver is not idle (RX pin is toggling) at the time of setting this bit, the RX FIFO will be filled with unknown data. Any data that is in the RX FIFO can be read out at any time whether the receiver is disabled or not.
3	Transmitter Disable	0 = Enable Transmitter (default). 1 = Disable Transmitter This bit can be used to disable the transmitter by halting the TSR. When this bit is set to a logic 1, the bytes already in the FIFO will not be sent out. Also, any more data loaded into the FIFO will stay in the FIFO and will not be sent out. When this bit is set to a logic 0, the bytes currently in the TX FIFO will be sent out. Please note that setting this

		bit to a logic 1 stops any character from going out. Also, this bit must be a logic 0 for the Send Char Immediate function (see MCR[3]).

3.4.11 Scratch Pad (SCR) – Read/Write

This 8-bit read/write register has no effect on the operation of either serial channel. It is provided as an aide to the programmer to temporarily hold data.

3.4.13 Feature Control Register (FCTR) – Read/Write

This register controls the UART enhanced functions that are not available on ST16C554 or ST16C654.

Table 3.21 FCTR – Feature Control Register

FCTR Bit	FUNCTION	PROGRAMMING
3-0	Auto RTS/DTR Flow Control Hysteresis Select	0000 = 0 Hysteresis (characters) 0001 = ±4 0010 = ±6 0011 = ±8 0100 = ±8 0101 = ±16 0110 = ±24 0111 = ±32 1100 = ±12 1101 = ±20 1110 = ±28 1111 = ±36 1000 = ±40 1001 = ±44 1010 = ±48 1011 = ±52
4	Not Used	N/A
5	Auto RS485 Enable	Must be a logic 0 (default) for the AP500 and AP520 and a logic 1 for the AP521.

7-6	Tx and Rx FIFO Trigger Table Select	00 = Table A 01 = Table B 10 = Table C 11 = Table D (refer to Table 3.10)

3.4.14 Enhanced Feature Register (EFR) – Read/Write

The Enhanced Feature register is used to enable or disable enhanced features, including software flow control. This register is also used to unlock access to programming the extended register functionality of IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7.

Table 3.21 EFR - Enhanced Feature Register

EFR Bit	FUNCTION	PROGRAMMING
3-0	Software Flow Control	00XX = No Transmit Flow Control 10XX = Transmit Xon1/Xoff1 01XX = Transmit Xon2/Xoff2 11XX = Transmit Xon1 and Xon2, Xoff1 and Xoff2 XX00 = No receive Flow Control XX10 = Receiver Compares Xon1/Xoff1 XX01 = Receiver Compares Xon2/Xoff2 1011 = Transmit Xon1/Xoff1, Receiver compares Xon1 or Xon2, Xoff1 or Xoff2. 0111 = Transmit Xon2/Xoff2. Receiver compares Xon1 or Xon2, Xoff1 or Xoff2. 1111 = Transmit Xon1 and Xon2, Xoff1 and Xoff2; Receiver compares Xon1 and Xon2, Xoff1 and Xoff2. 0011 = No transmit flow control. Receiver compares Xon1 and Xon2, Xoff1 and Xoff2. Software flow control can not be used on the AP521.
4	Enhanced Function Control	0 = Disable and latch the Enhanced Functions: the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7. This feature prevents existing software from altering or overwriting the enhanced functions.

		1 = Enables the enhanced functions. Allows the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 to be modified.
5	Special Character Detect Control	0 = Disable special character detect. 1 = Enable special character detect. Incoming receive characters are compared with Xoff-2 data. If a match exists, the receive data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Bit-0 of the Xoff/Xon registers corresponds with the LSB bit for the receive character. When this feature is enabled, the normal software flow control must be disabled (EFR bits 0-3 must be set to a logic "0").
6	RTS Hardware Flow Control	0 = Disable Automatic RTS flow control. 1= Enable Automatic RTS flow control. The RTS pin can be automatically controlled to indicate local buffer overflows to remote buffers. When automatic hardware flow control is enabled, an interrupt will be generated when the receive FIFO is filled to the program trigger level and RTS will go to a logic "1" at the next trigger level. RTS will return to a logic "0" when data is unloaded below the next lower trigger level. RTS functions normally when hardware flow control is disabled. FCTR bits0-1 are used to set the RTS delay timer/trigger level.
7	CTS Hardware Flow Control	0 = Disable Automatic CTS flow control. 1 = Enable Automatic CTS flow control. The CTS pin can be monitored for remote buffer overflow indication. When automatic CTS hardware flow control is enabled, a CTS transition from logic "0" to a logic "1" to indicate a flow control request, ISR bit-5 will be set to a logic "1" (if enabled via IER bit6-7), and transmission of data will be suspended as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS input returns to a logic "0", indicating more data may be sent.

The CTS and RTS signals are available on the AP500 and AP520 model.

3.4.15 Transmit FIFO Level Counter – Read Only

Transmit FIFO level byte count from 0x00 (0 bytes) to 0xFF (255 or 256 bytes). This 8-bit register gives an indication of the number of characters in the transmit FIFO. The FIFO level Byte count register is read only. The user can take advantage of the FIFO level byte counter for faster data loading to the transmit FIFO, which reduces CPU bandwidth requirements.

3.4.16 Transmit FIFO Trigger Level – Write Only

An 8-bit value written to this register sets the TX FIFO trigger level from 0x01 (one) to 0xFF (255). A value of 0x00 is invalid. The TX FIFO trigger level generates an interrupt whenever the data level in the transmit FIFO falls below this preset trigger level.

3.4.17 Receive FIFO Level Counter – Read Only

Receive FIFO level byte count from 0x00 (zero) to 0xFF (255). It gives an indication of the number of characters in the receive FIFO. The FIFO level byte count register is read only. The user can take advantage of the FIFO level byte counter for faster data unloading from the receiver FIFO, which reduces CPU bandwidth requirements.

3.4.18 Receive FIFO Trigger Level – Write Only

An 8-bit value written to this register, sets the RX FIFO trigger level from 0x01 (one) to 0xFF (255). A value of 0x00 is invalid. The RX FIFO trigger level generates an interrupt whenever the receive FIFO level rises to this preset trigger level.

3.4.19 XOFF1, XOFF2, XON1 and XON2 Registers – Write Only

These registers are used to program the Xoff1, Xoff2, Xon1 and Xon2 control characters respectively.

3.4.20 XCHAR Register – Read Only

This register gives the status of the last sent control character (Xon or Xoff) and the last received control character (Xon or Xoff). This register will be reset to 0x00 if, at any time, the Software Flow Control is disabled.

Table 3.22 XCHAR Register

XCHAR Bit	FUNCTION	PROGRAMMING
0	XOFF Detect Indicator	If the last received control character was a Xoff character or characters (Xoff1, Xoff2), this bit will be set to a logic 1. This bit will clear after the read.
1	XON Detect Indicator	If the last received control character was a Xon character, Xon characters (Xon1, Xon2) or an Xon-Any character, this bit will be set to a logic 1. This

		bit will clear after the read.
2	Transmit XOFF Indicator	If the last transmitted control character was a Xoff character or characters (Xoff1, Xoff2), this bit will be set to a logic 1. This bit will clear after the read.
3	Transmit XON Indicator	If the last transmitted control character was a Xon character or characters (Xon1, Xon2), this bit will be set to a logic 1. This bit will clear after the read.
7-4	Reserved.	Reserved.

4.0 SERVICE AND REPAIR

4.1 Service and Repair Assistance

Surface-Mounted Technology (SMT) boards like the AcroPack family of carrier boards are generally difficult to repair. The board can be easily damaged unless special SMT repair and service tools are used. For these and other reasons, it is strongly recommended that a non-functioning board be returned to Acromag for repair. Acromag has automated diagnostic and test equipment that thoroughly checks the performance of suspect boards. Furthermore, when any repair is made, the board is retested before return shipment to the customer.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts, or return parts for repair.

4.2 Preliminary Service Procedure

CAUTION: POWER MUST BE TURNED OFF BEFORE SERVICING BOARDS

Before beginning repair, be sure that all of the procedures in the "Preparation for Use" section have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique for isolating a faulty part.

4.3 Where to Get Help

If you continue to have problems, your next step should be to visit the Acromag website at https://www.acromag.com. Our website contains the most up-to-date product and software information.

Go to the "Support" tab or your specific AcroPack model ordering page.

Acromag's application engineers can also be contacted directly for technical assistance via email or telephone through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab. When needed, complete repair services are also available.

- Phone: 248-295-0310
  Email: solutions@acromag.com

5.0 SPECIFICATIONS

5.1 Physical

Height (carrier to top of module components): 12.5 mm (0.4921 in) [MAX]
Board Thickness: 1.0 mm (0.03937 in)
Length x Width: 70.0 mm x 30.0 mm (2.76 in x 1.18 in)
Unit Weight (not including shipping material): 8g (0.282 oz)

5.2 Power Requirements

Summarized below are the expected current draws for each of the specified power supply voltages.

Table 5.1 Power Requirements

Power Supply Voltage	Current Draw (Idle/Typical)[1]		
	AP500	AP520	AP521
3.3 VDC ± 5%	60/100mA	70/110mA	70/150mA
5.0 VDC ± 5%	NOT USED	NOT USED	40/40mA
1.5 VDC ± 5%	NOT USED		
12 VDC ± 5%	NOT USED		
-12 VDC ± 5%	NOT USED		

Note 1: *Idle current draw was measured with no external loopbacks installed and no active communication on any port.*

Typical current draw was measured with external loopbacks installed on every module port, actively running a loopback test using Passmark Burn-In Test.

5.3 Environmental Considerations

Summarized below are the operating temperature range, airflow and other environmental requirements and applicable standards for the AcroPack module.

5.3.1 Operating Temperature

All modules have an operational temperature range of -40°C to 85°C[1,2].

Note 1: An air cooled application with an AcroPack module will require a minimum airflow of 200LFM.

Note 2: A conduction cooled application with an AcroPack module will require purchase of the Heatsink **AP-CC-01**.

5.3.2 Other Environmental Requirements

5.3.2.1 Relative Humidity

The range of acceptable relative humidity is 5% to 95% non-condensing.

5.3.2.2 Isolation

The PCIe bus and field commons are non-isolated and have a direct electrical connection.

5.3.3 Vibration and Shock Standards

The AcroPack module is designed to pass the following Vibration and Shock standards.

Vibration, Sinusoidal Operating: Designed to comply with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis

Vibration, Random Operating: Designed to comply with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis

Shock, Operating: Designed to comply with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3mS half sine, 18 shocks at 6 orientations for both test levels

5.3.4 EMC Directives

The AcroPack module is designed to comply with EMC Directive 2004/108/EC.

- **Immunity per EN 61000-6-2:**
  Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2.
  Radiated Field Immunity (RFI), per IEC 61000-4-3.
  Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4.
  Surge Immunity, per IEC 61000-4-5.
  Conducted RF Immunity (CRFI), per IEC 61000-4-6.
- **Emissions per EN 61000-6-4:**
  Enclosure Port, per CISPR 16.
  Low Voltage AC Mains Port, per CISPR 16.
  Note: This is a Class A product

5.4 Reliability Prediction

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled,* $G_B G_C$

Table 5.4 MTBF (all models)

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	8,952,551	1,022.0	111.7
40°C	5,412,456	617.9	184.8

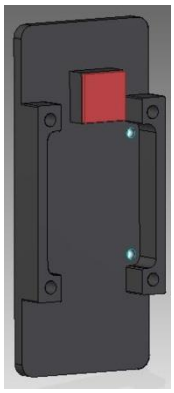
[1] FIT is Failures in 10^9 hours.

5.5 PCIe Bus Specifications

Compatibility	Conforms to PCI Express Base Specification, Revision 2.1
Line Speed	Gen1 (2.5Gbps)
Lane Operation	1-Lane
16K Memory Space Required	One Base Address Register

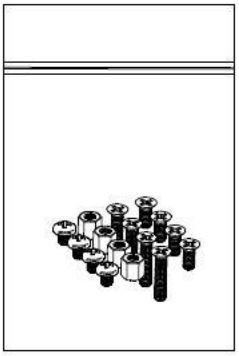
Appendix A

AP-CC-01 Heatsink Kit Installation



Bottom view

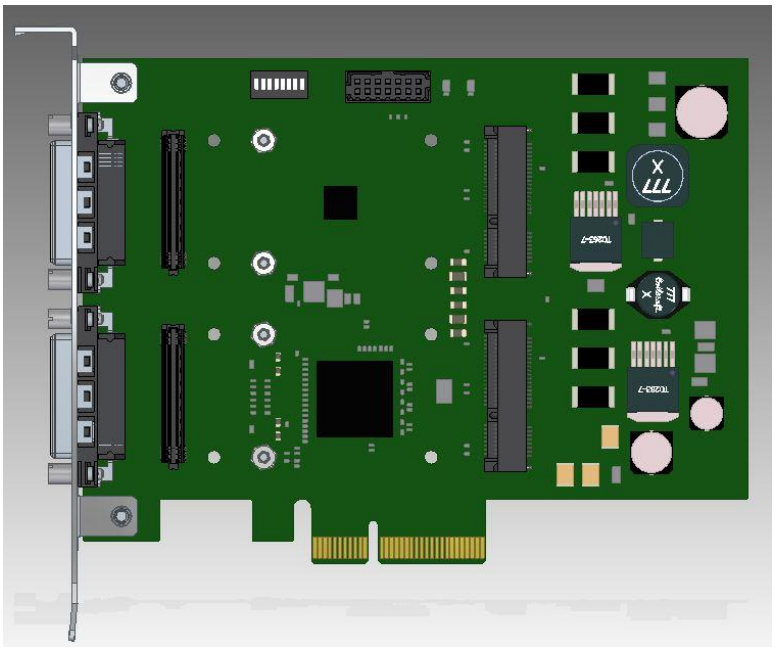
Top view



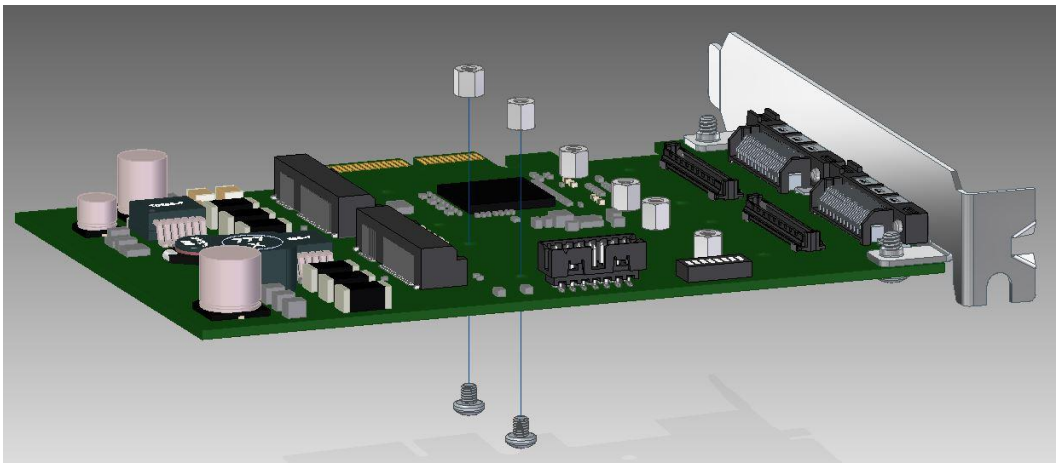
Hardware

AP-CC-01 Heat Sink Kit

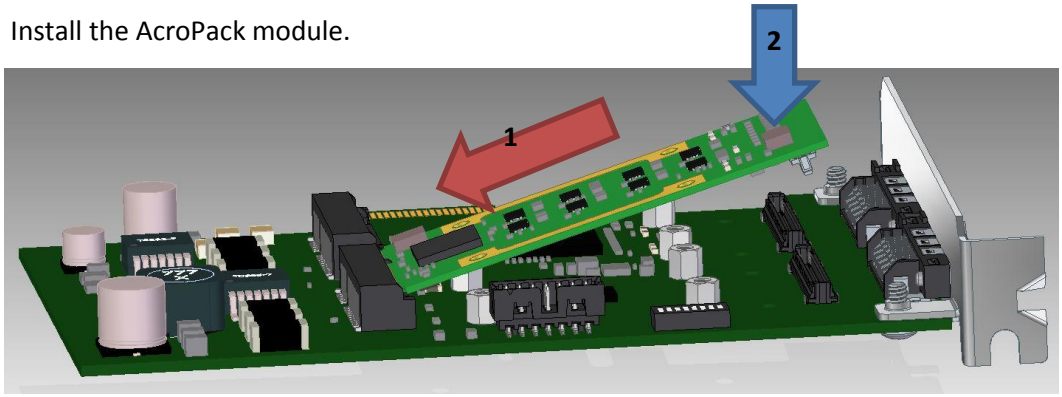
This example will show how to install the AP-CC-01 Heatsink kit with an APCe7020 carrier.



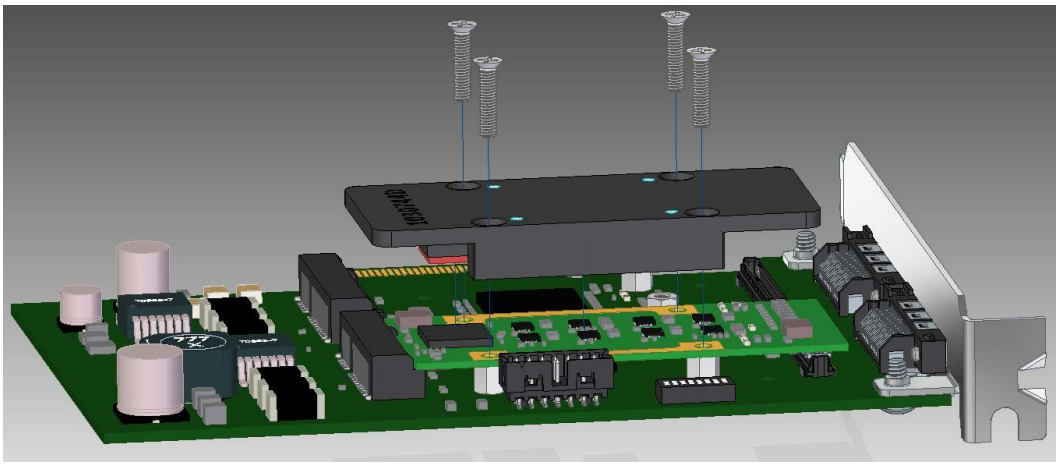
1. Install two standoffs and secure with two screws.



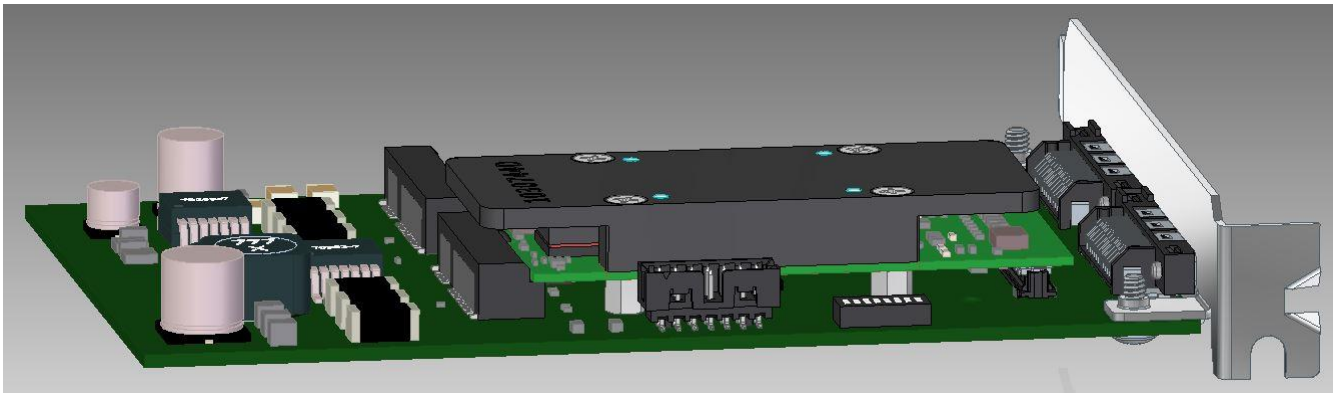
2. Install the AcroPack module.



3. Install the Heatsink and secure with 4 screws.



4. AP-CC-01 Installation is complete.



Note: Make sure the thermal pad is making contact with the UART IC.

Certificate of Volatility

<table>
<tr><th colspan="6">Certificate of Volatility</th></tr>
<tr><td colspan="2">Acromag Model
AP500E-LF
AP520-64E-LF
AP521-64E-LF</td><td colspan="4">Manufacturer:
Acromag, Inc.
30765 Wixom Rd
Wixom, MI 48393</td></tr>
<tr><th colspan="6">Volatile Memory</th></tr>
<tr><td colspan="6">Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed)
■ Yes □ No</td></tr>
<tr><td>Type (SRAM, SDRAM, etc.)

UART Internal Registers/FIFOs (SRAM)</td><td>Size:

4k bytes (AP500)

8k bytes (AP520/521)</td><td>User Modifiable:
■ Yes
□ No</td><td>Function:
UART Communication</td><td colspan="2">Process to Sanitize:
Power Down</td></tr>
<tr><th colspan="6">Non-Volatile Memory</th></tr>
<tr><td colspan="6">Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed)
□ Yes ■ No</td></tr>
<tr><th colspan="6">Acromag Representative</th></tr>
<tr><td>Name:
Russ Nieves</td><td>Title:
Director of Sales and Marketing</td><td colspan="2">Email:
solutions@acromag.com</td><td>Office Phone:
248-295-0310</td><td>Office Fax:
248-624-9234</td></tr>
</table>

Revision History

The revision history for this document is summarized in the table below.

Release Date (DD MMM YYYY)	Version	EGR/DOC	Description of Revision
27 APR 2016	A	DWR/ARP	Initial Release.
19 MAY 2016	B	DWR/ARP	Corrected shock & vibration specifications
18 JUNE 2018	C	LMP/MJO	Added UART Register Descriptions and 68 pin Connector Pin Assignments
18 SEPT 2018	D	LMP/MJO	Added Reliability Prediction MTBF Table Data
11 JUL 2019	E	ENZ/ARP	Updated UART register descriptions and Baud Rate selection details. Updated "Where to Get Help" section.