Acromag®

Series IP409 Industrial I/O Pack
24-Channel Differential Digital I/O Board

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP409 module is a 24-channel differential digital input/output board with interrupts. This model allows channels to be programmed as input or output on a bit basis, in any combination up to 24 channels. All channels can be programmed to generate Change-Of-State (COS), Low, or High level transition interrupts.

Each channel uses a robust RS485/RS422 transceiver which permits half duplex bi-directional data transfer (one direction at a time). The use of differential data transmission allows reliable transmission of data at high rates over up to 4000 meter distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals which appear as common-mode voltages on the line.

The IP409 is available in standard and extended temperature range modules. The IP409 model is the standard temperature range (0 to 70°C) version. The IP409E model is the extended temperature range (-40°C to +85°C) version.

Four units mounted on a carrier board provide up to 96 I/O points per 6U-VMEbus system slot. Since each channel can be independently programmed as an input or output, loopback monitoring is possible. A channel programmed as an input can be used to monitor another channel programmed as an output. The IP409 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its high channel density and is an ideal choice for a wide range of industrial control and monitor applications that require high-density, high-reliability, and high-performance at a low cost.

KEY IP409 FEATURES

- **High Channel Count** - Interfaces with up to 24 input/output points. Four units mounted on a carrier board provide up to 96 input and/or output channels in a single system slot. Input and output channels may be intermixed in any

combination. The input circuitry of a single channel can also be used to monitor the output state of a different channel to efficiently implement "loopback" output control.

- **Long Distance Data Transmission -** Data transmission with up to 32 nodes and up to 4000 feet is possible.
- **Robust RS485/RS422 Transceivers** - The IP409 is designed for electrically harsh environments. All differential I/O channels are protected against electrostatic discharge (ESD), electrical fast transient (EFT), and electromagnetic interference (EMI).
- **Programmable Change-of-State/Level Interrupts -** Interrupts are software programmable for any bit Change-Of-State or Level on an individual channel basis.
- **Socketed Termination Resistors** - The network termination resistors are installed in sockets on the board and may be easily inserted or removed as required.
- **No Configuration Jumpers or Switches** - All configuration is performed through software commands with no internal jumpers to configure or switches to set.
- **Power Up & System Reset is Failsafe** - For safety, all channels are configured as input upon power-up and after a system reset.
- **Output Channels With Read Back** - The differential output channel registers can be read back to verify programmed logic levels.

INDUSTRIAL I/O PACK INTERFACE FEATURES

- **High density -** Single-size, industry-standard, IP module footprint. Up to four units may be mounted on a 6U VMEbus carrier board or five units may be mounted on a PCI carrier board.
- **Local ID** - Each IP module has its own 8-bit ID information which is accessed via data transfers in the "ID Read" space.
- **16-bit & 8-bit I/O** - Channel register Read/Write is performed through D16 or D08 (EO) data transfer cycles in the IP module I/O space.
- **High Speed** - Access times for all data transfer cycles are described in terms of "wait" states. For Models IP409 and IP409E, 0 wait states are required for all read and write operations (see specifications for detailed information).

SIGNAL INTERFACE PRODUCTS

(See Appendix for more information on compatible products)

This IP module will mate directly to any industry standard IP carrier board (including Acromag's AVME9630/9660 VMEbus, APC8610 ISA bus, and APC8620 PCI bus non-intelligent carrier boards). A wide range of other Acromag IP modules are also available to serve your signal conditioning and interface needs.

The cables and termination panels, described in the following paragraphs, are also available. Consult your carrier board documentation for the correct interface product part numbers to ensure compatibility with your carrier board.

Cables:

Model 5025-551-X (Shielded Cable), or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9630/9660, or other compatible carrier boards, to Model 5025-552 termination panels. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.

Termination Panel:

Model 5025-552: A DIN-rail mountable panel that provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9630/9660, APC8610, APC8620, or other compatible carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

Transition Module:

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from a VMEbus card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. It connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within the card cage, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

INDUSTRIAL I/O PACK SOFTWARE LIBRARY

Acromag provides an Industrial I/O Pack Software Library diskette to simplify communication with the board (Model IPSW-LIB-M03, MSDOS format). Example software functions are provided. All functions are written in the "C" programming language and can be linked to your application. Refer to the "README.TXT" file in the root directory and the "INFO409.TXT" file in the "IP409" subdirectory on the diskette for more details.

IP MODULE OLE CONTROL SOFTWARE

Acromag provides a software product (sold separately) consisting of IP module OLE (Object Linking and Embedding) drivers for Windows 95® and Windows NT® compatible application programs (Model IPSW-OLE-PCI, MSDOS format). This software provides individual drivers that allow Acromag IP modules and our personal computer carriers to be easily integrated into Windows® application programs, such as Visual C++™, Visual Basic®, Borland Delphi®, Microsoft® Office® 97 applications and others. The OLE controls provide a high-level interface to IP modules, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the OLE controls. These functions are intended for use in conjunction with an Acromag personal computer carrier and consist of a Carrier OLE Control, and an OLE control for each Acromag IP module as well as a generic OLE control for non-Acromag IP modules.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is

suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-434 and the following discussion for configuration and assembly instructions. Model IP409 I/O Boards have no jumpers or switches to configure--interrupts are configured through software commands.

CONNECTORS

IP Field I/O Connector (P2)

P2 provides the field I/O interface connector for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly.

P2 pin assignments are unique to each IP model (see Table 2.1) and normally correspond to the pin numbers of the field-I/O interface connector on the carrier board (you should verify this for your carrier board). When reading Table 2.1 note that channel designations are abbreviated to save space. For example, channel 0 is abbreviated as I/O00+ and I/O00- for the + and - connections, respectively.

Table 2.1: IP409 Field I/O Pin Connections (P2)

Pin Description	Number	Pin Description	Number
I/O00+	1	I/O12-	26
I/O00-	2	I/O13+	27
I/O01+	3	I/O13-	28
I/O01-	4	I/O14+	29
I/O02+	5	I/O14-	30
I/O02-	6	I/O15+	31
I/O03+	7	I/O15-	32
I/O03-	8	I/O16+	33
I/O04+	9	I/O16-	34
I/O04-	10	I/O17+	35
I/O05+	11	I/O17-	36
I/O05-	12	I/O18+	37
I/O06+	13	I/O18-	38
I/O06-	14	I/O19+	39
I/O07+	15	I/O19-	40
I/O07-	16	I/O20+	41
I/O08+	17	I/O20-	42
I/O08-	18	I/O21+	43
I/O09+	19	I/O21-	44
I/O09-	20	I/O22+	45
I/O10+	21	I/O22-	46
I/O10-	22	I/O23+	47
I/O11+	23	I/O23-	48
I/O11-	24	RESERVED	49
I/O12+	25	GND	50

I/O Noise and Grounding Considerations

The IP409 is non-isolated between the logic and field I/O grounds since output common is electrically connected to the IP module ground. Consequently, the field I/O connections are not isolated from the carrier board and backplane. Two ounce copper ground plane foil has been employed in the design of this model to help minimize the effects of ground bounce, impedance drops, and switching transients. However, care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

To minimize high levels of EMI the signal ground connection at the field I/O port (pin 50) should be used to provide a path for induced common-mode noise and currents. The ground path provides a low-impedance path to reduce emissions.

EIA RS485/RS422 communication distances are generally limited to less than 4000 feet. To minimize transmission-line problems, all nodes connected to the cable must use minimum stub length connections. The optimal configuration for the RS485/RS422 bus is a daisy-chain connection from node 1 to node 2 to node 3 to node n. The bus must form a single continuous path, and the nodes in the middle of the bus must not be at the ends of long branches, spokes, or stubs. See Drawing 4501-702 for example connection and termination practices.

Transmission line signal reflections can be minimized with proper termination. The EIA RS485/RS422 standard allows up to 32 driver/receivers to be connected to a single bus. Termination resistors should only be used at the two extreme ends of the bus and not at each of the nodes of the bus. See Drawing 4501-703 to locate termination resistor SIPs.

IP Logic Interface Connector (P1)

P1 of the IP module provides the logic interface to the mating connector on the carrier board. This connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly. The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.2). Note that the IP409 does not utilize all of the logic signals defined for the P1 connector and these are indicated in ***BOLD ITALICS***.

Table 2.2: Standard Logic Interface Connections (P1)

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSEL*	29
D01	5	***DMAReq0****	30
D02	6	MEMSEL*	31
D03	7	***DMAReq1****	32
D04	8	IntSel*	33
D05	9	***DMAck0****	34
D06	10	IOSEL*	35
D07	11	***RESERVED***	36
D08	12	A1	37
D09	13	***DMAEnd****	38
D10	14	A2	39
D11	15	***ERROR****	40
D12	16	A3	41
D13	17	INTReq0*	42
D14	18	A4	43
D15	19	***INTReq1****	44
BS0*	20	A5	45
BS1*	21	***STROBE****	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	***RESERVED***	49
GND	25	GND	50

Asterisk (*) is used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by this IP Model.

3.0 PROGRAMMING INFORMATION

ADDRESS MAPS

This board is addressable in the Industrial Pack I/O space to control the data transfer, and steering logic of the 24 EIA RS485/RS422 serial ports. The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1..A6, but the IP409 only uses a portion of this space. The I/O space address map for the IP409 is shown in Table 3.1.

Table 3.1: IP409 I/O Space Address (Hex) Memory Map

EVEN Base Addr.+	EVEN Byte D15 D08	ODD Byte D07 D00	ODD Base Addr.+
00	Control Register		**01**
02	Input/Output Channel Reg B CH15 ↔ CH08	Input/Output Channel Reg A CH07 ↔ CH00	**03**
04	Not Used[2]	Input/Output Channel Reg C CH23 ↔ CH16	**05**
06	Direction Control Register B CH15 ↔ CH08	Direction Control Register A CH07 ↔ CH00	**07**
08	Not Used[2]	Direction Control Register C CH23 ↔ CH16	**09**
0A	R/W - Interrupt Enable Register B CH15 ↔ CH08	R/W - Interrupt Enable Register A CH07 ↔ CH00	**0B**
0C	Not Used[2]	R/W - Interrupt Enable Register C CH23 ↔ CH16	**0D**
0E	R/W - Interrupt Type Register B CH15 ↔ CH08	R/W - Interrupt Type Register A CH07 ↔ CH00	**0F**
10	Not Used[2]	R/W - Interrupt Type Register C CH23 ↔ CH16	**11**
12	R/W - Interrupt Status Register B CH15 ↔ CH08	R/W - Interrupt Status Register A CH07 ↔ CH00	**13**
14	Not Used[2]	R/W - Interrupt Status Register C CH23 ↔ CH16	**15**
16	R/W - Interrupt Polarity Register B CH15 ↔ CH08	R/W - Interrupt Polarity Register A CH07 ↔ CH00	**17**
18	Not Used[2]	R/W - Interrupt Polarity Register C CH23 ↔ CH16	**19**
1A	Not Used[2]	R/W - Interrupt Vector Register[1]	**1B**
1C ↓ 7E	NOT USED[2]		**1D ↓ 7F**

Notes (Table 3.1):

1. The upper 8 bits (even byte) of this register are not driven upon on interrupt select cycle. Pullups on the carrier board data bus will cause these bits to always read high (1's).
2. The IP will respond to addresses that are "Not Used" with an active IP module acknowledge ACK~. Data read at "Not Used" addresses will be driven low.

The base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown in Table 3.1 to properly access the I/O space. Accesses can be performed on an 8-bit (D08[EO]), or 16-bit (D16) word basis.

The memory map for this module is given assuming byte accesses using the "Big Endian" byte ordering format. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses. The Intel x86 family of microprocessors uses the opposite convention, or "Little Endian" byte ordering. Little Endian uses even-byte addresses to store the low-order byte. As such, use of the memory map for this module on a PC carrier board will require the use of the even address locations to access the lower 8-bit data. On a VMEbus carrier use of odd address locations are required to access the lower 8-bit data as shown in Table 3.1.

Control Register (Write) - (Base + 00H)

This read/write register is used to issue a software reset. Bit-0 when set to a logic high will perform a software reset. When read this register will return random values.

Input/Output Channel Registers (Read/Write) - (Base + 02, 03, 05)

Twenty-four possible input/output channels numbered 0 through 23 may be individually accessed via these registers. The Input/Output Channel registers are used to monitor/read or set/write channels 0 through 23. Channels 7 to 0 are accessed at the carrier base address +03 via data bits 7 to 0. Channels 15 to 8 are accessed at the carrier base address +02 via data bits 15 to 8. Channels 23 to 16 are accessed at carrier base address + 05 via data bits 7 to 0.

The table below shows all channels and their corresponding I/O data bit.

Input/Output Channel 7 to 0 Register							
Data Bit 07	Data Bit 06	Data Bit 05	Data Bit 04	Data Bit 03	Data Bit 02	Data Bit 01	Data Bit 00
Ch07	Ch06	Ch05	Ch04	Ch03	Ch02	Ch01	Ch00
Input/Output Channel 15 to 8 Register							
Data Bit 15	Data Bit 14	Data Bit 13	Data Bit 12	Data Bit 11	Data Bit 10	Data Bit 09	Data Bit 08
Ch15	Ch14	Ch13	Ch12	Ch11	Ch10	Ch09	Ch08
Input/Output Channel 23 to 16 Register							
Data Bit 07	Data Bit 06	Data Bit 05	Data Bit 04	Data Bit 03	Data Bit 02	Data Bit 01	Data Bit 00
Ch23	Ch22	Ch21	Ch20	Ch19	Ch18	Ch17	Ch16

Channel read/write operations use 8-bit, or 16-bit data transfers with the lower ordered bits corresponding to the lower-numbered channels for the register of interest. All input/output channels are configured as inputs on a power-on or software reset. The unused upper 8 bits of register C are "Not Used" and will always read low (0's) for D16 accesses.

Direction Control Registers (Read/Write) - (Base + 06, 07, 09)

The data direction (input or output) of the 24 differential channels is selected via these registers. The data direction of each channel can be independently set on a bit by bit basis. Setting a bit high configures the corresponding channel data direction for output. Setting the control bit low configures the corresponding channel data direction for input.

The default power-up state of these registers is logic low. Thus, all channels are configured as inputs on system reset or power-up. The unused upper byte of register C is "Not Used" and will always read low (0's).

Interrupt Enable Registers (Read/Write) - (Base + 0A, 0B, 0D)

The Interrupt Enable Registers provide a mask bit for each of the 24 channels. A "0" bit will prevent the corresponding input channel from generating an external interrupt. A "1" bit will allow the corresponding input channel to generate an interrupt. Only those channels configured as inputs can generate interrupts.

The Interrupt Enable register at the carrier's base address + offset 0B is used to control channels 00 through 07. For example, channel 00 is controlled via data bit-0 as seen in the table below. Registers for Channels 15 to 08 and Channels 23 to 16 are accessed similarly at offsets 0A and 0D hex, respectively.

Interrupt Enable Register							
MSB							LSB
Data Bit 07	Data Bit 06	Data Bit 05	Data Bit 04	Data Bit 03	Data Bit 02	Data Bit 01	Data Bit 00
Ch07	Ch06	Ch05	Ch04	Ch03	Ch02	Ch01	Ch00

Channel read operations use 8-bit, or 16-bit data transfers. The upper 8 bits of register C are "Not Used" and will always read low (0's) for D16 accesses.

All input channel interrupts are disabled (set to "0") following a power-on or software reset.

Interrupt Type (COS or H/L) Configuration Registers (Read/Write) - (Base + 0E, 0F, 11)

The Interrupt Type Configuration Registers determine the type of input channel transition that will generate an interrupt for each of the 24 possible interrupting channels. A "0" bit selects interrupt on level. An interrupt will be generated when the input channel level specified by the Interrupt Polarity Register occurs (i.e. Low or High level transition interrupt). A "1" bit means the interrupt will occur when a Change-Of-State (COS) occurs at the corresponding input channel (i.e. any state transition, low to high or high to low).

The Interrupt Type Configuration register at the carrier's base address + offset 0F is used to control channels 00 through 07. For example, channel 00 is controlled via data bit-0 as seen in the table below. Registers for Channels 15 to 08 and Channels 23 to 16 are accessed similarly at offsets 0E and 11 hex, respectively.

Interrupt Type (COS or H/L) Configuration Register							
MSB							LSB
Data Bit 07	Data Bit 06	Data Bit 05	Data Bit 04	Data Bit 03	Data Bit 02	Data Bit 01	Data Bit 00
Ch07	Ch06	Ch05	Ch04	Ch03	Ch02	Ch01	Ch00

Channel read or write operations use 8-bit, or 16-bit data transfers. The upper 8 bits of register C are "Not Used" and will always read low (0's) for D16 accesses. Note that interrupts will not occur unless they are enabled.

All bits are set to "0" following a reset which means that, if enabled, the inputs will cause interrupts for the levels specified by the digital input channel Interrupt Polarity Register.

Interrupt Status Registers (Read/Write) - (Base + 12, 13, 15)

The Interrupt Status Register reflects the status of each of the interrupting channels. A "1" bit indicates that an interrupt is pending for the corresponding channel. A channel that does not have interrupts enabled will never set its interrupt status flag. A channel's interrupt can be cleared by writing a "1" to its bit position in the Interrupt Status Register (writing a "1" acts as a reset signal to clear the set state). This is known as the "Release On Register Access" (RORA) method, as defined in the VME system architecture specification. However, if the condition which caused the interrupt to occur remains, the interrupt will be generated again (unless disabled via the Interrupt Enable Register). In addition, an interrupt will be generated if any of the channels enabled for interrupt have an interrupt pending (i.e. one that has not been cleared). Writing "0" to a bit location has no effect; that is, a pending interrupt will remain pending.

Note that interrupts are not prioritized via hardware. The system software must handle interrupt prioritization.

The Interrupt Status register at the carrier's base address + offset 13 is used to monitor pending interrupts corresponding to channels 00 through 07. For example, channel 00 is monitored via data bit-0 as seen in the table below. Registers for Channels 15 to 08 and Channels 23 to 16 are accessed similarly at offsets 12 and 15 hex, respectively.

Interrupt Status Register							
MSB							LSB
Data Bit 07	Data Bit 06	Data Bit 05	Data Bit 04	Data Bit 03	Data Bit 02	Data Bit 01	Data Bit 00
Ch07	Ch06	Ch05	Ch04	Ch03	Ch02	Ch01	Ch00

The unused upper 8 bits of register C are "Not Used" and will always read low (0's) for D16 accesses. All bits are set to "0" following a reset which means that all interrupts are cleared.

Interrupt Polarity Registers (Read/Write) - (Base + 16, 17, 19)

The Interrupt Polarity Register determines the level that will cause a channel interrupt to occur for each of the channels enabled for level interrupts. A "0" bit specifies that an interrupt will occur when the corresponding input channel is low (i.e. a "0" in the digital input channel data register). A "1" bit means that an interrupt will occur when the input channel is high (i.e. a "1" in the digital input channel data register). Note that no interrupts will occur unless they are enabled by the Interrupt Enable Register. Further, the Interrupt Polarity Register will have no effect if the Change-of-State (COS) interrupt type is configured by the Interrupt Type Configuration Register.

The Interrupt Polarity register at the carriers base address + offset 17 is used to control channels 00 through 07. For example, channel 00 is controlled via data bit-0 as seen in the table below. Registers for Channels 15 to 8 and Channels 23 to 16 are accessed similarly at offsets 16 and 19 hex, respectively.

Interrupt Polarity Register							
MSB							LSB
Data Bit 07	Data Bit 06	Data Bit 05	Data Bit 04	Data Bit 03	Data Bit 02	Data Bit 01	Data Bit 00
Ch07	Ch06	Ch05	Ch04	Ch03	Ch02	Ch01	Ch00

The upper 8 bits of register C are "Not Used" and will always read low (0's) for D16 accesses. All bits are set to "0" following a reset which means that the inputs will cause interrupts when they are below TTL threshold (provided they are enabled for interrupt on level).

Interrupt Vector Register (Read/Write) - (Base + 1B)

The Interrupt Vector Register maintains an 8-bit interrupt pointer for all channels configured as input channels. The Vector Register can be written with an 8-bit interrupt vector. This vector is provided to the carrier and system bus upon an active INTSEL* cycle. Reading or writing to this register is possible via 16-bit or 8-bit data transfers.

Interrupt Vector Register							
MSB							LSB
07	06	05	04	03	02	01	00

Interrupts are released on register access to the Interrupt Status register. Issue of a software or hardware reset will clear the contents of this register to 0.

IP Identification Space (Read Only, 32 odd-byte addresses)

Each IP module contains identification (ID) information that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID space. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP409 ID Space does not contain any variable (e.g. unique calibration) information. ID Space bytes are addressed using only the odd addresses in a 64 byte block (on the "Big Endian" VMEbus). Even addresses are used on the "Little Endian" PC ISA or PCI buses.

The IP409 ID Space contents are shown in Table 3.2. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID information. Execution of an ID Space Read operation requires 0 wait states.

Table 3.2: IP409 ID Space Identification (ID)

Hex Offset From ID Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All IP's have 'IPAC'
03	P	50	
05	A	41	
07	C	43	
09		A3	Acromag ID Code
0B		20	IP Model Code[1]
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		0C	Total Number of ID PROM Bytes
17		B6	CRC
19 to 3F		yy	Not Used

Notes (Table 3.2):

1. The IP model number is represented by a two-digit code within the ID space (the IP409 model is represented by 20 Hex).

IP409 PROGRAMMING CONSIDERATIONS

To make programming and communicating with the board easier, Acromag provides you with the Industrial I/O Pack Software Library diskette. The functions provided are written in the "C" programming language and can be linked into your application. Refer to the "README.TXT" file in the root directory and the "INFO409.TXT" file in the "IP409" subdirectory on the diskette for details.

Acromag also provides a software diskette of IP module Object Linking and Embedding (OLE) drivers for Windows 95® and Windows NT® compatible application programs (Model IPSW-OLE-PCI, MSDOS format). This software provides individual drivers that allow all IP modules and the APC8620 carrier to be easily integrated into Windows® application programs, such as Visual C++™, Visual Basic®, Borland Delphi®, Microsoft® Office® 97 applications and others. The OLE controls provide a high-level interface to IP modules, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the OLE controls. These functions are intended for use in conjunction with an Acromag personal computer carrier and consist of a carrier OLE control, and an OLE control for each Acromag IP module as well as a generic OLE control for non-Acromag IP modules.

I/O Handshake Operation

The IP409 has 24 channels that can be independently configured as input or output ports. With independent configuration of channels the IP409 can be used to move data in either direction on a word-by-word basis. The data word size can be any number of user defined bits up to the 24 channels, minus the number of handshake channels used.

Channels not used to move data can be defined as handshake signals. The handshake channels can consist of status input lines and control output lines.

There are a number of different handshake protocols available. For example; two directly connected IP409 modules could transfer 16-bit data from IP409A to IP409B. The IP409B will acknowledge the transfer.

For example, IP409A has channels 0 to 15 configured as outputs. Channel 16 is configured as input handshake signal (Ready For Data). Channel 17 is configured as output handshake signal (Output Data Valid~).

The IP409B has channels 0 to 15 configured as inputs. Channel 16 is configured as output handshake signal (Ready For Data). Channel 17 is configured as input handshake signal (Input Data Valid~).

The following step-by-step sequence gives an example of how data could be transferred from IP409A to IP module IP409B.

1. IP409B drives channel 16 (Ready For Data signal) to an active high state. This indicates to the IP409A that the IP409B is ready to receive data. The IP409A drives channel 17 (Output Data Valid~) inactive to a high state.
2. IP409A receives channel 16 (Ready For Data signal) as active high. This indicates to the IP409A that the IP409B is ready to receive new data.
3. IP409A drives valid data on channels 0 to 15 and drives channel 17 (Output Data Valid~) active to a low state.
4. IP409B receives channel 17 (Input Data Valid~) active low. IP409B drives channel 16 (Ready For Data) low, indicating that input register is full and is not ready for new data.
5. IP409B reads the new data from it's input register and then drives channel 16 (Ready For Data) high.

Steps 1-5 would be repeated to transfer additional data.

In addition, channel 17 could be programmed at the IP409B to generate an interrupt upon a change of state to logic low. The interrupt service routine could set channel 16 low and read the input data register. After the data is read, the interrupt service routine could set channel 16 high to inform IP409A it is ready for new data.

Programming Interrupts

Digital input channels can be programmed to generate interrupts for the following conditions:

- Change-of-State (COS) at selected input channels.
- Input level (polarity) match at selected input channels.

Interrupts generated by the IP409 use interrupt request line INTREQ0* (Interrupt Request 0). The interrupt release mechanism employed is the Release On Register Access (RORA) type. This means that the interrupter will release the Industrial I/O Pack interrupt request line (INTREQ0) after all pending interrupts have been cleared by writing a "1" to the appropriate bit positions in the input channel Interrupt Status Register.

The Interrupt Vector Register contains a pointer vector to an interrupt handling routine. One interrupt handling routine must be used to service all possible channel interrupts.

When using interrupts, input channel bandwidth should be limited to reduce the possibility of missing channel interrupts. For a given input channel, this could happen if multiple changes occur before the channel's interrupt is serviced. The response time of the input channels should also be considered when calculating this bandwidth. The total response time is the sum of the input buffer response time, plus the interrupt logic circuit response time, and this time must pass before another interrupt condition will be recognized. The Interrupt Input Response Time is specified in section 6.

The following programming examples assume that the IP409 is installed onto an Acromag AVME9630/9660 carrier board (consult your carrier board documentation for compatibility details).

Programming Example for AVME9630/9660 Carrier Boards:

1. Clear the global interrupt enable bit in the Carrier Board Status Register by writing a "0" to bit 3.
2. Perform Specific IP Module Programming - see the Change-of-State or Level Match programming examples that follow, as required for your application.
3. Write to the carrier board Interrupt Level Register to program the desired interrupt level per bits 2, 1, & 0.
4. Write "1" to the carrier board IP Interrupt Clear Register corresponding to the IP interrupt request(s) being configured.
5. Write "1" to the carrier board IP Interrupt Enable Register bits corresponding to the IP interrupt request to be enabled.
6. Enable interrupts from the carrier board by writing a "1" to bit 3 (the Global Interrupt Enable Bit) of the Carrier Board Status Register.

IP Programming Example for Change-of-State Interrupts:

1. Program the Interrupt Vector Register with the user specified interrupt vector. This vector forms a pointer to a location in memory that contains the address of the interrupt handling routine.
2. Select channel Change-of-State interrupts by writing a "1" to each channel's respective bit in the Interrupt Type Register. Note that Change-Of-State interrupts (specified with "1") may be mixed with polarity match interrupts (specified with "0").
3. Enable individual input channel interrupts by writing a "1" to each channel's respective bit in the Interrupt Enable Register.
4. Clear pending interrupts by writing a "1" to each channel's respective bit in the Interrupt Status Register.

   Change-of-State Interrupts may now be generated by the input channels programmed above for any Change-Of-State transition.

IP Programming Example for Level (Polarity) Match Interrupts:

1. Program the Interrupt Vector Register with the user specified interrupt vector. This vector forms a pointer to a location in memory that contains the address of the interrupt handling routine.
2. Select channel polarity match interrupts by writing a "0" to each channel's respective bit in the Interrupt Type Registers. Note that Change-Of-State interrupts (specified with "1") may be mixed with polarity match interrupts (specified with "0").
3. Select the desired polarity (High/Low) level for interrupts by writing a "0" (Low), or "1" (High) level to each channel's respective bit in the Interrupt Polarity Registers.
4. Enable individual input channel interrupts by writing a "1" to each channel's respective bit in the Interrupt Enable Registers.
5. Clear pending interrupts by writing a "1" to each channel's respective bit in the Interrupt Status Register.

   Interrupts can now be generated by matching the input level with the selected polarity for programmed interrupt channels.

General Sequence of Events for Processing an Interrupt

1. The IP409 asserts the Interrupt Request 0 Line (INTREQ0*) in response to an interrupt condition at one or more inputs.
2. The AVME9630/9660 carrier board acts as an interrupter in making the VMEbus interrupt request (asserts IRQx*) corresponding to the IP interrupt request.
3. The VMEbus host (interrupt handler) asserts IACK* and the level of the interrupt it is seeking on A01-A03.
4. When the asserted VMEbus IACKIN* signal (daisy-chained) is passed to the AVME9630/9660, the carrier board will check if the level requested matches that specified by the host. If it matches, the carrier board will assert the INTSEL* line to the appropriate IP together with (carrier board generated) address bit A1 to select which interrupt request is being processed (A1 low corresponds to IntReq0*; A1 high corresponds to INTREQ1*, which is not supported by the IP409).
5. The IP409 puts the appropriate interrupt vector on the local data bus (D00-D07 for the D08 [O] interrupter) and asserts ACK* to the carrier board. The carrier board passes this along to the VMEbus (D08[O]) and asserts DTACK*.
6. The host uses the vector to form a pointer to an interrupt service routine for the interrupt handler to begin execution.
7. Example of Generic Interrupt Handler Actions:
   A. Disable the interrupting IP by writing "0" to the appropriate bit in the AVME9630/9660 IP Interrupt Enable Register.
   B. Disable the interrupting channel(s) by writing a "0" to the appropriate bits in the IP409 Interrupt Enable Register.
   C. Clear the interrupting channel(s) by writing a "1" to the appropriate bits in the IP409 Interrupt Status Register.
   D. Enable the interrupting channel(s) by writing a "1" to the appropriate bits in the IP409 Interrupt Enable Register.
   E. Clear the interrupting IP by writing a "1" to the appropriate bit in the AVME9630/9660 IP Interrupt Clear Register.
   F. Enable the interrupting IP by writing a "1" to the appropriate bit in the AVME9630/9660 IP Interrupt Enable Register.
8. If the IP409 interrupt stimulus has been removed and no other IP modules have interrupts pending, the interrupt cycle

is complete (i.e. the carrier board negates its interrupt request, IRQ*).

A. If the IP409 interrupt stimulus remains, a new interrupt request will immediately follow. If the stimulus cannot be removed, the IP409 should be disabled or reconfigured.
B. If other IP modules have interrupts pending, then the interrupt request (IRQx*) will remain asserted. This will start a new interrupt cycle.

4.0 THEORY OF OPERATION

This section describes the basic functionality of the circuitry used on the board. Refer to the Block Diagram shown in Drawing 4501-701 as you review this material.

FIELD INPUT/OUTPUT SIGNALS

The field I/O interface to the IP module is provided through connector P2 (refer to Table 2.1). These pins are tied to the inputs and outputs of EIA RS485/RS422 line transceivers. Signals received are converted from the required EIA RS485/RS422 voltages signals to the TTL levels required by the Field Programmable Gate Array (FPGA). Likewise TTL signals are converted to the EIA RS485/RS422 voltages for data output transmission. The Field Programmable Gate Array provides the necessary interface to the RS485/RS422 transceivers for control of data output or input and monitoring of input signals for generation of interrupts, if enabled.

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.1). Field I/O points are NON-ISOLATED. This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring this effect may cause operational errors, and with extreme abuse, possible circuit damage.

LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1 (refer to Table 2.2). P1 also provides +5V power the module (±12V is not used). Note that the DMA control, INTREQ1*, ERROR*, and STROBE* signals are not used.

A Field Programmable Gate Array installed on the IP Module provides an interface to the carrier board per IP Module specification ANSI/VITA 4 1995. The FPGA logic includes: address decoding, I/O and ID read/write control circuitry, interrupt handling, and ID storage implementation.

Address decoding of the six IP address signals A(1:6) is implemented in the FPGA, in conjunction with the IP select signals, to identify access to the IP module's ID or I/O space. In addition, the byte strobes BS0* and BS1* are decoded to identify low byte, high byte, or double byte data transfers.

The carrier to IP module interface allows access to both ID and I/O space via 16 or 8-bit data transfers. Read only access to ID space provides the identification for the individual module (as given in Table 3.2). per the IP specification. Read and write accesses to the I/O space provide a means to control the IP409.

Access to both ID and I/O space are implemented with zero wait state read or write data transfers.

Interrupt Operation

Digital input channels of this model can be configured to generate interrupts for Change-Of-State (COS) and input level (polarity) match conditions at enabled inputs. An 8-bit interrupt service routine vector is provided during interrupt acknowledge cycles on data lines D0...D7. The interrupt release mechanism employed is RORA (Release On Register Access).

Fail-Safe Operation

The IP409 operation is considered 'Fail-safe'. That is, the input/output channels are always configured as input upon power-up reset, and a system software reset. This is done for safety reasons to ensure reliable control of the output state under all conditions.

EIA-RS485 AND RS422 SERIAL INTERFACE

The EIA-RS485 and RS422 interface specifies a balanced driver with balanced receivers. Balanced data transmission refers to the fact that two conductors are switched per signal and the logical state of the data is referenced by the difference in potential between the two conductors, not with respect to signal ground. The differential method of data transmission makes EIA-RS485 and RS422 ideal for noisy environments since it minimizes the effects of coupled noise and ground potential differences. That is, since these effects are seen as common-mode voltages (common to both lines), not differential, they are rejected by the receivers.

The EIA-RS422 standard defines a bus with a single driver and multiple receivers.

The EIA-RS485 standard defines a bi-directional, terminated, driver and receiver configuration. Half-duplex operation is provided by the sharing of a single data path for transmit and receive. The maximum data transmission cable length is generally limited to 4000 feet without a signal repeater installed.

With respect to EIA-RS485 and RS422, logic states are represented by differential voltages from 1.5 to 5V. The polarity of the differential voltage determines the logical state. A logic "0" is represented by a negative differential voltage between the terminals (measured A to B, or + to -). A logic "1" is represented by a positive differential voltage between the terminals (measured A to B, or + to -). The line receivers convert these signals to the conventional TTL level.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a

burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

PHISICAL

Physical Configuration……..Single Industrial Pack Module.
Length.....3.880 in. (98.5 mm).
Width.....1.780 in. (45.2 mm).
Board Thickness.....0.062 in. (1.59 mm).
Max Component Height.....0.290 in. (7.37 mm).
Connectors:
P1 (IP Logic Interface).....50-pin female receptacle header (AMP 173279-3 or equivalent).
P2 (Field I/O).....50-pin female receptacle header (AMP 173279-3 or equivalent).
Power:
Configured as Output with Termination Resistors Installed
+5 Volts (±5%).....600mA, Typical
800mA Maximum.
Configured as Input
+5 Volts (±5%).....20mA, Typical
30mA Maximum.
+/-12 Volts (±5%) from P1..0mA (Not Used)

Maximum Vcc Rise Time....100m seconds

ENVIRONMENTAL

Operating Temperature.....Standard Unit 0 to +70°C.
"E" suffixed units -40°C to +85°C.
Relative Humidity.....5-95% Non-Condensing.
Storage Temperature.....-55°C to +125°C.

Non-Isolated.....Logic and field commons have a direct electrical connection.
Resistance to RFI.....Designed to comply with IEC1000-4-3 Level 3 (10V/m at frequencies o f 27MHz to 500MHz) and European Norm EN50082-1.

Electromagnetic Interference
Immunity (EMI)…..No digital upset under the influence of EMI from switching solenoids, commutator motors, and drill motors.

Electrostatic Discharge
Immunity (ESD)…..Complies with IEC1000-4-2 Level 1 (2KV direct contact discharge) at field input/output terminals and European Norm EN50082-1.

Surge Immunity……Not required for signal I/O per European Norm EN50082-1.

Electric Fast Transient
Immunity EFT…….. Complies with IEC1000-4-4 Level 2 (0.5KV at field input and output terminals) and European Norm EN50082-1.

Radiated Emissions…….... Meets or exceeds European Norm EN50081-1 for class A equipment.

Warning: This is a class A product. In a domestic environment this product may cause radio interference in which the user may be required to take adequate measures.

EIA-RS485 TRANSCEIVERS

Channel Configuration…….. 24 independent, non-isolated EIA RS485/RS422 serial ports with a common signal return connection.
Data Rate…… 250K bits/sec, Maximum.
Cable Length…….. 4000 feet, Maximum. Use of a signal repeater can extend transmission distances beyond this limit.
Termination Resistors…….120Ω Termination Resistors installed in sockets on board at network end points only (see Drawing 4501-703 for location.
Differential Output Voltage…… 5V Maximum; 1.5V Minimum (with 27Ω load).
Common Mode Output
Voltage…….. 3V Maximum.
Output Short Circuit Current…. 250mA, Maximum.

Rise or Fall Time…… 250ns Minimum, 800ns Typical, 2000ns Maximum (R_{DIFF} = 54Ω, C_L =100pF).

Input Hysteresis…….. 70mV (V_{CM}=0V).

Interrupt Input Response
Time…….. 500nS minimum to 2250nS maximum, depending on when the input transition occurs with respect to the 8MHz clock. Measured from input transition to INTREQ0 line assertion.

INDUSTRIAL I/O PACK COMPLIANCE

Specification……. This device meets or exceeds all written Industrial I/O Pack specifications per ANSI/VITA 4 1995 for 8MHz operation for Type I Modules.
Electrical/Mechanical Interface……..... Single-Size IP Module.
I/O Space..... 16-bit and 8-bit:
ID Space..... 16 and 8-bit; Supports Type 1, 32 bytes per IP (consecutive odd byte addresses).
Memory Space..... Not Used.
Interrupts……..... Generates INTREQ0* interrupt request per IP and interrupt acknowledge cycles via access to IP INT space.

Access Times (8MHz Clock):
ID Space Read.....…….... 0 wait state (250ns cycle).
Channel Registers Read……... 0 wait state (250ns cycle).
Channel Registers Write……... 0 wait state (250ns cycle).
Interrupt Registers Read……... 0 wait state (250ns cycle).
Interrupt Registers Write……... 0 wait state (250ns cycle).

Interrupts:
Handling Format…….... An 8-bit vector is provided during interrupt acknowledge cycles on data lines D0…D7. The release mechanism is RORA type (Release On Register Access).

APPENDIX

CABLE: MODEL 5025-551-x (Shielded)

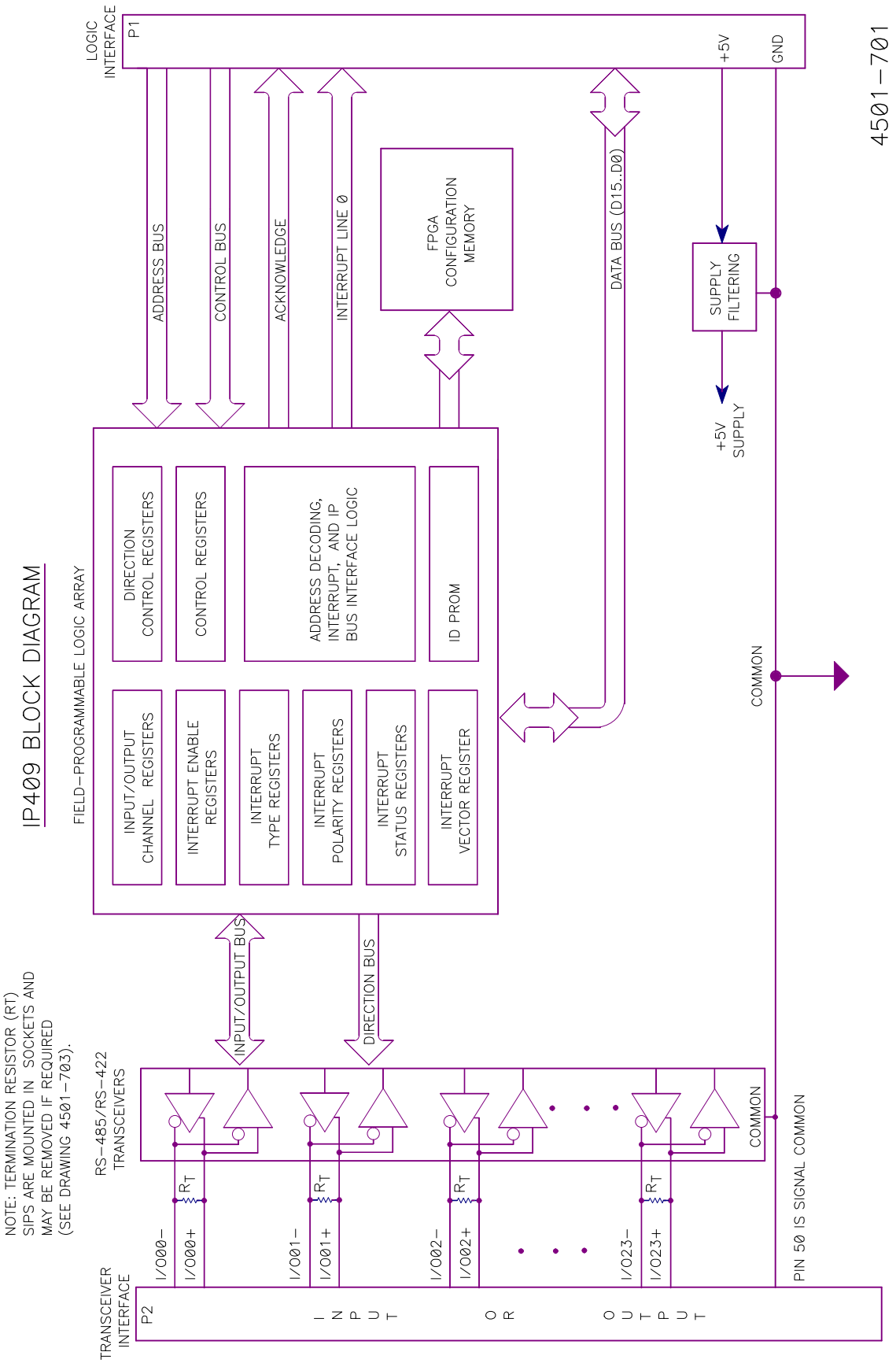
Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet (12 feet maximum). Choose shielded cable according to model number. The shielded cable is highly recommended for optimum performance with analog input or output modules.
Application: Used to connect a Model 5025-552 termination panel to the AVME9630/9660, APC8610, or APC8620 non-intelligent carrier board connectors (both have 50-pin connectors).
Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50-wire flat ribbon cable, 28 gage. Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).
Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).
Keying: Headers at both ends have polarizing key to prevent improper installation.
Schematic and Physical Attributes: See Drawing 4501-463.
Shipping Weight: 1.0 pound (0.5Kg) packaged.

TERMINATION PANEL: MODEL 5025-552

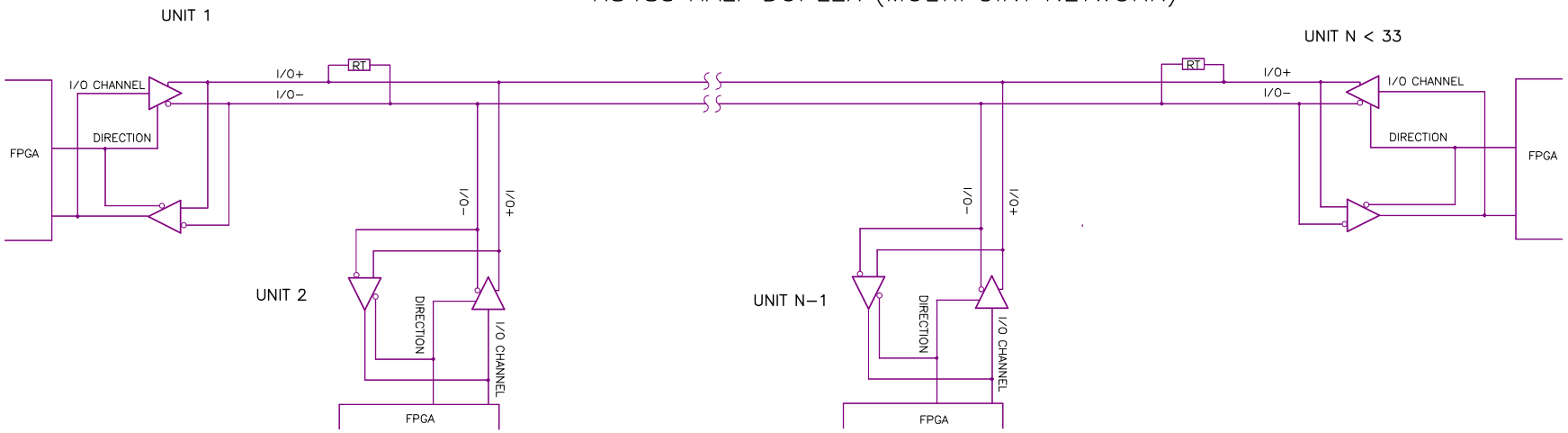
Type: Termination Panel For AVME9630/9660, APC8610, or APC8620 Boards
Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660 3U/6U, APC8610, or APC8620 non-intelligent carrier boards (field connectors only) via a flat ribbon cable (Model 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Connections to AVME9630/9660, APC8610, or APC8620: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight : 1.25 pounds (0.6kg) packaged.

TRANSITION MODULE: MODEL TRANS-GP

Type: Transition module for AVME9630/9660 boards.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-551-X).
Schematic and Physical Attributes: See Drawing 4501-465.
Field Wiring: 100-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-551-X).
Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-551-X).
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Printed Circuit Board: Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +85°C.
Storage Temperature: -55°C to +105°C.
Shipping Weight: 1.25 pounds (0.6Kg) packaged.


IP409 BLOCK DIAGRAM
4501-701
LOGIC INTERFACE
P1
+5V
GND
ADDRESS BUS
CONTROL BUS
ACKNOWLEDGE
INTERRUPT LINE 0
FPGA CONFIGURATION MEMORY
DATA BUS (D15..D0)
SUPPLY FILTERING
+5V SUPPLY
FIELD-PROGRAMMABLE LOGIC ARRAY
DIRECTION CONTROL REGISTERS
CONTROL REGISTERS
ADDRESS DECODING, INTERRUPT, AND IP BUS INTERFACE LOGIC
ID PROM
INPUT/OUTPUT CHANNEL REGISTERS
INTERRUPT ENABLE REGISTERS
INTERRUPT TYPE REGISTERS
INTERRUPT POLARITY REGISTERS
INTERRUPT STATUS REGISTERS
INTERRUPT VECTOR REGISTER
COMMON
INPUT/OUTPUT BUS
DIRECTION BUS
RS-485/RS-422 TRANSCEIVERS
COMMON
RT
I/O00-
I/O00+
I/O01-
I/O01+
I/O02-
I/O02+
I/O23-
I/O23+
TRANSCEIVER INTERFACE
P2
INPUT OR OUTPUT
PIN 50 IS SIGNAL COMMON
NOTE: TERMINATION RESISTOR (RT) SIPS ARE MOUNTED IN SOCKETS AND MAY BE REMOVED IF REQUIRED (SEE DRAWING 4501-703).

RS485 HALF DUPLEX (MULTIPOINT NETWORK)



NOTES:

THE RS−485 STANDARD ALLOWS UP TO 32 DRIVER/RECEIVERS TO BE CONNECTED TO A SINGLE BUS. THE BUS IS A HALF DUPLEX BI−DIRECTIONAL BUS, BUT ONLY ONE DRIVER SHOULD BE ACTIVE AT A TIME.

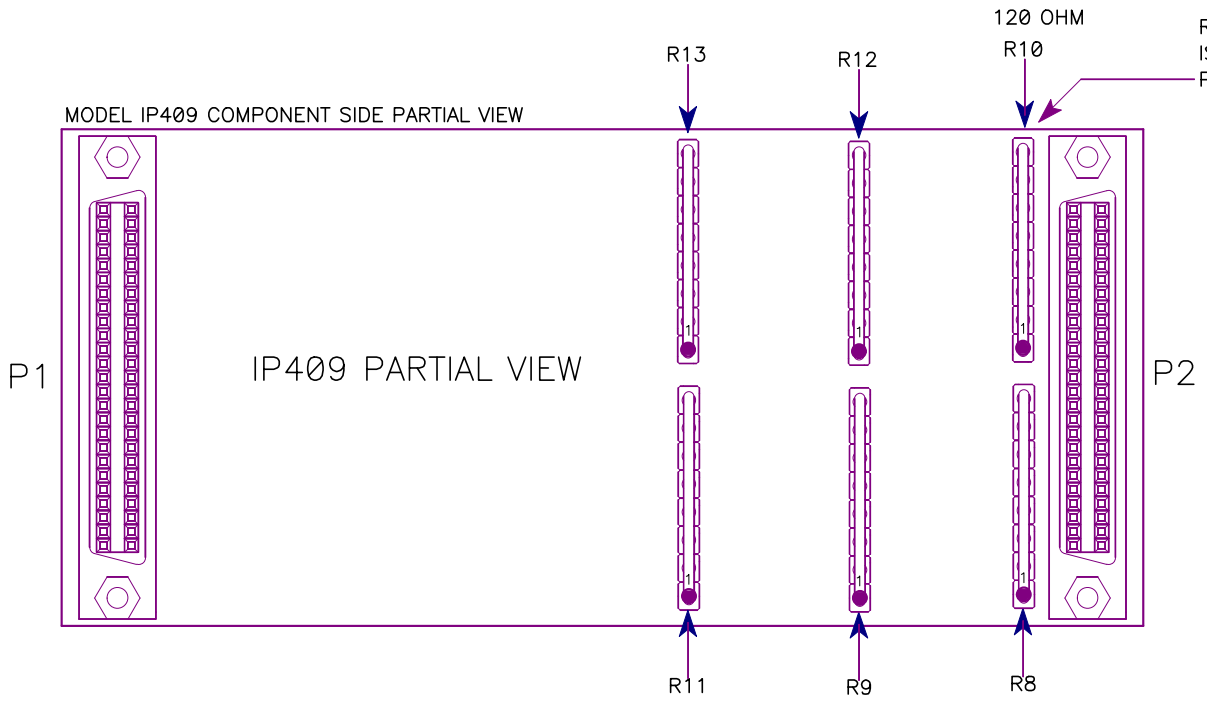
TERMINATION SHOULD BE USED AND ONLY LOCATED AT THE TWO EXTREME ENDS OF THE BUS (NOT AT EACH NODE). THE PURPOSE OF THE TERMINATION IS TO PREVENT ADVERSE TRANSMISSION−LINE REFLECTIONS. TO MINIMIZE POWER DISSIPATION THE TERMINATION RESISTORS CAN BE LEFT OFF. THIS IS POSSIBLE IF THE CABLE IS SHORT AND THE DATA RATE IS LOW. IT IS ALSO POSSIBLE TO MINIMIZE POWER DISSIPATION BY USING AN RC TERMINATION IN PLACE OF THE RESISTOR TERMINATION.

TO MINIMIZE TRANSMISSION−LINE PROBLEMS, ALL NODES CONNECTED TO THE CABLE MUST USE MINIMUM STUB LENGHT CONNECTIONS. IDEALLY ALL NODES SHOULD BE CONNECTED IN A DAISY CHAIN FASHION.

TO MINIMIZE HIGH LEVEL OF EMI THE GROUND WIRE (ON PIN 50) MUST BE USED TO PROVIDE A PATH FOR INDUCED COMMON−MODE NOISE AND CURRENTS. THE GROUND PROVIDES A LOW−IMPEDANCE PATH TO REDUCE EMMISSIONS.

4501−702

IP409 TERMINATION SIP RESISTOR LOCATION DRAWING



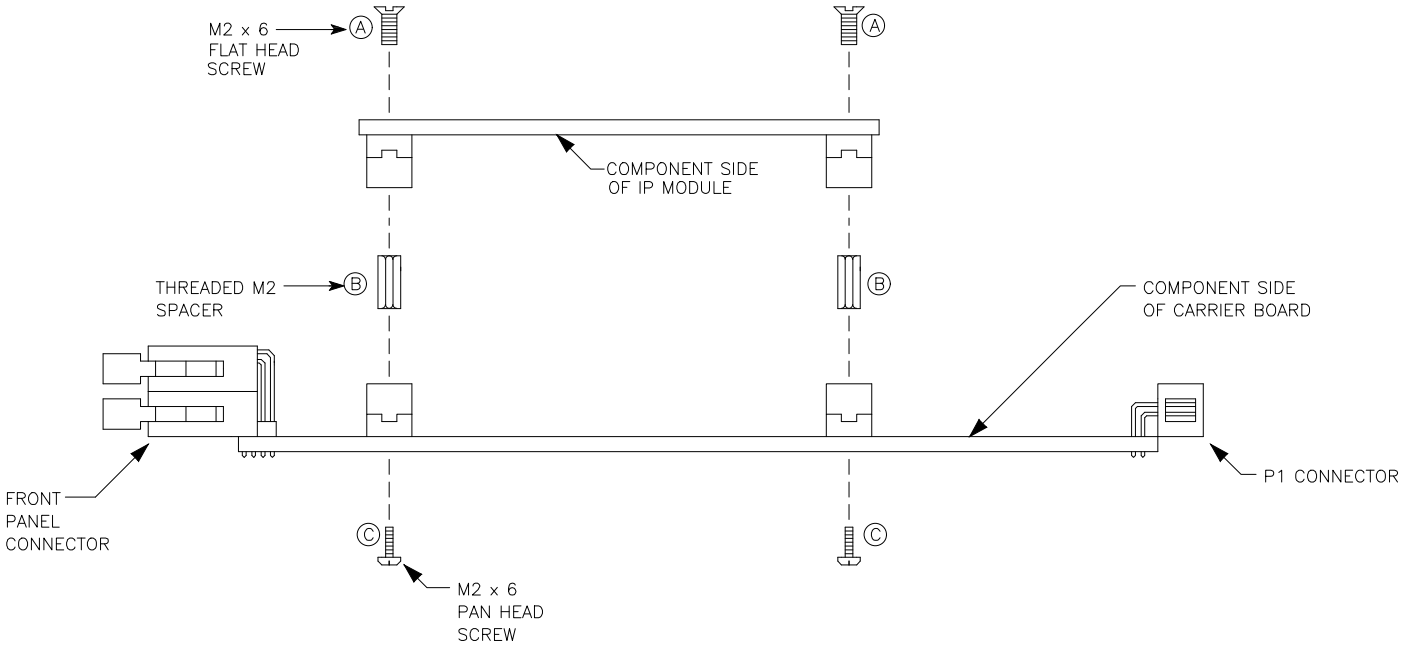
RESISTOR IDENTIFICATION

TERMINATION		
SIP	VALUE	CHANNELS
R8	120 OHM	0, 1, 2, 3
R9	120 OHM	4, 5, 6, 7
R10	120 OHM	8, 9, 10, 11
R11	120 OHM	13, 14, 15, 19
R12	120 OHM	12, 16, 17, 18
R13	120 OHM	20, 21, 22, 23

NOTES CONCERNING RESISTOR PLACEMENT AND REMOVAL:

1. TERMINATION RESISTORS SHOULD ONLY BE USED AT THE TWO EXTREME ENDS OF THE BUS AND NOT AT EACH NODE. THE SIP TERMINATION RESISTORS OF THE IP409 ARE MOUNTED IN SOCKETS AND CAN BE REMOVED IF REQUIRED.

4501-703

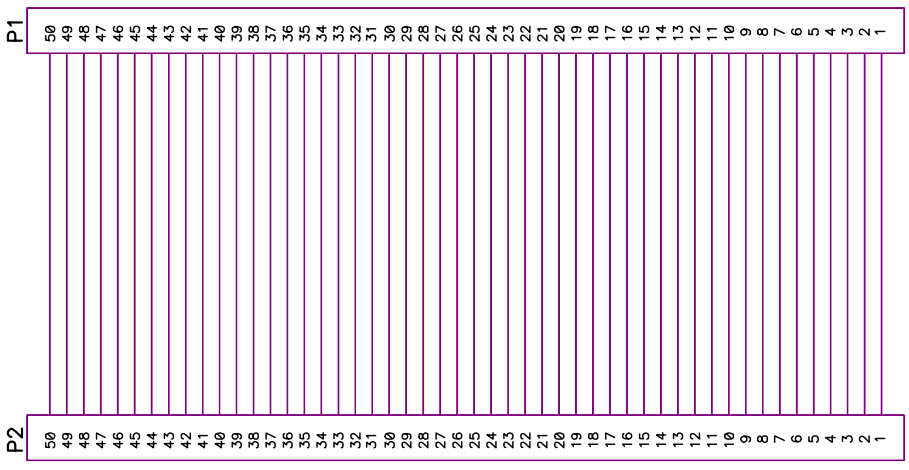


ASSEMBLY PROCEDURE:

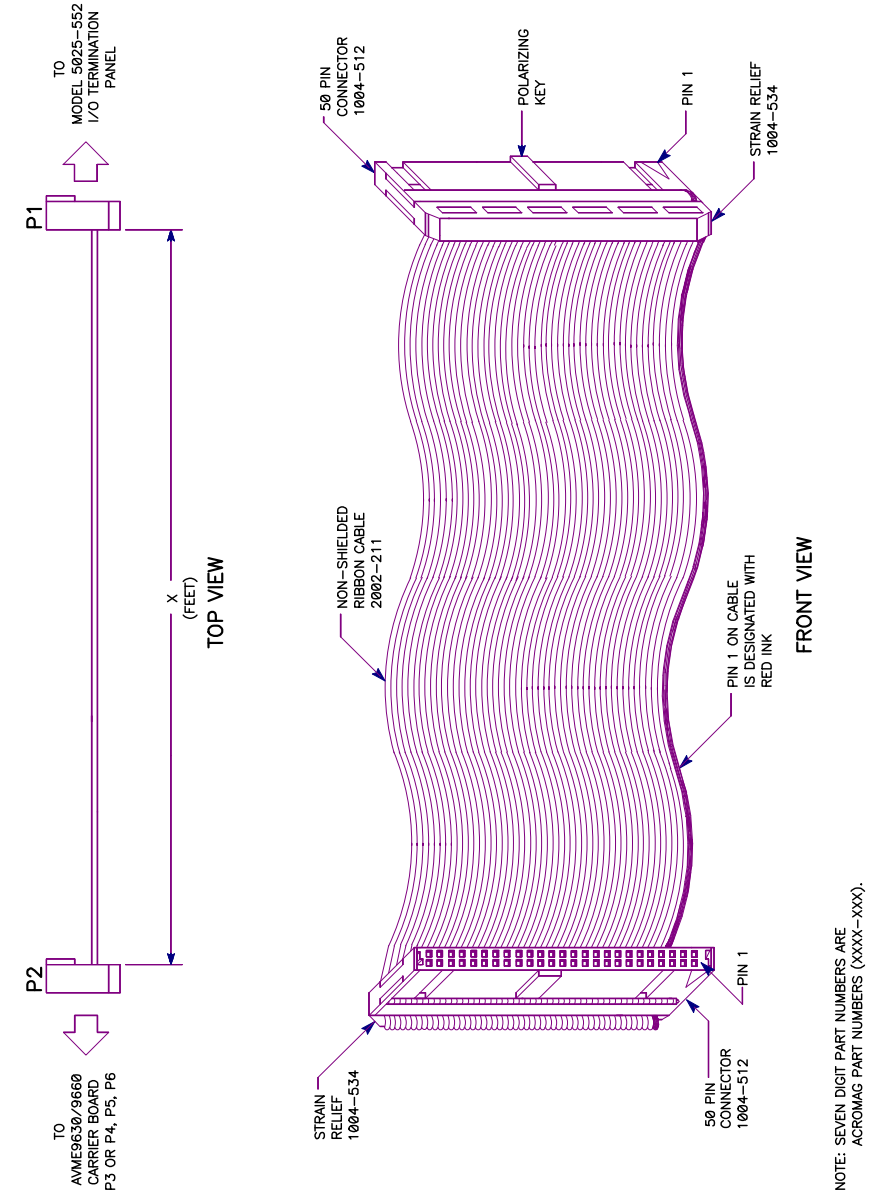
1. THREADED SPACERS ARE PROVIDED FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED. THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES). THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.

IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY

4501-434C

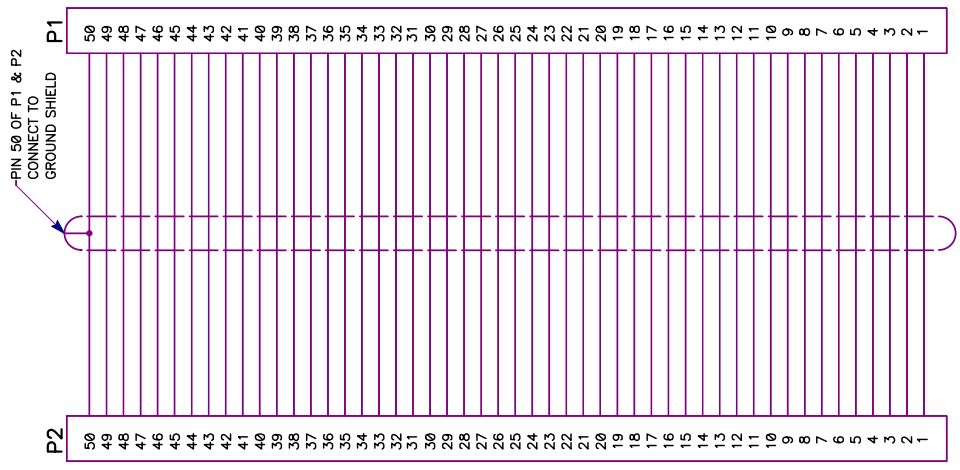


MODEL 5025-550-x SCHEMATIC

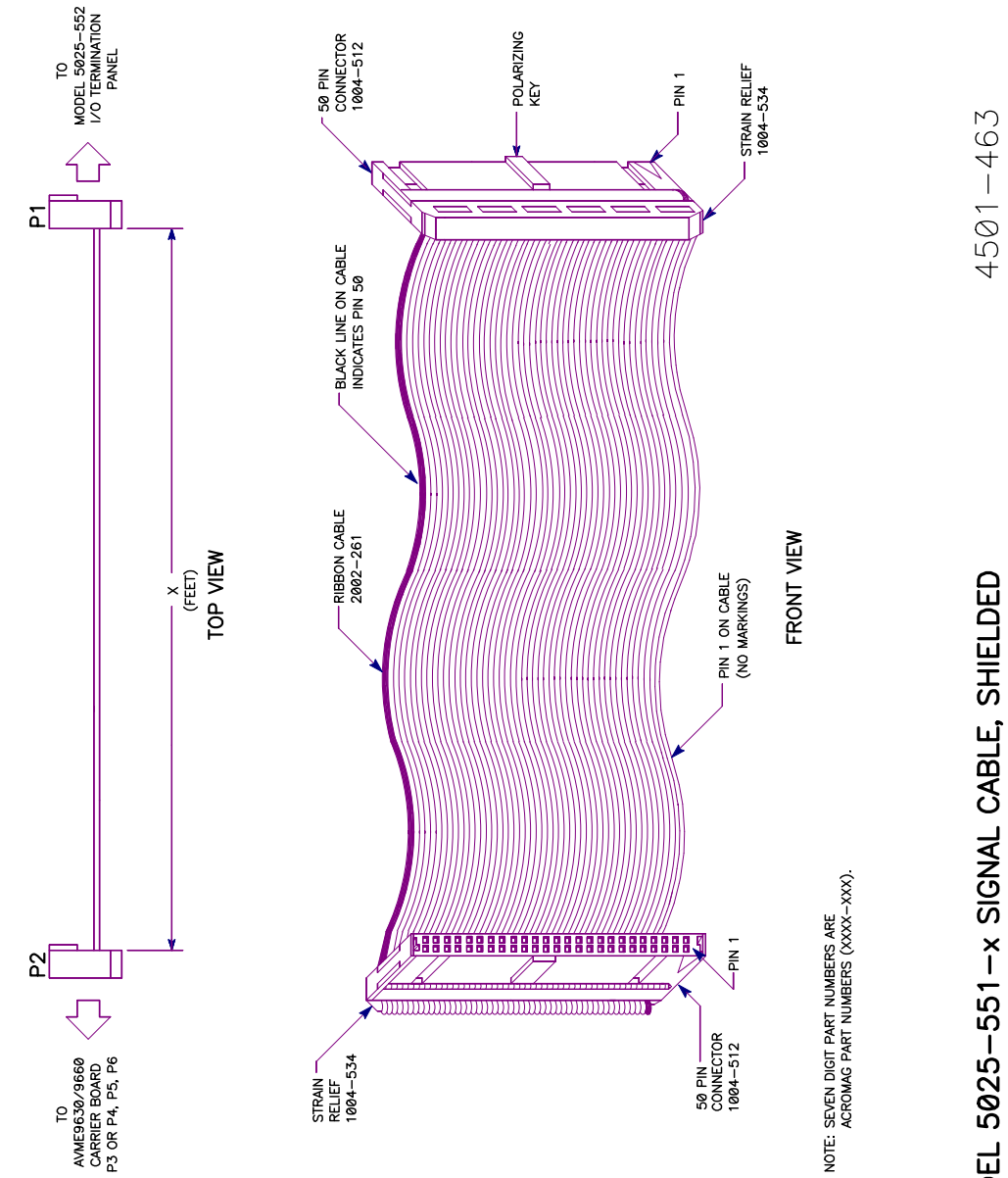


MODEL 5025-550-x SIGNAL CABLE, NON-SHIELDED

4501-462

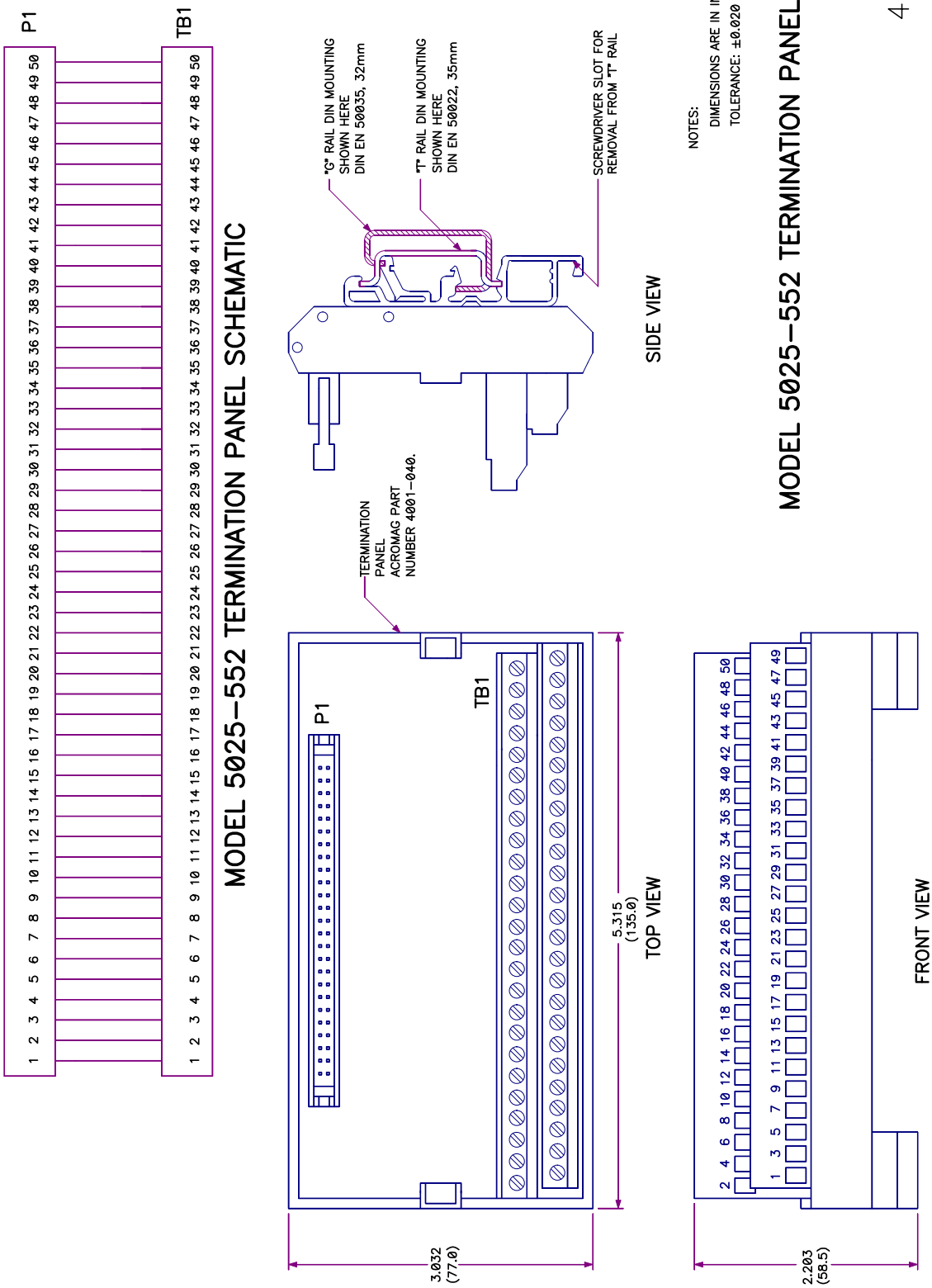


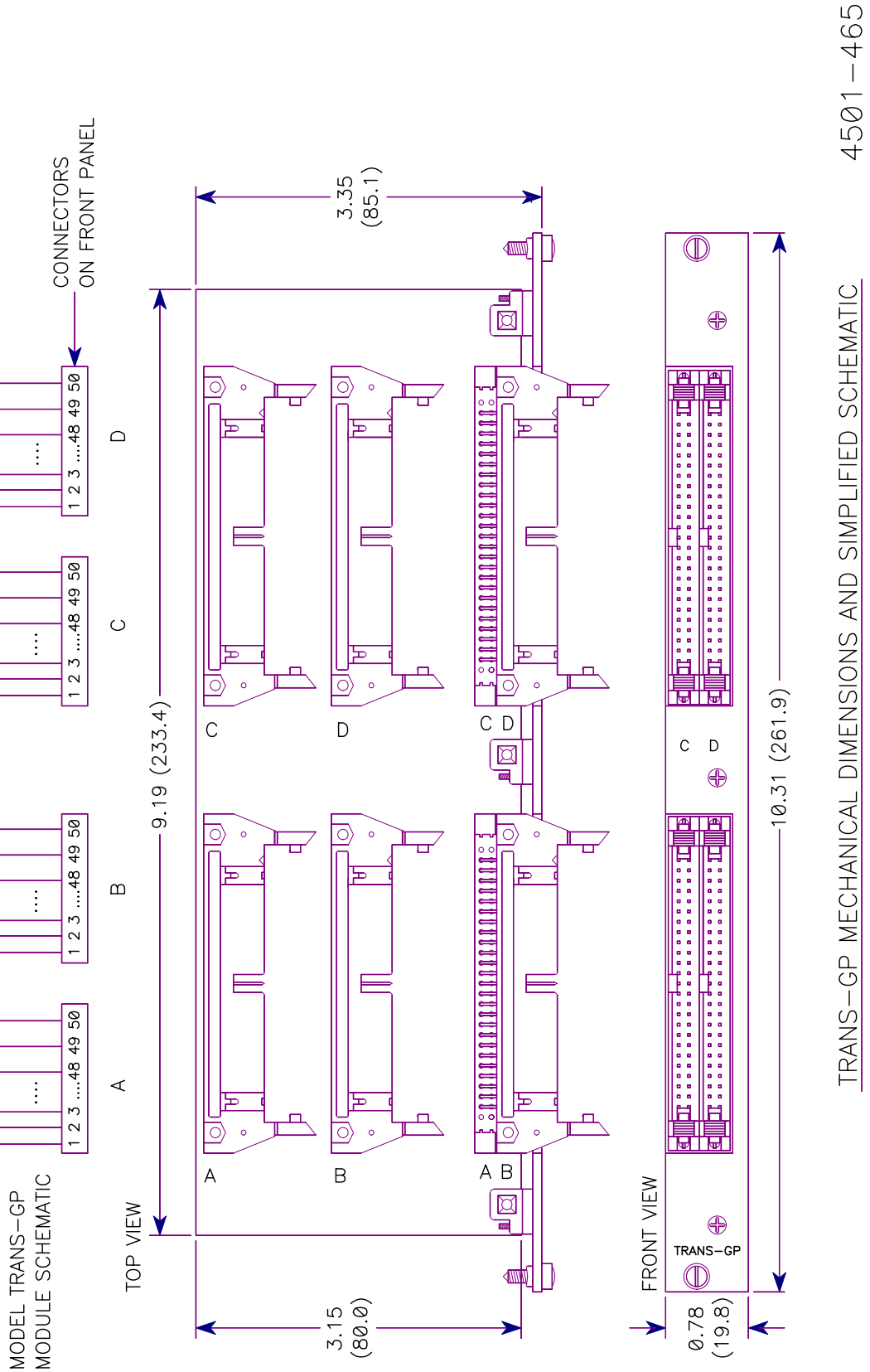
MODEL 5025-551-x SCHEMATIC



MODEL 5025-551-x SIGNAL CABLE, SHIELDED

4501-463


P1
TB1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
MODEL 5025-552 TERMINATION PANEL SCHEMATIC
"G" RAIL DIN MOUNTING SHOWN HERE DIN EN 50035, 32mm
"T" RAIL DIN MOUNTING SHOWN HERE DIN EN 50022, 35mm
SCREWDRIVER SLOT FOR REMOVAL FROM "T" RAIL
SIDE VIEW
NOTES:
DIMENSIONS ARE IN INCHES (MILLIMETERS).
TOLERANCE: ±0.020 (±0.5).
MODEL 5025-552 TERMINATION PANEL
4501-464
TERMINATION PANEL ACROMAG PART NUMBER 4001-040.
P1
TB1
5.315 (135.0)
TOP VIEW
3.032 (77.0)
2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48 50
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 41 43 45 47 49
FRONT VIEW
2.203 (58.5)


4501-465
TRANS-GP MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC
MODEL TRANS-GP
MODULE SCHEMATIC
CONNECTORS ON PC BOARD
CONNECTORS ON FRONT PANEL
A
B
C
D
1 2 3 ....48 49 50
TOP VIEW
9.19 (233.4)
3.35 (85.1)
3.15 (80.0)
FRONT VIEW
10.31 (261.9)
0.78 (19.8)
TRANS-GP
NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).