Series IP512 Industrial I/O Pack
Isolated Quad EIA-485 Communication Module

USER'S MANUAL

ACROMAG INCORPORATED
30765 South Wixom Road
P.O. BOX 437
Wixom, MI 48393-7037 U.S.A.
Tel: (248) 624-1541
Fax: (248) 624-9234

8500-549-D10B001

Table of Contents

IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP512 module provides four independently isolated EIA-485 serial communication ports for interfacing to the VMEbus or ISAbus, according to your carrier board. This module implements half-duplex EIA-485 and includes four independently isolated differential data paths for Transmit/ Receive (Tx/Rx±). Four units may be mounted on a carrier board to provide up to 16 asynchronous serial ports per system slot. For non-isolated applications, refer to Acromag Model IP502 (the non-isolated companion to this model).

The transmit and receive paths of each channel of IP512-16 units include generous 16-byte FIFO buffers to minimize CPU interaction. Model IP512-64 units utilize 64-byte FIFO buffers. Character size, stop bits, parity, and baud rate are software configurable. Prioritized interrupt generation is also supported for transmit, receive, line-status, and data set conditions. The IP512 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its wide functionality, and is an ideal choice for a wide range of industrial communication interface applications that require a highly reliable, high-performance interface at a low cost.

KEY IP512 FEATURES

- **High Density** - Provides programmable control of four EIA-485 serial I/O ports. Four units mounted on a carrier board provide 16 serial channels in a single VMEbus or ISAbus (PC/AT) system slot.
- **High-Voltage Isolation -** This module provides four independently isolated serial ports protected for voltages up to 250VAC. This module will survive a 1000VAC dielectric strength test for 1 minute without breakdown.
- **Large FIFO Buffers -** Both the transmit and receive channels of each serial port provide generous 16-byte (Model IP512-16), or 64-byte (Model IP512-64) data buffering (plus 3 framing bits per byte). This gives the host CPU additional time to process other applications and reduces CPU interactions and interrupts.
- **Programmable Character Size -** Each serial port is software programmable for 5, 6, 7, or 8 bit character sizes.
- **Programmable Stop Bits -** Each serial port allows 1, 1-1/2, or 2 stop-bits to be added to, or deleted from, the serial data stream.
- **Programmable Parity Generation & Detection** - Even, Odd, or No Parity generation and detection is supported**.**
- **Line-Break Generation & Detection -** provision for sending and detecting the line break character is provided.
- **False Start Bit Detection -** Prevents the receiver from assembling false data characters due to low-going noise spikes on the RxD input line.

- **Programmable Baud Rate -** The internal baud rate generator allows the 8MHz clock to be divided by any divisor between 1 and $2^{(16-1)}$, providing support for any bit rate up to 512Kbps.
- **Port Power Jumpers Provided for Non-Isolated Mode** - For isolated operation, the port connections must include external isolated +5V power. However, the IP +5V power supply may be jumpered to the port(s) for convenient non-isolated operation.
- **Software Flow Controls** - IP512-64 models provide software flow controls for special character detection and interrupt generation.
- **Interrupt Support -** Individually controlled transmit, receive, line status, and data set interrupts may be generated. Unique interrupt vectors may be assigned to each port. Interrupt generation uses a priority shifting scheme based on the last interrupt serviced, preventing the continuous interrupts of one port from freezing out the interrupts of another port.
- **Socketed Termination and Bias Resistors** - The network termination and bias resistors are installed in sockets on the board and may be easily inserted or removed where required.
- **Internal Diagnostic Capabilities** - Loopback controls for communication link fault isolation are included. Break, parity, overrun, and framing error simulation are also possible.
- **Industry Standard 16550 Family UART w/16C450 Mode** - The UART of this device is a member of the industry standard 16550 family of UART's and remains software compatible. Additionally, this device can operate in a 16C450 UART family software compatible mode. The transmit and receive channels are double-buffered in this mode. Hold and shift registers eliminate the need for precise synchronization between the host CPU and the serial data.

INDUSTRIAL I/O PACK INTERFACE FEATURES

- **High density -** Single-size, industry standard, IP module footprint. Four units mounted on a carrier board provide up to 16 serial ports in a single system slot. Both VMEbus and ISAbus (PC/AT) carriers are supported.
- **Local ID** - Each IP module has its own 8-bit ID PROM which is accessed via data transfers in the "ID Read" space.
- **8-bit I/O** - Port register Read/Write is performed through 8-bit data transfer cycles in the IP module I/O space.
- **High Speed** - Access times for all data transfer cycles are described in terms of "wait" states - 2 wait states are required for reading and writing channel data and interrupt select cycles. One wait state is required for reading the ID PROM (see the Specifications section for detailed information).

SIGNAL INTERFACE PRODUCTS

(See Appendix for more information on compatible products)

This IP module will mate directly to any industry standard IP carrier board (including Acromag AVME9630/9660 3U/6U non-intelligent VMEbus carrier boards). Additionally, ISAbus (PC/AT) carrier boards are supported (see Acromag Model APC8600). A wide range of other Acromag IP modules are also available to serve your signal conditioning and interface needs.

Note: Since all connections to field signals are made through the carrier board which passes them to the individual IP modules, you should consult the documentation of your carrier board to ensure compatibility with the following interface products.

Cables:

Model 5025-551-X (Shielded Cable), or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9630/9660, or other compatible carrier boards, to Model 5025-552 termination panels. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications. The "-X" suffix of the model is used to specify the required length in feet.

Model 5029-943 IP500 Serial Communication Cable: A 5 foot long, flat 50-pin cable with a female connector on one end (for connection to AVME9630/9660 or other compatible carrier boards) and four DE-9P connectors (serial ports) on the other end. Also used for interface with Acromag Model IP501/511 (RS-422) & IP502/512 (RS-485) serial communication modules.

Model 5029-900 APC8600 High-Density Cable: A 36-inch long interface cable that mates the high-density (25mil pitch) 50-pin I/O connectors of the APC8600 PCbus carrier board, to the high-density connectors on the APC8600 Termination Panel (described below).

Termination Panels:

Model 5025-552: A DIN-rail mountable panel that provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9630/9660, or other compatible carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

Model 5029-910 APC8600 High-Density-to-Screw-Terminal Termination Panel: This panel converts the high-density ribbon-cable connectors coming from the APC8600 carrier board (Acromag cable Model 5029-900) to screw terminals, for direct-wired interfaces.

Transition Module:

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from a VMEbus card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. It connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within the card cage, via flat 50-pin ribbon cable (cable Model 5025-550 or 5025-551).

INDUSTRIAL I/O PACK SOFTWARE LIBRARY

Acromag provides an Industrial I/O Pack Software Library diskette (Model IPSW-LIB-M03, MSDOS format) to simplify communication with the board. Example software functions are provided for both ISAbus (PC/AT) and VMEbus applications. All functions are written in the "C" programming language and can be linked to your application. Software functions are shared with Acromag Model IP511. For more details, refer to the "README.TXT" file in the root directory on the diskette and the "INFO511.TXT" file in the appropriate "IP511" subdirectory off of "\VMEIP" or "\PCIP", according to your carrier.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Remove power from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-434 and your IP module documentation for configuration and assembly instructions. Model IP512 communication boards normally have no hardware jumpers or switches to configure. However, there are power jumpers provided to optionally power each port from the IP supply for non-isolated operation. Likewise, network termination and bias resistors must be included on the network and installed where appropriate (see Drawings 4501-586 & 4501-587).

These resistor SIPS are installed in sockets on the board and can be easily removed where required (see below and refer to Drawing 4501-586 & 4501-587 for instructions).

Network Termination & Bias Resistor Placement

You need to consider your network application carefully, and remove or install network bias and termination resistors where appropriate. The IP512 comes with network termination (120Ω) resistor SIP's installed in sockets on the board at the receiver inputs (RxD±). Termination resistors should only be installed at the ends of a network and are usually placed at the far-most receiving end, and near the driving end. If the network transmitters are always enabled, then you should remove the termination resistors from the transmitter side. They are already installed in sockets between the transceiver data lines of the IP512, but may be removed if already present on the network, or if connecting to the network via a short stub off the main trunk.

Transceiver data lines (TxRxD±) may require that network bias resistors (560Ω) be installed, if not already included on your network. A network channel will require only one set of bias resistors--usually positioned near the driving end and only where the driving end transmitter may be disabled. The bias arrangement is comprised of a 560Ω pullup from the positive lead to +5V and a 560Ω pulldown from the negative lead to common. The bias resistors keep the transmit line from floating and held in the idle state when the transmitter is disabled. These resistors are already installed in sockets on the board for the IP512, but should be removed if already present on the network.

Failure to include bias and termination resistors where required will hinder the performance. Likewise, failure to remove redundant termination and bias resistors where required will significantly increase current draw, and in some cases, may affect performance. Refer to Drawing 4501-586 & 4501-587 for instructions.

Power Jumper Configuration

For isolated operation, each port must be supplied with an external isolated +5V power source (see Table 2.1) at the field side. When this is not convenient, each port's power and common may be jumpered to the +5V logic supply and common for non-isolated operation. The board is shipped with these jumpers (shorting bucks) installed and they must be removed for isolated operation (see Drawing 4501-587 for location). Because the ports are also isolated from each other, separate jumpers are provided for the +5V and common of each port. Be sure to install or remove these jumpers as required for your application. Refer to Acromag part 1004-799 when ordering replacement jumpers.

CONNECTORS

IP Field I/O Connector (P2)

P2 provides the field I/O interface connections for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly. P2 pin assignments are unique to each IP model (see Table 2.1) and normally correspond to the pin numbers of the field I/O interface connector on the carrier board (you should verify this for your carrier board).

Table 2.1: IP512 Field I/O Pin Connections (P2)

Pin Description	Number	Pin Description	Number
COMMON A	1	COMMON C	26
+5V INPUT A	2	+5V INPUT C	27
TXRXA+	3	TXRXC+	28
+5V INPUT A	4	+5V INPUT C	29
TXRXA-	5	TXRXC-	30
+5V INPUT A	6	+5V INPUT C	31
TXRXA-	7	TXRXC-	32
+5V INPUT A	8	+5V INPUT C	33
TXRXA+	9	TXRXC+	34
COMMON B	10	COMMON D	35
+5V INPUT B	11	+5V INPUT D	36
TXRXB+	12	TXRXD+	37
+5V INPUT B	13	+5V INPUT D	38
TXRXB-	14	TXRXD-	39
+5V INPUT B	15	+5V INPUT D	40
TXRXB-	16	TXRXD-	41
+5V INPUT B	17	+5V INPUT D	42
TXRXB+	18	TXRXD+	43
Not Used	19	Not Used	44
Not Used	20	Not Used	45
Not Used	21	Not Used	46
Not Used	22	Not Used	47
Not Used	23	Not Used	48
Not Used	24	Not Used	49
Not Used	25	Not Used	50

An Asterisk (*) is used to indicate an active-low signal.

From Table 2.1, note that the pin-wire assignments are arranged such that IDC D-SUB ribbon cable connectors can be conveniently attached to provide serial port A (pins 1-9), serial port B (pins 10-18), serial port C (pins 26-34), & serial port D (pins 35-43) connectivity. Plus (+) and minus (-) following the signal name indicates differential signal polarity. In Table 2.1, a suffix of “A”, “B”, “C”, or “D” is appended to each pin label to denote its port association. Note that two port pins are dedicated to each data line of each port. Likewise, four +5V supply lines are also provided per port. A brief description of each of the serial port signals at P2 is included below. A complete functional description of the P2 pin functions is included in Section 4.0 (Theory Of Operation). Be careful not to confuse the A-D port designations of the IP module with the IP carrier board A-D slot designations.

P2 Pin Signal Descriptions For Model IP512

SIGNAL ±	DESCRIPTION
TXRXA+ TXRXB+ TXRXC+ TXRXD+	Transmit Data Line Output and Receive Data Line Input Positive (two pin connections per port). To the communication network master, this line is used as the positive transmit data line. To the communication network slaves, this line is the positive receive data line. Because the line is used for both transit and receive, only half-duplex communication is possible. During Loopback Mode, the TxD output of the UART is internally connected to the RxD input of the UART and disconnected from this data path.
TXRXA- TXRXB- TXRXC- TXRXD-	Transmit Data Line Output and Receive Data Line Input Negative (two pin connections per port). To the communication network master, this line is the negative transmit data line. To the communication network slaves, this line is the negative receive data line. Because the line is used for both transmit and receive, only half-duplex communication is possible. During Loopback Mode, the TxD output of the UART is internally connected to the RxD input of the UART and disconnected from this data path.
+5V Input A +5V Input B +5V Input C +5V Input D	Isolated +5V Port Power Input (four pin connections per port). For isolated operation, an external isolated power supply must be connected here to power the port. Use independent supplies for each port to maintain port-to-port isolation. If non-isolated operation is acceptable, then the port may be powered from the +5V logic supply of the carrier by programming the port power and ground jumpers accordingly (see Drawing 4501-587).
Common A Common B Common C Common D	Isolated Signal Common and +5V return. For isolated operation, the external isolated power supply common must be connected here to complete power to the port. Use independent supplies for each port to maintain port-to-port isolation. If non-isolated operation is acceptable, then the port may be powered from the logic common of the carrier by programming the port power and ground jumpers accordingly (see Drawing 4501-587).

None of the input handshake lines of the UART are used by the IP512 and their corresponding UART pins are tied high to deassert them. This includes, CTS (Clear-to-Send), RI (Ring Indicator), DSR (Data Set Ready), and DCD (Data Carrier Detect). The DTR (Data Terminal Ready) signal line is not connected. However, the RTS (Request-to-Send) signal path is instead used internally to enable the port transceiver for transmitting data. That is, the Modem Control Register is used to assert the RTS signal (to transmit) and deassert RTS (to receive).

Noise and Grounding Considerations

The serial ports of this module are isolated from the IP module’s digital circuitry and from each other when external isolated +5V power is provided to the port. If separate isolated supplies are used, then the ports are also isolated from each other. Otherwise, if the ports share an isolated supply, they are isolated from the carrier, but not isolated from each other. Optionally, the IP modules own +5V supply and common may be jumpered to the port for non-isolated operation (in this mode, the ports share a common signal ground and +5V connection with the carrier).

If isolated port power is not provided to the port connector and the power jumpers are connecting the IP +5V and common to power the port, then the signal ground connection at the communication ports are common to each other and the IP interface ground, which is typically common to safety (chassis) ground when mounted on a carrier board and inserted in a backplane. As such, be careful not to attach signal ground to safety ground in this mode via any device connected to these ports, or a ground loop will be produced and this may adversely affect operation.

The communication cabling of the P2 interface carries digital data at a high transfer rate. For best performance, increased signal integrity, and safety reasons, you should isolate these connections away from power and other wiring to avoid noise-coupling and crosstalk interference. EIA-485 communication distances are generally limited to less than 4000 feet. Always keep interface cabling and ground wiring as short as possible for best performance. Please refer to Drawing 4501-585 for example connections and recommended grounding practices.

Note that rapidly changing isolation-mode voltages (voltage across the isolation barrier) can cause data errors by causing the receiver output to change states. As the rate of change of isolation mode voltage increases, an increase in data errors will occur. Approximately half of the IP512 modules will experience data errors with isolation mode voltage transients of 1.6KV/us. Some errors may be encountered with isolation-mode transients down to 500V/us. To help put this into perspective, a 1000Vrms, 60Hz, isolation mode voltage has a rate of change of only 0.5V/us and would never be a problem. But if you should experience data errors while operating in isolated mode, then some thought should be given to preventing the port power supplies from floating by referencing them to earth ground. Additional consideration may be given to filtering the port supply lines. In any case, after a data error is encountered, a channel will recover and subsequent changes in input data will produce correct output data.

IP Logic Interface Connector (P1)

P1 of the IP module provides the logic interface to the mating connector on the carrier board. This connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly. The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.2).

Table 2.2: Standard Logic Interface Connections (P1)

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSEL*	29
D01	5	***DMAReq0****	30
D02	6	MEMSEL*	31
D03	7	***DMAReq1****	32
D04	8	IntSel*	33
D05	9	***DMAck0****	34
D06	10	IOSEL*	35
D07	11	***RESERVED***	36
D08	12	A1	37
D09	13	***DMAEnd****	38
D10	14	A2	39
D11	15	***ERROR****	40
D12	16	A3	41
D13	17	INTReq0*	42
D14	18	A4	43
D15	19	***INTReq1****	44
BS0*	20	A5	45
BS1*	21	***STROBE****	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	***RESERVED***	49
GND	25	GND	50

An Asterisk (*) is used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by this IP Model.

3.0 PROGRAMMING INFORMATION

ADDRESS MAPS

This board is addressable in the Industrial Pack I/O space to control the interface configuration, data transfer, and steering logic of four EIA-485 serial ports. As such, three types of information are stored in the I/O space: control, status, and data. These registers are listed below along with their mnemonics used in this manual.

SERIAL DATA REGISTERS (Per Serial Port):	
RBR	Receive Buffer Register
THR	Transmitter Holding Register
SERIAL STATUS REGISTERS (Per Serial Port):	
LSR	Line Status Register
MSR	Modem Status Register
SERIAL CONTROL REGISTERS (Per Serial Port):	
LCR	Line Control Register
FCR	FIFO Control Register
MCR	Modem Control Register
DLL	Divisor Latch LSB
DLM	Divisor Latch MSB
IER	Interrupt Enable Register
SCR	Scratchpad/Interrupt Vector Register
EFR	Enhanced Feature Register (IP512-64 Models)
XON-1	XON-1 Word (IP512-64 Models)
XON-2	XON-2 Word (IP512-64 Models)
XOFF-1	XOFF-1 Word (IP512-64 Models)
XOFF-2	XOFF-2 Word (IP512-64 Models)

Shaded register entries apply to Model IP512-64 only and are accessible after writing “BF” to the Line Control Register (LCR).

The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1..A6, but the IP512 uses only a portion of this space. The I/O space address map for the IP512 is shown in Table 3.1. Note the base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space. All accesses are performed on an 8-bit byte basis (D0..D7).

This manual is presented using the "Big Endian" byte ordering format. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses. Thus, byte accesses are done on odd address locations. The Intel x86 family of microprocessors use the opposite convention, or "Little Endian" byte ordering. Little Endian uses even-byte addresses to store the low-order byte. As such, use of this module on an ISAbus (PC/AT) carrier board will require the use of the even address locations to access the 8-bit data, while a VMEbus carrier will require the use of odd address locations.

Note that some functions share the same register address. For these items, the address lines are used in combination with the divisor latch access bit (bit 7 of the Line Control Register) and/or the read and write signals to determine the function required. The enhanced feature registers of the Model IP512-64 are shaded in the table below and only accessible after writing "BF" to the Line Control Register (LCR).

Table 3.1: IP512 I/O Space Address (Hex) Memory Map

Base Addr+	MSB D15 D08	LSB D07 D00	LCR Bit7	Base Addr+
Serial Port A Registers:				
00	Not Driven[1]	READ - RBR Port A Receiver Buffer Register	0	**01**
00	Not Driven[1]	WRITE - THR Port A Transmitter Holding Register	0	**01**
00	Not Driven[1]	R/W - DLL Port A Divisor Latch LSB	1	**01**
02	Not Driven[1]	R/W - IER Port A Interrupt Enable Register	0	**03**
02	Not Driven[1]	R/W - DLM Port A Divisor Latch MSB	1	**03**
04	Not Driven[1]	R/W - EFR[4] Port A Enhanced Function Register ("-64" models only)	1	**05**
08	Not Driven[1]	R/W- XON-1 Word Port A SW Flow Control[4]	1	**09**
0A	Not Driven[1]	R/W- XON-2 Word Port A SW Flow Control[4]	1	**0B**
0C	Not Driven[1]	R/W- XOFF-1 Word Port A SW Flow Control[4]	1	**0D**
0E	Not Driven[1]	R/W- XOFF-2 Word Port A SW Flow Control[4]	1	**0F**

Shaded register entries apply to Model IP512-64 only and are accessible after writing "BF" to the Line Control Register (LCR).

Table 3.1: IP512 I/O Space Address (Hex) Memory Map

Base Addr+	MSB D15 D08	LSB D07 D00	LCR Bit7	Base Addr+
Serial Port A Registers...continued:				
04	Not Driven[1]	READ - IIR Port A Interrupt Identification Register		**05**
04	Not Driven[1]	WRITE - FCR Port A FIFO Control Register		**05**
06	Not Driven[1]	R/W - LCR Port A Line Control Register		**07**
08	Not Driven[1]	R/W - MCR Port A Modem Control Register		**09**
0A	Not Driven[1]	R/W - LSR Port A Line Status Register		**0B**
0C	Not Driven[1]	R/W - MSR Port A Modem Status Register		**0D**
0E	Not Driven[1]	R/W - SCR Port A Scratch Pad/Interrupt Vector Register		**0F**
Serial Port B Registers:				
Base Addr+	**MSB D15 D08**	**LSB D07 D00**	**LCR Bit7**	**Base Addr+**
10	Not Driven[1]	READ - RBR Port B Receiver Buffer Register	0	**11**
10	Not Driven[1]	WRITE - THR Port B Transmitter Holding Register	0	**11**
10	Not Driven[1]	R/W - DLL Port B Divisor Latch LSB	1	**11**
12	Not Driven[1]	R/W - IER Port B Interrupt Enable Register	0	**13**
12	Not Driven[1]	R/W - DLM Port B Divisor Latch MSB	1	**13**
14	Not Driven[1]	R/W - EFR[4] Port B Enhanced Function Register ("-64" models only)	1	**15**
18	Not Driven[1]	R/W- XON-1 Word Port B SW Flow Control[4]	1	**19**
1A	Not Driven[1]	R/W- XON-2 Word Port B SW Flow Control[4]	1	**1B**
1C	Not Driven[1]	R/W- XOFF-1 Word Port B SW Flow Control[4]	1	**1D**
1E	Not Driven[1]	R/W- XOFF-2 Word Port B SW Flow Control[4]	1	**1F**

Shaded register entries apply to Model IP512-64 only and are accessible after writing "BF" to the Line Control Register (LCR).

Table 3.1: IP512 I/O Space Address (Hex) Memory Map

Base Addr+	MSB D15 D08	LSB D07 D00	LCR Bit7	Base Addr+
Serial Port B Registers...continued:				
14	Not Driven[1]	READ - IIR Port B Interrupt Identification Register		**15**
14	Not Driven[1]	WRITE - FCR Port B FIFO Control Register		**15**
16	Not Driven[1]	R/W - LCR Port B Line Control Register		**17**
18	Not Driven[1]	R/W - MCR Port B Modem Control Register		**19**
1A	Not Driven[1]	R/W - LSR Port B Line Status Register		**1B**
1C	Not Driven[1]	R/W - MSR Port B Modem Status Register		**1D**
1E	Not Driven[1]	R/W - SCR Port B Scratch Pad/Interrupt Vector Register		**1F**
Serial Port C Registers:				
20	Not Driven[1]	READ - RBR Port C Receiver Buffer Register	0	**21**
20	Not Driven[1]	WRITE - THR Port C Transmitter Holding Register	0	**21**
20	Not Driven[1]	R/W - DLL Port C Divisor Latch LSB	1	**21**
22	Not Driven[1]	R/W - IER Port C Interrupt Enable Register	0	**23**
22	Not Driven[1]	R/W - DLM Port C Divisor Latch MSB	1	**23**
24	Not Driven[1]	R/W - EFR[4] Port C Enhanced Function Register ("-64" models only)	1	**25**
28	Not Driven[1]	R/W- XON-1 Word Port C SW Flow Control[4]	1	**29**
2A	Not Driven[1]	R/W- XON-2 Word Port C SW Flow Control[4]	1	**2B**
2C	Not Driven[1]	R/W- XOFF-1 Word Port C SW Flow Control[4]	1	**2D**
2E	Not Driven[1]	R/W- XOFF-2 Word Port C SW Flow Control[4]	1	**2F**

Shaded register entries apply to Model IP512-64 only and are accessible after writing "BF" to the Line Control Register (LCR).

Table 3.1: IP512 I/O Space Address (Hex) Memory Map

Base Addr+	MSB D15 D08	LSB D07 D00	LCR Bit7	Base Addr+
Serial Port C Registers...continued:				
24	Not Driven[1]	READ - IIR Port C Interrupt Identification Register		**25**
24	Not Driven[1]	WRITE - FCR Port C FIFO Control Register		**25**
26	Not Driven[1]	R/W - LCR Port C Line Control Register		**27**
28	Not Driven[1]	R/W - MCR Port C Modem Control Register		**29**
2A	Not Driven[1]	R/W - LSR Port C Line Status Register		**2B**
2C	Not Driven[1]	R/W - MSR Port C Modem Status Register		**2D**
2E	Not Driven[1]	R/W - SCR Port C Scratch Pad/ Interrupt Vector Register		**2F**
Serial Port D Registers:				
30	Not Driven[1]	READ - RBR Port D Receiver Buffer Register	0	**31**
30	Not Driven[1]	WRITE - THR Port D Transmitter Holding Register	0	**31**
30	Not Driven[1]	R/W - DLL Port D Divisor Latch LSB	1	**31**
32	Not Driven[1]	R/W - IER Port D Interrupt Enable Register	0	**33**
32	Not Driven[1]	R/W - DLM Port D Divisor Latch MSB	1	**33**
34	Not Driven[1]	R/W - EFR[4] Port D Enhanced Function Register ("-64" models only)	1	**35**
38	Not Driven[1]	R/W- XON-1 Word Port D SW Flow Control[4]	1	**39**
3A	Not Driven[1]	R/W- XON-2 Word Port D SW Flow Control[4]	1	**3B**
3C	Not Driven[1]	R/W- XOFF-1 Word Port D SW Flow Control[4]	1	**3D**
3E	Not Driven[1]	R/W- XOFF-2 Word Port D SW Flow Control[4]	1	**3F**

Shaded register entries apply to Model IP512-64 only and are accessible after writing "BF" to the Line Control Register (LCR).

Table 3.1: IP512 I/O Space Address (Hex) Memory Map

Base Addr+	MSB D15 D08	LSB D07 D00	Base Addr+
Serial Port D Registers...continued:			
34	Not Driven[1]	READ - IIR Port D Interrupt Identification Register	**35**
34	Not Driven[1]	WRITE - FCR Port D FIFO Control Register	**35**
36	Not Driven[1]	R/W - LCR Port D Line Control Register	**37**
38	Not Driven[1]	R/W - MCR Port D Modem Control Register	**39**
3A	Not Driven[1]	R/W - LSR Port D Line Status Register	**3B**
3C	Not Driven[1]	R/W - MSR Port D Modem Status Register	**3D**
3E	Not Driven[1]	R/W - SCR Port D Scratch Pad/ Interrupt Vector Register	**3F**
40 ↓ 7E	Registers Repeated[2]		**41 ↓ 7F**

Notes (Table 3.1):

1. The upper 8 bits of these registers are not driven. Pullups on the carrier board data bus will cause these bits to always read high (1's).
2. Due to simplified address decoding, registers are repeated where the uppermost address bit is set (A6=1).
3. All Reads and writes are 2 wait states (except ID PROM reads which are 1 wait state).
4. Shaded registers apply only to the enhanced functionality of the Model IP512-64 and are accessible after writing "BF" to the Line Control Register (LCR).

This board operates in two different modes. In one mode, this device remains software compatible with the industry standard 16C450 family of UARTS and provides double-buffering of data registers. In the FIFO Mode (enabled via bit 0 of the FCR register), data registers are FIFO-buffered so that read and write operations can be performed while the UART is performing serial-to-parallel and parallel-to-serial conversions. Two FIFO modes are possible: FIFO Interrupt Mode and FIFO Polled Mode. Some registers operate differently between the available modes and this is noted in the following paragraphs.

RBR - Receiver Buffer Register, Ports A-D (READ Only)

The Receiver Buffer Register (RBR) is a serial port input data register that receives the input data from the receiver shift register and holds from 5 to 8 bits of data, as specified by the character size programmed in the Line Control Register (LCR bits 0 & 1). If less than 8 bits are transmitted, then data is right-justified to the LSB. If parity is used, then LCR bit 3 (parity enable) and LCR bit 4 (type of parity) are required. Status for the receiver is provided via the Line-Status Register (LSR). When a full character is received (including parity and stop bits), the data-received indication bit (bit 0) of the LSR is set to 1. The host CPU then reads the Receiver Buffer Register, which resets LSR bit 0 low.

If the character is not read prior to a new character transfer between the receiver shift register and the receiver buffer register, the overrun-error status indication is set in LSR bit 1. If there is a parity error, the error is indicated in LSR bit 2. If a stop bit is not detected, a framing error indication is set in bit 3 of the LSR.

Serial asynchronous data is input to the receiver shift register via the receive data line (RxD). From the idle state, this line is monitored for a high-to-low transition (start bit). When the start bit is detected, a counter is reset and counts the 16x clock to 7-1/2 (which is the center of the start bit). The start bit is judged valid if RxD is still low at this point. This is known as false start-bit detection. By verifying the start bit in this manner, it helps to prevent the receiver from assembling an invalid data character due to a low-going noise spike on RxD. If the data on RxD is a symmetrical square wave, the center of the data cells will occur within ±3.125% of the actual center (providing an error margin of 46.875%). Thus, the start bit can begin as much as one 16x clock cycle prior to being detected.

Note that the tranceiver is enabled to receive data upon power-up or after a reset (RTS deasserted). Asserting the RTS signal via the Modem Control Register (MCR bit 1=1) will enable the port transceiver for transmitting data. Due to the isolation scheme employed, under some conditions the first bit received immediately after power-up may be initialized "high" and a data error may be detected if the first bit was expected to be low. However, subsequent bits will be received correctly.

THR - Transmitter Holding Register, Ports A-D (WRITE Only)

The Transmitter Holding Register (THR) is a serial port output data register that holds from 5 to 8 bits of data, as specified by the character size programmed in the Line Control Register. If less than 8 bits are transmitted, then data is entered right-justified to the LSB. This data is framed as required, then shifted to the transmit data line (TxD). In the idle state, TxD is held high. In Loopback Mode, this data is looped back into the Receiver Buffer Register.

For this model, note that the port transceiver is only enabled for transmission by asserting the RTS signal bit via the Modem Control Register (MCR bit 1 = 1). However, due to the isolation scheme employed, under some conditions the first bit transmitted immediately after power-up may be initialized "high" at the output of the isolation buffers and a data error may occur if the first bit was intended to be low. However, subsequent bits will be transmitted correctly.

DLL & DLM - Divisor Latch Registers, Ports A-D (R/W)

The Divisor Latch Registers form the divisor used by the internal baud-rate generator to divide the 8MHz system clock to produce an internal sampling clock suitable for synchronization to the desired baud rate. The output of the baud generator (RCLK) is sixteen times the baud rate. Two 8-bit divisor latch registers per port are used to store the divisors in 16-bit binary format. The DLL register stores the low-order byte of the divisor, DLM stores the high-order byte. These registers must be loaded during initialization. Note that bit 7 of the LCR register must first be set high to access the divisor latch registers (DLL & DLM) during a read/write operation.

Upon loading either latch, a 16-bit baud counter is immediately loaded (this prevents long counts on initial load). The clock may be divided by any divisor from 1 to $2^{(16-1)}$. The output frequency of the baud rate generator (RCLK) is 16x the data rate. The relationship between the output of the baud generator (RCLK), the baud rate, the divisor, and the 8MHz system clock can be summarized in the following equations:

DIVISOR = CLOCK FREQUENCY ÷ [BAUD RATE x 16];
RCLK = 16 x BAUD RATE;
= 16 x [CLOCK ÷ (16 x DIVISOR)] = CLOCK ÷ DIVISOR

The following table shows the correct divisor to use for generation of some standard baud rates (based on the 8MHz clock). Note that baud rates up to 512K may be configured.

Table 3.2: Baud Rate Divisors and Relative Error (8MHz Clk)

BAUD RATE DESIRED	DIVISOR (N) USED FOR 16x CLOCK		% ERROR DIFF BET DESIRED & ACTUAL
50	10000	2710H	0
75	6667	1A06H	0.005
110	4545	11C1H	0.010
134.5	3717	0E85H	0.013
150	3333	0D05H	0.010
300	1667	0683H	0.020
600	833	0341H	0.040
1200	417	01A1H	0.080
1800	277	0115H	0.080
2000	250	00FAH	0
2400	208	00D0H	0.160
3600	139	0086H	0.080
4800	104	0068H	0.160
7200	69	0045H	0.644
9600	52	0034H	0.160
19200	26	001AH	0.160
38400	13	000DH	0.160
56000	9	0009H	0.790
128000	4	0004H	2.344
256000	2	0002H	2.344
512000	1	0001H	2.400

With respect to this device, the baud rate may be considered equal to the number of bits transmitted per second (bps). The bit rate (bps), or baud rate, defines the bit time. This is the length of time a bit will be held on before the next bit is transmitted. A receiver and transmitter must be communicating at the same bit rate, or data will be garbled. A receiver is alerted to an incoming character by the start bit, which marks the beginning of the character. It then times the incoming signal, sampling each bit as near to the center of the bit time as possible.

To better understand the asynchronous timing used by this device, note that the receive data line (RxD) is monitored for a high-to-low transition (start bit). When the start bit is detected, a counter is reset and counts the 16x sampling clock to 7-1/2 (which is the center of the start bit). The receiver then counts from 0 to 15 to sample the next bit near its center, and so on, until a stop bit is detected, signaling the end of the data stream.

Use of a sampling rate 16x the baud rate reduces the synchronization error that builds up in estimating the center of each successive bit following the start bit. As such, if the data on RxD is a symmetrical square wave, the center of each successive data cell will occur within ±3.125% of the actual center (this is 50% ÷ 16, providing an error margin of 46.875%). Thus, the start bit can begin as much as one 16x clock cycle prior to being detected.

EFR - Enhanced Function Register, Ports A-D (R/W)
(Model IP512-64 Only)

The enhanced features of the Model IP512-64 can be enabled or disabled via this register. This register is only accessible after writing "BF" to the Line Control Register (LCR). This register is used to unlock access to programming the extended register functionality provided via IER bits 4-7, IIR bits 4-5, FCR bits 4-5, and MCR bits 5-7. It is also used to program software flow control. Note that bits 6 & 7 are used for hardware flow control, but the handshake lines RTS & CTS are not implemented on this model and bits 6 & 7 should be programmed to 0 (RTS is instead used to enable the port transceiver for transmitting data).

Enhanced Function Register (EFR)

EFR BIT	FUNCTION
0-3	Allows combinations of software flow control to be programmed (see table below).
4	Enhanced Functions Enable bit. 0 = disable enhanced functions controlled via IER bits 4-7, IIR bits 4-5, FCR bits 4-5, and MCR bits 5-7 (Note that after reset, these bits are set to "0" to maintain compatibility with the 16C550 standard functionality mode). 1 = Enable all enhanced features. Allows IER bits 4-7, IIR bits 4-5, FCR bits 4-5, and MCR bits 5-7 to be modified. Then after modification, EFR bit 4 can be set to "0" to latch the contents, and prevent existing software from overwriting the enhanced functionality provided by these bits.
5	0 = Normal; 1 = Enable Special Character Detect. If enabled, the UART will compare the received data with the XOFF-2 data. Upon a correct match, the received data will be transferred to the FIFO and IIR bit 4 will be set to indicate the detection of the special character.
6	Hardware RTS flow Control Enable (Not Supported) 0 = Normal (RTS flow control disabled); 1 = Enable RTS* pin to go high (deassert) when the receive FIFO has reached its programmed trigger level.
7	Hardware CTS flow Control Enable (Not Supported) 0 = Normal (CTS flow control disabled); 1 = Resume transmission when a low input signal is detected on the CTS* pin.

Different conditions can be set to detect XON/XOFF characters in the data stream, or start/stop transmission. The following table lists all the possible conditions:

Software Flow Control Via EFR Bits 3-0

Bit3	Bit2	Bit1	Bit0	Tx/Rx Software Flow Controls
0	**0**	**X**	**X**	No Transmit Flow Control
1	**0**	**X**	**X**	Transmit XON1, XOFF1
0	**1**	**X**	**X**	Transmit XON2, XOFF2
1	**1**	**X**	**X**	Transmit XON1, XON2: XOFF1, XOFF2
X	**X**	**0**	**0**	No Receive Flow Control
X	**X**	**1**	**0**	Receiver Compares XON1,XOFF1
X	**X**	**0**	**1**	Receiver Compares XON2,XOFF2
1	**0**	**1**	**1**	Transmit XON1, XOFF1. Receiver Compares XON1 or XON2, XOFF1 or XOFF2.
0	**1**	**1**	**1**	Transmit XON2, XOFF2. Receiver Compares XON1 or XON2, XOFF1 or XOFF2.
1	**1**	**1**	**1**	Transmit XON1 & XON2: XOFF1 & XOFF2. Receiver Compares XON1 & XON2: XOFF1 & XOFF2.
0	**0**	**1**	**1**	No Transmit Flow Control. Receiver Compares XON1 & XON2: XOFF1 and XOFF2.

EFR Bits 0-7 are set to 0 upon power-up or system reset.

XON/XOFF-1,2 Registers, Ports A-D (R/W)
(IP512-64 Models Only)

These registers hold the programmed XON and XOFF characters for software flow control. XON or XOFF characters may be 1 or 2 bytes long. The UART compares incoming data to these values and restarts (XON) or suspends (XOFF) data transmission when a match is detected. Note that access to these registers are granted only after writing "BF" to the Line Control Register (LCR). All XON/XOFF bits are set to 0 upon power-up or system reset. Refer to "Software Flow Control" later in this section for more information.

IER - Interrupt Enable Register, Ports A-D (R/W)

The Interrupt Enable Register is used to independently enable/ disable the four possible serial channel interrupt sources that drive the INTREQ0* line (Ports A-D share this line). Interrupts are disabled by resetting the corresponding IER bit low (0), and enabled by setting the IER bit high (1). Disabling the interrupt system (IER bits 0-3 low) also inhibits the Interrupt Identification Register (IIR) and the interrupt request line (INTREQ0*). All other functions operate in their normal manner, including the setting of the Line Status Register (LSR) and the Modem Status Register (MSR).

Interrupt Enable Register

IER BIT	INTERRUPT ACTION
0	0 = Disable the Received Data Available Interrupt 1 = Enable Received Data Available Interrupt and Time-out Interrupt (FIFO Mode)
1	0 = Disable Transmitter Holding Register Empty Interrupt. 1 = Enable Transmitter Holding Register Empty Interrupt

Interrupt Enable Register...continued

IER BIT	INTERRUPT ACTION
2	0 = Disable Receiver Line Status Interrupt. 1 = Enable Receiver Line Status Interrupt.
3	Modem Status Interrupt Enable (NO FUNCTION FOR MODEL IP512)
4-7	Not Used on IP512-16 Models - Set to Logic 0
MODELS IP512-64 ONLY	
4	0 = Disable Sleep Mode. 1 = Enable Sleep Mode - The UART will enter a "sleep" power-down mode and the clock/oscillator circuit is disabled. Any change of state on Rx, RI, CTS, DSR, and DCD will wake-up the UART (note that none of the handshake lines are implemented on this model). The UART will not lose the programmed bits when sleep mode is activated or deactivated. The UART will not enter sleep mode if any interrupt is pending.
5	0 = Disable the Received XOFF interrupt. 1 = Enable the Received XOFF interrupt. The UART issues an interrupt when XOFF characters are received and correctly matched against the pre-programmed XOFF-1,2 words.
6	NO FUNCTION FOR MODEL IP512 0 = Disable the RTS* interrupt 1 = Enable the generation of an RTS* interrupt when RTS* changes from a low to high state. The IP512 does not implement the RTS* handshake line and this bit should be programmed to 0.
7	NO FUNCTION FOR MODEL IP512 0 = Disable the CTS interrupt 1 = Enable the generation of the CTS interrupt when CTS changes from a low to high state. The IP512 does not implement the CTS* line and this bit should be programmed to 0.

Shaded Entries apply to Model IP512-64 only

Note that bit 3 will have no effect for IP512 boards since no signal paths are provided for any of the UART handshake lines (modem status lines). A power-up or system reset sets all IER bits to 0 (bits 0-3 forced low, bits 4-7 permanently low for IP512-16). Program access to the enhanced functionality provided via bits 4-7 is gained through setting EFR bit 4. Programmed values for bits 4-7 cannot be overwritten via existing software if EFR bit 4 is clear (these values are latched when EFR bit 4 is cleared).

IIR - Interrupt Identification Register, Ports A-D (READ Only)

The Interrupt Identification Register (IIR) is used to indicate that a prioritized interrupt is pending and the type of interrupt that is pending. This register will indicate the highest-priority interrupt type pending for the channel. Individual serial channels prioritize their interrupts into four levels (IP512-16 models), or six levels (IP512-64 models) as shown below. This helps minimize software overhead during data character transfers. Additionally, with respect to the four channels sharing interrupt request line 0 (IntReq0), interrupts are served according to a shifting priority scheme that is a function of the last interrupting port served.

PRIORITY/LEVEL	INTERRUPT
1	Receiver Line Status
2	Received Data Ready or Character Time-out
3	Transmitter Holding Register Empty
4	Modem Status (No Function for IP512)
5	Received XOFF/Special Character
6	CTS/RTS Change-of-State Detect

Note that a priority level 4 or 6 interrupt will never occur for this model since no handshake signal paths (modem status lines) are provided. The four lower order bits of this register are used to identify the interrupt pending as follows:

Interrupt Identification Register

BITS 3-0	INT PRTY	INT TYPE	INTERRUPT SOURCE	RESET CONTROL
0001	--	None	None	--
0110	1st	Receiver Line Status	OE, PE, FE, or BI (See LSR Bits 1-4)	LSR Read
0100	2nd	Received Data Available	Receiver Data Available or Trigger Level Reached	RBR Read till FIFO below trigger level
1100	2nd	Character Time-out Indication	No characters have been re-moved from or input to the Rx FIFO during last 4 character times and there is at least 1 character in it during this time	RBR Read
0010	3rd	THRE (LSR Bit 5)	THRE (LSR Bit 5)	IIR Read (if LSR bit 5 is the int. source) or a THR Write
0000	4th	Modem Status	CTS* asserted (NOT USED)	MSR Read

A modem status interrupt (4th priority) will never occur for this model since no handshake lines are provided. Bits 4 and 5 of this register are always set to 0 on IP512-16 units. Bits 6 and 7 are set to "1" when bit 0 of the FIFO Control Register is set to 1 (bits 6 & 7 are "0" in 16C450 mode). A power-up or system reset sets IIR bit 0 to 1, bits 1-7 to 0.

BITS 5	BITS 4	INT PRTY	INTERRUPT SOURCE
0	1	5	Received XOFF Signal/Special Character
1	0	6	CTS/RTS Change-of-State Detected (NO FUNCTION FOR IP512)

Bits 4 & 5 are set to 0 on IP512-16 units.

FCR - FIFO Control Register, Ports A-D (WRITE Only)

This write-only register is used to enable and clear the FIFO buffers, set the trigger level of the Rx FIFO, set the trigger level of the Tx FIFO (IP512-64 Models only), and select the type of DMA signaling (DMA is NOT supported by this model).

FIFO Control Register

FCR BIT	FUNCTION
0	When set to "1", this bit enables both the Tx and Rx FIFO's. All bytes in both FIFO's can be cleared by resetting this bit to 0. Data is cleared automatically from the FIFO's when changing from FIFO mode to the alternate (16C450) mode and visa-versa. This bit should be enabled (set to "1") before setting the FIFO trigger levels. Programming of other FCR bits is enabled by setting this bit to 1.
1	When set to "1", this bit clears all bytes in the Rx-FIFO and resets its counter logic to 0 (this does not clear the receive shift register). This bit will return to zero after clearing the FIFO's.
2	When set to "1", this bit clears all bytes in the Tx-FIFO and resets its counter logic to 0 (this does not clear the transmitter shift register). This bit will return to zero after clearing the FIFO's.
3	When set to "1", this bit sets DMA Signal from Mode 0 to Mode 1, if FIFO Control Register Bit 0 = 1 (DMA is Not Supported).
4,5	Not Used on IP512-16 Models. (IP512-64 Only) Used for setting the trigger level of the Tx FIFO interrupt as follows: BIT 5-4 Tx-FIFO TRIGGER LEVEL 00 08 Bytes for IP512-64 Models 01 16 Bytes for IP512-64 Models 10 32 Bytes for IP512-64 Models 11 56 Bytes for IP512-64 Models
6,7	Used for setting the trigger level of the Rx FIFO interrupt as follows: BIT 7-6 Rx-FIFO TRIGGER LEVEL 00 01 Bytes /08 Bytes for IP512-64 Models 01 04 Bytes /16 Bytes for IP512-64 Models 10 08 Bytes /56 Bytes for IP512-64 Models 11 14 Bytes /60 Bytes for IP512-64 Models

A power-up or system reset sets all FCR bits to 0.

LCR - Line Control Register, Ports A-D (Read/Write)

The individual bits of this register control the format of the data character as follows:

Line Control Register

LCR Bit	FUNCTION	PROGRAMMING
1 and 0	Word Length Sel	0 0 = 5 Data Bits 1 0 = 7 Data Bits 0 1 = 6 Data Bits 1 1 = 8 Data Bits
2	Stop Bit Select	0 = 1 Stop Bit (data lengths 5,6,7,8) 1 = 1.5 Stop Bits if 5 data bits selected, 2 Stop Bits if 6, 7, or 8 data bits selected.
3	Parity Enable	0 = Parity Disabled 1 = Parity Enabled A parity bit is generated during transmission and checked for between the last data word bit and the stop bit.
4	Even-Parity Select	0 = Odd Parity (forces an ODD number of 1's in the transmitted data, receiver also checks for the same format). 1 = Even Parity (forces an EVEN number of 1's in the transmitted data, receiver also checks for the same format).

Line Control Register...continued

LCR Bit	FUNCTION	PROGRAMMING
5	Stick Parity	0 = Stick Parity Disabled 1 = Stick Parity Enabled When parity is enabled, stick parity causes the transmission and reception of a parity bit to be in the opposite state from the value selected via bit 4. This is used as a diagnostic tool to force parity to a known state and allow the receiver to check the parity bit in a known state.
6	Break Control	0 = Break Disabled 1 = Break Enabled When break is enabled, the serial output line (TxD) is forced to the space state (low), thus transmitting a break condition. This bit acts only on the serial output and does not affect transmitter logic. For example, if the following sequence is used, no invalid characters are transmitted due to the presence of the break. 1. Load a zero byte in response to the Transmitter Holding Register Empty (THRE) status indication. 2. Set the break in response to the next THRE status indication. 3. Wait for the transmitter to become idle when the Transmitter Empty status signal is set high (TEMT=1); then clear the break when normal transmission has to be restored.
7	Divisor Latch Access Bit	0 = Access Receiver Buffer (normal) 1 = Allow Access to Divisor Latches

Note that bit 7 must be set high to access the divisor latch registers of the baud rate generator (DLL & DLM) during a read/write operation. For IP512-64 Models, "BF" must be written to the LCR register to access the enhanced functionality registers. Bit 7 must be low to access the Receiver Buffer register (RBR), the Transmitter Holding Register (THR), or the Interrupt-Enable Register (IER). A power-up or system reset sets all LCR bits to 0.

A detailed discussion of word length, stop bits, parity, and the break signal is included in Section 4.0 (Theory of Operation).

MCR - Modem Control Register, Ports A-D (R/W)

The Modem Control register normally controls the interface with the modem or data set as described below. Although this model does not support any of the handshake lines controlled via this register, it does use the RTS signal to enable the port transceiver for transmission as described below.

Modem Control Register

MCR Bit	FUNCTION	PROGRAMMING
0	Data Terminal Ready (DTR)[2]	0 = DTR* Not Asserted (Inactive) 1 = DTR* Asserted (Active) The DTR handshake signal is not implemented on this model and this bit has no effect.
1	Request to Send Output Signal (RTS)[2]	0 = RTS* Not Asserted (Inactive) Places port transceiver in the receive mode (default). 1 = RTS* Asserted (Active) Places port transceiver in the transmit mode. The RTS handshake signal is not implemented on this model and this bit is instead used to enable the transceiver for transmitting data .
2	Out1 (Internal)	Used in Loopback Mode only. No Effect on External Operation
3	Out2 (Internal)	Interrupt Control 0 = External Serial Channel Interrupt Disabled 1 = External Serial Channel Interrupt Enabled
4	Loop[1]	0 = Loop Disabled (Normal Mode) 1 = Local Loopback Enabled
5,6,7	Not Used on IP512-16 units.	On IP512-16 models, these bits are set to logic 0 (see below).

Modem Control Register Extended Functions (IP512-64 Only)

MCR Bit	FUNCTION	PROGRAMMING
5	XON Enable	0 = Disable Any XON function (Standard 16C550 Mode) 1 = Enable Any XON function
6	Rx/Tx I/O Mode	Not Used on IP512 (set to 0)
7	Clock Divide	0 = Normal divide by 1 clock (8MHz clock baud rates apply) 1 = Divide clock by 4 (2MHz baud rates apply)

Notes (Modem Control Register):

1. MCR Bit 4 provides a local loopback feature for diagnostic testing of the UART channel. When set high, the UART serial output (connected to the TXD driver) is set to the marking (logic 1 state), and the UART receiver serial input is disconnected from the RxD receiver path. The output of the UART transmitter shift register is looped back into the receiver shift register input. The four modem control inputs (CTS,DSR, DCD, & RI) are disconnected from their receiver input paths (the IP512 does not include data paths for these signals). The four modem control outputs (DTR, RTS, OUT1, & OUT2) are internally connected to the four modem control inputs (while their associated pins are forced to their high/inactive state). Thus, in Loopback Mode, transmitted data is immediately received permitting the host processor to verify the transmit and receive data paths of the selected serial channel. Thus, in Loopback Mode, interrupts are generated by controlling the state of the four lower order MCR bits internally, instead of by the external hardware paths. However, no interrupt requests or interrupt vectors are actually served in Loopback Mode and interrupt pending status is only reflected internally.
2. Note that the port transceiver is only placed in transmit mode if Request-to-Send (RTS) is asserted.
   RTS is used to enable the transceiver for transmitting data.

The RTS output is directly controlled by its respective control bit in this register and a "1" input asserts the RTS signal and places the port transceiver in transmit mode.

Note that on Model IP512-64, bits 5-7 are programmable only when EFR bit 4 is set to "1" and latched when EFR bit 4 is cleared. Bits 4-7 are permanently low on IP512-16 units. A power-up or system reset sets all MCR bits to 0.

LSR - Line Status Register, Ports A-D (Read/Write-Restricted)

The Line Status Register (LSR) provides status indication corresponding to the data transfer. LSR bits 1-4 are the error conditions that produce receiver line-status interrupts (a priority 1 interrupt in the Interrupt Identification Register). The line status register may be written, but this is intended for factory test and should be considered read-only by the application software.

Line Status Register

LSR Bit	FUNCTION	PROGRAMMING
0	Data Ready (DR)	0 = Not Ready (reset low by CPU Read of RBR or FIFO). Indicates no data in RBR or FIFO. 1 = Data Ready (set high when character received and transferred into the RBR or FIFO).
1	Overrun Error (OE)	0 = No Overrun Error (Normal) 1 = Indicates that data in the RBR is not being read before the next character is transferred into the RBR, overwriting the previous character. In the FIFO mode, it is set after the FIFO is filled and the next character is received. The overrun error is detected by the CPU on the first LSR read after it happens. The character in the shift register is not transferred into the FIFO, but is overwritten. This bit is reset low when the CPU reads the LSR.
2	Parity Error (PE)	0 = No Parity Error (Normal) 1 = Parity Error - the received character does not have the correct parity as configured via LCR bits 3 & 4. This bit is set high on detection of a parity error and reset low when the host CPU reads the contents of the LSR. In the FIFO mode, the parity error is associated with a particular character at the top of the FIFO (LSR Bit 2 reflects the error when the character is at the top of the FIFO).

Line Status Register...continued

LSR Bit	FUNCTION	PROGRAMMING
3	Framing Error (FE)	0 = No Error 1 = Framing Error - Indicates that the received character does not have a valid stop bit (stop bit following last data bit or parity bit detected as a zero/space bit). This bit is reset low when the CPU reads the contents of the LSR. In FIFO mode, the framing error is associated with a particular character in the FIFO (LSR Bit 3 reflects the error when the character is at the top of the FIFO).
4	Break Interrupt (BI)	0 = No Break 1 = Break - the received data input has been held in the space (logic 0) state for more than a full-word transmission time (start bits + data + parity bit + stop bits). Reset upon read of LSR. In FIFO mode, this bit is associated with a particular character in the FIFO and reflects the Break Interrupt when the break character is at the top of the FIFO. It is detected by the host CPU during the first LSR read. Only one "0" character is loaded into the FIFO when BI occurs.
5	Transmitter Holding Register Empty (THRE)	0 = Not Empty 1 = Empty - indicates that the channel is ready to accept a new character for transmission. Set high when character is transferred from the THR into the transmitter shift register. Reset low by loading the THR (It is not reset by a host CPU read of the LSR). In FIFO mode, this bit is set when the Tx FIFO is empty and cleared when one byte is written to the Tx FIFO. When a Transmitter Holding Register Empty interrupt is enabled by IER bit 1, this signal causes a priority 3 interrupt in the IIR. If the IIR indicates that this signal is causing the interrupt, the interrupt is cleared by a read of the IIR.
6	Transmitter Empty (TEMT)	0 = Not Empty 1 = Transmitter Empty - set when both the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. Reset low when a character is loaded into the THR and remains low until the character is transmitted (it is not reset low by a read of the LSR). In FIFO mode, this bit is set when both the transmitter FIFO and shift register are empty.

Line Status Register...continued

LSR Bit	FUNCTION	PROGRAMMING
7	Receiver FIFO Error	0 = No Error in FIFO (it is always 0 in the 16C450 mode--FCR bit 0 low). 1 = Error in FIFO - set when one of the following data errors is present in the FIFO: parity error, framing error, or break interrupt indication. Cleared by a host CPU read of the LSR if there are no subsequent errors in the FIFO.

Note that LSR Bits 1-4 (OE, PE, FE, BI) are the error conditions that produce a receiver-line-status interrupt (a priority 1 interrupt in the IIR register when any one of these conditions are detected). This interrupt is enabled by setting IER bit 2 to 1.

A power-up or system reset sets all LSR bits to 0, except bits 5 and 6 which are high.

MSR - Modem Status Register, Ports A-D (Read/Write)
NO FUNCTION FOR MODEL IP512

Normally, the Modem Status Register (MSR) provides the host CPU with an indication on the status of the handshake input lines from a modem or other peripheral device. However, this model does not provide signal paths for any of the handshake lines. As such, this register has no function for the IP512 and should be ignored.

Modem Status Register (No Function For Model IP512)

MSR BIT	FUNCTION
0	ΔCTS - NOT SUPPORTED
1	ΔDSR - NOT SUPPORTED
2	ΔRI - NOT SUPPORTED
3	ΔDCD - NOT SUPPORTED
4	CTS - NOT SUPPORTED
5	DSR - NOT SUPPORTED
6	RI - NOT SUPPORTED
7	DCD - NOT SUPPORTED

SCR - Scratch Pad/Interrupt Pointer Register, Ports A-D (R/W)

This 8-bit read/write register has no effect on the operation of either serial channel. Rather, it is provided as an aid to the programmer to temporarily hold data. Alternately, if interrupt generation is desired, then this port is used to store the interrupt vector for the port. In response to an interrupt select cycle, the IP module will execute a read of this register for the interrupting port (see Interrupt Generation section for more details).

IP Identification PROM - (Read Only, 32 Odd-Byte Addresses)

Each IP module contains identification (ID) PROM memory that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID PROM. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP512 ID PROM does not contain any variable (e.g. unique calibration) information. ID PROM bytes are addressed using only the odd addresses in a 64 byte block (on the “Big Endian” VMEbus).

Even addresses are used on the “Little Endian” PC/ISA bus. The IP512 ID PROM contents are shown in Table 3.2. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID PROM. Execution of an ID PROM Read requires 1 wait state.

Table 3.2: IP512 ID Space Identification (ID) PROM

Hex Offset From ID PROM Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All IP's have 'IPAC'
03	P	50	
05	A	41	
07	C	43	
09		A3	Acromag ID Code
0B		15	IP Model Code[1]
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		0C	Total Number of ID PROM Bytes
17		9C	CRC
19 to 3F		yy	Not Used

Notes (Table 3.2):

1. The IP model number is represented by a two-digit code within the ID PROM (the IP512 model is represented by 15 Hex).

THE EFFECT OF RESET

A software or hardware reset puts the serial channels into an idle-mode until initialization (programming). It also places the port transceiver in receive mode (RTS deasserted). A reset initializes the receiver and transmitter clock counters. It also clears the Line-Status Register (LSR), except for the transmitter shift-register empty (TEMT) and transmit holding-register empty (THRE) bits which are set to 1 (note that when interrupts are subsequently enabled, an interrupt will occur due to THRE being set). The Modem Control Register (MCR) is also cleared, placing the ports in receive mode (RTS deasserted). All of the discrete signal lines, memory elements, and miscellaneous logic associated with these register bits are cleared, de-asserted, or turned off. However, the Line Control Register (LCR), divisor latches, Receiver Buffer Register (RBR), and Transmitter Holding Register (THR) are not affected. The following table summarizes the effect of a reset on the various registers and internal and external signals:

The Effect of Reset:

REGISTER/ SIGNAL	RESET CONTROL	STATE/EFFECT
REGISTERS:		
IER	Reset	All bits low .
IIR	Reset	Bit 0 high, Bits 1-7 low.
LCR	Reset	All bits low.
MCR	Reset	All bits low .
FCR	Reset	All bits low.
LSR	Reset	All bits low, except bits 5 & 6 which are high.
MSR	Reset	All bits low.
EFR	Reset	All bits low.
XON-1,2	Reset	All bits low
XOFF-1,2	Reset	All bits low
SIGNALS (INTERNAL & EXTERNAL):		
TxD	Reset	High
Interrupt (RCVR errors)	Read LSR/ Reset	Low
Interrupt (RCVR data ready)	Read RCVR Buffer Register/ Reset	Low
Interrupt (THRE)	Read IIR/Write THR/Reset	Low
Interrupt (Modem Status Changes)	Read MSR/ Reset	Low
RTS*	Reset	High (Receive Mode)
OUT1*	Reset	High
OUT2*	Reset	High

IP512 PROGRAMMING

Each serial channel of this module is programmed by the control registers: LCR, IER, DLL, DLM, MCR, and FCR. Since none of the handshake lines are supported by this model, not all of the register status and controls are functional. However, control words are available to define the character length, number of stop bits, parity, baud rate, interrupts, and transceiver mode (receive or transmit). The control registers can be written in any order, but the IER register should normally be written last since it controls the interrupt enables. The contents of these registers may be updated any time the serial channel is not transmitting or receiving data.

The complete status of each channel can be read by the host CPU at any time during operation. Two registers are used to report the status of a particular channel: the Line Status Register (LSR) and the Modem Status Register (MSR). However, since this model provides no handshake support, the Modem Status Register has no function.

Serial channel data is read from the Receiver Buffer Register (RBR), and written to the Transmitter Holding Register (THR). Writing data to the THR initiates the parallel-to-serial transmitter shift register to the TxD line. Likewise, input data is shifted from the RxD pin to the Receiver Buffer Register. Asserting the RTS bit via the Modem Control Register will enable the TxD transmitter of the port. Deasserting RTS will enable the port for receiving data.

The Scratchpad Register is used to store the interrupt vector for the port. In response to an interrupt select cycle, the IP module will provide a read of this port. As such, each port may have a unique interrupt vector assigned. Interrupts are served in a shifting-priority fashion that is a function of the last interrupting port serviced. This prevents continuous interrupts from one channel from freezing out service of another interrupting channel.

This board operates in two different modes. In one mode, this device remains software compatible with the industry standard 16C450 family of UART's, and provides double-buffering of data registers. In the FIFO Mode (enabled via bit 0 of the FCR register), data registers are FIFO-buffered so that read and write operations can be performed while the UART is performing serial-to-parallel and parallel-to-serial conversions.

Two FIFO modes of operation are possible: FIFO Interrupt Mode and FIFO Polled Mode. In FIFO Interrupt Mode, data transfer is initiated by reaching a pre-determined trigger-level or generating time-out conditions. In FIFO-Polled Mode, there is no time-out condition indicated or trigger-level reached. The transmit and receive FIFO's simply hold characters and the Line Status Register must be read to determine the channel status.

Acromag provides an Industrial I/O Pack Software Library diskette (Model IPSW-LIB-M03, MSDOS format) to simplify communication with the board. Example software functions are provided for both ISA bus (PC/AT) and VMEbus applications. All functions are written in the "C" programming language and can be linked to your application. Software functions are shared with Acromag Model IP511. For more details, refer to the "README.TXT" file in the root directory on the diskette and the "INFO511.TXT" file in the appropriate "IP511" subdirectory off of "\VMEIP" or "\PCIP", according to your carrier.

FIFO Polled-Mode

Resetting Interrupt Enable Register Bit 0, Bit 1, Bit 2, Bit 3, or all four to 0, with FIFO Control Register (FCR) Bit 0 =1, puts the channel into the polled-mode of operation. The receiver and transmitter are controlled separately and either one or both may be in the polled mode. In FIFO-Polled Mode, there is no time-out condition indicated or trigger-level reached, the transmit and the receive FIFO's simply hold characters and the Line Status Register must be read to determine the channel status.

FIFO-Interrupt Mode

In FIFO Interrupt Mode, data transfer is initiated by reaching a pre-determined trigger-level or generating a time-out condition. Please note the following with respect to this mode of operation.

When the receiver FIFO and receiver interrupts are enabled, the following receiver status conditions apply:

1. LSR Bit 0 is set to 1 when a character is transferred from the shift register to the receiver FIFO. It is reset to 0 when the FIFO is empty.
2. The receiver line-status interrupt (IIR=06) has a higher priority than the received data-available interrupt (IIR=04).
3. The receive data-available interrupt is issued to the CPU when the programmed trigger level is reached by the FIFO. It is cleared when the FIFO drops below its programmed trigger level. The receive data-available interrupt indication (IIR=04) also occurs when the FIFO reaches its trigger level, and is cleared when the FIFO drops below its trigger level.

When the receiver FIFO and receiver interrupts are enabled, the following receiver FIFO character time-out status conditions apply:

1. A FIFO character time-out interrupt occurs if:
   - A minimum of one character is in the FIFO.
   - The last received serial character occurred longer than four continuous prior character times earlier (if 2 stop bits are programmed, the second one is included in the time delay).
   - The last CPU read of the FIFO is more than four continuous character times earlier. At 300 baud, and with 12-bit characters, the FIFO time-out interrupt causes a latency of 160ms maximum from received character to interrupt issued.
2. From the clock signal input, the character times can be calculated. The delay is proportional to the baud rate.
3. The time-out timer is reset after the CPU reads the receiver FIFO or after a new character is received when there has been no time-out interrupt.
4. A time-out interrupt is cleared and the timer is reset when the CPU reads a character from the receiver FIFO.

When the transmit FIFO and transmit interrupts are enabled (FCR Bit 0 = 1 and IER=01), a transmitter interrupt will occur as follows:

1. When the transmitter FIFO is empty, the transmitter holding register interrupt (IIR=02) occurs. The interrupt is cleared when the Transmitter Holding Register (THR) is written to or the Interrupt Identification Register (IIR) is read. One to sixteen characters can be written to the transmit FIFO when servicing this interrupt.
2. The transmit FIFO empty indications are delayed one character time minus the last stop bit time when the following occurs: Bit 5 of the LSR (THRE) is 1 and there is not a minimum of two bytes at the same time in the transmit FIFO since the last time THRE=1. The first transmitter interrupt after changing FCR Bit 0 is immediate, assuming it is enabled.

The receiver FIFO trigger level and character time-out interrupts have the same priority as the received data-available interrupt. The Transmitter Holding-Register-Empty interrupt has the same priority as the Transmitter FIFO-Empty interrupt.

Loopback Mode Operation

This device may be operated in a “loopback mode”, useful for troubleshooting a serial channel without physically wiring to the channel. Bit 4 of the Modem Control Register (MCR) is used to program the local loopback feature for the UART channel. When set high, the UART channel’s serial output line (Transmit Data Path) is set to the marking (logic 1 state), and the UART receiver serial data input lines are disconnected from the transceiver RxD path. The output of the UART transmitter shift register is then looped back into the receiver shift register input. Thus, a write to the Transmitter Holding Register is automatically looped back to the corresponding Receiver Buffer Register. Likewise, the four modem control outputs of the UART (DTR, RTS, OUT1, and OUT2 of the MCR Register) are internally connected to the corresponding four modem control inputs (monitored via the Modem Status Register), while their associated pins are forced to their high/ inactive state. However, this model does not normally provide signal paths for any of the handshake I/O lines. In the loopback diagnostic mode, transmitted data is immediately received permitting the host processor to verify the transmit and receive data paths of the selected serial channel. Further, modem status interrupt generation can be controlled manually in loopback mode by controlling the state of the four lower order MCR bits internally, instead of by external hardware paths (these handshake lines are not used for this model). However, in loopback mode, no interrupt requests or interrupt vectors will actually be served, the UART only reflects that an interrupt is pending.

Interrupt Generation

This model provides individual control for generation of transmit, receive, line status, and data set interrupts on each of four channels. Each channel shares interrupt request line 0 (Intreq0) according to a unique priority shifting scheme that prevents the continuous interrupts of one channel from freezing out interrupt requests of other channels.

After pulling the IntReq0 line low and in response to an Interrupt Select cycle, the current highest priority interrupt channel will serve up its interrupt vector first. Interrupt serving priority will shift as a function of the last port served. A unique interrupt vector may be assigned to each communication port and is loaded into the Scratchpad Register/Interrupt Vector Register (SCR) for the port. The IP module will thus execute a read of the Scratchpad Register in response to an interrupt select cycle. Two wait states are required to complete this cycle.

Interrupt priority is assigned as follows. Initially, with no prior interrupt history, Port A has the highest priority and will be served first, followed by port B, followed by port C, then followed by port D. However, if port A was the last interrupt serviced, then port B will have the highest priority, followed by port C, followed by port D, then port A, in a last-serviced last-out fashion. Priority continues to shift in the same fashion if port B or port C was the last interrupt serviced. This is useful in preventing continuous interrupts on one channel from freezing out interrupt service for other channels.

Software Flow Control (Model IP512-64 Only)

Model IP512-64 modules includes support for software flow control. However, since this module implements half-duplex EIA-485 (i.e. one combined transmit/receive path), the value of this feature is diminished. Normally, software flow control utilizes special XON & XOFF characters to control the flow of data, for more efficient data transfer and to minimize overrun errors.

Software flow control (sometimes called XON/XOFF pacing) sends a signal from one node to another by adding flow control characters to the data stream. The receiving node will detect the XON or XOFF character and respond by suspending transmission of data (XOFF turns the data flow off), or resuming transmission of data (XON turns the data flow on). Flow control is used frequently in data communications to prevent overrun errors or the loss of excess data. For example, a node might transmit the XOFF character to the host computer if the host is sending data to quickly to be processed or buffered, thus preventing the loss of excess data.

The flow control characters are stored in the XON-1,2 and XOFF-1,2 registers. Two XON & XOFF registers are provided because the flow control character may be 1 or 2 bytes long. The contents of the XON-1,2 and XOFF-1,2 registers are reset to "0" upon power-up or system reset, and may be programmed to any value for software flow control. Different conditions may be set to detect the XON/XOFF characters or start/stop the transmission.

When software flow control is enabled, the UART of this model will compare two sequential received data bytes with preprogrammed XOFF-1,2 characters. When a match is detected, the UART will halt transmission after completing the transmission of the current character. The receive ready flag of the Interrupt Identification Register will be set (IIR bit 4 is set to "1" when the XOFF character has been detected), only if enabled via bit 5 of the Interrupt Enable register (IER bit 5 is used to enable the received XOFF interrupt). An interrupt will then be generated. After recognition of the XOFF characters, the UART will compare the next two incoming characters with the preprogrammed XON-1,2 characters. If a match is detected, the UART will resume transmission and clear the received XOFF interrupt flag (Interrupt Identification Register bit 4). After more data has been received, the UART will automatically send XOFF-1,2 characters as soon as the received data passes the programmed FIFO trigger level, causing the host to suspend transmission. The UART will then transmit the programmed XON-1,2 characters as soon as the received data reaches the next lowest trigger level, thus causing the host to resume transmission (received data trigger levels are 8, 16, 56, and 60).

When single XON/XOFF characters are selected, the UART compares the received data to these values and controls the transmission accordingly (XON=restart transmission, XOFF=suspend transmission). These characters are not stacked in the data buffer or FIFO. When the *ANY* XON function is enabled (MCR bit 5 is set), the UART will automatically resume transmission after receiving *ANY* character after having recognized XOFF and suspended transmission. Note that the UART will automatically transmit the XON character(s) after the flow control function is disabled, if the XOFF character(s) had been sent prior to disabling the software flow control function. Special cases are provided to detect the special character and stack it into the data buffer or FIFO and these conditions are configured via bits 0-3 of the Enhanced Feature Register (EFR).

Programming Example

The following example will demonstrate data transfer between one channel of the host IP512 and another node, while using RTS to invoke the transmit or receive modes of the transceiver. Both nodes will use the FIFO mode of operation with a FIFO threshold set at 14 bytes. The data format will use 8-bit characters, odd-parity, and 1 stop bit. Please refer to Table 3.1 for address locations. The "H" following data below refers to the Hexadecimal data format.

1. Write 80H to the Line Control Register (LCR).

   This sets the Divisor Latch Access bit to permit access to the two divisor latch bytes used to set the baud rate. These bytes share addresses with the Receive and Transmit buffers, and the Interrupt Enable Register (IER).

2. Write 00H to the Divisor Latch MSB (DLM). Write 34H to the Divisor Latch LSB (DLL).

   This sets the divisor to 52 for 9600 baud (i.e. 9600 = 8MHz ÷ [16*52]).

3. Write 0BH to the Line Control Register (LCR).

   This first turns off the Divisor Latch Access bit to cause accesses to the Receiver and Transmit buffers and the Interrupt Enable Register. It also sets the word length to 8 bits, the number of stop bits to one, and enables odd-parity.

4. (OPTIONAL) Write xxH to the Scratch Pad Register.

   This has no effect on the operation, but is suggested to illustrate that this register can be used as a 1-byte memory cell. Alternately, the interrupt vector for the port may be written to this register and a read will be performed on this register in response to an interrupt select cycle.

5. Write 07H to the Interrupt Enable Register (IER).

   This enables the receiver line status interrupts. Support for the modem status interrupt is not available since no handshake lines are present for this model. The line status interrupt is used to signal unexpected error cases, such as parity or overrun errors. The received data available and transmit holding buffer empty interrupts have also been enabled to aid control by the host CPU in moving data back and forth.

6. Write C7H to the FIFO Control Register (FCR).

   This enables and initializes the transmit and receive FIFO's, and sets the trigger level of the receive FIFO interrupt to 14 bytes.

7. Read C1H from the Interrupt Identification Register (IIR).

   This is done to check that the device has been programmed correctly. The upper nibble "C" indicates that the FIFO's have been enabled and the lower nibble "1" indicates that no interrupts are pending.

8. Write 02H to the Modem Control Register (MCR).

   This sets the Request-To-Send bit. This is done to place the port transceiver in transmit mode. The host CPU may begin loading data into the transmit buffer.

9. The host should begin writing data repeatedly to the Transmitter Holding Register.

   This loads the transmit FIFO and initiates transmission of serial data by the transceiver. The first serial byte will take about 100us to transmit, so it is likely that the transmit FIFO will fill before the first byte has been sent.

   Depending on the protocol, the receiving side may have to acknowledge receipt of the data stream before more data may be sent. In this case, the host CPU would have to pause sending data and listen (receive data) for the acknowledgement (since half-duplex EIA-485 shares a single transmission line for both receiving and transmitting data).

10. Stop loading the transmit buffer, then write 00H to the Modem Control Register (MCR).

    This clears the Request-To-Send bit and places the transceiver in receive mode. The host CPU may listen for an acknowlegement signal that data had been received properly.

11. Assuming data has been received, read data repeatedly from the Receiver Buffer Register.

    After 14 bytes have been received (or fewer bytes with a timeout), an interrupt will be generated if the host CPU has not unloaded the receive FIFO.

4.0 THEORY OF OPERATION

This section contains information regarding the EIA-485 serial data interface. A description of the basic functionality of the circuitry used on the board is also included. Refer to the Block Diagram (Drawing 4501-588), Interface Diagram (Drawing 4501-586), and Interface Level Diagram (Drawing 4501-589), as you review this material.

EIA-485 SERIAL INTERFACE

To understand the application of this interface, you must first understand what is meant by the terms half-duplex and full-duplex. Duplex refers to the way information is exchanged on a transmission line and the number of lines used. *Full-duplex* means that data can be sent in both directions at the same time, like a two-lane highway with cars moving in each direction at the same time. However, *half-duplex* means that data can only be sent in one direction at a time, like a single lane road where cars must take turns going in opposite directions. The Model IP512 implements half-duplex EIA-485 using one pair of combined transmit/receive lines.

The Electronic Industries Association (EIA) introduced EIA-485 as a balanced (differential) serial data transmission interface standard for the exchange of binary information via a multipoint interconnection (network). That is, multiple generators (transmitters) and receivers may be connected via a common interconnection cable as shown in Drawing 4501-586. Data can be both transmitted and received from any node on the network, but since the data path is shared, the nodes must take turns sending data to avoid contention errors (various protocols are employed to accomplish this).

The EIA-485 interface standard specifies both balanced drivers and balanced receivers. Balanced data transmission refers to the fact that two conductors are switched per signal and the logical state of the data is referenced by the difference in potential between the two conductors, not with respect to signal ground. The differential method of data transmission makes EIA-485 ideal for noisy environments since it minimizes the effects of coupled noise and ground potential differences. That is, since these effects are seen as common-mode voltages (common to both lines), not differential, they are rejected by the receivers. Additionally, balanced drivers have faster transition times and allow operation at higher data rates over longer distances.

The EIA-485 standard defines a bidirectional, terminated, multiple driver and multiple receiver configuration. By sharing a single pair of wires for both transmit and receive, only half-duplex operation is possible. The maximum data transmission cable length is generally limited to 4000 feet without a signal repeater installed.

EIA-485 is electrically similar to EIA/TIA-422B, except that EIA-485 supports multiple driver operation over a shared transmit and receive data path (half-duplex), while EIA/TIA-422B supports a single driver (per path) with multiple receivers and separate transmit and receive data paths (full-duplex).

The chief application of EIA-485 is for multi-point data transmission on long busy lines in noisy environments. The same can be said for EIA/TIA-422B. However, EIA-485 implements half-duplex networks (one combined transmit and receive data path), while EIA/TIA-422B implements full-duplex networks (separate transmit and receive data paths). Acromag offers both isolated and non-isolated models for EIA/TIA-422B and EIA-485 (consult the factory for information on other serial communication modules).

With respect to EIA-485, logic states are represented by differential voltages from 1.5V to 5V. The polarity of the differential voltage determines the logical state. A logic 0 (the ‘space’ or ON state) is represented by a negative differential voltage between the terminals (measured A to B, or + to -). A logic 1 (the ‘mark’ or OFF state) is represented by a positive differential voltage between the terminals (measured A to B, or + to -). The transceiver converts the interface signals to the conventional TTL level associations required by the UART (receiver). The transceiver also converts the TTL signals of the UART to the differential voltages required at the interface (Refer to Drawing 4501-589).

EIA-485	BINARY 0 (SPACE/ON)	BINARY 1 (MARK/OFF)
SIGNAL A to B (+) to (-)	Negative Differential Voltage	Positive Differential Voltage

Start and stop bits are used to synchronize the receiver (DCE) to the asynchronous serial data of the transmitter (DTE).
The transmit data line is normally held in the mark state (logical 1).

The transmission of a data byte requires that a start bit (a logical 0 or a transition from mark to space) be sent first. This tells the receiver that the next bit is a data bit. The data bits are followed by a stop bit (a logical 1 or a return to the mark state). The stop bit tells the receiver that a complete byte has been received. Thus, 10 bits make up a data byte if the data character is 8 bits long (and no parity is assumed). Nine bits are required if only standard ASCII data is being transmitted (1 start bit + 7 data bits + 1 stop bit). The character size for this module is programmable from 5 to 8 bits.

Parity is a method of judging the integrity of the data. Odd, even, or no parity may be configured for this module. If parity is selected, then the parity bit precedes transmission of the stop bit. The parity bit is a 0 or 1 bit appended to the data to make the total number of 1 bits in a byte even or odd. Parity is not normally used with 8-bit data. Even parity specifies that an even number of logical 1's be transmitted. Thus, if the data byte has an odd number of 1's, then the parity bit is set to 1 to make the parity of the entire character even. Likewise, if the transmitted data has an even number of 1's, then the parity bit is set to 0 to maintain even parity. Odd parity works the same way using an odd number of logical 1's. Thus, both the transmitter and receiver must have the same parity. If a byte is received that has the wrong parity, an error is assumed and the sending system is typically requested to retransmit the byte. Two other parity formats not supported by this module are mark parity and space parity. Mark parity specifies that the parity bit will always be a logical 1, space parity requires the parity bit to always be 0.

The most common asynchronous serial data format is 1 start bit, 8 data bits, and 1 stop bit, with no parity. The following table summarizes the available data formats:

START BIT	Binary 0 (a shift from "Mark" to "Space")
DATA BITS	5,6,7, or 8 Bits
PARITY	Odd, Even, or None
STOP BIT	Binary 1 (1, 1-1/2, or 2 Bit times)

With start, stop, and parity in mind, for an asynchronous data byte, note that at least one bit will be a 1 (the stop bit). This defines the break signal (all 0 bits with a 1 stop bit lasting longer than one character). A break signal is a transfer from "mark" to "space" that lasts longer than the time it takes to transfer one character. Because the break signal doesn't contain any logical 1's, it cannot be mistaken for data. Typically, whenever a break signal is detected, the receiver will interpret whatever follows as a command rather than data. The break signal is used whenever normal signal processing must be interrupted. In the case of a modem, it will usually precede a modem control command. Do not confuse the break signal with the ASCII Null character, since a break signal is longer than one character time. That is, it is any "space" condition on the line that lasts longer than a single character (including its framing bits) and is usually 1-1/2 to 2 character times long.

The baud rate is a unit of transmission speed equal to the number of electrical signals (signal level changes) sent on a line in one second. It is thus, the electrical signaling rate or frequency at which electrical impulses are transmitted on a communication line. The baud rate is commonly confused with the bit transfer rate (bits-per-second), but baud rate does not equate to the number of bits transmitted per second unless one bit is sent per electrical signal.

One electrical signal (change in signal level) may represent more than one bit (as is the case with most phone modems). While bits-per-second (bps) refers to the actual number of bits transmitted in one second, the baud rate refers to the number of signal level changes that may occur in one second. Thus, 2400 baud does not equate to 2400 bits per second unless 1 bit is sent per electrical signal. Likewise, a 1200bps or 2400bps modem operates at a signalling rate of only 600 baud since they encode 2 and 4 bits, respectively, in one electrical impulse (through amplitude, phase, and frequency modulation techniques). However, for this device, the baud rate is considered equivalent to the bit rate.

This model includes a combined data path for both Transmit and Receive, providing half-duplex communication. No handshake signals are supported. Pins 1-18 and pins 26-43 of the field I/O connector P2 provide connectivity to serial Ports A-D of this module (Refer to Table 2.1 for pin assignments). A suffix of 'A', 'B', 'C', or 'D', followed by plus (+) or minus (-), is appended to the port signal names to indicate their port association and signal polarity. The UART handshake signal lines not used by this module have their corresponding UART pins tied high (+5V). This includes, RI (Ring Indication), DSR (Data Set Ready), Clear-to-Send (CTS), and DCD (Data Carrier Detect). However, the UART RTS signal line of each port is used to set the port transceiver mode (transmit or receive).

Port Signal Descriptions For Model IP512

SIGNAL ±	DESCRIPTION
TXRXA+ TXRXB+ TXRXC+ TXRXD+	Transmit Data Line Output and Receive Data Line Input Positive (two pin connections per port). To the communication network master, this line is used as the positive transmit data line. To the communication network slaves, this line is the positive receive data line. Because the line is used for both transit and receive, only half-duplex communication is possible. During Loopback Mode, the TxD output of the UART is internally connected to the RxD input of the UART and disconnected from this data path.
TXRXA- TXRXB- TXRXC- TXRXD-	Transmit Data Line Output and Receive Data Line Input Negative (two pin connections per port). To the communication network master, this line is the negative transmit data line. To the communication network slaves, this line is the negative receive data line. Because the line is used for both transmit and receive, only half-duplex communication is possible. During Loopback Mode, the TxD output of the UART is internally connected to the RxD input of the UART and disconnected from this data path.
+5V Input A +5V Input B +5V Input C +5V Input D	Isolated +5V Port Power Input (four pin connections per port). For isolated operation, an external isolated power supply must be connected here to power the port. If non-isolated operation is acceptable, then the port may be powered from the +5V logic supply provided by the carrier by programming the power and ground jumpers accordingly (see Drawing 4501-587).
Common A Common B Common C Common D	Individually Isolated Signal Common and +5V returns. For isolated operation, the external isolated power supply common must be connected here to complete power to the port. If non-isolated operation is acceptable, then the port may be powered from the logic common provided by the carrier by programming the power and ground jumpers accordingly (see Drawing 4501-587).

IP512 OPERATION

Connection to each serial port is provided through connector P2 (refer to Table 2.1). These pins are tied to the I/O pins of EIA-485 line transceivers. The transceiver convert the EIA-485 received signal levels to the TTL levels required by the UART (Universal Asynchronous Receiver/Transmitter). The transceiver also converts the UART TTL transmitted levels to the EIA-485 voltages required at the interface. The TTL TxD & RxD signal paths to the UART are isolated via capacitively coupled digital isolators. An optical isolator is used to isolate the RTS signal that controls the transceiver mode (transmit or receive). The UART provides the necessary conversion from serial-to-parallel (receive) and parallel-to-serial (transmit) for interfacing to the data bus. Additionally, it provides data buffering and data formatting capabilities. A programmable logic device (PLD) is used to control the interface between the UART, the IP bus, line transceivers, isolation buffers, and to provide IDPROM memory.

Note that the field serial interface to the carrier board provided through connector P2 (refer to Table 2.1) is considered isolated, but only when isolated external port power is provided to the port. Optionally, the port may use the power provided by carrier by programming the power and common jumpers appropriately. In this mode, the port is considered non-isolated, and this means that the field signal return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage. Refer to Drawing 4501-585 for example communication wiring and grounding connections.

LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1 (refer to Table 2.2). Not all of the IP logic P1 pin functions are used. P1 also provides +5V to power the module (±12V is not used). Optionally, P1 may also provide power to each port when the P3 & P4 power jumpers are present for non-isolated operation.

A programmable logic device installed on the IP Module provides the control signals required to operate the board. It decodes the selected addresses in the I/O and ID spaces and produces the chip selects, control signals, and timing required by the communication registers, as well as, the acknowledgement signal required by the carrier board per the IP specification. It also provides the ID PROM memory and prioritizes the interrupt requests coming from the serial ports in a shifting priority fashion, based on the last interrupt serviced.

The ID PROM (read only) implemented in the PLD of the IP module provides the identification for the individual module per the IP specification. The ID PROM, configuration control registers, and FIFO buffers are all accessed through an 8-bit data bus interface to the carrier board.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

GENERAL SPECIFICATIONS

UART.....Texas Instruments TL16C554FN or equivalent (Model IP512-16). Startech ST16C654CJ68 (Model IP512-64). UART's are pin-for-pin compatible, but the Startech version includes enhanced functionality, such as: larger FIFO's and software flow controls.
Operating Temperature.....0 to +70°C.
Relative Humidity.....5-95% non-condensing.
Storage Temperature.....-40°C to +125°C.
Physical Configuration.....Single Industrial I/O Pack Module.
- Length.....3.880 inches (98.5 mm).
- Width.....1.780 inches (45.2 mm).
- Board Thickness.....0.062 inches (1.59 mm).
- Max Component Height.....0.314 inches (7.97 mm).

Connectors:
- P1 (IP Logic Interface).....50-pin female receptacle header (AMP 173279-3 or equivalent).
- P2 (Field I/O).....50-pin female receptacle header (AMP 173279-3 or equivalent).

Power:
+5 Volts (±5%).....110mA Typical, 170mA Maximum in isolated mode with ports powered externally. 155mA Typical, 245mA Maximum, in non-isolated mode with port power jumpers present and ports sharing the logic supply.
±12 Volts (±5%) from P1.....0mA (Not Used).
Isolation.....Port-to-Logic - Logic and field lines are isolated from each other for voltages up to 250VAC, or 354V DC on a continuous basis when ports are powered externally with isolated supplies (will withstand 1000V AC dielectric strength test for one minute without break-down). Note that port power and common may be jumpered to share logic power for non-isolated operation. These ratings apply in isolated mode with power jumpers removed.
Isolation Spacing.....Minimum printed circuit board isolation spacings are as follows: Port-to-Logic - 0.023" Minimum; Port-to-Port - 0.022" Minimum. These spacings apply to inner layer foil spacings (outer layer clearances are greater).
Resistance to RFI.....No data upsets occur for field strengths up to 10V per meter at 27MHz, 151MHz, & 460MHz per SAMA PMC 33.1 test procedures.
Resistance to EMI.....Unit has been tested with no data upsets under the influence of EMI from switching solenoids, commutator motors, & drill motors.
Surge Withstand Capability.....Interface lines exhibit no damage when tested with a waveform representative of surges (high frequency transient electrical interference) to ±1KV in isolated mode.
ESD Protection.....EIA/TIA-422B lines are protected from ESD voltages to ≥ ±2KV in isolated mode.

EIA-485 PORTS
Configuration.....Four independently isolated EIA-485 serial ports with separate signal common and +5V input power connections. Capacitively coupled isolation is provided by an isolated buffer on the digital side of the port transceiver.
Interface.....Asynchronous serial only, half-duplex. Up to 32 transceivers may be networked together without the use of a repeater.
Port Transceiver.....Linear Technology LTC1481CS8 or equivalent. Designed for EIA/TIA-422B or EIA-485 applications.
Port Power Requirements.....Isolated +5V (+4.75V to +5.25V), 18mA maximum (no line faults), each port. Note: If non-isolated operation is desired, the port power and ground jumpers may be programmed to provide port power from the +5V logic supply provided by the carrier board (see Drawing 4501-587).
Data Rate.....Programmable to 512K bits/sec using internal baud rate generator derived from 8MHz carrier clock.
Maximum Cable Length.....1200M (4000 feet) typical. Use of a signal repeater can extend this distance beyond this limit.
Character Size.....Software programmable 5-8 bits.
Parity.....Software programmable odd, even, or no parity.
Stop Bits.....Software programmable 1, 1-1/2, or 2 bits.
Data Register Buffers.....The data registers are double-buffered (16C450 mode), or 16-byte FIFO buffered (IP512-16 FIFO mode), or 64-byte FIFO buffered (IP512-64 mode).
Interrupts.....Receiver Line Status Interrupt (i.e. Overrun error, Parity error, Framing error, or Break Interrupt); Received Data Available (FIFO level reached) or Character Time-Out; Transmitter Holding Register Empty. Multiple port Interrupts share the IntReq0 line according to a shifting-priority scheme based on the last interrupting port serviced.
Termination Resistors.....120Ω Termination Resistors are installed in sockets on board and may be removed if required (see Drawing 4501-587 for location). Install termination resistors at the end of a network only.
Bias Resistors.....560Ω pullup to +5V on (+) output lines, 560Ω pull-down to COM on (-) lines, installed in sockets on board and may be removed if required (see Drawing 4501-587 for location). Only one set of bias resistors should be installed per line pair.
Differential Input Threshold.....-0.2V Min. to +0.2V Max.
Input Hysteresis.....45mV, Typical.
Receiver Input Resistance.....12KΩ Minimum.
Common Mode Output Voltage.....3V Maximum (27Ω or 50Ω load).
Differential Output Voltage .....5V Max. (Unloaded); 2V Min. (EIA-485, 50Ω load); 1.5V Min. (EIA-485, 27Ω load).

Output Short Circuit Current.....250mA Maximum (Vout=-7V).
Driver Rise or Fall Time.....30ns Maximum into 54Ω and 100pF load.

INDUSTRIAL I/O PACK COMPLIANCE

Specification.....This module meets or exceeds all written Industrial I/O Pack specifications per revision 0.7.1.
Electrical/Mechanical Interface....Single-Size IP Module.
IP Data Transfer Cycle Types Supported:
- Input/Output (IOSel*).....D16 or D08 least significant read/write of data.
- ID Read (IDSel*).....32 x 8 ID PROM read on D0..D7.
- Interrupt Select (INTSel*).....8-bit word (D08) read of Scratch Pad/Interrupt Vector Register contents.

Access Times (8MHz Clock):
- ID PROM Read.....1 wait state (375ns cycle).
- Register Read or Write.....2 wait states (500ns cycle).
- Interrupt Select Read.....2 wait states (500ns cycle).

APPENDIX

CABLE: MODEL 5025-550-x (Non-Shielded)
MODEL 5025-551-x (Shielded)

Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet (12 feet maximum). Choose shielded or unshielded cable according to model number. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.
Application: Used to connect a Model 5025-552 termination panel to the AVME9630/9660 non-intelligent carrier board A-D connectors (both have 50-pin connectors).
Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50-wire flat ribbon cable, 28 gage. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent). Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).
Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).
Keying: Headers at both ends have polarizing key to prevent improper installation.
Schematic and Physical Attributes: For Non-Shielded cable model, see Drawing 4501-462. For Shielded cable model, see Drawing 4501-463.
Shipping Weight: 1.0 pound (0.5Kg) packaged.

CABLE: MODEL 5029-943

Type: Model 5029-943 IP500 Communication Cable: A five foot long, flat 50-pin cable with a female connector on one end (for connection to AVME9630/9660 or other compatible carrier boards) and four DE-9P connectors (serial ports) on the other end.
Application: Used to connect up to four DB-9 serial ports to AVME9630/9660 non-intelligent carrier board A-D connectors. It is used primarily with Acromag Model IP500, IP512, & IP502 serial communication modules.
Length: 5 feet.
Cable: 50-wire, 28 gage, flat ribbon cable. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent).
Headers: 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).
Port Connectors: Four DE-9P (9-pin, D-SUB, Male) connectors with strain relief (3M connector U89809-9000 with 3448-8D09A strain relief, or equivalent).
Keying: 50-pin Header at one end has polarizing key to prevent improper installation.
Schematic and Physical Attributes: See Drawing 4501-552.
Shipping Weight: 1.0 pound (0.5Kg) packaged.

CABLE: MODEL 5029-900

Type: Model 5029-900 APC8600 High-Density Cable: A 36-inch long interface cable that mates the high-density (25mil pitch) 50-pin I/O connectors of the APC8600 PC/AT ISAbus carrier board, to the high density connectors on the APC8600 Termination Panels (described below).

Application: Used with the APC8600 PC carrier and termination panel. It mates the high-density (25mil pitch) 50-pin I/O connectors of the APC8600 PC/AT ISAbus carrier board, to the high density connectors on the APC8600 Termination Panel (described below).

Length: 36-inches

Cable: 50-wire flat ribbon cable, 28 gage, Non-Shielded, T&B/Ansley Part 135-050 or equivalent.

Headers: 50-pin, high-density, 25-mil pitch, female header. Header-T&B Ansley Part 311-050302 or equivalent.

Keying: Headers at both ends have polarizing key to prevent improper installation.

Shipping Weight: 1.0 pound (0.5Kg) packaged.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For AVME9630/9660 Boards

Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660 3U/6U non-intelligent carrier boards (A-D connectors only) via a flat ribbon cable (Model 5025-550-x or 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.

Schematic and Physical Attributes: See Drawing 4501-464.

Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.

Connections to AVME9630/9660: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-550-x or 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.

Mounting: Termination panel is snapped on the DIN mounting rail.

Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.

Operating Temperature: -40°C to +100°C.

Storage Temperature: -40°C to +100°C.

Shipping Weight : 1.25 pounds (0.6kg) packaged.

TERMINATION PANEL: MODEL 5029-910

Type: Screw-Terminal Termination Panel For Acromag APC8600 PC/AT ISAbus Carrier Boards.

Application: This panel converts the high-density ribbon-cable connectors coming from the APC8600 carrier board (Acromag cable Model 5029-900) to screw terminals, for direct-wired interfaces. This panel facilitates the connection of up to 50 field I/O signals and connects to the APC8600 PC/AT ISAbus carrier board via high-density (25-mil pitch) flat ribbon cable and connectors (see cable Model 5029-900). The A & B connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.

Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.

Connections to APC8600: P1, 50-pin, high-density male header with strain relief.

Mounting: Termination Panel includes mounting holes.

Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.

Operating Temperature: -40°C to +85°C.

Storage Temperature: -55°C to +125°C.

Shipping Weight : 1.25 pounds (0.6kg) packaged.

TRANSITION MODULE: MODEL TRANS-GP

Type: Transition module for AVME9630/9660 boards.

Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).

Schematic and Physical Attributes: See Drawing 4501-465.

Field Wiring: 100-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).

Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).

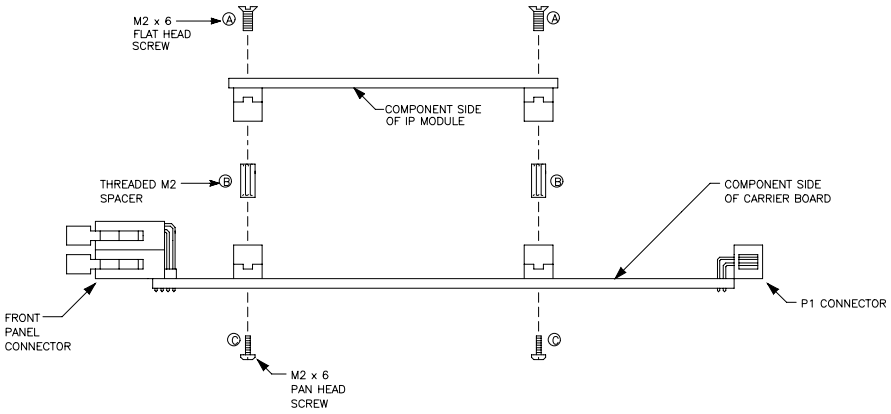
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.

Printed Circuit Board: Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.

Operating Temperature: -40°C to +85°C.

Storage Temperature: -55°C to +105°C.

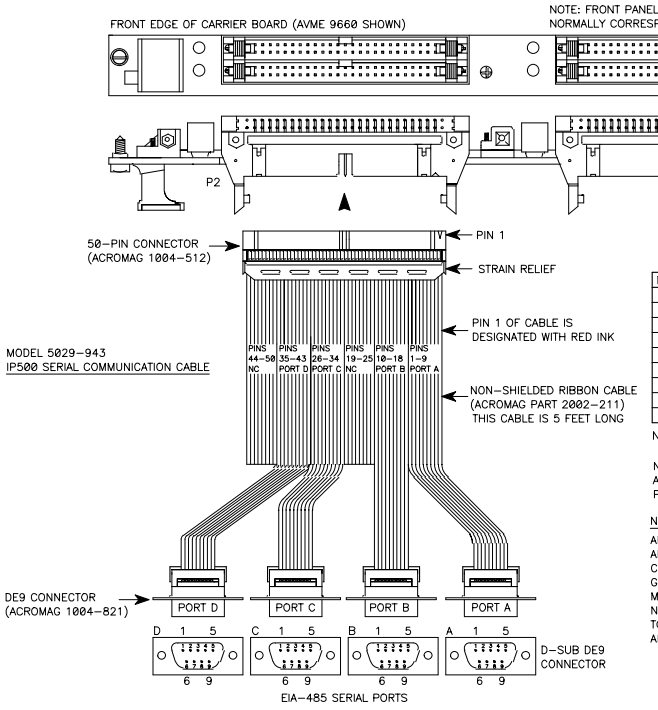
Shipping Weight: 1.25 pounds (0.6Kg) packaged.



ASSEMBLY PROCEDURE:

1. THREADED SPACERS ARE PROVIDED IN TWO DIFFERENT LENGTHS. THE SHORTER LENGTH IS FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES).

IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY 4501–434B



IP512 EIA–485 PIN ASSIGNMENTS		RIBBON CABLE/P2 PIN NUMBER			
DE9 PIN	EIA–485 SIGNAL	PORT A	PORT B	PORT C	PORT D
5	GND – PORT SIGNAL COMMON	1	10	26	35
9	+5V – PORT POWER SUPPLY INPUT	2	11	27	36
4	RxD+/TxD+ (DATA POSITIVE)	3	12	28	37
8	+5V – PORT POWER SUPPLY INPUT	4	13	29	38
3	RxD–/TxD– (DATA NEGATIVE)	5	14	30	39
7	+5V – PORT POWER SUPPLY INPUT	6	15	31	40
2	RxD–/TxD– (DATA NEGATIVE)	7	16	32	41
6	+5V – PORT POWER SUPPLY INPUT	8	17	33	42
1	RxD+/TxD+ (DATA POSITIVE)	9	18	34	43

NOTE: P2 PINS 19–25 & 44–50 ARE NOT CONNECTED.

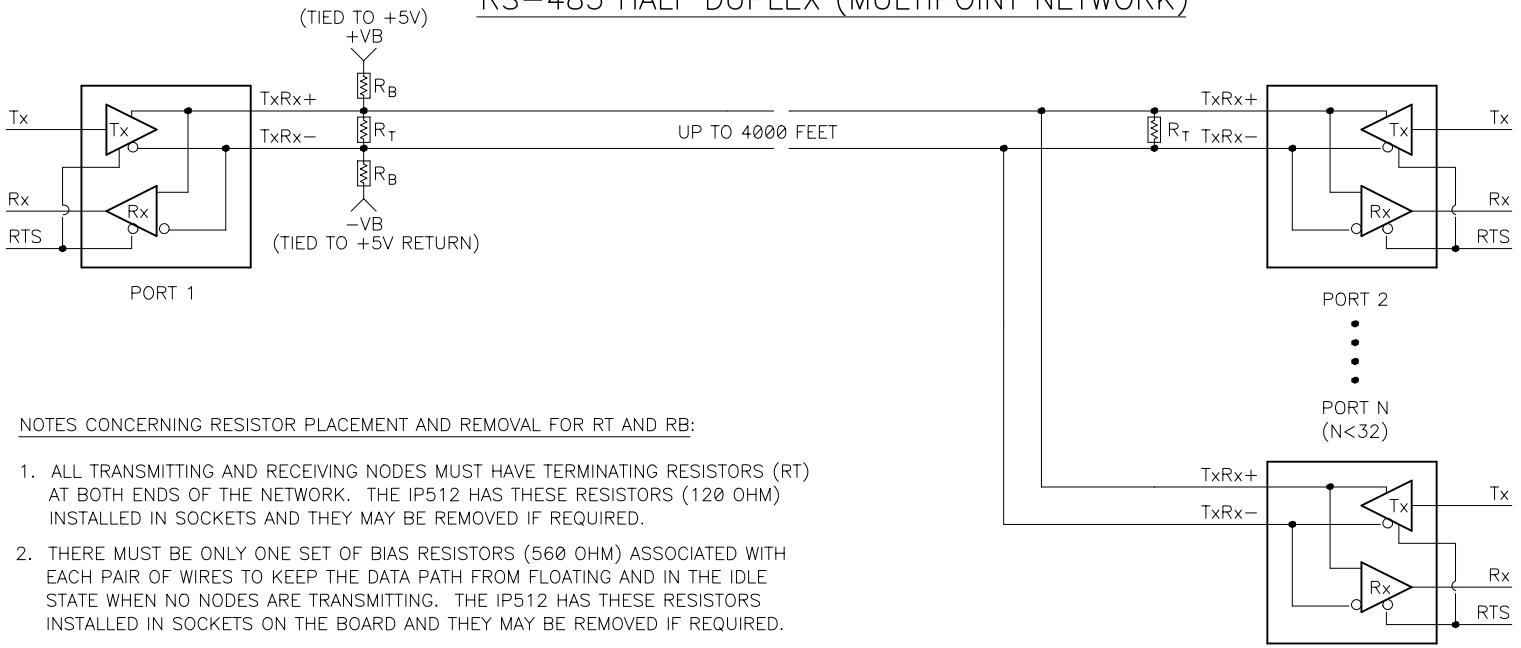
NOTE: MODEL 5029–943 CABLE CONNECTIONS SHOWN AT LEFT. OPTIONALLY, AN ACROMAG MODEL 5025–552 TERMINATION PANEL MAY BE CONNECTED TO PROVIDE DIRECT (WIRED) SCREW TERMINAL HOOK–UP AT THE FIELD SIDE.

NON–ISOLATED MODE

ABOUT GROUNDING: IF ISOLATED POWER IS NOT PROVIDED TO THE IP512 PORTS AND THE IP POWER IS JUMPERED TO THE PORT INSTEAD, THEN THE SIGNAL COMMON CONNECTION AT THE COMMUNICATION PORTS IS COMMON TO THE IP INTERFACE GROUND, WHICH IS TYPICALLY COMMON TO SAFETY (CHASSIS) GROUND WHEN MOUNTED ON A CARRIER BOARD AND INSERTED IN A BACKPLANE. BE CAREFUL NOT TO ATTACH SIGNAL COMMON TO SAFETY GROUND VIA ANY DEVICE ATTACHED TO THESE PORTS OR A GROUND LOOP MAY DEVELOP AND THIS MAY ADVERSELY AFFECT OPERATION.

4501-585A

RS–485 HALF DUPLEX (MULTIPOINT NETWORK)



NOTES CONCERNING RESISTOR PLACEMENT AND REMOVAL FOR RT AND RB:

1. ALL TRANSMITTING AND RECEIVING NODES MUST HAVE TERMINATING RESISTORS (RT) AT BOTH ENDS OF THE NETWORK. THE IP512 HAS THESE RESISTORS (120 OHM) INSTALLED IN SOCKETS AND THEY MAY BE REMOVED IF REQUIRED.
2. THERE MUST BE ONLY ONE SET OF BIAS RESISTORS (560 OHM) ASSOCIATED WITH EACH PAIR OF WIRES TO KEEP THE DATA PATH FROM FLOATING AND IN THE IDLE STATE WHEN NO NODES ARE TRANSMITTING. THE IP512 HAS THESE RESISTORS INSTALLED IN SOCKETS ON THE BOARD AND THEY MAY BE REMOVED IF REQUIRED.
3. THE IDLE STATE OF THE DATA PAIR TxRx+/– IS HIGH ON TxRx+ CORRESPONDING TO THE MARK (1) STATE ON THE LINE.
4. AN RS–485 NETWORK IS GENERALLY LIMITED TO LESS THAN 4000 FEET WITH NO MORE THAN 32 NODES. THIS DISTANCE AND NODE CAPACITY MAY BE EXPANDED WITH THE USE OF A SIGNAL REPEATER.

POSSIBLE NETWORK PROTOCOLS FOR MULTIPLE PORTS ON THE NETWORK:

1. POLLING: ONE NETWORK NODE IS DESIGNATED AS THE MASTER, WHILE ALL OTHER NODES ARE DESIGNATED SLAVES. THE MASTER CONTROLS WHICH NODES TRANSMIT BY POLLING EACH SLAVE PERIODICALLY. A SLAVE MAY BE PERMITTED TO SEND A MESSAGE TO THE MASTER OR TO ANY NODE ON THE NETWORK.
2. TOKEN–BUS: ALL NODES ON THE NETWORK MAY TRANSMIT DATA IN THE FORM OF A "TOKEN", BUT ONLY WHEN GRANTED PERMISSION. THE NODE THAT HAS POSSESSION OF THE TOKEN CAN TRANSMIT A PACKET TO ANY OTHER NETWORK NODE. THE TOKEN THUS PASSES FROM NODE–TO–NODE IN A SPECIAL PACKET AND IN CIRCULAR FASHION. A NODE THAT HAS NOTHING TO PASS SIMPLY PASSES THE TOKEN TO THE ADJACENT NODE.
3. COMBINED POLLING & TOKEN–BUS: THIS PROTOCOL ASSIGNS MULTIPLE MASTER NODES AND MULTIPLE SLAVE NODES. THE MASTER NODES THEN PASS THE TOKEN AMONGST THEMSELVES AS DESCRIBED IN THE TOKEN–BUS PROTOCOL ABOVE.

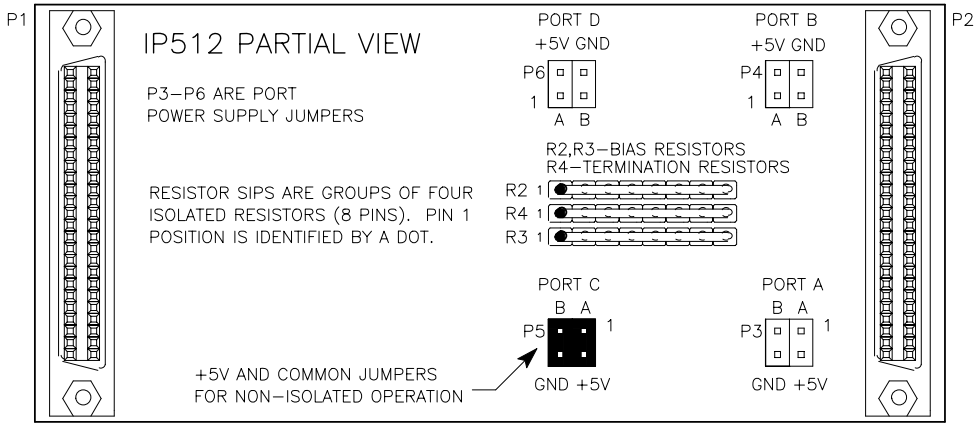
NOTE THAT THE BIAS RESISTORS HAVE BEEN REMOVED FROM NODES 2 THROUGH N, SINCE ONLY ONE SET OF BIAS RESISTORS IS REQUIRED PER NETWORK PAIR.

THE TERMINATION RESISTORS ARE ONLY REQUIRED AT THE ENDS OF A NETWORK, USUALLY THE FAR–MOST ENDS. THEY ARE NOT REQUIRED FOR SHORT STUBS OFF THE MAIN TRUNK AND ARE NOT SHOWN FOR PORT N.

4501–586A

IP512 TERMINATION RESISTOR, BIAS RESISTOR, AND POWER JUMPER LOCATION DRAWING

MODEL IP512 COMPONENT SIDE PARTIAL VIEW

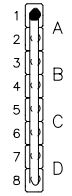


IP512 RESISTOR IDENTIFICATION

SIP	VALUE	FUNCTION	PORT	
R4:A	120 OHM	A TERMINATION	PORT A	T
R4:B	120 OHM	B TERMINATION	PORT B	E
R4:C	120 OHM	C TERMINATION	PORT C	R
R4:D	120 OHM	D TERMINATION	PORT D	M
R2:A	560 OHM	TxRx A+ BIAS	PORT A	
R2:B	560 OHM	TxRx A– BIAS	PORT A	
R2:C	560 OHM	TxRx B+ BIAS	PORT B	B
R2:D	560 OHM	TxRx B– BIAS	PORT B	I
R3:A	560 OHM	TxRx C+ BIAS	PORT C	A
R3:B	560 OHM	TxRx C– BIAS	PORT C	S
R3:C	560 OHM	TxRx D+ BIAS	PORT D	
R3:D	560 OHM	TxRx D– BIAS	PORT D	

RESISTOR SIPS ARE MOUNTED IN A SOCKET AND CAN BE REMOVED IF REQUIRED.

RESISTOR SIPS ARE DIVIDED AS SHOWN



DETAIL "A"

MODULE IS SHIPPED WITH ALL SIP RESISTORS INSTALLED

NOTES CONCERNING RESISTOR PLACEMENT AND REMOVAL:

1. ALL TRANSMITTING AND RECEIVING CHANNELS OF THE IP512 MUST HAVE TERMINATING RESISTORS (RT) AT BOTH ENDS OF THE NETWORK. THE IP512 HAS USER–REMOVEABLE PLUG–IN SIP TERMINATION RESISTORS (120 OHM) ALREADY INSTALLED AND THESE MAY BE REMOVED IF REQUIRED, OR IF ALREADY PRESENT ON THE NETWORK. BE SURE TO REMOVE REDUNDANT TERMINATION RESISTORS FROM THE NETWORK.
2. THERE MUST BE NO MORE THAN ONE SET OF BIAS RESISTORS ASSOCIATED WITH EACH PAIR OF SIGNAL WIRES TO KEEP THE NETWORK FROM FLOATING WHEN NO UNITS ARE TRANSMITTING. THE IP512 HAS THESE RESISTORS INSTALLED IN SOCKETS ON THE BOARD AND THEY MAY BE REMOVED WHERE REQUIRED, OR IF ALREADY PRESENT ON THE NETWORK. BE SURE TO REMOVE REDUNDANT BIAS RESISTORS FROM THE NETWORK.
3. THE IDLE STATE OF THE TxRx DATA PAIRS ARE HIGH ON TxRx+ AND THIS CORRESPONDS TO A MARK (1) ON THE DATA LINE.

POWER JUMPERS:

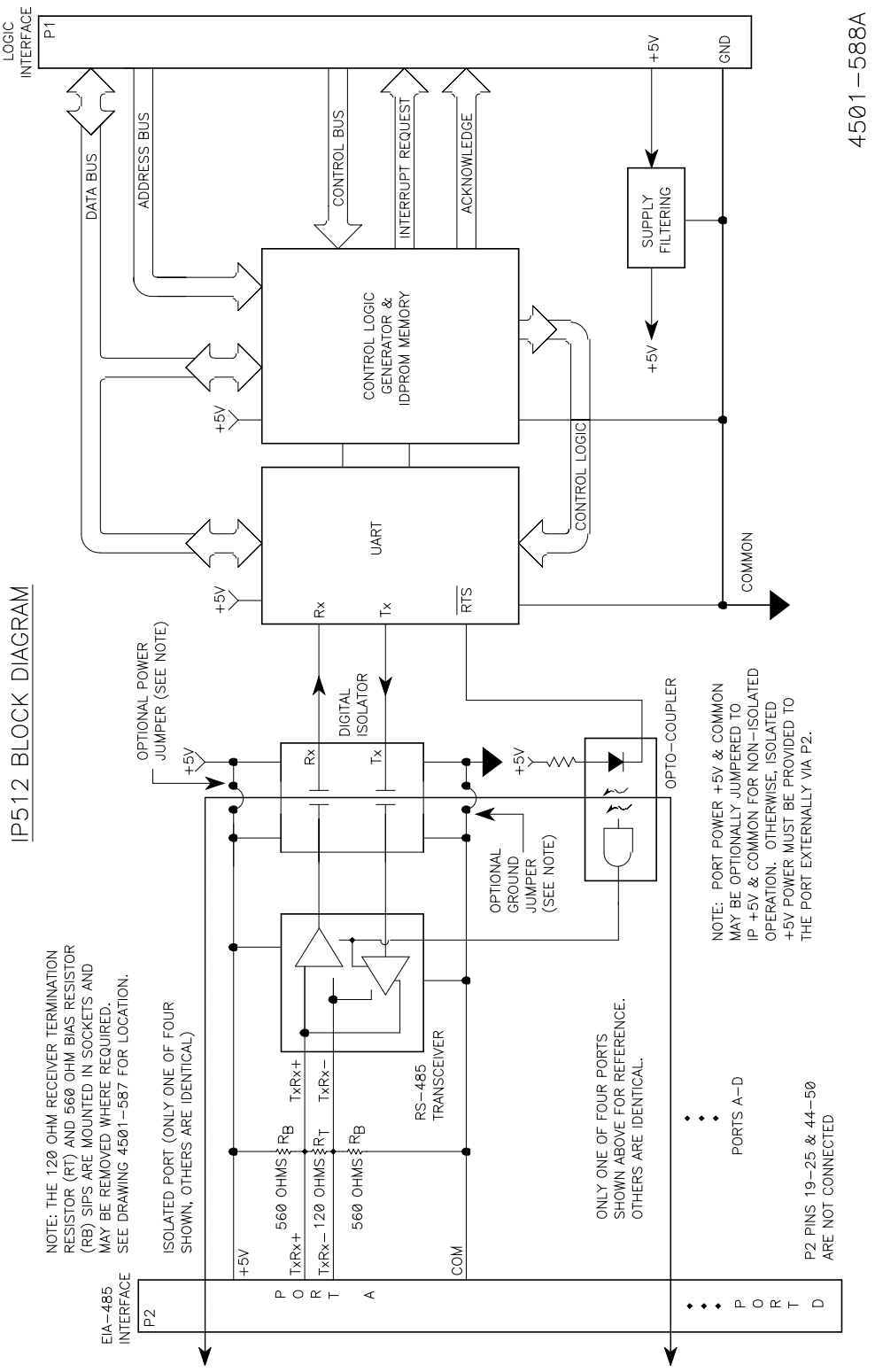
JUMPERS ARE PLACED VERTICALLY AND CONNECT THE IP512 +5V AND COMMON SUPPLIES TO POWER THE PORT WHEN AN ISOLATED SUPPLY IS NOT AVAILABLE AND NON–ISOLATED OPERATION IS DESIRED.

REMOVE THESE JUMPERS FOR ISOLATED OPERATION (THE PORTS MUST THEN BE POWERED EXTERNALLY).

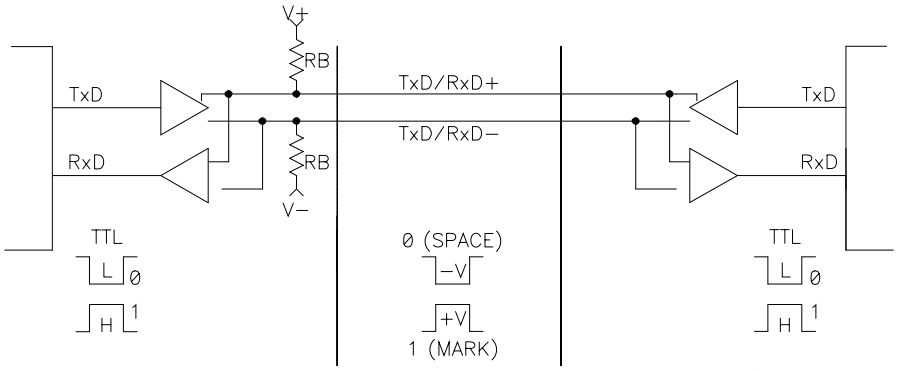
AS SHOWN, THE PORT C JUMPERS ARE PRESENT AND PORT C IS THUS POWERED OFF THE IP SUPPLY FOR NON–ISOLATED OPERATION.

MODULE IS SHIPPED WITH POWER JUMPERS INSTALLED. THESE MUST BE REMOVED AND ISOLATED PORT POWER PROVIDED EXTERNALLY FOR ISOLATED OPERATION.

4501–587A


IP512 BLOCK DIAGRAM
4501-588A
LOGIC INTERFACE
P1
DATA BUS
ADDRESS BUS
CONTROL BUS
INTERRUPT REQUEST
ACKNOWLEDGE
+5V
GND
SUPPLY FILTERING
CONTROL LOGIC GENERATOR & IDPROM MEMORY
UART
CONTROL LOGIC
COMMON
Rx
Tx
RTS
OPTIONAL POWER JUMPER (SEE NOTE)
DIGITAL ISOLATOR
OPTO-COUPLER
OPTIONAL GROUND JUMPER (SEE NOTE)
RS-485 TRANSCEIVER
560 OHMS
120 OHMS
TxRx+
TxRx-
COM
EIA-485 INTERFACE
P2
PORT A
PORTS A-D
PORT D
NOTE: THE 120 OHM RECEIVER TERMINATION RESISTOR (RT) AND 560 OHM BIAS RESISTOR (RB) SIPS ARE MOUNTED IN SOCKETS AND MAY BE REMOVED WHERE REQUIRED. SEE DRAWING 4501-587 FOR LOCATION.
ISOLATED PORT (ONLY ONE OF FOUR SHOWN, OTHERS ARE IDENTICAL)
ONLY ONE OF FOUR PORTS SHOWN ABOVE FOR REFERENCE. OTHERS ARE IDENTICAL.
NOTE: PORT POWER +5V & COMMON MAY BE OPTIONALLY JUMPERED TO IP +5V & COMMON FOR NON-ISOLATED OPERATION. OTHERWISE, ISOLATED +5V POWER MUST BE PROVIDED TO THE PORT EXTERNALLY VIA P2.
P2 PINS 19-25 & 44-50 ARE NOT CONNECTED

RS-485 TxD/RxD DATA LINES (HALF DUPLEX ONLY)

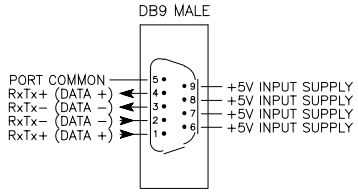


DIFFERENCE VOLTAGE
[TxD/RxD+] – [TxD/RxD-]

NOTE:

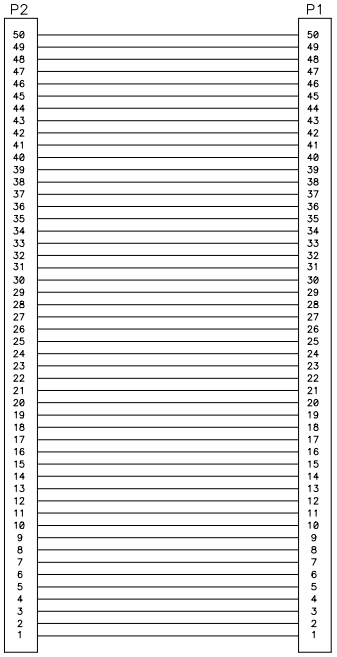
1. RS-485 IS CONSIDERED A BALANCED (DIFFERENTIAL) TRANSMISSION STANDARD BECAUSE THE VOLTAGE OF ONE SIGNAL LINE IS TAKEN WITH RESPECT TO ANOTHER TO DETERMINE THE SIGNAL LEVEL.
2. NOTE THAT ONE PAIR OF WIRES IS USED FOR BOTH TRANSMIT AND RECEIVE. AS SUCH, ONLY HALF-DUPLEX OPERATION IS POSSIBLE.
3. NOTE THAT ONLY ONE SET OF NETWORK BIAS RESISTORS SHOULD EXIST PER NETWORK WIRE PAIR. MODEL IP512 BOARDS HAVE THESE RESISTORS INSTALLED IN SOCKETS ON THE BOARD.

RS-485 CONNECTOR (IP512)

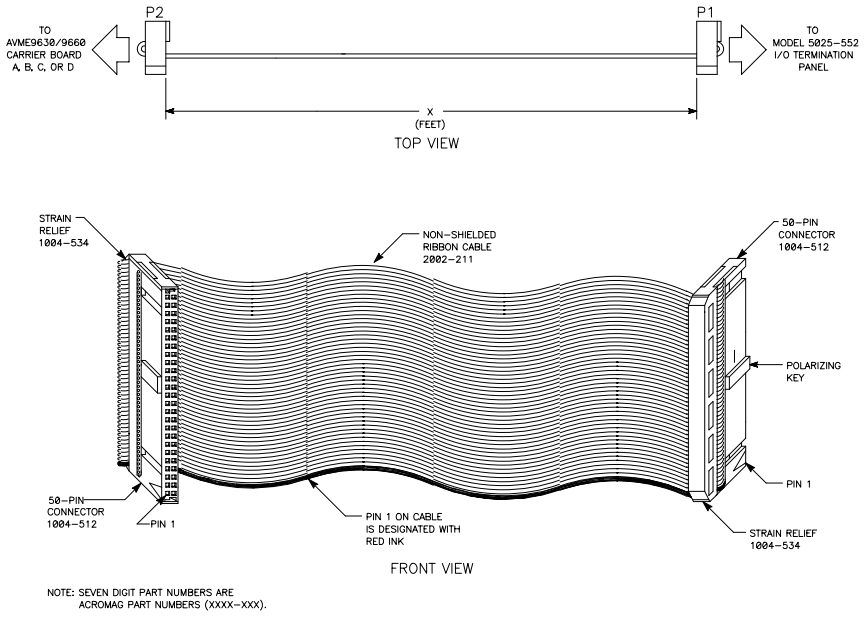


SEE ACROMAG CABLE MODEL 5029-943

4501-589A

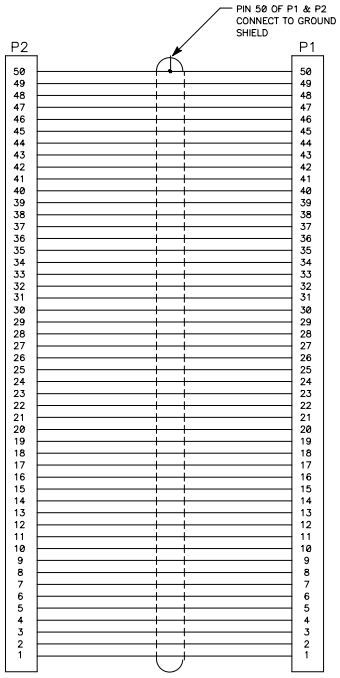


MODEL 5025-550-x SCHEMATIC

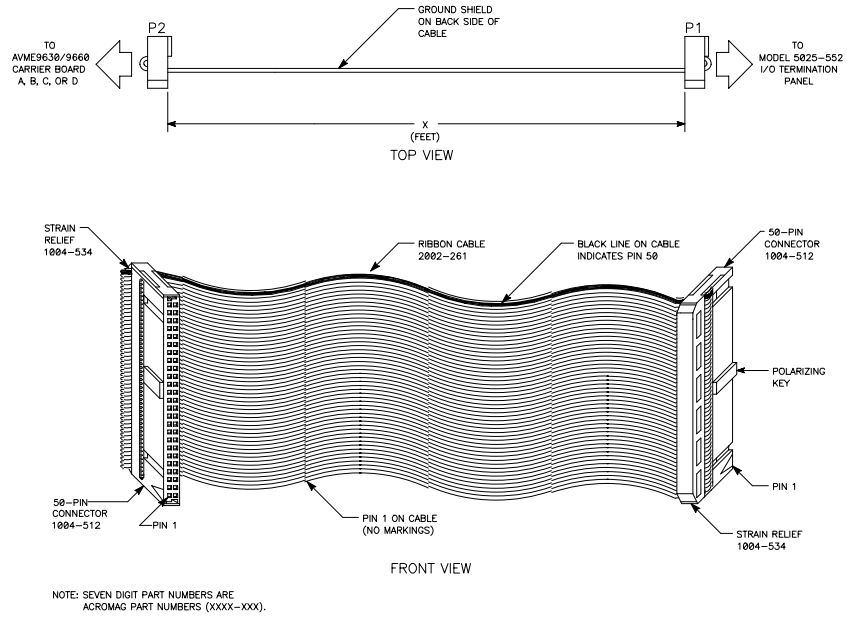


MODEL 5025-550-x SIGNAL CABLE, NON-SHIELDED

4501-462A

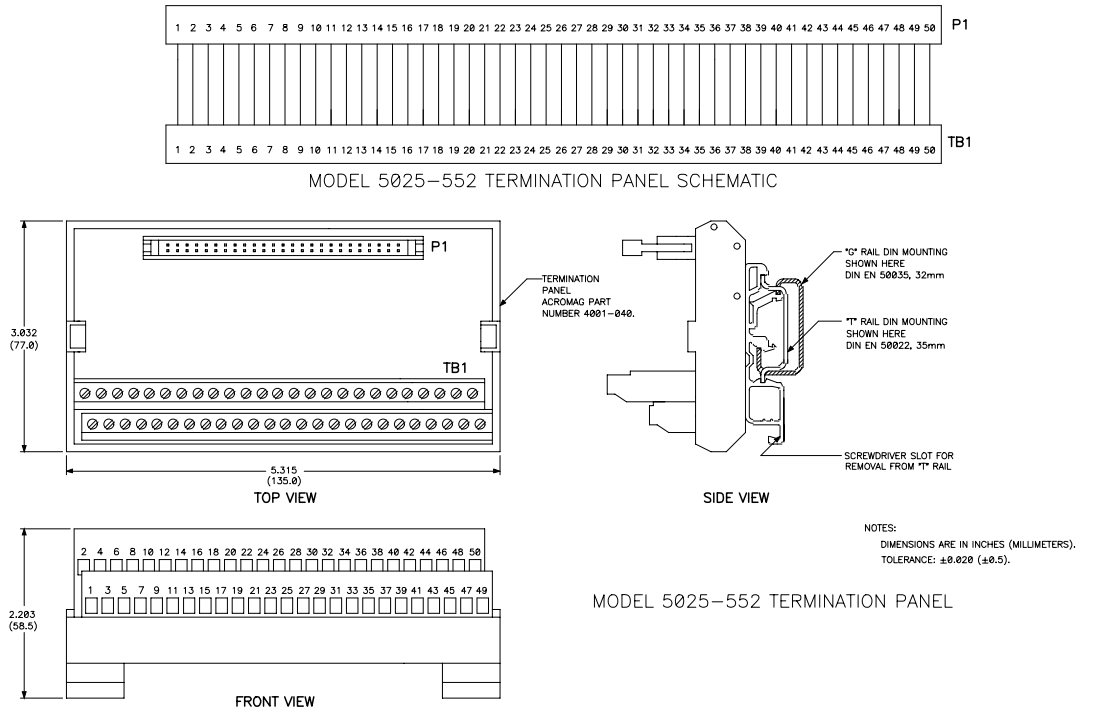


MODEL 5025-551-x SCHEMATIC

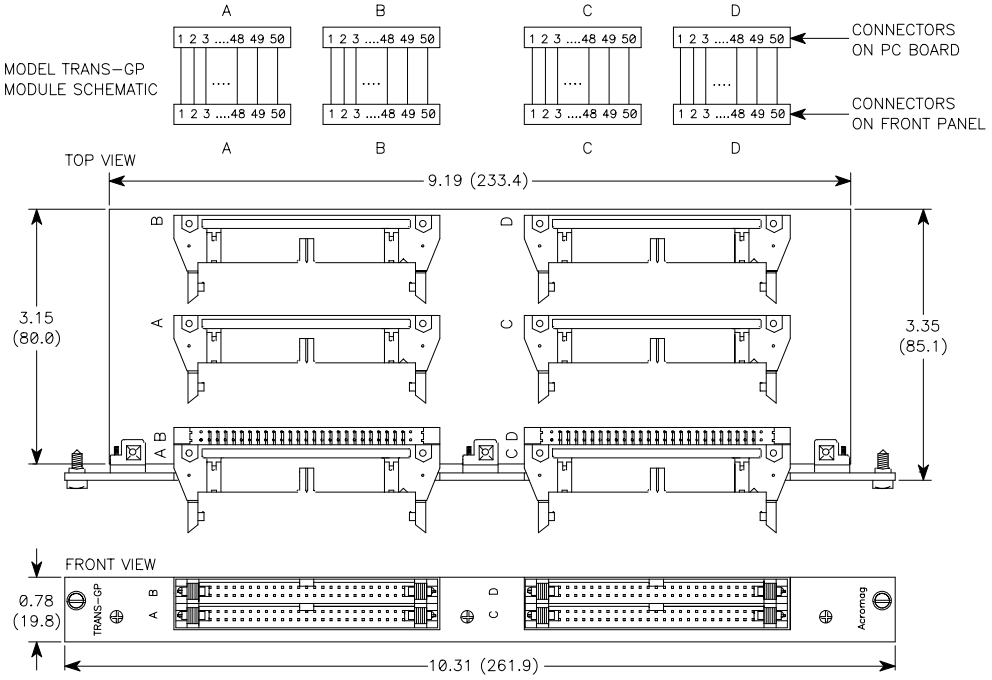


MODEL 5025-551-x SIGNAL CABLE, SHIELDED

4501-463A



4501-464A



TRANS-GP MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC

NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).

4501-465A