Series IP500A Industrial I/O Pack
Quad EIA/TIA-232E Communication Module

USER'S MANUAL

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Table of Contents

IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP500A module provides four EIA/TIA-232E serial communication ports for interfacing to the VMEbus or ISAbus, according to your carrier board. Four units may be mounted on a carrier board to provide up to 16 asynchronous serial ports per system slot.

The transmit and receive paths of each channel include generous 16-byte FIFO buffers to minimize CPU interaction. Full EIA/TIA-232E DB-9 signal support for dial-up and modem control is included. Character size, stop bits, parity, and baud rate are software configurable. Prioritized interrupt generation is also supported for transmit, receive, line status, and data set conditions. The IP500A utilizes state of the art Surface-Mounted Technology (SMT) to achieve its wide functionality and is an ideal choice for a wide range of industrial communication interface applications that require a highly reliable, high-performance interface at a low cost.

KEY IP500A FEATURES

- **High Density** - Provides programmable control of four EIA/TIA-232E serial ports. Four units mounted on a carrier board provide 16 serial channels in a single VMEbus or PCI bus (PC) system slot.
- **16-Character FIFO Buffers -** Both the transmit and receive channels of each serial port provide 16-byte (plus 3 bits per byte) data buffering to reduce CPU interactions and interrupts.
- **Programmable Character Size -** Each serial port is software programmable for 5, 6, 7, or 8 bit character sizes.
- **Programmable Stop Bits -** Each serial port allows 1, 1-1/2, or 2 stop-bits to be added to, or deleted from, the serial data stream**.**
- **Programmable Parity Generation & Detection** - Even, Odd, or No Parity generation and detection is supported**.**
- **Line-Break Generation & Detection -** provision for sending and detecting the line break character is provided.
- **False Start Bit Detection -** Prevents the receiver from assembling false data characters due to low-going noise spikes on the RxD input line.
- **Programmable Baud Rate -** The internal baud rate generator allows the 8MHz clock to be divided by any divisor between 1 and $2^{(16-1)}$, providing support for any bit rate up to 128Kbps.
- **Interrupt Support -** Individually controlled transmit, receive, line status, and data set interrupts may be generated. Unique interrupt vectors may be assigned to each port. Interrupt generation uses a priority shifting scheme based on the last interrupt serviced, preventing the continuous interrupts of one port from freezing out the interrupts of another port.
- **Individual Modem Control Signals** - Each serial channel includes a modem-control and modem-status register and provides full EIA/TIA-232E modem line support, including RTS, CTS, DTR, DSR, DCD, and RI.

- **Internal Diagnostic Capabilities** - Loopback controls for communication link fault isolation are included. Break, parity, overrun, and framing error simulation is also possible.
- **Industry Standard 16550 Family UART w/16C450 Mode** - The UART of this device is a member of the industry standard 16550 family of UART's and remains software compatible. Additionally, this device can operate in a 16C450 UART family software compatible mode. The transmit and receive channels are double-buffered in this mode. Hold and shift registers eliminate the need for precise synchronization between the host CPU and the serial data.

INDUSTRIAL I/O PACK INTERFACE FEATURES

- **High density -** Single-size, industry standard, IP module footprint. Four units mounted on a carrier board provide up to 16 serial ports in a single system slot. Both VMEbus and PCI bus (PC) carriers are supported.
- **Local ID** - Each IP module has its own 8-bit ID PROM which is accessed via data transfers in the "ID Read" space.
- **8-bit I/O** - Port register Read/Write is performed through 8-bit data transfer cycles in the IP module I/O space.
- **High Speed** - Access times for all data transfer cycles are described in terms of "wait" states - 1 wait state is required for reading and writing channel data, 2 wait states for interrupt select cycles, and 0 wait state for reading the ID PROM (see the Specifications section for detailed information).

SIGNAL INTERFACE PRODUCTS
(See Appendix for more information on compatible products)

This IP module will mate directly to any industry standard IP carrier board (including Acromag's AVME9630/9660 3U/6U non-intelligent VMEbus carrier boards). Additionally, PC carrier boards are also supported (see the Acromag Model APC8620A/8621A PCIbus carrier board). A wide range of other Acromag IP modules are available to serve your signal conditioning and interface needs.

Note: Since all connections to field signals are made through the carrier board which passes them to the individual IP modules, you should consult the documentation of your carrier board to ensure compatibility with the following interface products.

Cables:
Model 5025-551-X (Shielded Cable) or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting carrier boards, to Model 5025-552 termination panels. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications. The cables are available in 4, 7, or 10 feet lengths. Custom lengths (12 feet maximum) are available upon request.

Termination Panels:
Model 5025-552: A DIN-rail mountable panel that provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9630/9660, or other compatible carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).
100

Transition Module:
Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from a VMEbus card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. It connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within the card cage, via flat 50-pin ribbon cable (cable Model 5025-550 or 5025-551).

IP MODULE Win32 DRIVER SOFTWARE

Acromag provides a software product (sold separately) to facilitate the development of Windows (98/Me/2000/XP®) applications accessing Industry Pack modules installed on Acromag PCI Carrier Cards and CompactPCI Carrier Cards. This software (Model IPSW-API-WIN) consists of low-level drivers and Windows 32 Dynamic Link Libraries (DLLS) that are compatible with a number of programming environments including Visual C++, Visual Basic, Borland C++ Builder and others. The DLL functions provide a high-level interface to the carriers and IP modules eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

IP MODULE VXWorks SOFTWARE

Acromag provides a software product (sold separately) consisting of board VxWorks® software. This software (Model IPSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all Acromag IP modules and carriers including the AVME9670, AVME9660/9630, APC8620A/21A, ACPC8630/35, and ACPC8625. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag PCI boards.

IP MODULE QNX SOFTWARE

Acromag provides a software product (sold separately) consisting of board QNX® software. This software (Model IPSW-API-QNX) is composed of QNX® (real time operating system) libraries for all Acromag IP modules and carriers including the AVME9670, AVME9660/9630, APC8620A/21A, ACPC8630/35, and ACPC8625. The software supports X86 PCI bus only and is implemented as library of "C" functions. These functions link with existing user code to make possible simple control of all Acromag IP modules and carriers.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static-sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Most, if not all, computer chassis do not provide a fan for cooling of add-in boards. The dense packing of the IP modules to the carrier board alone results in elevated IP module and carrier board temperatures, and the restricted air flow within the chassis aggravates this problem. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-434 and your IP module documentation for configuration and assembly instructions. The Model IP500A communication board has no hardware jumpers that require configuration. The jumpers on the board are for factory use only and the user should not adjust the default settings. The correct setting is to have two jumpers covering both leads of the four pin header.

CONNECTORS

IP Field I/O Connector (P2)

P2 provides the field I/O interface connections for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly. P2 pin assignments are unique to each IP model (see Table 2.1) and normally correspond to the pin numbers of the field I/O interface connector on the carrier board (you should verify this for your carrier board).

Note that the pin-wire assignments are arranged such that IDC D-SUB ribbon cable connectors can be conveniently attached to provide serial port A (pins 1-9), serial port B (pins 10-18), serial port C (pins 26-34), & serial port D (pins 35-43) connectivity. In Table 2.1, a suffix of "_A", "_B", "_C", or "_D" is appended to each pin label to denote its port association. A brief description of each of the serial port signals at P2 is included in Table 2.2. A complete functional description of all P2 pin functions is included in Section 4.0 (Theory of Operation). Be careful not to confuse the A-D port designations of the IP module with the IP carrier board A-D slot designations.

Table 2.1: IP500A Field I/O Pin Connections (P2)

Pin Description	Number	Pin Description	Number
COMMON	1	COMMON	26
RI_A*	2	RI_C*	27
DTR_A*	3	DTR_C*	28
CTS_A*	4	CTS_C*	29
TXD_A	5	TXD_C	30
RTS_A*	6	RTS_C*	31
RXD_A	7	RXD_C	32
DSR_A*	8	DSR_C *	33
1DCD_A*	9	DCD_C*	34
COMMON	10	COMMON	35
RI_B*	11	RI_D*	36
DTR_B*	12	DTR_D*	37
CTS_B*	13	CTS_D*	38
TXD_B	14	TXD_D	39
RTS_B*	15	RTS_D*	40
RXD_B	16	RXD_D	41
DSR_B*	17	DSR_D*	42
DCD_B*	18	DCD_D*	43
COMMON	19	COMMON	44
COMMON	20	COMMON	45
COMMON	21	COMMON	46
COMMON	22	COMMON	47
COMMON	23	COMMON	48
COMMON	24	COMMON[1]	49
COMMON	25	COMMON	50

An Asterisk (*) is used to indicate an active-low signal.
1. This pin has a dual purpose and is used during factory programming. The pin function is controlled by the board jumper which must not be changed from the default setting.

Table 2.2: P2 Pin Signal Descriptions

SIGNAL	DESCRIPTION
DCD_A* DCD_B* DCD_C* DCD_D*	Data Carrier Detect - An active low signal that indicates the carrier has been detected by the modem. The status of this signal is read via bit 7 of the Modem Status Register.
DSR_A* DSR_B* DSR_C* DSR_D*	Data Set Ready - A modem status signal to indicate that it is connected to the line (it has no effect on the transmit or receive operation). The status of this signal is read via bit 5 of the Modem Status Register.
RxD_A RxD_B RxD_C RxD_D	Receive Data Line Input - This is the receive data input line. During Loopback Mode, the RxD input is disabled from the external connection and connected to the TxD output internally.
TxD_A TxD_B TxD_C TxD_D	Transmit Data Line Output - This is the transmit output data line. In the idle state, this signal line is held in the mark (logic 1) state. During Loopback Mode, the TxD output is internally connected to the RxD input.
RTS_A* RTS_B* RTS_C* RTS_D*	Request-to-Send Output - The RTS output is turned on to tell the modem it is ready to send data. This signal has no effect on the transmit or receive operation. This signal can be set low (active) by writing a 1 to the Modem Control Register.

Table 2.2: P2 Pin Signal Descriptions...continued

SIGNAL	DESCRIPTION
DTR_A* DTR_B* DTR_C* DTR_D*	Data Terminal Ready Output - used to signal a modem or data set to indicate equipment readiness to establish communications. Placed in the active state by setting bit 0 of the Modem Control Register. The DTR output is placed in the inactive (high) state either as a result of a system reset during loop mode operation, or by resetting bit 0 (DTR*) of the Modem Control Register.
CTS_A* CTS_B* CTS_C* CTS_D*	Clear-to-Send Input - Turned on by the receiving device to indicate it is ready to receive data. The input status of this signal can be read via bit 4 of the Modem Status Register. CTS has no effect on the transmit or receive operation.
RI_A* RI_B* RI_C* RI_D*	Ring Detect Indicator Input - When the receiving device receives a call (auto-answer), RI is switched on and off in sequence with the phone ringer to signal that a call is present and a remote modem is requesting a dial-up connection. The status of this signal can be read via bit 6 of the Modem Status Register.

Noise and Grounding Considerations

The serial channels of this module are non-isolated and share a common signal ground connection. Further, the IP500A is non-isolated between the logic and field I/O grounds since signal common is electrically connected to the IP module ground. Consequently, the field interface connections are not isolated from the carrier board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

The signal ground connection at the communication ports are common to the IP interface ground, which is typically common to safety (chassis) ground when mounted on a carrier board and inserted in a backplane. As such, be careful not to attach signal ground to safety ground via any device connected to these ports, or a ground loop will be produced, and this may adversely affect operation.

The communication cabling of the P2 interface carries digital data at a high transfer rate. For best performance, increased signal integrity, and safety reasons, you should isolate these connections away from power and other wiring to avoid noise-coupling and crosstalk interference. Historically, RS-232 communication distances were generally limited to less than 50 feet. Actual distance limits are set by the EIA/TIA-232E driver load capacitance limit (2500pF). In any case, interface cabling and ground wiring should always be kept as short as possible for best performance. Please refer to Drawing 4501-548 for example connections.

IP Logic Interface Connector (P1)

P1 of the IP module provides the logic interface to the mating connector on the carrier board. This connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly. The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.2).

Table 2.2: Standard Logic Interface Connections (P1)

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSEL*	29
D01	5	***DMAReq0****	30
D02	6	MEMSEL*	31
D03	7	***DMAReq1****	32
D04	8	IntSel*	33
D05	9	***DMAck0****	34
D06	10	IOSEL*	35
D07	11	**RESERVED**	36
D08	12	A1	37
D09	13	***DMAEnd****	38
D10	14	A2	39
D11	15	**ERROR***	40
D12	16	A3	41
D13	17	INTReq0*	42
D14	18	A4	43
D15	19	***INTReq1****	44
BS0*	20	A5	45
BS1*	21	***STROBE****	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	**RESERVED**	49
GND	25	GND	50

An Asterisk (*) is used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by this IP Model.
Bold Underlined Logic Lines are Reserved for Factory Use Only.

3.0 PROGRAMMING INFORMATION

ADDRESS MAPS

This board is addressable in the Industrial Pack I/O space to control the interface configuration, data transfer, and steering logic of four EIA/TIA-232E serial ports. As such, three types of information are stored in the I/O space: control, status, and data. These registers are listed below along with their mnemonics used throughout this manual.

SERIAL DATA REGISTERS (Per Serial Port):	
RBR	Receive Buffer Register
THR	Transmitter Holding Register
SERIAL STATUS REGISTERS (Per Serial Port):	
LSR	Line Status Register
MSR	Modem Status Register
SERIAL CONTROL REGISTERS (Per Serial Port):	
LCR	Line Control Register
FCR	FIFO Control Register
MCR	Modem Control Register
DLL	Divisor Latch LSB
DLM	Divisor Latch MSB
IER	Interrupt Enable Register
SCR	Scratch Pad/Interrupt Vector Register

The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1..A6, but the IP500A uses only a portion of this space. The I/O space address map for the IP500A is shown in Table 3.1. Note the base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space. All accesses are performed on an 8-bit word basis (D0..D7).

This manual is presented using the “Big Endian” byte ordering format. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses. Thus, byte accesses are done on odd address locations. The Intel x86 family of microprocessors use the opposite convention, or “Little Endian” byte ordering. Little Endian uses even-byte addresses to store the low-order byte. As such, use of this module on a PC carrier board will require the use of the even address locations to access the 8-bit data, while a VMEbus carrier requires the use of odd address locations.

Note that some functions share the same register address. For these items, the address lines are used along with the divisor latch access bit (bit 7 of the Line Control Register) and/or the read and write signals to determine the function required. Beyond the first two address locations for each serial port, the state of the divisor latch access bit is irrelevant.

Table 3.1: IP500A I/O Space Address (Hex) Memory Map

Base Addr+	MSB D15 D08	LSB D07 D00	LCR Bit7	Base Addr+
Serial Port A Registers:				
00	Not Driven[1]	READ - RBR Port A Receiver Buffer Register	0	**01**
00	Not Driven[1]	WRITE - THR Port A Transmitter Holding Register	0	**01**
00	Not Driven[1]	R/W - DLL Port A Divisor Latch LSB	1	**01**
02	Not Driven[1]	R/W - IER Port A Interrupt Enable Register	0	**03**
02	Not Driven[1]	R/W - DLM Port A Divisor Latch MSB	1	**03**
Base Addr+	**MSB D15 D08**	**LSB D07 D00**		**Base Addr+**
Serial Port A Registers:				
04	Not Driven[1]	READ - IIR Port A Interrupt Ident. Reg.		**05**
04	Not Driven[1]	WRITE - FCR Port A FIFO Control Reg.		**05**
06	Not Driven[1]	R/W - LCR Port A Line Control Register		**07**
08	Not Driven[1]	R/W - MCR Port A Modem Control Reg.		**09**
0A	Not Driven[1]	R/W - LSR Port A Line Status Register		**0B**
0C	Not Driven[1]	R/W - MSR Port A Modem Status Reg.		**0D**
0E	Not Driven[1]	R/W - SCR Port A Scratch Pad/Interrupt Vector Register		**0F**

Table 3.1: IP500A I/O Space Address (Hex) Memory Map

Base Addr+	MSB D15 D08	LSB D07 D00	LCR Bit7	Base Addr+
Serial Port B Registers:				
10	Not Driven[1]	READ - RBR Port B Receiver Buffer Register	0	**11**
10	Not Driven[1]	WRITE - THR Port B Transmitter Holding Register	0	**11**
10	Not Driven[1]	R/W - DLL Port B Divisor Latch LSB	1	**11**
12	Not Driven[1]	R/W - IER Port B Interrupt Enable Register	0	**13**
12	Not Driven[1]	R/W - DLM Port B Divisor Latch MSB	1	**13**
Base Addr+	**MSB D15 D08**	**LSB D07 D00**		**Base Addr+**
14	Not Driven[1]	READ - IIR Port B Interrupt Ident. Reg.		**15**
14	Not Driven[1]	WRITE - FCR Port B FIFO Control Reg.		**15**
16	Not Driven[1]	R/W - LCR Port B Line Control Register		**17**
18	Not Driven[1]	R/W - MCR Port B Modem Control Reg.		**19**
1A	Not Driven[1]	R/W - LSR Port B Line Status Register		**1B**
1C	Not Driven[1]	R/W - MSR Port B Modem Status Reg.		**1D**
1E	Not Driven[1]	R/W - SCR Port B Scratch Pad/Interrupt Vector Register		**1F**
Serial Port C Registers:				
Base Addr+	**MSB D15 D08**	**LSB D07 D00**	**LCR Bit7**	**Base Addr+**
20	Not Driven[1]	READ - RBR Port C Receiver Buffer Register	0	**21**
20	Not Driven[1]	WRITE - THR Port C Transmitter Holding Register	0	**21**
20	Not Driven[1]	R/W - DLL Port C Divisor Latch LSB	1	**21**
22	Not Driven[1]	R/W - IER Port C Interrupt Enable Register	0	**23**
22	Not Driven[1]	R/W - DLM Port C Divisor Latch MSB	1	**23**
Base Addr+	**MSB D15 D08**	**LSB D07 D00**		**Base Addr+**
24	Not Driven[1]	READ - IIR Port C Interrupt Identification Register		**25**
24	Not Driven[1]	WRITE - FCR Port C FIFO Control Register		**25**

Table 3.1: IP500A I/O Space Memory Map...continued

Base Addr+	MSB D15 D08	LSB D07 D00	LCR Bit7	Base Addr+
Serial Port C Registers:				
26	Not Driven[1]	R/W - LCR Port C Line Control Register		**27**
28	Not Driven[1]	R/W - MCR Port C Modem Control Reg.		**29**
2A	Not Driven[1]	R/W - LSR Port C Line Status Register		**2B**
2C	Not Driven[1]	R/W - MSR Port C Modem Status Reg.		**2D**
2E	Not Driven[1]	R/W - SCR Port C Scratch Pad/ Interrupt Vector Register		**2F**
Serial Port D Registers:				
Base Addr+	**MSB D15 D08**	**LSB D07 D00**	**LCR Bit7**	**Base Addr+**
30	Not Driven[1]	READ - RBR Port D Receiver Buffer Register	0	**31**
30	Not Driven[1]	WRITE - THR Port D Transmitter Holding Register	0	**31**
30	Not Driven[1]	R/W - DLL Port D Divisor Latch LSB	1	**31**
32	Not Driven[1]	R/W - IER Port D Interrupt Enable Register	0	**33**
32	Not Driven[1]	R/W - DLM Port D Divisor Latch MSB	1	**33**
Base Addr+	**MSB D15 D08**	**LSB D07 D00**		**Base Addr+**
34	Not Driven[1]	READ - IIR Port D Interrupt Ident. Reg.		**35**
34	Not Driven[1]	WRITE - FCR Port D FIFO Control Reg.		**35**
36	Not Driven[1]	R/W - LCR Port D Line Control Register		**37**
38	Not Driven[1]	R/W - MCR Port D Modem Control Reg.		**39**
3A	Not Driven[1]	R/W - LSR Port D Line Status Register		**3B**
3C	Not Driven[1]	R/W - MSR Port D Modem Status Reg.		**3D**
3E	Not Driven[1]	R/W - SCR Port D Scratch Pad/ Interrupt Vector Register		**3F**
40 ↓ 7E	NOT USED[2]			**41 ↓ 7F**

Notes (Table 3.1):

1. The upper 8 bits of these registers are not driven. Pullups on the carrier data bus will cause these bits to read high (1's).
2. The IP will not respond to addresses that are "Not Used".
3. All Reads and Writes have 1 wait states, while ID PROM reads have 0 wait state.

This board operates in two different modes. In one mode, this device remains software compatible with the industry standard 16C450 family of UART's and provides double-buffering of data registers. In the FIFO Mode (enabled via bit 0 of the FCR register), data registers are FIFO-buffered so that read and write operations can be performed while the UART is performing serial-to-parallel and parallel-to-serial conversions. Two FIFO modes are possible: FIFO Interrupt Mode and FIFO Polled Mode. Some registers operate differently between the available modes and this is noted in the following paragraphs.

RBR - Receiver Buffer Register, Ports A-D (READ Only)

The Receiver Buffer Register (RBR) is a serial port input data register that receives the input data from the receiver shift register and holds from 5 to 8 bits of data, as specified by the character size programmed in the Line Control Register (LCR bits 0 & 1). If less than 8 bits are transmitted, then data is right-justified to the LSB. If parity is used, then LCR bit 3 (parity enable) and LCR bit 4 (type of parity) are required. Status for the receiver is provided via the Line-Status Register (LSR). When a full character is received (including parity and stop bits), the data-received indication bit (bit 0) of the LSR is set to 1. The host CPU then reads the Receiver Buffer Register, which resets LSR bit 0 low. If the character is not read prior to a new character transfer between the receiver shift register and the receiver buffer register, the overrun-error status indication is set in LSR bit 1. If there is a parity error, the error is indicated in LSR bit 2. If a stop bit is not detected, a framing error indication is set in bit 3 of the LSR.

Serial asynchronous data is input to the receiver shift register via the receive data line (RxD). From the idle state, this line is monitored for a high-to-low transition (start bit). When the start bit is detected, a counter is reset and counts the 16x clock to 7-1/2 (which is the center of the start bit). The start bit is judged valid if RxD is still low at this point. This is known as false start-bit detection. By verifying the start bit in this manner, it helps to prevent the receiver from assembling an invalid data character due to a low-going noise spike on RxD. If the data on RxD is a symmetrical square wave, the center of the data cells will occur within ±3.125% of the actual center (providing an error margin of 46.875%). Thus, the start bit can begin as much as one 16x clock cycle prior to being detected.

THR - Transmitter Holding Register, Ports A-D (WRITE Only)

The Transmitter Holding Register (THR) is a serial port output data register that holds from 5 to 8 bits of data, as specified by the character size programmed in the Line Control Register. If less than 8 bits are transmitted, then data is entered right-justified to the LSB. This data is framed as required, then shifted to the transmit data line (TxD). In the idle state, TxD is held high. In Loopback Mode, this data is looped back into the Receiver Buffer Register.

DLL & DLM - Divisor Latch Registers, Ports A-D (R/W)

The Divisor Latch Registers form the divisor used by the internal baud-rate generator to divide the 8MHz system clock to produce an internal sampling clock suitable for synchronization to the desired baud rate. The output of the baud generator (RCLK) is sixteen times the baud rate. Two 8-bit divisor latch registers per port are used to store the divisors in 16-bit binary format. The DLL register stores the low-order byte of the divisor; DLM stores the high-order byte. These registers must be loaded during initialization.

Note that bit 7 of the LCR register must first be set high to access the divisor latch registers (DLL & DLM) during a read/write operation.

Upon loading either latch, a 16-bit baud counter is immediately loaded (this prevents long counts on initial load). The clock may be divided by any divisor from 1 to $2^{(16-1)}$. The output frequency of the baud rate generator (RCLK) is 16x the data rate. The relationship between the output of the baud generator (RCLK), the baud rate, the divisor, and the 8MHz system clock can be summarized in the following equations:

DIVISOR = CLOCK FREQUENCY ÷ [BAUD RATE x 16]
RCLK = 16 x BAUD RATE
= 16 x [CLOCK ÷ (16 x DIVISOR)] = CLOCK ÷ DIVISOR

The following table shows the correct divisor to use for generation of some standard baud rates (based on the 8MHz clock). Note that baud rates up to 512K may be configured, but the EIA/TIA-232E drivers of this module limits data rates to 128Kbps maximum for performance within rated specifications. However, limited performance at 256Kbps and 512Kbs is possible, but not recommended or guaranteed. Provisions for the installation of an external crystal have been provided on the circuit board, allowing for custom baud rates. *See Appendix: Model 4860A-X* for further information on custom crystal frequencies.

Table 3.2: Baud Rate Divisors and Relative Error (8MHz Clk)

BAUD RATE DESIRED	DIVISOR (N) USED FOR 16x CLOCK		% ERROR DIFF BET DESIRED & ACTUAL
50	10000	2710H	0
75	6667	1A06H	0.005
110	4545	11C1H	0.010
134.5	3717	0E85H	0.013
150	3333	0D05H	0.010
300	1667	0683H	0.020
600	833	0341H	0.040
1200	417	01A1H	0.080
1800	277	0115H	0.080
2000	250	00FAH	0
2400	208	00D0H	0.160
3600	139	0086H	0.080
4800	104	0068H	0.160
7200	69	0045H	0.644
9600	52	0034H	0.160
19200	26	001AH	0.160
38400	13	000DH	0.160
56000	9	0009H	0.790
128000	4	0004H	2.344
256000	2	0002H	2.344
512000	1	0001H	2.400

SHADED entries are not recommended due to driver limitations.

With respect to this device, the baud rate may be considered equal to the number of bits transmitted per second (bps). The bit rate (bps), or baud rate, defines the bit time. This is the length of time a bit will be held on before the next bit is transmitted. A receiver and transmitter must be communicating at the same bit rate, or data will be garbled. A receiver is alerted to an incoming character by the start bit, which marks the beginning of the character. It then times the incoming signal, sampling each bit as near to the center of the bit time as possible.

To better understand the asynchronous timing used by this device, note that the receive data line (RxD) is monitored for a high-to-low transition (start bit). When the start bit is detected, a counter is reset and counts the 16x sampling clock to 7-1/2 (which is the center of the start bit). The receiver then counts from 0 to 15 to sample the next bit near its center, and so on, until a stop bit is detected, signaling the end of the data stream. Use of a sampling rate 16x the baud rate reduces the synchronization error that builds up in estimating the center of each successive bit following the start bit. As such, if the data on RxD is a symmetrical square wave, the center of each successive data cell will occur within ±3.125% of the actual center (this is 50% ÷ 16, providing an error margin of 46.875%). Thus, the start bit can begin as much as one 16x clock cycle prior to being detected.

IER - Interrupt Enable Register, Ports A-D (R/W)

The Interrupt Enable Register is used to independently enable/ disable the four possible serial channel interrupt sources that drive the INTREQ0* line (Ports A-D share this line). Interrupts are disabled by resetting the corresponding IER bit low (0), and enabled by setting the IER bit high (1). Disabling the interrupt system (IER bits 0-3 low) also inhibits the Interrupt Identification Register (IIR) and the interrupt request line (INTREQ0*). All other functions operate in their normal manner, including the setting of the Line Status Register (LSR) and the Modem Status Register (MSR).

Interrupt Enable Register

IER BIT	INTERRUPT ACTION
0	Received Data Available Interrupt Enable and Time-Out Interrupt (FIFO Mode) Enable
1	Transmitter Holding Register Empty Interrupt Enable
2	Receiver Line Status Interrupt Enable
3	Modem Status Interrupt Enable
4-7	Not Used - Set to Logic 0

A power-up or system reset sets all IER bits to 0 (bits 0-3 forced low, bits 4-7 permanently low).

IIR - Interrupt Identification Register, Ports A-D (READ Only)

The Interrupt Identification Register is used to indicate that a prioritized interrupt is pending and the type of interrupt that is pending. This register will indicate the highest-priority interrupt pending. Individual serial channels prioritize their interrupts into four levels (indicated below). This helps minimize software overhead during data character transfers. Additionally, with respect to the four individual channels sharing INTREQ0, interrupt vectors are served according to a shifting priority scheme that is a function of the last interrupting port served.

PRIORITY/LEVEL	INTERRUPT
1	Receiver Line Status
2	Received Data Ready or Character Time-out
3	Transmitter Holding Register Empty
4	Modem Status

The four lower order bits of this register are used to identify the interrupt pending as follows:

Interrupt Identification Register

BITS 3-0	INT. PRTY	INT. TYPE	INTERRUPT SOURCE	RESET CONTROL
0001	--	None	None	--
0110	1st	Receiver Line Status	OE, PE, FE, or BI (See LSR Bits 1-4)	LSR Read
0100	2nd	Received Data Available	Receiver Data Available or Trigger Level Reached	RBR Read till FIFO below trigger level
1100	2nd	Character Time-out Indication	No characters have been removed from or input to the Rx FIFO during last 4 character times & there is at least 1 character in it during this time.	RBR Read
0010	3rd	THRE (LSR Bit 5)	THRE (LSR Bit 5)	IIR Read (if LSR bit 5 is the interrupt source) or a THR Write
0000	4th	Modem Status	CTS*, DSR*, RI*, or DCD* asserted	MSR Read

Note that IIR bit 0 can be used to indicate whether an interrupt is pending (bit 0 low when interrupt is pending). IIR bits 1 & 2 are used to indicate the highest priority interrupt pending. IIR bit 3 is always logic 0 in the 16C450 mode. IIR bit 3 is set along with bit 2 when in the FIFO mode and a timeout interrupt is pending.

Bits 4 and 5 of this register are always set to 0. Bits 6 and 7 are set when bit 0 of the FIFO Control Register is set to 1. A power-up or system reset sets IIR bit 0 to 1, bits 1,2,3,6, and 7 to 0, while bits 4 & 5 are permanently low.

FCR - FIFO Control Register, Ports A-D (WRITE Only)

This write-only register is used to enable and clear the FIFO buffers, set the trigger level of the Rx FIFO, and select the type of DMA signaling (DMA is NOT supported by this model).

FIFO Control Register

FCR BIT	FUNCTION
0	When set to "1", this bit enables both the Tx and Rx FIFO's. All bytes in both FIFO's can be cleared by resetting this bit to 0. Data is cleared automatically from the FIFO's when changing from FIFO mode to the alternate (16C450) mode and visa-versa. Programming of other FCR bits is enabled by setting this bit to 1.
1	When set to "1", this bit clears all bytes in the Rx-FIFO and the resets counter logic to 0 (this does not clear the shift register).
2	When set to "1", this bit clears all bytes in the Tx-FIFO and resets the counter logic to 0 (this does not clear the shift register).
3	When set to "1", this bit sets DMA Signal from Mode 0 to Mode 1, if FIFO Control Register Bit 0 = 1 (DMA Not Supported)
4,5	Not Used

FIFO Control Register...continued

FCR BIT	FUNCTION
6,7	Used for setting the trigger level of the Rx FIFO interrupt as follows: BIT 7-6 Rx-FIFO TRIGGER LEVEL 00 01 Bytes 01 04 Bytes 10 08 Bytes 11 14 Bytes

A power-up or system reset sets all FCR bits to 0.

LCR - Line Control Register, Ports A-D (Read/Write)

The individual bits of this register control the format of the data character as follows:

Line Control Register

LCR Bit	FUNCTION	PROGRAMMING
1 and 0	Word Length Sel.	0 0 = 5 Data Bits 0 1 = 6 Data Bits 1 0 = 7 Data Bits 1 1 = 8 Data Bits
2	Stop Bit Select	0 = 1 Stop Bit 1 = 1.5 Stop Bits if 5 data bits; 2 Stop Bits if 6, 7, or 8 data bits selected.
3	Parity Enable	0 = Parity Disabled 1 = Parity Enabled A parity bit is generated and checked for between the last data word bit and the stop bit.
4	Even-Parity Select	0 = Odd Parity, 1 = Even Parity
5	Stick Parity	0 = Disabled, 1 = Enabled When parity is enabled, stick parity causes the transmission and reception of a parity bit to be in the opposite state from the value selected via bit 4. This is used as a diagnostic tool to force parity to a known state and allow the receiver to check the parity bit in a known state.
6	Break Control	0 = Break Disabled, 1 = Break Enabled When break is enabled, the serial output line (TxD) is forced to the space state (low). This bit acts only on the serial output and does not affect transmitter logic. For example, if the following sequence is used, no invalid characters are transmitted due to the presence of the break. 1. Load a zero byte in response to the Transmitter Holding Register Empty (THRE) status indication. 2. Set the break in response to the next THRE status indication. 3. Wait for the transmitter to become idle when the Transmitter Empty status signal is set high (TEMT=1); then clear the break when normal transmission has to be restored.
7	Divisor Latch Access Bit	0 = Access Receiver Buffer 1 = Allow Access to Divisor Latches

Note that bit 7 must be set high to access the divisor latch registers DLL & DLM of the baud rate generator during a read/write operation. Bit 7 must be low to access the Receiver Buffer Register (RBR), the Transmitter Holding Register (THR), or the Interrupt Enable Register (IER). A power-up or system reset sets all LCR bits to 0.

A detailed discussion of word length, stop bits, parity, and the break signal is included in Section 4.0 (Theory of Operation).

MCR - Modem Control Register, Ports A-D (R/W)

The Modem Control register controls the interface with the modem or data set as described below. The RTS and DTR outputs are directly controlled by their control bits in this register (a high input asserts these signals).

Modem Control Register

MCR Bit	FUNCTION	PROGRAMMING
0	Data Terminal Ready Output Signal (DTR)	0 = DTR* Not Asserted (Inactive) 1 = DTR* Asserted (Active)
1	Request to Send Output Signal (RTS)	0 = RTS* Not Asserted (Inactive) 1 = RTS* Asserted (Active)
2	Out1 (Internal)	No Effect on External Operation
3	Out2 (Internal)	0 = External Serial Channel Interrupt Disabled 1 = External Serial Channel Interrupt Enabled
4	Loop[1]	0 = Loop Disabled 1 = Loop Enabled
5,6,7	Not Used	Bits are set to logic 0

Notes (Modem Control Register):

1. MCR Bit 4 provides a local loopback feature for diagnostic testing of the UART channel. When set high, the UART serial output (connected to the TXD driver) is set to the marking (logic 1 state), and the UART receiver serial data input is disconnected from the RxD receiver path. The output of the UART transmitter shift register is then looped back into the receiver shift register input. The four modem control inputs (CTS,DSR, DCD, and RI) are disconnected from their receiver input paths. The four modem control outputs (DTR, RTS, OUT1, and OUT2) are internally connected to the four modem control inputs (while their associated pins are forced to their high/ inactive state). Thus, in the loopback diagnostic mode, transmitted data is immediately received permitting the host processor to verify the transmit and receive data paths of the selected serial channel. In this mode, interrupts are generated by controlling the state of the four lower order MCR bits internally, instead of by the external hardware paths. However, no interrupt requests or interrupt vectors are actually served in loopback mode, and interrupt pending status is only reflected internally.

A power-up or system reset sets all MCR bits to 0 (bits 5-7 are permanently low).

LSR - Line Status Register, Ports A-D (Read/Write-Restricted)

The Line Status Register (LSR) provides status indication corresponding to the data transfer. LSR bits 1-4 are the error conditions that produce receiver line-status interrupts (a priority 1 interrupt in the Interrupt Identification Register). The line status register may be written, but this is intended for factory test and should be considered read-only by the applications software.

Line Status Register

LSR Bit	FUNCTION	PROGRAMMING
0	Data Ready (DR)	0 = Not Ready (reset low by CPU Read of RBR or FIFO) 1 = Data Ready (set high when character received and transferred into the RBR or FIFO).
1	Overrun Error (OE)	0 = No Error 1 = Indicates that data in the RBR is not is not being read before the next character is transferred into the RBR, overwriting the previous character. In the FIFO mode, it is set after the FIFO is filled and the next character is received. The overrun error is detected by the CPU on the first LSR read after it happens. The character in the shift register is not transferred into the FIFO, but is overwritten. This bit is reset low when the CPU reads the LSR.
2	Parity Error (PE)	0 = No Error 1 = Parity Error - the received character does not have the correct parity as configured via LCR bits 3 & 4. This bit is set high on detection of a parity error and reset low when the host CPU reads the contents of the LSR. In the FIFO mode, the parity error is associated with a particular character in the FIFO (LSR Bit 2 reflects the error when the character is at the top of the FIFO).
3	Framing Error (FE)	0 = No Error 1 = Framing Error - Indicates that the received character does not have a valid stop bit (stop bit following last data bit or parity bit detected as a zero/space bit). This bit is reset low when the CPU reads the contents of the LSR. In FIFO mode, the framing error is associated with a particular character in the FIFO (LSR Bit 3 reflects the error when the character is at the top of the FIFO).

Line Status Register...continued

LSR Bit	FUNCTION	PROGRAMMING
4	Break Interrupt (BI)	0 = No Break 1 = Break - the received data input has been held in the space (logic 0) state for more than a full-word transmission time (start bits+ data+ parity bit+ stop bits). Reset upon read of LSR. In FIFO mode, this bit is associated with a particular character in the FIFO and reflects the Break Interrupt when the break character is at the top of the FIFO. It is detected by the host CPU during the first LSR read. Only one "0" character is loaded into the FIFO when BI occurs
5	Transmitter Holding Register Empty (THRE)	0 = Not Empty 1 = Empty - indicates that the channel is ready to accept a new character for transmission. Set high when character is transferred from the THR into the transmitter shift register. Reset low by loading the THR (It is not reset by a host CPU read of the LSR). In FIFO mode, this bit is set when the Tx FIFO is empty and cleared when one byte is written to the Tx FIFO. When a Transmitter Holding Register Empty interrupt is enabled by IER bit 1, this signal causes a priority 3 interrupt in the IIR. If the IIR indicates that this signal is causing the interrupt, the interrupt is cleared by a read of the IIR.
6	Transmitter Empty (TEMT)	0 = Not Empty 1 = Transmitter Empty - set when both the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. Reset low when a character is loaded into the THR and remains low until the character is transmitted (it is not reset low by a read of the LSR). In FIFO mode, this bit is set when both the transmitter FIFO and shift register are empty.
7	Receiver FIFO Error	0 = No Error in FIFO (it is always 0 in 16C450 mode--FCR bit 0 low). 1 = Error in FIFO - set when one of the following data errors is present in the FIFO: parity error, framing error, or break interrupt indication. Cleared by a host CPU read of the LSR if there are no subsequent errors in the FIFO.

Note that LSR Bits 1-4 (OE, PE, FE, BI) are the error conditions that produce a receiver-line-status interrupt (a priority 1 interrupt in the IIR register when any one of these conditions is detected). This interrupt is enabled by setting IER bit 2 to 1.

A power-up or system reset sets all LSR bits to 0, except bits 5 and 6 which are high.

MSR - Modem Status Register, Ports A-D (Read/Write)

The Modem Status Register (MSR) provides the host CPU with an indication on the status of the modem input lines from a modem or other peripheral device. This register allows the current state of the four modem input lines (CTS, DSR, RI, and DCD) to be read (bits 4-7) and provides indication on whether the states of these lines have changed since the last read of the MSR (bits 0-3 are set high when the corresponding control inputs from the modem changes state and are reset low when the CPU reads the MSR).

Modem Status Register

MSR BIT	FUNCTION
0	ΔCTS (Set if CTS has changed states since last read of MSR)
1	ΔDSR (Set if DSR has changed states since last read of MSR)
2	ΔRI (Trailing Edge Only - Indicates RI* input to the serial channel has changed state from Low-to-High since last read of MSR). Not affected by High-to-Low RI* transitions.
3	ΔDCD (Set if DCD has changed states since last read of MSR)
4	CTS - the complement of the CTS* input from the modem indicating that the modem is ready to receive data. If the channel is in the loopback mode (MCR bit 4 = 1), then the state of RTS in the MCR is reflected
5	DSR - the complement of the DSR* input from the modem indicating that the modem is ready to provide received data to the serial channel receiver circuitry. In Loopback mode (see MCR bit 4 description), the state of DTR in the MCR is reflected.
6	RI - the complement of the RI* input from the modem. In Loopback mode (see MCR bit 4 description), this bit reflects the state of OUT1 in the MCR.
7	DCD - the current status of the DCD* input from the modem (a "1" indicates DCD* asserted). In Loopback mode (see MCR bit 4 description), this bit reflects the value of OUT2 in the MCR.

An Asterisk (*) is used to indicate an active-low signal.

Note that reading MSR clears the delta-modem status indications (bits 0-3), but has no effect on the other status bits. For both the LSR & MSR, the setting of the status bits during a status register read operation is inhibited (the status bit will not be set until the trailing edge of the read). However, if the same status condition occurs during a read operation, that status bit is cleared on the trailing edge of the read instead of being set again.

In Loopback Mode, when the modem status interrupts are enabled, the CTS*, DSR*, RI*, and DCD* inputs are ignored. However, a modem status interrupt can still be generated by writing to MCR bits 3-0 (see Loopback Mode Operation section).

A power-up or system reset sets MSR bits 0-3 to 0 (bits 4-7 are determined by the corresponding input signals).

SCR - Scratch Pad Register, Ports A-D (Read/Write)

This 8-bit read/write register has no effect on the operation of either serial channel. It is provided as an aide to the programmer to temporarily hold data. Alternately, it stores the interrupt vector for the port.

If interrupt generation is desired, then this port is used to store the interrupt vector for the port. In response to an interrupt select cycle, the IP module will execute a read of this register for the interrupting port (see Interrupt Generation section for more details).

IP Identification PROM - (Read Only, 32 Odd-Byte Addresses)

Each IP module contains an identification (ID) PROM that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID PROM. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP500A ID PROM does not contain any variable (e.g. unique calibration) information. ID PROM bytes are addressed using only the odd addresses in a 64 byte block (on the “Big Endian” VMEbus). Even addresses are used on the “Little Endian” PC/AT ISAbus. The IP500A ID PROM contents are shown in Table 3.2. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID PROM. Execution of an ID PROM Read requires 1 wait state.

Table 3.2: IP500A ID Space Identification (ID) PROM

Hex Offset From ID PROM Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All IP's have 'IPAC'
03	P	50	
05	A	41	
07	C	43	
09		A3	Acromag ID Code
0B		04	IP Model Code[1]
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		0C	Total Number of ID PROM Bytes
17		86	CRC
19 to 3F		00	Not Used

Notes (Table 3.2):

1. The IP model number is represented by a two-digit code within the ID PROM (the IP500A model is represented by 04 Hex).

THE EFFECT OF RESET

A software or hardware reset puts the serial channels into an idle-mode until initialization (programming). A reset initializes the receiver and transmitter clock counters. It also clears the Line-Status Register (LSR), except for the transmitter shift-register empty (TEMT) and transmit holding-register empty (THRE) bits which are set to 1 (note that when interrupts are subsequently enabled, an interrupt will occur due to THRE being set). The Modem Control Register (MCR) is also cleared. All of the discrete signal lines, memory elements, and miscellaneous logic associated with these register bits are cleared, de-asserted, or turned off. However, the Line Control Register (LCR), divisor latches, Receiver Buffer Register (RBR), and Transmitter Holding Register (THR) are not affected. The following table summarizes the effect of a reset on the various registers and internal and external signals:

REG/SIGNAL	RESET CTRL	STATE/EFFECT
REGISTERS:		
IER	Reset	All Bits low (Bits 0-3 forced low, Bits 4-7 permanently low)
IIR	Reset	Bit 0 high, Bits 1,2,3,6,7 low, Bits 4 & 5 permanently low
LCR	Reset	All bits low
MCR	Reset	All bits low (bits 5-7 permanently low)
FCR	Reset	All bits low
LSR	Reset	All bits low, except bits 5 & 6 are high
MSR	Reset	Bits 0-3 low, bits 4-7 per corresponding input signal
SIGNALS (INTERNAL & EXTERNAL):		
TxD	Reset	High
Interrupt (RCVR errors)	Read LSR/ Reset	Low
Interrupt (RCVR data ready)	Read RCVR Buffer Register/ Reset	Low
Interrupt (THRE)	Read IIR/Write THR/Reset	Low
Interrupt (Modem Status Changes)	Read MSR/ Reset	Low
RTS*	Reset	High
DTR*	Reset	High
OUT1*	Reset	High
OUT2*	Reset	High

IP500A PROGRAMMING

Each serial channel of this module is programmed by the control registers: LCR, IER, DLL, DLM, MCR, and FCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface. The control registers can be written in any order, but the IER register should be written last since it controls the interrupt enables. The contents of these registers can be updated any time the serial channel is not transmitting or receiving data.

The complete status of each channel can be read by the host CPU at any time during operation. Two registers are used to report the status of a particular channel: the Line Status Register (LSR) and the Modem Status Register (MSR).

Serial channel data is read from the Receiver Buffer Register (RBR), and written to the Transmitter Holding Register (THR). Writing data to the THR initiates the parallel-to-serial transmitter shift register to the TxD line. Likewise, input data is shifted from the RxD pin to the Receiver Buffer Register as it is received.

The Scratchpad Register is used to store the interrupt vector for the port. In response to an interrupt select cycle, the IP module will provide a read of this port. As such, each port may have a unique interrupt vector assigned. Interrupts are served in a shifting-priority fashion as a function of the last interrupting port serviced to prevent continuous interrupts from a higher-priority interrupt channel from freezing out service of a lower priority channel.

This board operates in two different modes. In one mode, this device remains software compatible with the industry standard 16C450 family of UART's, and provides double-buffering of data registers. In the FIFO Mode (enabled via bit 0 of the FCR register), data registers are FIFO-buffered so that read and write operations can be performed while the UART is performing serial-to-parallel and parallel-to-serial conversions.

Two FIFO modes of operation are possible: FIFO Interrupt Mode and FIFO Polled Mode. In FIFO Interrupt Mode, data transfer is initiated by reaching a pre-determined trigger-level or generating time-out conditions. In FIFO-Polled Mode, there is no time-out condition indicated or trigger-level reached. The transmit and the receive FIFO's simply hold characters and the Line Status Register must be read to determine the channel status.

Acromag provides an Industrial I/O Pack Software Library diskette (Model IPSW-LIB-M03, MSDOS format) to simplify communication with the board. Example software functions are provided for both personal computer and VMEbus applications. All functions are written in the "C" programming language and can be linked to your application. For more details, refer to the "README.TXT" file in the root directory on the diskette and the "INFO500A.TXT" file in the appropriate "IP500A" subdirectory off of "\VMEIP" or "\PCIP", according to your carrier.

FIFO Polled-Mode

Resetting Interrupt Enable Register Bit 0, Bit 1, Bit 2, Bit 3, or all four to 0, with FIFO Control Register (FCR) Bit 0 =1, puts the channel into the polled-mode of operation. The receiver and transmitter are controlled separately and either one or both may be in the polled mode. In FIFO-Polled Mode, there is no time-out condition indicated or trigger-level reached, the transmit and the receive FIFO's simply hold characters and the Line Status Register must be read to determine the channel status.

FIFO-Interrupt Mode

In FIFO Interrupt Mode, data transfer is initiated by reaching a pre-determined trigger-level or generating a time-out condition. Please note the following with respect to this mode of operation.

When the receiver FIFO and receiver interrupts are enabled, the following receiver status conditions apply:

1. LSR Bit 0 is set to 1 when a character is transferred from the shift register to the receiver FIFO. It is reset to 0 when the FIFO is empty.
2. The receiver line-status interrupt (IIR=06) has a higher priority than the received data-available interrupt (IIR=04).
3. The receive data-available interrupt is issued to the CPU when the programmed trigger level is reached by the FIFO. It is cleared when the FIFO drops below its programmed trigger level. The receive data-available interrupt indication (IIR=04) also occurs when the FIFO reaches its trigger level, and is cleared when the FIFO drops below its trigger level.

When the receiver FIFO and receiver interrupts are enabled, the following receiver FIFO character time-out status conditions apply:

1. A FIFO character time-out interrupt occurs if:
   - A minimum of one character is in the FIFO.
   - The last received serial character is longer than four continuous prior character times ago (if 2 stop bits are programmed, the second one is included in the time delay).
   - The last CPU read of the FIFO is more than four continuous character times earlier. At 300 baud, and with 12-bit characters, the FIFO time-out interrupt causes a latency of 160ms maximum from received character to interrupt issued.
2. From the clock signal input, the character times can be calculated. The delay is proportional to the baud rate.
3. The time-out timer is reset after the CPU reads the receiver FIFO or after a new character is received when there has been no time-out interrupt.
4. A time-out interrupt is cleared and the timer is reset when the CPU reads a character from the receiver FIFO.

When the transmit FIFO and transmit interrupts are enabled (FCR Bit 0 = 1 and IER=01), a transmitter interrupt will occur as follows:

1. When the transmitter FIFO is empty, the transmitter holding register interrupt (IIR=02) occurs. The interrupt is cleared when the Transmitter Holding Register (THR) is written to or the Interrupt Identification Register (IIR) is read. One to sixteen characters can be written to the transmit FIFO when servicing this interrupt.
2. The transmit FIFO empty indications are delayed one character time minus the last stop bit time when the following occurs:
   Bit 5 of the LSR (THRE) is 1 and there is not a minimum of two bytes at the same time in the transmit FIFO since the last time THRE=1. The first transmitter interrupt after changing FCR Bit 0 is immediate, assuming it is enabled.

The receiver FIFO trigger level and character time-out interrupts have the same priority as the received data-available interrupt. The Transmitter Holding-Register Empty interrupt has the same priority as the Transmitter FIFO-Empty interrupt.

Loopback Mode Operation

This device can be operated in a "loopback mode", useful for troubleshooting a serial channel without physically wiring to the channel. Bit 4 of the Modem Control Register (MCR) is used to program the local loopback feature for the UART channel. When set high, the UART channel's serial output line (Transmit Data Path) is set to the marking (logic 1 state), and the UART receiver serial data input lines are disconnected from the RxD receiver path. The output of the UART transmitter shift register is then looped back into the receiver shift register input. Thus, a write to the Transmitter Holding Register is automatically looped back to the corresponding Receiver Buffer Register. Additionally, the four modem control inputs (CTS, DSR, DCD, and RI) are disconnected from their receiver input paths. With modem status interrupts enabled in the Loopback Mode, the CTS*, DSR*, RI*, and DCD* inputs are ignored. Instead, the four modem control outputs (DTR, RTS, OUT1, and OUT2 of the MCR Register) are internally connected to the corresponding four modem control inputs (monitored via the Modem Status Register), while their associated pins are forced to their high/inactive state. Thus, in loopback diagnostic mode, transmitted data is immediately received permitting the host processor to verify the transmit and receive data paths of the selected serial channel. Further, modem status interrupt generation is controlled manually in loopback mode by controlling the state of the four lower order MCR bits internally, instead of by the external hardware paths.

Interrupt Generation

This model provides individual control for generation of transmit, receive, line status, and data set interrupts on each of four channels. Each channel shares interrupt request line 0 (Intreq0) according to a unique priority shifting scheme that prevents the continuous interrupts of one channel from freezing out another channels' interrupt requests.

After pulling the IntReq0 line low and in response to an Interrupt Select cycle, the current highest priority interrupt channel will serve its interrupt vector first. Interrupt serving priority will shift as a function of the last port served. A unique interrupt vector may be assigned to each communication port and is loaded into the Scratchpad Register (SCR) for the port. The IP module will thus execute a read of the scratchpad register in response to an interrupt select cycle. Two wait states are required to complete this cycle.

Interrupt priority is assigned as follows. Initially, with no prior interrupt history, Port A has the highest priority and will be served first, followed by port B, followed by port C, then followed by port D. However, if port A was the last interrupt serviced, then port B will have the highest priority, followed by port C, followed by port D, then port A, in a last-serviced last-out fashion. Priority continues to shift in the same fashion if Port B or Port C was the last interrupt serviced. This is useful in preventing continuous interrupts on one channel from freezing out interrupt service for other channels.

Programming Example

The following example will demonstrate data transfer between one channel of the host IP500A and another node using an RTS/CTS protocol. Both nodes will use the FIFO Mode of operation with a FIFO threshold set at 14 bytes. The data format will use 8-bit characters, odd-parity, and 1 stop bit.

Please refer to Table 3.1 for address locations. The "H" following data below refers to the Hexadecimal format.

1. Write 80H to the Line Control Register (LCR).

   This sets the Divisor Latch Access bit to permit access to the two divisor latch bytes used to set the baud rate. These bytes share addresses with the Receive and Transmit buffers, and the Interrupt Enable Register (IER).

2. Write 00H to the Divisor Latch MSB (DLM). Write 34H to the Divisor Latch LSB (DLL).

   This sets the divisor to 52 for 9600 baud (i.e. 9600 = 8MHz ÷ [16*52]).

3. Write 0BH to the Line Control Register (LCR).

   This first turns off the Divisor Latch Access bit to cause accesses to the Receiver and Transmit buffers and the Interrupt Enable Register. It also sets the word length to 8 bits, the number of stop bits to one, and enables odd-parity.

4. (OPTIONAL) Write xxH to the Scratch Pad Register.

   This has no effect on the operation, but is suggested to illustrate that this register can be used as a 1-byte memory cell. Optionally, this register is also used to store the interrupt vector for the port.

5. Write 0FH to the Interrupt Enable Register (IER).

   This enables the modem status interrupts and the receiver line status interrupts. The modem status interrupt is used to signal changes in CTS* to handle the protocol. The line status interrupt is used to signal error cases, such as parity or overrun errors. The modem status interrupts are expected, but the line status interrupts are not. The received data available and transmit holding buffer empty interrupts have also been enabled to aide control by the host CPU in moving data back and forth.

6. Write C7H to the FIFO Control Register (FCR).

   This enables and initializes the transmit and receive FIFO's, and sets the trigger level of the receive FIFO interrupt to 14 bytes.

7. Read C1H from the Interrupt Identification Register (IIR).

   This is done to check that the device has been programmed correctly. The upper nibble "C" indicates that the FIFO's have been enabled and the lower nibble "1" indicates that no interrupts are pending.

8. Write 02H to the Modem Control Register (MCR).

   This sets the Request-To-Send bit and asserts the RTS* signal line. It is used to signal a receiver that the device is ready to transmit some data. Note the modem control lines, either input or output, have no effect on the parallel-to-serial output data or serial-to-parallel input data. These lines interact only through CPU control to provide the handshaking necessary for this data transfer protocol.

9. Read 11H from the Modem Status Register (MSR)

   This is an indication from the receiver that the Clear-To-Send signal has been asserted and that there has been a change in the CTS* signal since the last read of the MSR. Consequently, an interrupt will be generated on interrupt request line 0 (INTREQ0*) to signal the host CPU that it can begin loading data into the transmit buffer.

10. The host should acknowledge the interrupt to clear it, then begin writing data repeatedly to the Transmitter Holding Register.

    This loads the transmit FIFO and initiates transmission of serial data on the TxD line. The first serial byte will take about 100us to transmit, so it is likely that the transmit FIFO will fill before the first byte has been sent. The receiving side may release CTS* if it cannot keep up with the data stream. In this case, the host CPU would have to pause in loading the data to prevent lost data.

11. Stop loading the transmit buffer, then write 00H to the Modem Control Register (MCR).

    This clears the Request-To-Send bit and releases the RTS* signal line, signifying that transmission is complete.

12. Read 01H from the Modem Status Register (MSR).

    This indicates that the receiving side has released its Clear-To-Send (CTS*) signal in response to the transmitting side dropping its Request-To-Send signal (RTS*).

13. Read 22H from the Modem Status Register (MSR).

    This informs the host CPU that the Data-Set-Ready (DSR*) input line has been asserted, thus requesting that the host receiver accept data (the ΔDSR bit is also set indicating that the change in DSR is current).

14. Write 01H to the Modem Control Register (MCR).

    This indicates that the host receiver is ready to accept data by setting Data-Terminal-Ready (DTR*). The host CPU should be prepared to accept data before asserting DTR*.

15. Read data repeatedly from the Receiver Buffer Register.

    After 14 bytes have been received (or fewer bytes with a timeout), an interrupt will be generated if the host CPU has not unloaded the receive FIFO.

16. Read 02H from the Modem Status Register.

    The sending side indicates to the host receiver that it has completed sending data and is releasing the Data-Set-Ready (DSR*) signal.

17. Write 00H to the Modem Control Register

    The host receiver clears the Data-Terminal-Ready (DTR*) signal in response to Data-Set-Ready (DSR*) being dropped.

4.0 THEORY OF OPERATION

This section contains information regarding the EIA/TIA-232E serial data interface. A description of the basic functionality of the circuitry used on the board is also provided. Refer to the Block Diagram shown in Drawing 4501-549 as you review this material.

EIA/TIA-232E SERIAL INTERFACE

The Electronic Industries Association (EIA) first introduced the RS-232 standard in 1962 to standardize the serial binary data interface between Data Terminal Equipment (DTE) and Data Communication Equipment (DCE). By this definition, DTE is used to represent the data source, data sink, or both. DCE is used to represent the devices used to establish, maintain, and terminate a connection, and to code/decode the signals between the DTE and the transmission channel. Most computers are considered DTE devices, while modems are DCE devices.

The EIA/TIA-232E interface is the fifth revision of this standard and defines an unbalanced (single-ended) transmission standard for unidirectional (point-to-point, one direction at a time) data transmission. As unbalanced, this standard uses a voltage referenced to signal ground to denote the logical state of the data. A logic 0 is represented by a driven voltage between +5V and +15V (space), and a logic 1 by a driven voltage between -5V and -15V (mark). At the receiving end, a logic '0' is represented by a voltage between +3V and +15V (space), a logic '1' is represented by a voltage between -3V and -15V (mark). Voltages between ±3V are undefined and lie in the transition region. Note that at the interface, a logic '0' is represented by a high voltage, and a logic '1' by a low voltage. The line drivers and receivers invert these signals to the conventional TTL level associations.

EIA/TIA-232E SIGNAL	BINARY 0 (SPACE/OFF)	BINARY 1 (MARK/ON)
TRANSMIT	+5 to +15V DC	-5 to -15V DC
RECEIVE	+3 to +13V DC	-3 to -13V DC

Start and stop bits are used to synchronize the DCE to the asynchronous serial data of the DTE. The transmit data line is normally held in the mark state (logical 1). The transmission of a data byte requires that a start bit (a logical 0 or a transition from mark to space) be sent first. This tells the receiver that the next bit is a data bit. The data bits are followed by a stop bit (a logical 1 or a return to the mark state). The stop bit tells the receiver that a complete byte has been received. Thus, 10 bits make up a data byte if the data character is 8 bits long (and no parity is assumed). Nine bits are required if only standard ASCII data is being transmitted (1 start bit + 7 data bits + 1 stop bit). The character size for this module is programmable between 5 and 8 bits.

Parity is a method of judging the integrity of the data. Odd, even, or no parity may be configured for this module. If parity is selected, then the parity bit precedes transmission of the stop bit. The parity bit is a 0 or 1 bit appended to the data to make the total number of 1 bits in a byte even or odd. Parity is not normally used with 8-bit data. Even parity specifies that an even number of logical 1's be transmitted. Thus, if the data byte has an odd number of 1's, then the parity bit is set to 1 to make the parity of the entire character even. Likewise, if the transmitted data has an even number of 1's, then the parity bit is set to 0 to maintain even parity. Odd parity works the same way using an odd number of logical 1's.

Thus, both the DTE & DCE must have the same parity. If a byte is received that has the wrong parity, an error is assumed and the sending system is typically requested to retransmit the byte. Two other parity formats not supported by this module are mark and space parity. Mark parity specifies that the parity bit will always be a logical 1, space parity requires that the parity bit will always be 0.

The most common asynchronous serial data format is 1 start bit, 8 data bits, and 1 stop bit, with no parity. The following table summarizes the available data formats:

START BIT	Binary 0 (a shift from “Mark” to “Space”)
DATA BITS	5,6,7, or 8 Bits
PARITY	Odd, Even, or None
STOP BIT	Binary 1 (1, 1-1/2, or 2 Bit times)

With start, stop, and parity in mind, for an asynchronous data byte, note that at least one bit will be a 1 (the stop bit). This defines the break signal (all 0 bits with a 1 stop bit lasting longer than one character). A break signal is a transfer from “mark” to “space” that lasts longer than the time it takes to transfer one character. Because the break signal doesn’t contain any logical 1’s, it cannot be mistaken for data. Typically, whenever a break signal is detected, the receiver will interpret whatever follows as a command rather than data. The break signal is used whenever normal signal processing must be interrupted. In the case of a modem, it will usually precede a modem control command. Do not confuse the break signal with the ASCII Null character, since a break signal is longer than one character time. That is, it is any “space” condition on the line that lasts longer than a single character (including its framing bits) and is usually 1-1/2 to 2 character times long.

The baud rate is a unit of transmission speed equal to the number of electrical signals (signal level changes) sent on a line in one second. It is thus, the electrical signaling rate or frequency at which electrical impulses are transmitted on a communication line. The baud rate is commonly confused with the bit transfer rate (bits-per-second), but baud rate does not equate to the number of bits transmitted per second unless one bit is sent per electrical signal. However, one electrical signal (change in signal level) may contain more than one bit (as is the case with most phone modems). While bits-per-second (bps) refers to the actual number of bits transmitted in one second, the baud rate refers to the number of signal level changes that may occur in one second. Thus, 2400 baud does not equal 2400 bits per second unless 1 bit is sent per electrical signal. Likewise, a 1200bps or 2400bps modem operates at a signaling rate of only 600 baud since they encode 2 and 4 bits, respectively, in one electrical impulse (through amplitude, phase, and frequency modulation techniques). However, for this device, the baud rate is considered equivalent to the bit rate.

This module supports the common EIA/TIA-232E DB9 interface definition which is a subset of the full EIA/TIA-232E standard. This subset includes support of Data Carrier Detect (DCD), Data Set Ready (DSR), Receive Data Line (RxD), Request to Send (RTS), Transmit Data Line (TxD), Clear to Send (CTS), Data Terminal Ready (DTR), and Ring Indication (RI), plus signal ground. A complete DB9 DTE port would require 3 transmitters and 5 receivers, a complete DB9 DCE port would require 5 transmitters and 3 receivers. A DTE port will connect directly to a DCE port without swapping wires. However, a null-modem cable connection is required to connect two DTE ports due to the imbalance of drivers and receivers (see Drawing 4501-572).

Pins 1-18 and 26-43 of the field I/O connector P2 provides connectivity to serial Ports A-D of this module (Refer to Table 2.1 for pin assignments). Note that a suffix of ‘_A’, ‘_B’, ‘_C’, or ‘_D’ is appended to the signal names to indicate their port association. Each of these signals are described in detail below assuming that a local DTE device (PC) is connected to a local DCE device (modem) communicating over a telephone line to a remote DCE device (remote modem) connected to a remote DTE (another PC).

EIA/TIA-232E Signal Descriptions

SIGNAL	DESCRIPTION
DCD_A* DCD_B* DCD_C* DCD_D*	Data Carrier Detect (DCE-to-DTE) - This signal is driven by the DCE to inform the DTE that it is receiving a carrier signal. If it is held off locally, then it tells the local DTE that the remote DTE has not switched its RTS circuit on yet and the local DTE can gain control over the line if needed. If held on locally, then it tells the local DTE that the remote modem has received an RTS on condition from its remote DTE and the remote DTE is in control over the carrier line.
DSR_A* DSR_B* DSR_C* DSR_D*	Data Set Ready (DCE-to-DTE) - This signal is driven by the DCE to indicate to the DTE that it is connected to the line. Both modems turn DSR on to indicate that a communication path has been established between the local and remote modems.
RxD_A RxD_B RxD_C RxD_D	Receive Data Line (DCE-to-DTE) - This is the receive data line from the modem to the DTE. The signals on this line are in serial form. When DCD is held off, this line is held in the mark state.
TxD_A TxD_B TxD_C TxD_D	Transmit Data Line (DTE-to-DCE) - This is the transmit data line from the DTE to the modem. When no data is being transmitted, the signal line is held in the mark state. For data to be transmitted, DSR, DTR, RTS, and CTS must all be in the on state (asserted).
RTS_A* RTS_B* RTS_C* RTS_D*	Request-to-Send (DTE-to-DCE) - RTS is turned on by the DTE to tell the DCE it is ready to transmit data. This is also passed to the remote DCE. The DCE will turn CTS on in response to tell the DTE it is ready to receive data. As such, RTS acts to control the direction of data transmission. It is turned ON in transmit mode and turned OFF when transmission is completed or in receive mode (the DCE will turn CTS off in response).
DTR_A* DTR_B* DTR_C* DTR_D*	Data Terminal Ready (DTE-to-DCE) - DTR is used in conjunction with DSR to indicate equipment readiness. DTR is turned on by the DTE to tell the DCE it is ready to receive or transmit data. DTR must be on before the DCE can turn DSR on. By keeping DTR on, the DTE lets an auto-answer modem accept a call unattended. When DTR is turned off, the DCE is removed from the communication channel following completion of transmission and blocked from accepting calls from the remote DCE.
CTS_A* CTS_B* CTS_C* CTS_D*	Clear-to-Send (DCE-to-DTE) - CTS is turned on by the DCE to indicate it is ready to receive data from the DTE and the local modem has control over the telephone line. CTS is turned on in response to simultaneous on conditions of the RTS, DSR, and DTR signals.
RI_A* RI_B* RI_C* RI_D*	Ring Indicator (DCE-to-DTE) - When the modem receives a call (auto-answer), the DCE switches RI on and off in sequence with the phone ringer to tell the DTE that a call is present and a remote modem is requesting a dial-up connection.

An Asterisk (*) is used to indicate an active-low signal.

IP500A OPERATION

Connection to each serial port is provided through connector P2 (refer to Table 2.1). These pins are tied to the inputs and outputs of EIA/TIA-232E line receivers and drivers. The function of the line receivers is to convert the required EIA/TIA-232E signals to the TTL levels required by the UART (Universal Asynchronous Receiver/Transmitter). The line drivers convert the UART TTL levels to the EIA/TIA-232E voltage levels. The UART provides the necessary conversion from serial-to-parallel (receive) and parallel-to-serial (transmit) for interfacing to the data bus. Additionally, it provides data buffering and data formatting capabilities. A programmable logic device is used to control the interface between the UART, the IP bus, and the IDPROM.

Note that the field serial interface to the carrier board provided through connector P2 (refer to Table 2.1) is NON-ISOLATED. This means that the field signal return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage. Refer to Drawing 4501-548 for example communication wiring connections.

LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1 (refer to Table 2.2). Not all of the IP logic P1 pin functions are used. P1 also provides +5V & ±12V to power the module.

A programmable logic device installed on the IP Module provides the control signals required to operate the board. It decodes the selected addresses in the I/O and ID spaces and produces the chip selects, control signals, and timing required by the communication registers and ID PROM, as well as, the acknowledgement signal required by the carrier board per the IP specification. It also prioritizes the serving of port interrupts.

The ID PROM (read only) installed on the IP module provides the identification for the individual module per the IP specification. The ID PROM, configuration control registers, and FIFO buffers are all accessed through an 8-bit data bus interface to the carrier board.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation for Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Verify that there are no blown fuses. Replacement of the carrier and/or IP with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

Go to the “Support” tab to access:

- Application Notes
- Frequently Asked Questions (FAQ’s)
- Product Knowledge Base
- Tutorials
- Software Updates/Drivers

An email question can also be submitted from within the Knowledge Base or directly from the “Contact Us” tab.

Acromag’s application engineers can also be contacted directly for technical assistance via telephone or FAX through the numbers listed below. When needed, complete repair services are also available.

Phone: 248-295-0310
Fax: 248-624-9234
Email: solutions@acromag.com

6.0 SPECIFICATIONS

GENERAL SPECIFICATIONS

UART.....Texas Instruments TL16C554FN
Physical Configuration.....Single Industrial I/O Pack Module.
Length.....3.880 inches (98.5 mm).
Width.....1.780 inches (45.2 mm).
Board Thickness.....0.062 inches (1.59 mm).
Max Component Height.....0.314 inches (7.97 mm).
Connectors:
P1 (IP Logic Interface).....50-pin female receptacle header
& P2 (Field I/O) (AMP 173279-3 or equivalent).
Power:
+5 Volts (±5%) from P1.....200mA Typical; 300mA Maximum.
+12 Volts (±5%) from P1.....100mA Maximum.
-12 Volts (±5%) from P1.....100mA Maximum.

ENVIROMENTAL

Operating Temperature.....0 to +70°C.
Relative Humidity.....5-95% non-condensing.
Storage Temperature.....-55°C to +125°C.
Non-Isolated.....Logic and field commons have a direct electrical connection.
Radiated Field Immunity (RFI).....Complies with EN61000-4-3 (3V/m, 80 to 1000MHz AM & 900MHz. keyed) and European Norm EN50082-1 with no register upsets.
Conducted RF Immunity (CRFI)....Complies with EN61000-4-6 3V/rms, 150KHz to 80MHz) and European Norm EN50082-1 with no register upsets.
Electromagnetic Interference Immunity (EMI).....No digital upset under the influence of EMI from switching solenoids, commutator motors, and drill motors.
Electrostatic Discharge Immunity (ESD).....Complies with EN61000-4-2 Level 3 (8KV enclosure port air discharge) and Level 2 (4KV enclosure port contact discharge) and European Norm EN50082-1.
Surge Immunity.....Not required for signal I/O per European Norm EN50082-1.
Electric Fast Transient Immunity EFT..... Complies with EN61000-4-4 Level 2 (0.5KV at field I/O terminals) and European Norm EN50082-1.
Radiated Emissions..... Meets or exceeds European Norm EN50081-1 for class B equipment. Shielded cable with I/O connections in shielded enclosure are required to meet compliance.

EIA/TIA-232E PORTS

Configuration..... Four independent, non-isolated, EIA/TIA-232E serial ports with a common signal return connection.
Compatibility.....Compatible with EIA/TIA-232F communications standard.
Data Rate..... Programmable up to 128K bits per second using internal baud rate generator for rated performance. Data rates of 256Kbps and 512K bps may be programmed and communication is possible for some conditions at these rates, but performance is limited and not guaranteed at these rates.
Interface.....Asynchronous serial only.
Maximum Cable Length.....15M (50 feet) typical, limited to a cable capacitive load of 2500pF.
Character Size.....Software Programmable 5 to 8 bits.
Parity..... Software Programmable odd, even, or no parity.
Stop Bits.....Software Programmable 1, 1-1/2, or 2 bits.
Data Register Buffers.....The data registers are double-buffered (16C450 mode), or 16-byte FIFO buffered (FIFO mode).
Interrupts.....Receiver Line Status Interrupt (i.e. Overrun, Parity, or Framing error, or Break Interrupt); Received Data Available (FIFO level reached) or Character Time-Out; Transmitter Holding Register Empty; or Modem Status (CTS, DSR, RI, or DCD).

DRIVERS:

Output Voltage Swing.....±10V Typical, ±8V Minimum (Loaded with 3KΩ to ground).
Output Short Circuit Current.....±12mA Max, ±6mA Min.
Output Resistance.....300Ω Minimum.
Propagation Delay (Hi-to-Lo).....2us Max (R_L = 3KΩ, C_L = 50pF).
Propagation Delay (Lo-to-Hi).....2us Max (R_L = 3KΩ, C_L = 50pF).
Output Slew Rate (+3 to -3V)....4V/us Min to 30V/us Max (C_L = 50-2500pF, R_L = 3KΩ to 7KΩ).

RECEIVERS:

Data Rate.....Up to 128 Kbps.
Input Voltage Range.....±25V DC Maximum.
Input High Threshold.....1.55V Minimum, 2.4V Maximum.
Input Low Threshold.....0.65V Minimum, 1.35V Maximum.
Input Resistance.....3KΩ to 7KΩ.
Input Current.....3.6mA to 8.3mA (V_{IN} = ±15V); 0.43mA to 1mA (V_{IN} = ±3V).
Rise Time.....175ns Maximum.
Fall Time.....20ns Maximum.
Propagation Delay (High-to-Low)....50ns Maximum.
Propagation Delay (Low-to-High)....50ns Maximum.

INDUSTRIAL I/O PACK COMPLIANCE:

Specification.....This module meets or exceeds all written Industrial I/O Pack specifications per ANSI/VITA 4 1995 for 8MHz operation.
Electrical/Mechanical Interface...Single-Size IP Module.

I/O Space (IOSEL*).....8 bit read/write of all registers.
ID Space (IDSEL*).....8-bit: Supports Type 1, 32 bytes per IP (Consecutive odd byte address).
Interrupt Space (INTSEL*).....8-bit read of Scratch Pad/ Interrupt Vector Register Contents.

Access Times (8MHz Clock):
ID PROM Read.....0 wait states (250ns cycle).
Channel Register Read.....1 wait states (375ns cycle).
Channel Register Write.....1 wait states (375ns cycle).
Interrupt Select Cycle Read....2 wait states (500ns cycle).

APPENDIX

CUSTOM CRYSTAL: MODEL 4860A-X

This is a modified IP500A with an external crystal to provide a customer specified baud rate. The '-x' suffix designates the crystal frequency or desired baud rate. The standard crystal frequency provided with this module is 3.6864MHz (4860A-3.6864MHz). The table below shows the correct divisor to use for generation of some standard baud rates based on the 3.6864MHz clock. Contact Acromag for further details on this model or assistance in selecting a proper crystal frequency.

Table 7.1: Baud Rate Divisors and Relative Error with 3.6864MHz Clk

BAUD RATE DESIRED	DIVISOR (N) USED FOR 16x CLOCK		% ERROR
1800	768	0115H	0
2000	192	00FAH	0
2400	96	00D0H	0
3600	48	0086H	0
4800	32	0068H	0
9600	24	0045H	0
14400	16	0034H	0
19200	12	001AH	0
28800	8	000DH	0
38400	6	0009H	0
57600	4	0004H	0
115200	2	0002H	0

CABLE: MODEL 5025-550-x (Non-Shielded)
MODEL 5025-551-x (Shielded)

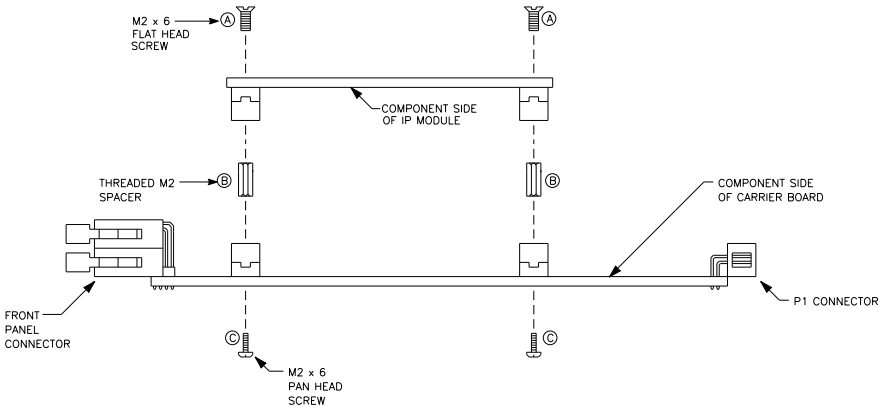
Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet. The cables are available in 4, 7, or 10 feet lengths. Custom lengths (12 feet maximum) are available upon request. Choose shielded or unshielded cable according to model number. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.
Application: Used to connect a Model 5025-552 termination panel to the AVME9630/9660 non-intelligent carrier board A-D connectors (both have 50-pin connectors).
Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50-wire flat ribbon cable, 28 gage. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent). Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).
Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).
Keying: Headers at both ends have polarizing key to prevent improper installation.
Schematic and Physical Attributes: For Non-Shielded cable model, see Drawing 4501-462. For Shielded cable model, see Drawing 4501-463.
Shipping Weight: 1.0 pound (0.5Kg) packaged.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel for AVME9630/9660 Boards
Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660/9668 3U/6U non-intelligent carrier boards (A-D connectors only) via a flat ribbon cable (Model 5025-550-x or 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Connections to AVME9630/9660/9668: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-550-x or 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight : 1.25 pounds (0.6kg) packaged.

TRANSITION MODULE: MODEL TRANS-GP

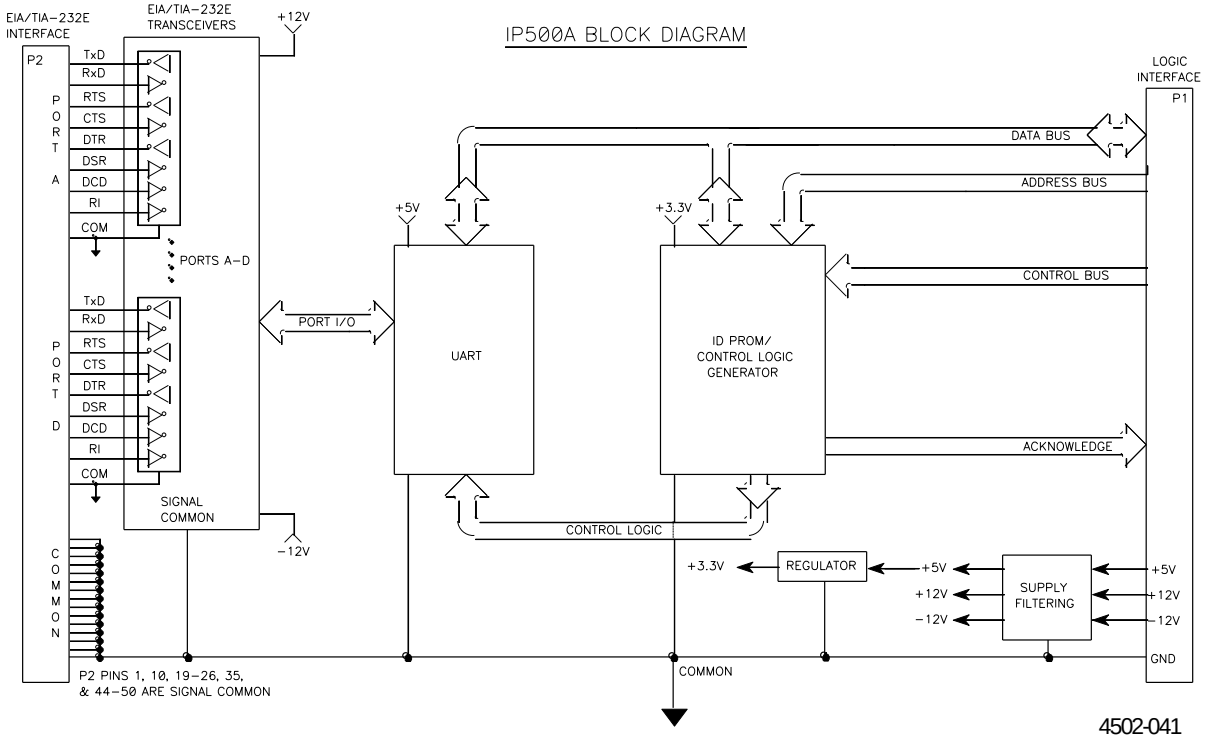
Type: Transition module for AVME9630/9660/9668 boards.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660/9668 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Schematic and Physical Attributes: See Drawing 4501-465.
Field Wiring: 100-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Connections to AVME9630/9660/9668: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660/9668 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Printed Circuit Board: Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +85°C.
Storage Temperature: -55°C to +105°C.
Shipping Weight: 1.25 pounds (0.6Kg) packaged.



ASSEMBLY PROCEDURE:

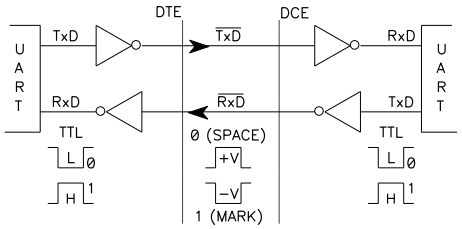
1. THREADED SPACERS ARE PROVIDED FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED. THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES). THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.

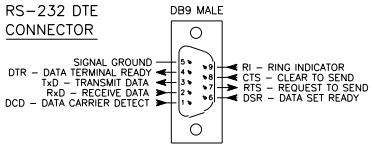
IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY 4501-434C



RS−232 INTERFACE LEVELS

1.) RS−232 DATA LINES (RxD, TxD)

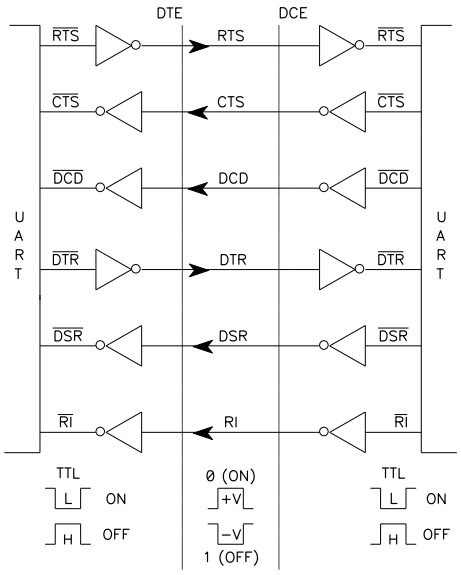




NOTE:

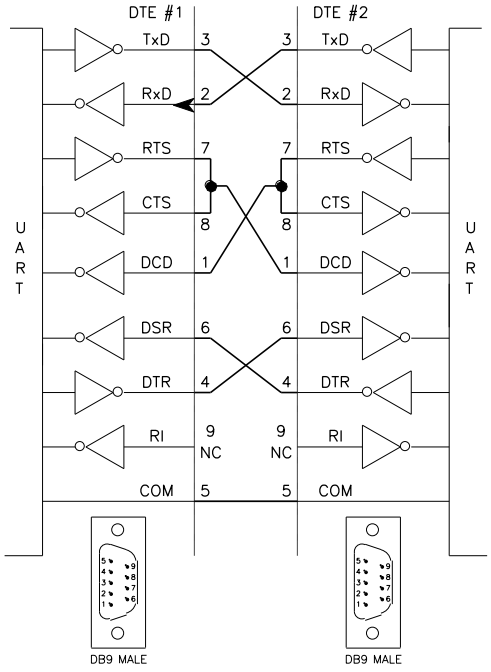
1. RS−232 IS CONSIDERED AN UNBALANCED (SINGLE−ENDED) TRANSMISSION STANDARD BECAUSE THE VOLTAGE OF ONE SIGNAL LINE IS TAKEN WITH RESPECT TO COMMON TO DETERMINE THE SIGNAL LEVEL.
2. NOTE THAT FOR RS−232, A LOGIC 0 (SPACE) IS REPRESENTED BY A POSITIVE VOLTAGE, WHILE A LOGIC 1 (MARK) IS REPRESENTED BY A NEGATIVE VOLTAGE AT THE INTERFACE.

2.) RS−232 HANDSHAKE LINES (RTS, CTS, DCD, DTR, DSR, RI)



4501−569

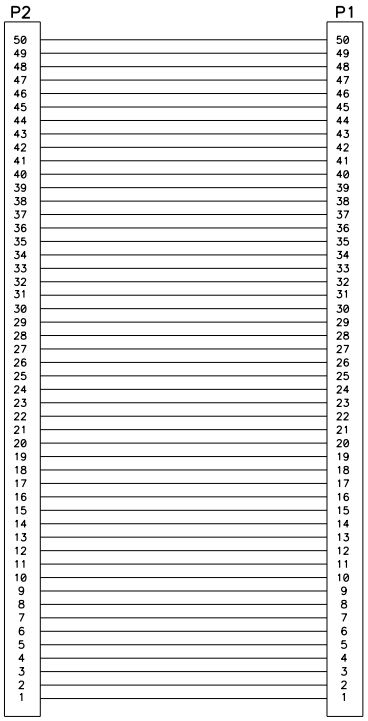
EIA/TIA−232E NULL MODEM CONNECTIONS FOR CONNECTING TWO DTE PORTS



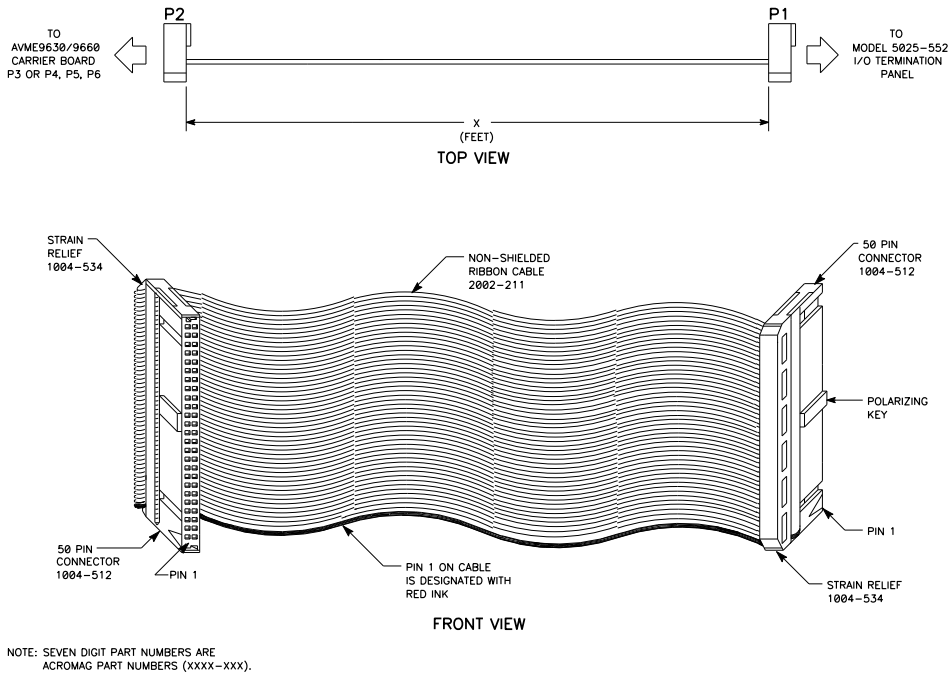
NOTE:

1. A DTE PORT CONNECTS DIRECTLY TO A DCE PORT WITHOUT SWAPPING WIRES. HOWEVER, A NULL MODEM CABLE CONNECTION IS REQUIRED TO CONNECT TWO LIKE−CONFIGURED DTE PORTS.
2. BECAUSE A DTE PORT HAS 3 DRIVING SIGNALS AND 5 RECEIVING SIGNALS, WHILE A DCE PORT HAS 3 RECEIVING SIGNALS AND 5 DRIVING SIGNALS, THEN A NULL MODEM CABLE CONNECTION MUST BE EMPLOYED TO CONNECT TWO DTE PORTS DUE TO THE IMBALANCE OF DRIVERS AND RECEIVERS.
3. NOTE THAT PINS 7 & 8 OF THE DB9 CONNECTOR ARE SHORTED TOGETHER AT EACH DTE AND DRIVE THE OTHER DTE'S DCD LINE.

4501−572

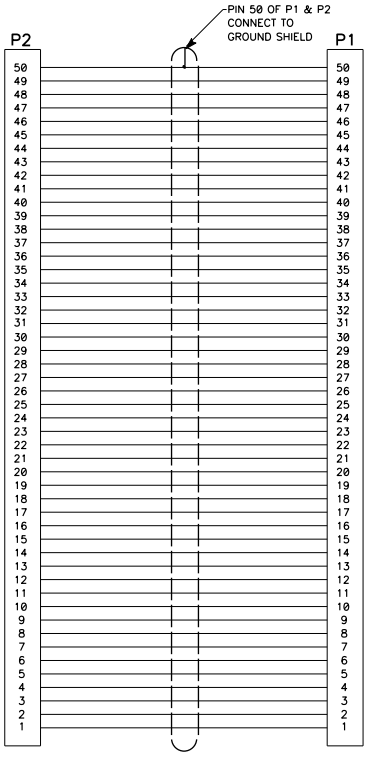


MODEL 5025-550-x SCHEMATIC

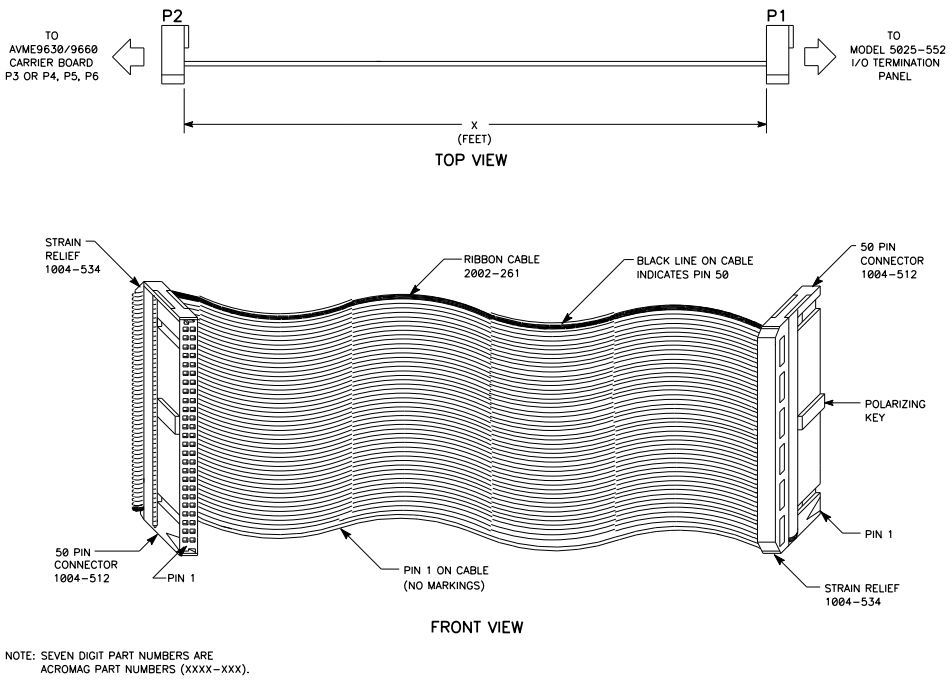


MODEL 5025-550-x SIGNAL CABLE, NON-SHIELDED

4501-462

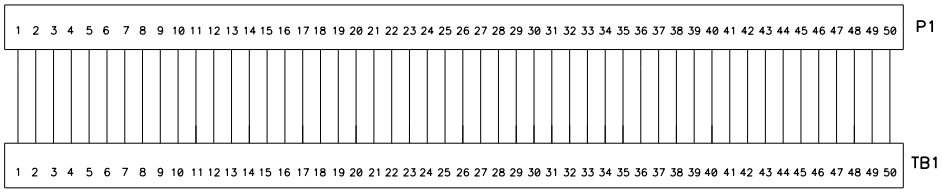


MODEL 5025-551-x SCHEMATIC

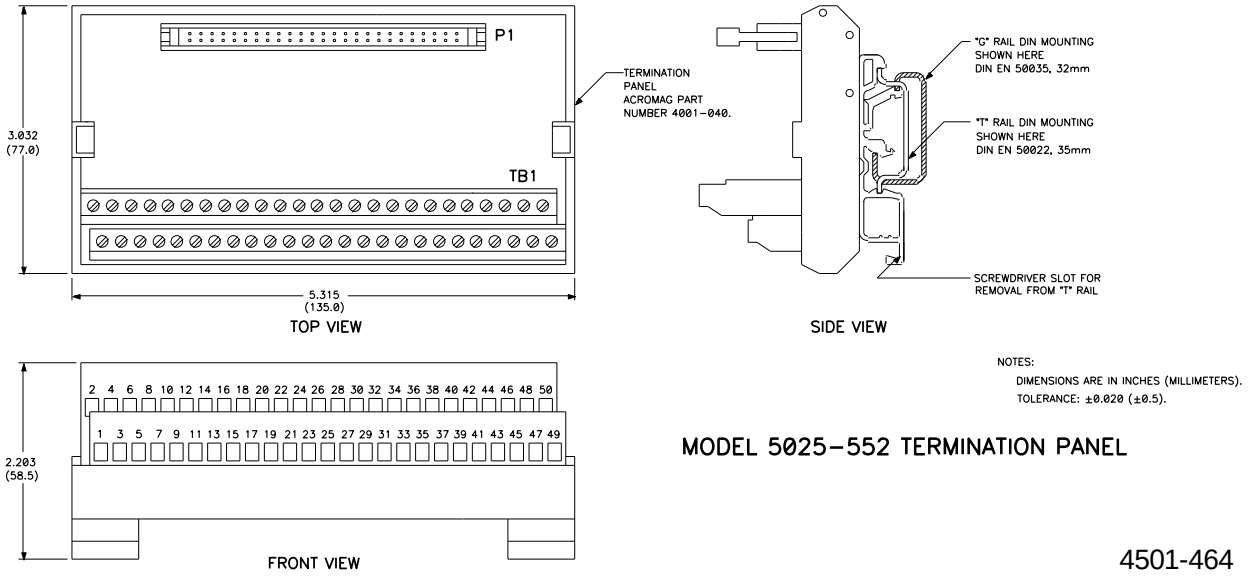


MODEL 5025-551-x SIGNAL CABLE, SHIELDED

4501-463



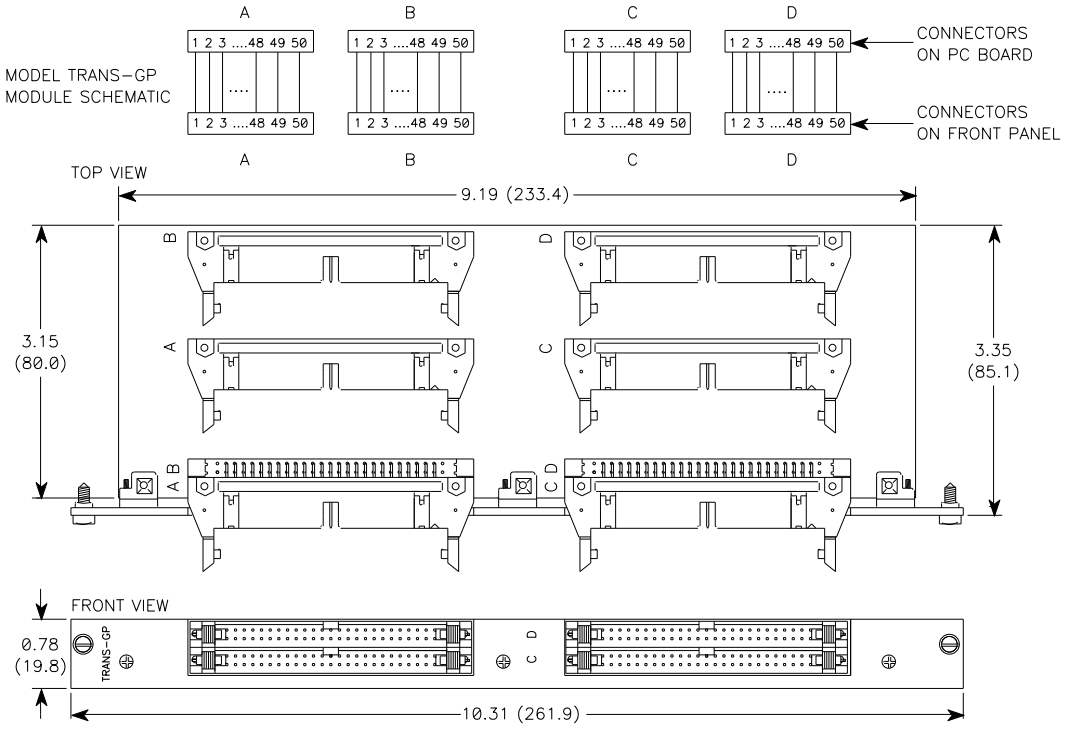
MODEL 5025-552 TERMINATION PANEL SCHEMATIC



NOTES:
DIMENSIONS ARE IN INCHES (MILLIMETERS).
TOLERANCE: ±0.020 (±0.5).

MODEL 5025-552 TERMINATION PANEL

4501-464



TRANS-GP MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC

NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).

4501-465