Acromag®

Series IP484 Industrial I/O Pack
Counter Timer Module

USER'S MANUAL

ACROMAG INCORPORATED
30765 South Wixom Road
P.O. BOX 437
Wixom, MI 48393-7037 U.S.A.

Tel: (248) 295-0310
Fax: (248) 624-9234

8500-729-D11M004

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IMPORTANT SAFETY CONSIDERATIONS
You must consider the possible negative effects of power, wiring, component, sensor, or software failure in the design of any type of control or monitoring system. This is very important where property loss or human life is involved. It is important that you perform satisfactory overall system design and it is agreed between you and Acromag, that this is your responsibility.

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1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP484 module provides support for five independent 16-bit multifunction counter/timers. Each counter/timer can be configured for quadrature position measurement, pulse width modulated output, watchdog timer, event counter, frequency measurement, pulse width measurement, period measurement, or one shot pulse output.

Table 1.1: *The IP482/3/4 module is available in standard and extended temperature ranges*

MODEL	Counters	I/O Type	OPERATING TEMPERATURE RANGE
IP482	10 16-bit	TTL	0°C to +70°C
IP483	5 16-bit 2 16-bit	TTL RS485/RS422	0°C to +70°C
IP484	**5 16-bit**	**RS485/RS422**	**0°C to +70°C**
IP482E	10 16-bit	TTL	-40°C to +85°C
IP483E	5 16-bit 2 16-bit	TTL RS485/RS422	-40°C to +85°C
IP484E	**5 16-bit**	**RS485/RS422**	**-40°C to +85°C**

KEY IP484 COUNTER/TIMER FEATURES

- **TTL/Differential I/O** – The IP484 model has only RS485/RS422 I/O available. Mixed TTL and RS485/RS422 I/O are available on the IP483. The IP482 Counter/Timer I/O is available as TTL only.
- **Quadrature Position Measurement –** Three input signals can be used to determine bi-directional motion. The sequence of logic high pulses for two input signals, A and B, indicate direction and a third signal (index) is used to initialize the counter. X1, X2, and X4 decoding is also implemented. X1 decoding executes one count per duty cycle of the A and B signals, while X2, and X4 execute two and four counts per duty cycle, respectively.
- **Pulse Width Modulation** – Each counter can be programmed for pulse width modulation. The duration of the logic high and low levels of the output signal can be independently controlled. An external gate signal can also be used to start/stop generation of the output signal.
- **Watchdog Timer** – Each counter can be configured as a countdown timer for implementation as a watchdog timer. A gate-off signal is available for use to stop the count down operation. Interrupt generation upon a countdown to zero condition is available.
- **Event Counter** – Each counter can be configured to count input pulses or events. A gate-off signal is provided to control count-up or count down with each event. Interrupt generation upon programmed count condition is available.
- **Frequency Measurement** – Each counter can be configured to count how many active edges are received during a period defined by an external count enable signal. An interrupt can be generated upon measurement complete.

KEY IP484 COUNTER/TIMER FEATURES

- **Pulse-Width or Period Measurement –** Each counter can be configured to measure pulse-width or waveform period. In addition, an interrupt can be generated upon measurement complete.
- **One-Shot and Repetitive One-Shot** – A one-shot pulse waveform may also be generated by each counter. The duration of the pulse and the delay until the pulse goes active is user programmable. A repetitive one-shot can be initiated with repetitive trigger pulses.
- **Programmable Interface Polarity –** The polarities of the counter's external trigger, input, and output pins are programmable for active high or low operation.
- **Internal or External Triggering –** A software or hardware trigger is selectable to initiate quadrature position measurement, pulse width modulation, watchdog countdown, event counting, frequency measurement, pulse-width measurement, period measurement, or one shot.
- **Digital I/O –** The IP484 has 3 RS485/RS422 outputs and 1 RS485/RS422 input available for use.

INDUSTRIAL I/O PACK INTERFACE FEATURES

- **High density -** Single-size, industry-standard, IP module footprint. Up to four units may be mounted on a 6U VMEbus carrier board or five units may be mounted on a PCI carrier board.
- **Local ID** - Each IP module has its own 8-bit ID information which is accessed via data transfers in the "ID Read" space.
- **16-bit & 8-bit I/O** - Channel register Read/Write is performed through D16 or D08 (EO) data transfer cycles in the IP module I/O space.
- **High Speed** - Access times for all data transfer cycles are described in terms of "wait" states. For the supplied IP module example, wait states are utilized for all read and write operations (see specifications for detailed information).
- **8 and 32 MHz Clock Support** – Module supports IP operating clocks of 8 and 32 MHz.

SIGNAL INTERFACE PRODUCTS

This IP module will mate directly to any industry standard IP carrier board (including Acromag's AVME9630/60/70/75 VMEbus, APC8620/21 PCI bus, and ACPC8625/30/35 Compact PCI bus non-intelligent carrier boards). A wide range of other Acromag IP modules are also available to serve your signal conditioning and interface needs.

The cables and termination panels, described in the following paragraphs, represent some of the accessories available from Acromag. Each Acromag carrier has its own unique accessories. They are not all listed in this document. Consult your carrier board documentation for the correct interface product part numbers to ensure compatibility with your carrier board.

SIGNAL INTERFACE PRODUCTS

See the Appendix for further information on these products.

Cables:

Model 5025-551-X (Shielded Cable), or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9630/9660, or other compatible carrier boards, to Model 5025-552 termination panels. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.

Termination Panel:

Model 5025-552: A DIN-rail mountable panel that provides 50 screw terminals for universal field I/O termination. Connects to all Acromag carriers (or other compatible carrier boards) via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

Transition Module:

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from a VMEbus card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. It connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within the card cage, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

IP MODULE ActiveX CONTROL SOFTWARE

Acromag provides a software product (sold separately) consisting of IP module ActiveX (OLE) controls for Windows 98, ME, 2000, and XP® compatible application programs (Model IPSW-ATX-PCI). This software provides individual controls that allow Acromag IP modules to be easily integrated into Windows® application programs, such as Visual C++™, Visual Basic®, and others. The ActiveX controls provide a high-level interface to IP modules, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the ActiveX controls. These functions are intended for use in conjunction with an Acromag personal computer carrier and consist of an ActiveX Carrier Control, and an ActiveX control for each Acromag IP module, as well as, a generic control for non-Acromag IP modules.

IP MODULE Win32 DRIVER SOFTWARE

Acromag provides a software product (sold separately) to facilitate the development of Windows (98/Me/2000/XP®) applications accessing Industry Pack modules installed on Acromag PCI Carrier Cards and CompactPCI Carrier Cards. This software (Model IPSW-API-WIN) consists of low-level drivers and Windows 32 Dynamic Link Libraries (DLLS) that are compatible with a number of programming environments including Visual C++, Visual Basic, Borland C++ Builder and others. The DLL functions provide a high-level interface to the carriers and IP modules eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

IP MODULE VxWORKS SOFTWARE

Acromag provides a software product (sold separately) consisting of IP module VxWorks® libraries. This software (Model IPSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all Acromag IP modules and carriers including the AVME9670, AVME9660/9630, APC8620/21, ACPC8630/35, and ACPC8625. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag IP modules and carriers.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

WARNING: **This board utilizes static sensitive components and should only be handled at a static-safe workstation.**

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier/CPU board, plus the installed IP modules, within the voltage tolerances specified.

The dense packing of the IP module to the carrier/CPU board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

IMPORTANT: *Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.*

BOARD CONFIGURATION

Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-434 and the following discussion for configuration and assembly instructions. Model IP484 Counter/Timer Boards have no jumpers or switches to configure—all configuration is through software commands.

CONNECTORS

IP Field I/O Connector (P2)

P2 provides the field I/O interface connector for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly.

P2 pin assignments are unique to each IP model (see Table 2.1) and normally correspond to the pin numbers of the field-I/O interface connector on the carrier board (you should verify this for your carrier board).

Table 2.1: *IP484 Field I/O Pin Connections*

The IP484 has 5 RS485/RS422 16-bit counters available.

Additionally, it has 1 RS485 Digital Input and 3 RS485 Digital Outputs. The Digital I/O's are emphasized in ***bold italics***.

Pin Description	Pin Number	Pin Description	Pin Number
RS485/RS422			
In1_A+	1	In4_B-	26
In1_A-	2	In5_B+	27
In2_A+	3	In5_B-	28
In2_A-	4	In1_C+	29
In3_A+	5	In1_C-	30
In3_A-	6	In2_C+	31
In4_A+	7	In2_C-	32
In4_A-	8	In3_C+	33
In5_A+	9	In3_C-	34
In5_A-	10	In4_C+	35
In1_B+	11	In4_C-	36
In1_B-	12	In5_C+	37
In2_B+	13	In5_C-	38
In2_B-	14	***DIn1+***	39
In3_B+	15	***DIn1-***	40
In3_B-	16	Out5+	41
Out1+	17	Out5-	42
Out1-	18	***DOut1+***	43
Out2+	19	***DOut1-***	44
Out2-	20	***DOut2+***	45
Out3+	21	***DOut2-***	46
Out3-	22	***DOut3+***	47
Out4+	23	***DOut3-***	48
Out4-	24	D.N.C. [1]	49
In4_B+	25	GND	50

1. ***Do Not Connect:*** *Pin has direct connection to FPGA. Reserved for programming purposes. (TDI#) Pin has active pull-up.*

CONNECTORS

IP Logic Interface Connector (P1)

P1 of the IP module provides the logic interface to the mating connector on the carrier board. This connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly. The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.2).

Pin Description	Pin Number	Pin Description	Pin Number
GND	1	GND	26
CLK	2	+5V	27
Reset#	3	R/W#	28
D00	4	IDSEL#	29
D01	5	DMAReq0#	30
D02	6	MEMSEL#	31
D03	7	DMAReq1#	32
D04	8	IntSel#	33
D05	9	DMAck0#	34
D06	10	IOSEL#	35
D07	11	RESERVED[3]	36
D08	12	A1	37
D09	13	DMAEnd#	38
D10	14	A2	39
D11	15	ERROR[3]	40
D12	16	A3	41
D13	17	INTReq0#	42
D14	18	A4	43
D15	19	INTReq1#	44
BS0#	20	A5	45
BS1#	21	STROBE#	46
-12V[2]	22	A6	47
+12V[2]	23	ACK#	48
+5V	24	RESERVED[3]	49
GND	25	GND	50

Table 2.2: *Standard Logic Interface Connections (P1)*

1. # is used to indicate an Active-low signal.

2. Logic Lines are NOT USED by this IP Model.

3. Logic Lines are reserved for programming purposes. (TMS#, TDO#, and TCLK) Each has an active pull-up.

CONNECTORS

I/O Noise and Grounding Considerations

The IP484 is non-isolated between the logic and field I/O grounds since output common is electrically connected to the IP module ground. Consequently, the field I/O connections are not isolated from the carrier board and backplane. Two ounce copper ground plane foil has been employed in the design of this model to help minimize the effects of ground bounce, impedance drops, and switching transients. However, care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

To minimize high levels of EMI the signal ground connection at the field I/O port (pin 50) should be used to provide a path for induced common-mode noise and currents. The ground path provides a low-impedance path to reduce emissions.

EIA RS485/RS422 communication distances are generally limited to less than 4000 feet. To minimize transmission-line problems, all nodes connected to the cable must use minimum stub length connections. The optimal configuration for the RS485/RS422 bus is a daisy-chain connection from node 1 to node 2 to node 3 to node n. The bus must form a single continuous path, and the nodes in the middle of the bus must not be at the ends of long branches, spokes, or stubs. See Drawing 4501-702 for example connection and termination practices.

Transmission line signal reflections can be minimized with proper termination. The EIA RS485/RS422 standard allows up to 32 driver/receivers to be connected to a single bus. Termination resistors should only be used at the two extreme ends of the bus and not at each of the nodes of the bus. Termination resistors are not provided on the IP484. They can be added to the field wiring as near to the IP module as possible.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the IP484 module.

IP Identification Space (Read Only)

Each IP module contains identification (ID) information that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID space. Fixed information includes the "IPAH" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP484 ID space does not contain any variable (e.g. unique calibration) information. ID space bytes are addressed using only the odd addresses in a 64 byte block (on the "Big Endian" VMEbus). Even addresses are used on the "Little Endian" PC ISA or PCI buses.

The IP484 ID Space is shown in Table 3.1. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID information. Execution of an ID Space Read operation requires 0 wait states.

Table 3.1: *IP484 ID Space Identification (ID)*

Hex Offset From ID Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All 32MHz IP's have 'IPAH'
03	P	50	
05	A	41	
07	H	48	
09		A3	Acromag ID Code
0B		47	IP Model Code[1]
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		0C	Total Number of ID PROM Bytes
17		E8	CRC
19 to 3F		yy	Not Used

1. The IP model number is represented by a two-digit code within the ID space. The IP484 is represented by 47 Hex.

MEMORY MAP

This board is addressable in the Industrial Pack I/O space to monitor and control the status and configuration of up to five 16-bit counter/timers. Additionally, there are Digital I/O available for use. The IP484 has one RS485/RS422 digital input and three RS485/RS422 digital outputs. All the Digital I/O's are controlled by the Digital Registers. The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1..A6, but the IP484 uses only a portion of this space.

The memory space address map for the IP484 is shown in Table 3.2. Note that the base address for the IP484 in memory space must be added to the addresses shown to properly access the IP484 registers. Accesses are generally performed on a 16-bit basis (D0..D15), but 8-bit (D0..D8) (EO) accesses are possible in most cases.

Table 3.2: *IP484 Memory Map*

EVEN Base Addr.+	EVEN Byte D15 D08	ODD Byte D07 D00	ODD Base Addr.+
00	Board Control Register		**01**
02	Counters Interrupt Status/Clear Register		**03**
04	Counter Trigger Register		**05**
06	Counter Stop Register		**07**
08	Counter 1 Control Register		**09**
0A	Counter 2 Control Register		**0B**
0C	Counter 3 Control Register		**0D**
0E	Counter 4 Control Register		**0F**
10	Counter 5 Control Register		**11**
12 ↓ 1A	Not Used[1]		**13 ↓ 1B**
1C	Counter 1 Read Back Register		**1D**
1E	Counter 2 Read Back Register		**1F**
20	Counter 3 Read Back Register		**21**
22	Counter 4 Read Back Register		**23**
24	Counter 5 Read Back Register		**25**
26 ↓ 2E	Not Used[1]		**27 ↓ 2F**

1. The IP484 will return 0 for all addresses that are "Not Used".

MEMORY MAP

30	Counter 1 Constant A Register		**31**
32	Counter 2 Constant A Register		**33**
34	Counter 3 Constant A Register		**35**
36	Counter 4 Constant A Register		**37**
38	Counter 5 Constant A Register		**39**
3A ↓ **42**	Not Used[1]		**3B** ↓ **43**
44	Counter 1 Constant B Register		**45**
46	Counter 2 Constant B Register		**47**
48	Counter 3 Constant B Register		**49**
4A	Counter 4 Constant B Register		**4B**
4C	Counter 5 Constant B Register		**4D**
4E ↓ **56**	Not Used[1]		**4F** ↓ **57**
58	Not Used[1]	Digital Input Register	**59**
5A	Not Used[1]	Digital Output Register	**5B**
5C	Not Used[1]	Interrupt Vector Register	**5D**
5E ↓ **7E**	Not Used[1]		**5F** ↓ **7F**

1. The IP484 will return 0 for all addresses that are "Not Used".

MEMORY MAP

The memory map for this module is given assuming byte accesses using the "Big Endian" byte ordering format. Big Endian is the convention used in the Motorola 68000 and PowerPC microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses. The Intel x86 family of microprocessors uses the opposite convention, or "Little Endian" byte ordering. Little Endian uses even-byte addresses to store the low-order byte. As such, use of the memory map for this module on a PC carrier board will require the use of the even address locations to access the lower 8-bit data. On a VMEbus carrier use of odd address locations are required to access the lower 8-bit data.

CONTROL REGISTERS

CAUTION: *Bit 0 of the Board Control Register must be set correctly for proper module operation.*

Board Control Register (Read/Write)- (Base + 00H)

This read/write register is used to identify the IP48x model, set the carrier operational frequency, and for software reset. The function of each of the board control register bits is described in Table 3.3. This register can be read or written with either 8-bit or 16-bit data transfers. A power-up or system reset sets board control register bit 0 to logic 0.

Table 3.3: *Board Control Register*

BIT	FUNCTION
0	IP Carrier Clock Speed (Read/Write Bit) 0 = 8MHz Carrier 1 = 32MHz Carrier This bit must be set correctly for proper operation.
1 to 7	Not Used[1]
10, 9, 8	Identify IP48x model. (Read Only Bits) 111 = IP482 100 = IP483 001 = IP484
11 to 14	Not Used[1]
15	Software Reset: Write logic "1" to this bit to reset the IP484.[1]

1. All bits labeled "Not Used" and the Software Reset bit will return logic "0" when read.

Interrupt Status/Clear Register (Read/Write) – (Base +02H)

This read/write register is used to determine the pending status of the Counter/Timer interrupts, and release pending interrupts

The Counter/Timer interrupt status/clear bits 0 to 9 reflect the status of each of the Counter/Timers. A "1" bit indicates that an interrupt is pending for the corresponding counter/timer. The Counter/Timer and its corresponding interrupt Pending/Clear bits are as shown in Table 3.4.

Table 3.4: *IP484 Counter/Timer Interrupt Status/Clear*

BIT	FUNCTION
0	Counter/Timer 1 Interrupt Pending/Clear
1	Counter/Timer 2 Interrupt Pending/Clear
2	Counter/Timer 3 Interrupt Pending/Clear
3	Counter/Timer 4 Interrupt Pending/Clear
4	Counter/Timer 5 Interrupt Pending/Clear
5-15	Not Used[1]

1. All bits labeled "Not Used" will return logic "0" when read.

- **Read** of this bit reflects the interrupt pending status of the counter timer logic.
  0 = Interrupt Not Pending
  1 = Interrupt Pending

- **Write** a logic "1" to this bit to release a counter timer pending interrupt. A counter timer pending interrupt can also be released by disabling interrupts via bit-15 of the Counter Control registers.

A Counter/Timer that is not interrupt enabled will never set its interrupt status flag. A Counter/Timer interrupt can be cleared by writing a "1" to its bit position in the Interrupt Status/Clear Register (writing a "1" acts as a reset signal to clear the set state). The interrupt will be generated again, if the condition which caused the interrupt to occur remains. Writing "0" to a bit location has no effect. That is, a pending interrupt will remain pending.

Writing to this register is possible via 16-bit or 8-bit data transfers.

A power-up or system reset clears all interrupts, setting all bits in the Interrupt Status/Clear Register to logic 0.

Counter Trigger Register (Write) - (Base + 04H)

This register is used to implement software triggering for all counter/timers. Writing a 1 to the counter's corresponding trigger bit of this register will cause the counter function to be triggered. Table 3.5 identifies the trigger bit location corresponding to each of the counters. The contents of this register are not stored and merely act to trigger the corresponding counters.

BIT	FUNCTION
0	Counter 1 Trigger[1]
1	Counter 2 Trigger[1]
2	Counter 3 Trigger[1]
3	Counter 4 Trigger[1]
4	Counter 5 Trigger[1]
5-15	Not Used[1]

Table 3.5: *IP484 Counter Trigger Register*

1. All bits will return logic "0" when read.

Triggering may be used to initiate quadrature position measurement, pulse width modulation, watchdog timer (initiates countdown), event counting, frequency measurement, pulse-width measurement, period measurement, or one-shot.

Writing to this register is possible via 16-bit or 8-bit data transfers.

CONTROL REGISTERS

Counter Stop Register (Write) - (Base + 06H)

This register is used to stop the counters of one or a group of Counter/Timers. Writing a 1 to the counter's corresponding stop bit of this register will cause the counter to be disabled. That is, bits 2, 1, and 0 of the counter control register are cleared to "000" thus disabling the counter. Table 3.6 identifies the stop bit location corresponding to each of the counters. The bits of this register are not stored and merely act to stop the corresponding counter when set logic high.

Table 3.6: *IP484 Counter Stop Register*

1. All bits will return logic "0" when read.

BIT	FUNCTION
0	Counter 1 Stop[1]
1	Counter 2 Stop[1]
2	Counter 3 Stop[1]
3	Counter 4 Stop[1]
4	Counter 5 Stop[1]
5-15	Not Used[1]

Writing to this register is possible via 16-bit or 8-bit data transfers.

Counter Read Back Register (Read Only)

This read-only register is a dynamic function register that returns the current value held in the counter. It is updated with the value stored in the internal counter each time it is read.

The internal counter is generally initialized with the value in the Counter Constant Register, and its value is incremented or decremented according to the application.

The addresses corresponding to the Counter Read Back registers are given in Table 3.2. This register must be read using 16-bit accesses.

Counter Constant A Register (Read/Write)

This read/write register is used to store the counter/timer constant A value (initial value) for the various counting modes. It is necessary to load the constant value into the counter in one clock cycle. Thus, access to this register is allowed on a 16-bit basis, only. The addresses corresponding to the Counter Constant A registers are given in Table 3.2.

Note that the Counter Constant Registers are cleared (set to 0) following a system or software reset.

Counter Constant B Register (Read/Write)

This read/write register is used to store the counter/timer constant B value. It is necessary to load the constant value into the counter in one clock cycle. Thus, a 16-bit write access is required. The addresses corresponding to the Counter Constant B registers are given in Table 3.2.

Digital Input Register (Read) – (Base + 58H)

This 8-bit read only register contains the value of the digital RS485/RS422 inputs. A read value of one symbolizes a logic "high" while a value of zero represents a logic "low". Table 3.7 identifies the position of the available input bits.

BIT	FUNCTION
0	DIn1[1] (RS485/RS422)
1-7	Not Used[2]

Table 3.7: IP484 Digital Input Register

1. Digital Input bit will read logic "1" if left unconnected.

2. All bits labeled "Not Used" will return logic "0" when read.

Reading this register is possible via 16-bit or 8-bit data transfers.

Digital Output Register (Read/Write) – (Base + 5AH)

This 8-bit read/write register contains the value of the digital RS485/RS422 outputs. To set a digital output "high" write a one to the proper bit position. To set the value logic "low" write a zero to the proper bit. On power-up output bits are initialized to logic "1". Table 3.8 identifies the position of the available output bits.

BIT	FUNCTION
0	DOut1[1] (RS485/RS422)
1	DOut2[1] (RS485/RS422)
2	DOut3[1] (RS485/RS422)
3-7	Not Used[2]

Table 3.8: IP484 Digital Input Register

1. Bit is initialized to logic "1".

2. All bits labeled "Not Used" will return logic "0" when read.

Writing to this register is possible via 16-bit or 8-bit data transfers. A software or hardware reset will set bits 0 to 2 to logic "1".

Interrupt Vector Register (Read/Write) - (Base + 5CH)

The Interrupt Vector Register maintains an 8-bit interrupt pointer for all channels configured as input channels. The Vector Register can be written with an 8-bit interrupt vector as seen in Table 3.9. This vector is provided to the carrier and system bus upon an active INTSEL∗ cycle. Reading or writing to this register is possible via 16-bit or 8-bit data transfers.

Interrupt Vector Register							
MSB							LSB
07	06	05	04	03	02	01	00

Table 3.9: IP483 Interrupt Vector Register

Interrupts are released on access to the Interrupt Status register. Issue of a software or hardware reset will clear the contents of this register to 0.

COUNTER CONTROL REGISTER

Counter Control Register (Read/Write)

This register is used to configure counter/timer functionality. It defines the counter mode, output polarity, input polarity, clock source, debounce enable, and interrupt enable.

The IP484 has five 16-bit Counter/Timers. The Counter/Timers have Differential (RS485/RS422) I/O. The memory map addresses corresponding to the control registers are given in Table 3.2. The Counter Control Register is cleared (set to 0) following a reset, thus disabling the counter/timer. Reading or writing to this register is possible via 16-bit or 8-bit data transfers.

Eight modes of operation are provided: quadrature position measurement, pulse width modulation, watchdog timer, event counting, frequency measurement, pulse width measurement, period measurement, and one-shot pulse mode. The following sections describe the features of each method of operation and how to best use them.

Quadrature Position Measurement

The counter/timers may be used to perform position measurements from quadrature motion encoders. Bits 2 to 0 of the Counter Control Register set to logic "001" configure the counter for quadrature measurement.

A quadrature encoder can have up to three channels: A, B, and Index. When channel A leads channel B by 90° in a quadrature cycle, the counter increments. When channel B leads channel A by 90° in a quadrature cycle, the counter decrements. The number of increments or decrements per cycle depends on the type of encoding: X1, X2, or X4.

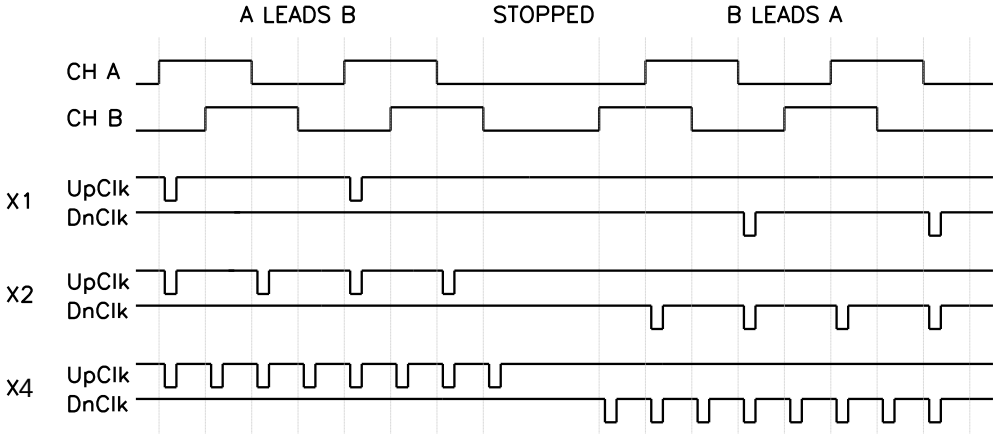


Figure 3.1: Shows a quadrature cycle and the resulting increments and decrements for X1, X2, and X4 encoding.

An X1 encoding Increment occurs on the rising edge of channel A when channel A leads channel B. An X1 encoding decrement occurs on the falling edge of channel A when channel B leads channel A.

For X2 encoding, two increments or decrements (on each edge of channel A) result from each cycle. The counter increments when A leads B and decrements when B leads A.

For X4 encoding, four increments or decrements (on each edge of channel A and B) result from each cycle. The counter increments when A leads B and decrements when B leads A.

Quadrature measurement must be triggered internally via the Counter Trigger Register at the base address + offset 04H. An initial software trigger starts quadrature position measurement operation.

InA and InB input signals are used to input the channel A and channel B input signals, respectively. The counter will increment when channel A leads channel B and will decrement when channel B leads channel A. Three rates of increments and decrements are available X1, X2, and X4 which are programmed via counter timer control register bits 5 and 4. Channel B is enabled for input by setting bit-6 to a logic "1".

InC can be used for the Index signal. Encoders that have an index channel can cause the counter to reload with the Counter Constant B value in a specified phase of the quadrature cycle. Reload can be programmed to occur in any one of the four phases in a quadrature cycle. You must ensure that the Index channel is high during at least a portion of the phase you specify for reload. The phase can be selected via the counter timer control register bits 9, 8, and 7 as seen in Table 3.10.

COUNTER CONTROL REGISTER

COUNTER CONTROL REGISTER

QUADRATURE POSITION MEASUREMENT

The quadrature measurement value can be read from the Counter Read Back Register.

Table 3.10: *Counter Control Register (Quadrature Position Measurement)*

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

An interrupt can be generated upon index reload, or when the counter value equals the constant value stored in the Counter Constant A Register. Interrupts must be enabled via the interrupt enable bit-15 of the Counter Control Register. The interrupt type must also be selected via bits 10 and 11 of the Counter Control Register. The interrupt will remain pending until released by setting the required bit of the Counter/Timer Interrupt Status/Clear register or setting bit-15 of the Counter Control register to "0". Note that interrupts in Quadrature Position Measurement are generated whenever the interrupt conditions exists. If a pending interrupt is cleared, but the interrupt conditions still exists, another interrupt will be generated.

Bit(s)	FUNCTION	
2,1,0	Specifies the Counter Mode:	
	001	Quadrature Position Measurement
3	Output Polarity (Output Pin ACTIVE Level):	
	0	Active LOW (Default)[1]
	1	Active HIGH
5, 4	InA / Channel A	
	00	Disabled (Default)
	01	X1 Encoding
	10	X2 Encoding
	11	X4 Encoding
6	InB / Channel B	
	0	Disabled (Default)
	1	Enabled
9,8,7	InC / Index: Channel Interrupt/Reload occurs when Index signal=1 and the A & B input signals are as selected below. See Control bits 11 & 10 for additional interrupt/load control.	
	000	Disabled (Default) 101, 110, and 111 also Disable
	001	A = 0 , B = 1
	010	A = 1 , B = 0
	011	A = 1 , B = 1
	100	A = 0 , B = 0
11,10	Interrupt Condition Select	
	00	No Interrupt Selected
	01	Interrupt on counter equal Constant A Register.
	10	Interrupt on Index and reload on Index
	11	Interrupt on Index but do not reload counter on Index.
12	Not Used (bit reads back as 0)	
13	Input Debounce Enable	
	0	Disabled (Default) – No Debounce Applied to any Input.
	1	Enabled – Reject A, B, or Index Pulses less than or equal to 2.5μs.
14	Not Used (bit reads back as 0)	
15	Interrupt Enable	
	0	Disable Interrupt Service (Default)
	1	Enable Interrupt Service

COUNTER CONTROL REGISTER

The Counter Control register bits 11 and 10 are used to control the operation of the counter output signal. With bits 11 and 10 set to "01", the output signal will be driven active while the counter equals the counter Constant A value. With bit 11 set to logic "1" the output signal will be driven active while the index condition remains true.

QUADRATURE POSITION MEASUREMENT

Encoder output signals can be noisy. It is recommended that the InA, InB, and InC input signals be debounced by setting bit-13 of the Counter Control register to logic "1". Noise transitions less than 2.5μs will be removed with debounce enabled.

COUNTER CONTROL REGISTER

Pulse Width Modulation

Pulse width modulated waveforms may be generated at the counter timer output. The pulse width modulated waveform is generated continuously. Pulse Width Modulation generation is selected by setting Counter Control Register bits 2 to 0 to logic "010".

Counter Constant A value controls the time until the pulse goes active. The duration of the pulse is set via the Counter Constant B register. Note that a high pulse will be generated if active high output is selected while a low pulse will be generated if active low output is selected.

The counter goes through a countdown sequence for each Counter Constant value. When the 0 count is detected, the output toggles to the opposite state. Then the second Counter Constant value is loaded into the counter, and countdown resumes, decrementing by one for each rising edge of the clock selected via Control Register bits 12, 11, and 10. For example, a counter constant value of 3 will provide a pulse duration of 3 clock cycles of the selected clock. Note, when the maximum internal clock frequency is selected (8MHz or 32MHz), a delay of one extra clock cycle will be added to the counter constant value.

InA can be used as a Gate-Off signal to stop and start the counter and thus the pulse-width modulated output. When InA is enabled via bits 5 and 4 of the control register for active low Gate-Off input, a logic low input will enable pulse-width modulation counting while a logic high will stop PWM counting. When InA is enabled for active high Gate-Off operation, a logic high will enable PWM counting while a logic low will stop PWM counting.

InB can be used to input an external clock for use in PWM. Bits 7 and 6 must be set to either logic "01" or "10". Additionally, the clock source bits 12, 11, and 10 must be set to logic "101" to enable external clock input. PWM can alternatively be internally clocked using control register bits 12, 11, and 10. Available frequencies vary depending on the carrier operational frequency.

InC can be used to externally trigger Pulse Width Modulation generation. Additionally PWM can be triggered internally via the Counter Trigger Register at the base address + offset 04H. An initial trigger, software or external, causes the pulse width modulated signal to be generated. After an initial trigger do not issue additional triggers. Triggers issued while running will cause the Constant A and B values to load at the wrong time. In addition, changing the Control register setting while running can also cause the Constant A and B values to load at the wrong time.

If the Interrupt Enable bit of the Counter Control Register is set (bit 15), an interrupt is generated when the output pulse transitions from low to high and also for transitions from high to low. Thus, an interrupt is generated at each pulse transition.

COUNTER CONTROL REGISTER

PULSE WIDTH MODULATION

Bit(s)	FUNCTION			
2,1,0	Specifies the Counter Mode:			
	010	Pulse Width Modulation		
3	Output Polarity (Output Pin ACTIVE Level):			
	0	Active LOW (Default)[1]		
	1	Active HIGH		
5, 4	InA Polarity / Gate-Off Polarity			
	00	Disabled (Default)		
	01	Active LOW In A=0 Counter is Enabled In A=1 Counter is Disabled		
	10	Active HIGH In A=0 Counter is Disabled In A=1 Counter is Enabled		
	11	Disabled		
7, 6	InB Polarity / External Clock Input			
	00	Disabled (Default)		
	01	External Clock Enabled		
	10	External Clock Enabled		
	11	Disabled		
9,8	InC Polarity / External Trigger			
	00	Disabled (Default)		
	01	Active LOW External Trigger		
	10	Active HIGH External Trigger		
	11	Disabled		
12,11,10	Clock Source[2]			
	Carrier Operational Freq.		8MHz	32MHz
	000	Internal @ (Default)	0.5MHz	2MHz
	001	Internal @	1MHz	4MHz
	010	Internal @	2MHz	8MHz
	011	Internal @	4MHz	16MHz
	100	Internal @	8MHz	32MHz
	101	External Clock	Up to 2MHz	Up to 8MHz
13	Input Debounce Enable			
	0	Disabled (Default) – No Debounce Applied to any Input.		
	1	Enabled – Reject Gate-Off or Trigger Pulses (noise) less than or equal to 2.5μs.		
14	Not Used (bit reads back as 0)			
15	Interrupt Enable			
	0	Disable Interrupt Service (Default)		
	1	Enable Interrupt Service		

Table 3.11: *Counter Control Register (Pulse Width Modulation)*

1. The default state of the output pin is high (output has pullup installed). Bit 3 specifies the active output polarity when the output is driven.

2. The available clock sources are determined by the operational frequency of the carrier board. For an 8MHz carrier, bit 0 of the Board Control Register located at the base address plus an offset of 0H must be set low. For a 32MHz carrier, the bit must be set high.

COUNTER CONTROL REGISTER

Watchdog Timer Operation

The watchdog operation counts down from a programmed (Counter Constant A) value until it reaches 0. While counting, the counter output will be in its active state (the output polarity is programmable). Upon time-out, the counter output will return to its inactive state, and an optional interrupt may be generated. Watchdog operation is selected by setting Counter Control Register bits 2 to 0 to logic "011".

A timed-out watchdog timer will not re-cycle until it is reloaded and then followed with a new trigger. Failure to cause a reload would generate an automatic time-out upon re-triggering, since the counter register will contain the 0 it previously counted down to.

InA input can be used to reload the counter with the Constant A register value. InA reload input is enabled via Control register bits 5 and 4. The counter can also be reloaded via a software write to the Counter Constant A register. Writing to the Counter Constant A register will load the value directly into the counter even if watchdog counting is actively counting down.

InB can be used to input an external clock for watchdog timing. Bits 7 and 6 must be set to either logic "01" or "10". Additionally, the clock source bits 12, 11, and 10 must be set to logic "101" to enable external clock input. The timer can alternatively be internally clocked using control register bits 12, 11, and 10. Available frequencies vary depending on carrier opertional frequency.

InC can be used to either continue/stop watchdog counting or as an external trigger input. When control register bits 9 and 8 are set to logic "11", InC functions as a Continue/Stop signal. When the Continue/Stop signal is high the counter continues counting (when low the counter stops counting). Alternately, when control register bits 9 and 8 are set to logic "01" or "10", the InC input functions as an external trigger input. The watchdog timer may also be internally triggered (via the Trigger Control Register at the base address + offset 04H).

When triggered, the counter/timer contents are decremented by one for each clock cycle, until it reaches 0, upon which a watchdog timer time-out occurs. For example, a counter constant value of 30 will provide a time-out delay of 30 clock cycles of the selected clock. However, due to the asynchronous relationship between the trigger and the selected clock, one clock cycle of error can be expected. The counter can be read from the Counter Read Back register at any time during watchdog operation.

Upon time-out, the counter output pin returns to its inactive state. The IP484 will also issue an interrupt upon detection of a count value equal to 0, if enabled via bit-15 of the Counter Control Register. This could be useful for alerting the host that a watchdog timer time-out has occurred and may need to be reinitialized. The interrupt will remain pending until the watchdog timer is reinitialized and the interrupt is released by setting the required bit of the Counter/Timer Interrupt Status/Clear register.

COUNTER CONTROL REGISTER

WATCHDOG TIMER OPERATION

Table 3.12: *Counter Control Register (Watchdog Timer)*

Bit(s)	FUNCTION			
2,1,0	Specifies the Counter Mode:			
	011	Watchdog Function		
3	Output Polarity (Output Pin ACTIVE Level):			
	0	Active LOW (Default)[1]		
	1	Active HIGH		
5, 4	InA Polarity / Counter Reload			
	00	Disabled (Default)		
	01	Active LOW In A=0 Counter Reinitialized In A=1 Inactive State		
	10	Active HIGH In A=0 Inactive State In A=1 Counter Reinitialized		
	11	Disabled		
7, 6	InB Polarity / External Clock Input			
	00	Disabled (Default)		
	01	External Clock Enabled		
	10	External Clock Enabled		
	11	Disabled		
9,8	InC Polarity / External Trigger			
	00	Disabled (Default)		
	01	Active LOW Trigger		
	10	Active HIGH Trigger		
	11	Gate-Off (Continue when high/Stop when low)		
12,11,10	Clock Source[2]			
	Carrier Operational Freq.		8MHz	32MHz
	000	Internal @ (Default)	0.5MHz	2MHz
	001	Internal @	1MHz	4MHz
	010	Internal @	2MHz	8MHz
	011	Internal @	4MHz	16MHz
	100	Internal @	8MHz	32MHz
	101	External Clock	Up to 2MHz	Up to 8MHz
13	Input Debounce Enable			
	0	Disabled (Default) – No Debounce Applied to any Input.		
	1	Enabled – Reject Reinitialize or Trigger Pulses (noise) less than or equal to 2.5μs.		
14	Not Used (bit reads back as 0)			
15	Interrupt Enable			
	0	Disable Interrupt Service (Default)		
	1	Enable Interrupt Service		

1. The default state of the output pin is high (output has pullup installed). Bit 3 specifies the active output polarity when the output is driven.

2. The available clock sources are determined by the operational frequency of the carrier board. For an 8MHz carrier, bit 0 of the Board Control Register located at the base address plus an offset of 0H must be set low. For a 32MHz carrier, the bit must be set high.

COUNTER CONTROL REGISTER

Event Counting Operation

Positive or negative polarity events can be counted. Event Counting is selected by setting Counter Control Register bits 2 to 0 to logic "100" and setting bits 12 to 10 to logic "000".

Input pulses or events occurring at the input InB of the counter will increment the counter until it reaches the Counter Constant A value. Upon reaching the count limit, an output pulse of 1.75μs will be generated at the counter output pin, and an optional interrupt may be generated. Additionally, the internal event counter is cleared. The counter will continue counting, again from 0, until it reaches the Counter Constant A value. Once triggered, event counting will continue until disabled via Control register bits 2 to 0.

InA can be used as a Gate-Off signal to stop and start event counting. When InA is enabled via bits 5 and 4 of the control register for active low Gate-Off input, a logic low input will enable event counting while a logic high will stop event counting. When InA is enabled for active high Gate-Off operation, a logic high will enable event counting while a logic low will stop event counting.

InB is used as the event input signal. Active high or low input events can be selected via Control register bits 7 and 6. A minimum event pulse width (InB) of 125ns is required for correct pulse detection with input debounce disabled. Programmable clock selection is not available in event counter mode.

InC can be used to either control up/down counting or as an external trigger input. When control register bits 9 and 8 are set to logic "11", InC functions as an Up/Down signal. When the Up/Down signal is high the counter is in the count down mode (when low the counter counts up). The counter will not count down below a count of zero. Alternately, when control register bits 9 and 8 are set to logic "01" or "10", the InC input functions as an external trigger input. Event counting may also be internally triggered (via the Trigger Control Register at the base address + offset 04H).

The Counter Constant A Register holds the count-to value (constant). Reading the Counter Read Back Register will return the current count (variable). **The Counter Constant A value must not be left as 0**. The counter upon trigger starts counting from 0 and since the counter would match the count-to value the counter resets and starts counting from zero again.

If the Interrupt Enable bit of the Counter Control Register is set (bit 15), an interrupt is generated when the number of input pulse events is equal to the Counter Constant A register value. The internal counter is then cleared and will continue counting events until the counter constant A value is again reached and a new interrupt generated. An interrupt will remain pending until released by setting the required bit of the Counters Interrupt Status/Clear register at the base address + offset 02H. A pending interrupt can also be cleared, by setting Control register bit-15 to logic low.

COUNTER CONTROL REGISTER

EVENT COUNTING OPERATION

Bit(s)	FUNCTION	
2,1,0	Specifies the Counter Mode:	
	100	Event Counting
3	Output Polarity (Output Pin ACTIVE Level):	
	0	Active LOW (Default)[1]
	1	Active HIGH
5, 4	InA Polarity / Gate-Off	
	00	Disabled (Default)
	01	Active LOW In A=0: Continue Counting In A=1: Stop Counting
	10	Active HIGH In A=0: Stop Counting In A=1: Continue Counting
	11	Disabled
7, 6	InB Polarity / Event Input	
	00	Disabled (Default)
	01	Active LOW Events
	10	Active HIGH Events
	11	Disabled
9,8	InC Polarity / External Trigger	
	00	Disabled (Default)
	01	Active LOW Trigger
	10	Active HIGH Trigger
	11	Up when logic low /Down when logic high Count Control
12,11,10	Specifies the Counter Mode:	
	000	Event Counting
13	Input Debounce Enable	
	0	Disabled (Default) – No Debounce Applied to any Input.
	1	Enabled – Reject Gate-Off, Event Input, Up/Down or Trigger Pulses (noise) less than or equal to 2.5μs.
14	Not Used (bit reads back as 0)	
15	Interrupt Enable	
	0	Disable Interrupt Service (Default)
	1	Enable Interrupt Service

Table 3.13: *Counter Control Register (Event Counting)*

1. The default state of the output pin is high (output has pullup installed). Bit 3 specifies the active output polarity when the output is driven.

COUNTER CONTROL REGISTER

Frequency Measurement Operation

Frequency Measurement is selected by setting Counter Control Register bits 2 to 0 to logic "100" and setting bits 12 to 10 to logic "111". The counter counts how many InB edges (low to high or high to low) are received during the InA enable interval. The frequency is the number of counts divided by the duration of the InA enable signal.

InA is used as an enable signal to start frequency measurement. The InA signal must be a pulse of known width. When InA is configured (via bits 5 and 4 of the control register) as an active low enable input, a logic low input will enable frequency measurement while a logic high will stop frequency measurement. When InA is configured as an active high enable signal, a logic high will enable frequency measurement while a logic low will stop frequency measurement.

InB is used to input the signal whose frequency is to be measured. Input pulses occurring at input InB of the counter are counted while the enable signal present on InA is active. When the InA signal goes inactive, the counter output will generate a 1.75μs output pulse and an optional interrupt.

InC can be used as an external trigger input. When control register bits 9 and 8 are set to logic "01" or "10", the InC input functions as an external trigger input. Frequency measurement may also be internally triggered (via the Trigger Control Register at the base address + offset 04H). An initial trigger, software or external, starts frequency measurement upon the active edge of the InA enable signal.

The Counter Constant A Register is not used for frequency measurement. Do not write to this register while the counter is actively counting since this will cause the counter to be loaded with the Constant A value.

Reading the Counter Read Back Register will return the current count (variable). A minimum event pulse width (InB) is required for correct pulse detection with input debounce disabled. A carrier operating at 8MHz requires an 125ns event pulse, while a carrier operating at 32MHz requires an 31.25ns event pulse. With debounce enabled, a minimum event pulse width of 2.5μs is required for correct pulse detection. Programmable clock selection is not available for frequency measurement.

If the Interrupt Enable bit-15 of the Counter Control Register is set, an interrupt is generated when the input InA enable pulse goes inactive. An interrupt will remain pending until released by setting the required bit of the Interrupt Status/Clear register at the base address + offset 02H. A pending interrupt can also be cleared, by setting the Counter Control register bit-15 to logic low.

COUNTER CONTROL REGISTER

FREQUENCY MEASUREMENT OPERATION

Bit(s)	FUNCTION	
2,1,0	Specifies the Counter Mode:	
	100	Frequency Measurement
3	Output Polarity (Output Pin ACTIVE Level):	
	0	Active LOW (Default)[1]
	1	Active HIGH
5, 4	InA Polarity / Enable Pulse of Known Width	
	00	Disabled (Default)
	01	Active LOW Pulse
	10	Active HIGH Pulse
	11	Disabled
7, 6	InB Polarity / Signal Measured/Counted	
	00	Disabled (Default)
	01	Active LOW Pulse Counted
	10	Active HIGH Pulse Counted
	11	Disabled
9,8	InC Polarity / External Trigger	
	00	Disabled (Default)
	01	Active LOW Trigger
	10	Active HIGH Trigger
	11	Disabled
12,11,10	Specifies the Counter Mode:	
	111	Frequency Measurement
13	Input Debounce Enable	
	0	Disabled (Default) – No Debounce Applied to any Input.
	1	Enabled – Reject Frequency Input Enable, or Trigger Pulse (noise) less than or equal to 2.5μs.
14	Not Used (bit reads back as 0)	
15	Interrupt Enable	
	0	Disable Interrupt Service (Default)
	1	Enable Interrupt Service

Table 3.14: *Counter Control Register (Frequency Measurement)*

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

COUNTER CONTROL REGISTER

Input Pulse Width Measurement

Setting bits 2 to 0 of the Counter Control Register to logic "101" configures the counter for pulse-width measurement. After pulse-width measurement is triggered, the first input pulse is measured.

InA is used to input the pulse to be measured. An active low or high pulse can be measured.

InB can be used to input an external clock for Pulse-Width Measurement. Bits 7 and 6 must be set to either logic "01" or "10". Additionally, the clock source bits 12, 11, and 10 must be set to logic "101" to enable external clock input. Pulse Width Measurement can alternatively be internally clocked using control register bits 12, 11, and 10. Available frequencies vary depending on carrier operational frequency.

InC can be used to externally trigger Pulse Width Measurement. Additionally, Pulse Width Measurement can be triggered internally via the Counter Trigger Register at the base address + offset 04H. An initial trigger, software or external, starts pulse width measurement at the beginning of the next active pulse.

For pulse-width measurement, the pulse-width being measured serves as an enable control for an up-counter whose value can be read from the Counter Read Back Register. When triggered, the counter is reset and then increments by one for each clock pulse while the input signal level remains in the active state (high or low according to the programmed polarity of input InA). The resultant pulse-width is equivalent to the count value read from the Counter Read Back Register, multiplied by the clock period. An output pulse will be generated at the counter output pin to signal the completion of a given measurement. Note that the measured pulse may be in error by $\pm$ 1 clock cycle.

Reading a counter value of 0xFFFF hex indicates that the pulse duration is longer than the current counter size and clock frequency can measure. Upon reading of this overflow value you must select a slower frequency and re-measure.

An interrupt can be generated upon completion of a given pulse width measurement (the pulse has returned to the opposite polarity), if enabled via the interrupt enable bit of the Counter Control Register (bit 15). The interrupt will remain pending until released by setting the required bit of the Interrupt Status/Clear register at the base address + offset 02H. A pending interrupt can also be cleared, by setting the Counter Control register bit-15 to logic low.

COUNTER CONTROL REGISTER

INPUT PULSE WIDTH MEASUREMENT

Bit(s)	FUNCTION			
2,1,0	Specifies the Counter Mode:			
	101	Pulse-Width Measurement		
3	Output Polarity (Output Pin ACTIVE Level):			
	0	Active LOW (Default)[1]		
	1	Active HIGH		
5, 4	InA Polarity / Pulse Polarity to be Measured			
	00	Disabled (Default)		
	01	Active LOW Pulse is Measured		
	10	Active HIGH Pulse is Measured		
	11	Disabled		
7, 6	InB Polarity / External Clock Input			
	00	Disabled (Default)		
	01	External Clock Enabled		
	10	External Clock Enabled		
	11	Disabled		
9,8	InC Polarity / External Trigger			
	00	Disabled (Default)		
	01	Active LOW Trigger		
	10	Active HIGH Trigger		
	11	Disabled		
12,11,10	Clock Source[2]			
	Carrier Operational Freq.		8MHz	32MHz
	000	Internal @ (Default)	0.5MHz	2MHz
	001	Internal @	1MHz	4MHz
	010	Internal @	2MHz	8MHz
	011	Internal @	4MHz	16MHz
	100	Internal @	8MHz	32MHz
	101	External Clock	Up to 2MHz	Up to 8MHz
13	Input Debounce Enable			
	0	Disabled (Default) – No Debounce Applied to any Input.		
	1	Enabled – Reject Input Pulse Measured or Trigger Pulses (noise) less than or equal to 2.5µs. *Using Debounce will add an error of up to 800ns when used for input pulse measurement.*		
14	Not Used (bit reads back as 0)			
15	Interrupt Enable			
	0	Disable Interrupt Service (Default)		
	1	Enable Interrupt Service		

Table 3.15: *Counter Control Register (Input Pulse Width Measurement)*

1. The default state of the output pin is high (output has pullup installed). Bit 3 specifies the active output polarity when the output is driven.

2. The available clock sources are determined by the operational frequency of the carrier board. For an 8MHz carrier, bit 0 of the Board Control Register located at the base address plus an offset of 0H must be set low. For a 32MHz carrier, the bit must be set high.

COUNTER CONTROL REGISTER

Input Period Measurement

The counter/timer may be used to measure the period of an input signal at the counter input InA. Setting bits 2 to 0 of the Counter Control Register to logic "110" configures the counter for period measurement. The first input cycle after period measurement is triggered will be measured.

InA is used to input the signal to be measured. Period measurement can be initiated on the active low or high portion of the waveform. The period of signal is the time the signal is low added to the time the signal is high, before it repeats.

InB can be used to input an external clock for period measurement. Bits 7 and 6 must be set to either logic "01" or "10". Additionally, the clock source bits 12, 11, and 10 must be set to logic "101" to enable external clock input. Period measurement can alternatively be internally clocked using control register bits 12, 11, and 10. Available frequencies vary depending on carrier operational frequency.

InC can be used to externally trigger period measurement. Additionally, Period Measurement can be triggered internally via the Counter Trigger Register at the base address + offset 04H. An initial trigger, software or external, starts period measurement at the beginning of the next active period.

The period being measured serves as an enable control for an up-counter whose value can be read from the Counter Read Back Register. When triggered the counter is reset. Then, the active polarity of InA starts period measurement. The counter increments by one for each clock pulse during the input signal period (InA). The resultant period is equivalent to the count value read from the Counter Read Back Register, multiplied by the clock period. A 1.75μs output pulse will be generated at the counter output pin to signal the completion of a given measurement. Note that the measured period may be in error by $\pm$ 1 clock cycle.

Reading a counter value of 0xFFFF hex indicates that the pulse duration is longer than the current counter size and clock frequency can measure. Upon reading of this overflow value you must select a slower frequency and re-measure.

An interrupt can be generated upon completion of a given period measurement, if enabled via the interrupt enable bit of the Counter Control Register (bit 15). The interrupt will be generated upon completion of the first complete waveform cycle after the counter is triggered. The interrupt will occur even if an external clock is selected but no clock signal is provided on InB. The count value will be zero in this case. The interrupt, once driven active, will remain pending until released by setting the required bit of the Interrupt Status/Clear register at the base address + offset 02H. A pending interrupt can also be cleared, by setting Counter Control register bit-15 to logic low.

COUNTER CONTROL REGISTER

INPUT PERIOD MEASUREMENT

Bit(s)	FUNCTION			
2,1,0	Specifies the Counter Mode:			
	110	Period Measurement		
3	Output Polarity (Output Pin ACTIVE Level):			
	0	Active LOW (Default)[1]		
	1	Active HIGH		
5, 4	InA Polarity / Signal Measured			
	00	Disabled (Default)		
	01	Active LOW portion of the signal starts period measurement.		
	10	Active HIGH portion of the signal starts period measurement.		
	11	Disabled		
7, 6	InB Polarity / External Clock Input			
	00	Disabled (Default)		
	01	External Clock Enabled		
	10	External Clock Enabled		
	11	Disabled		
9,8	InC Polarity / External Trigger			
	00	Disabled (Default)		
	01	Active LOW Trigger		
	10	Active HIGH Trigger		
	11	Disabled		
12,11,10	Clock Source			
	Carrier Operational Freq.		8MHz	32MHz
	000	Internal @ (Default)	0.5MHz	2MHz
	001	Internal @	1MHz	4MHz
	010	Internal @	2MHz	8MHz
	011	Internal @	4MHz	16MHz
	100	Internal @	8MHz	32MHz
	101	External Clock	Up to 2MHz	Up to 8MHz
13	Input Debounce Enable			
	0	Disabled (Default) – No Debounce Applied to any Input.		
	1	Enabled – Reject Source or Trigger Pulses (noise) less than or equal to 2.5μs. *Using Debounce will add an error of up to 800ns when used for period measurement.*		
14	Not Used (bit reads back as 0)			
15	Interrupt Enable			
	0	Disable Interrupt Service (Default)		
	1	Enable Interrupt Service		

Table 3.16: *Counter Control Register (Input Period Measurement)*

1. The default state of the output pin is high (output has pullup installed). Bit 3 specifies the active output polarity when the output is driven.

2. The available clock sources are determined by the operational frequency of the carrier board. For an 8MHz carrier, bit 0 of the Board Control Register located at the base address plus an offset of 0H must be set low. For a 32MHz carrier, the bit must be set high.

COUNTER CONTROL REGISTER

One-Shot Pulse Mode

One-Shot pulse mode provides an output pulse that is asserted one time or repeated each time it is re-triggered. One-Shot generation is selected by setting Counter Control Register bits 2 to 0 to logic "111".

The Counter Constant A value controls the time until the pulse goes active. The duration of the pulse high or low is set via the Counter Constant B value. Note that the Constant B value defines the logic high pulse width, if active high output is selected, and a low pulse if active low output is selected.

The counter goes through a full countdown sequence for each Counter Constant value. When the 0 count is detected, on the next rising-edge of the clock, the output toggles to the opposite state, and the Counter Constant B value is loaded into the counter and countdown resumes, decrementing by one each clock cycle. For example, a counter constant value of 7 will provide a pulse duration of 7 clock cycles of the selected clock, then 125ns will be added for the count detection of 0. Note that this extra delay is only 31.25ns for 32MHz carrier operation.

InA can be used as a Gate-Off signal to stop and start the counter and, thus output. When InA is enabled via bits 5 and 4 of the control register for active low Gate-Off input, a logic low input will enable the one-shot counter while a logic high will stop the one-shot counter. When InA is enabled for active high Gate-Off operation, a logic high will enable the one-shot counter while a logic low will stop the one-shot counter.

InB can be used to input an external clock for use in one-shot. Bits 7 and 6 must be set to either logic "01" or "10". Additionally, the clock source bits 12, 11, and 10 must be set to logic "101" to enable external clock input. One-Shot pulse mode can alternatively be internally clocked via control register bits 12, 11, and 10. Available frequencies vary depending on carrier operational frequency.

InC can be used to externally trigger One-Shot pulse mode. Additionally, a one-shot pulse can be triggered internally via the Counter Trigger Register at the base address + offset 04H. An initial trigger, software or external, causes the one-shot signal to be generated with no additional triggers required. Additional triggers must not be input until the one shot pulse has completed count down of the Constant B value.

If the Interrupt Enable bit-15 of the Counter Control Register is set, an interrupt is generated when the pulse transitions from low to high and also when the pulse transitions from high to low. The interrupt will remain pending until released by setting the required bit of the Interrupt Status/Clear register at the base address + offset 02H. A pending interrupt can also be cleared, by setting the Counter Control register bit-15 to logic low.

COUNTER CONTROL REGISTER

ONE-SHOT PULSE MODE

Table 3.17: *Counter Control Register (One-Shot Pulse)*

Bit(s)	FUNCTION			
2,1,0	Specifies the Counter Mode:			
	111	One-Shot Generation		
3	Output Polarity (Output Pin ACTIVE Level):			
	0	Active LOW (Default)[1]		
	1	Active HIGH		
5, 4	InA Polarity / Gate-Off Polarity			
	00	Disabled (Default)		
	01	Active LOW In A=0 Output Enabled In A=1 Output Disabled		
	10	Active HIGH In A=0 Output Disabled In A=1 Output Enabled		
	11	Disabled		
7, 6	InB Polarity / External Clock Input			
	00	Disabled (Default)		
	01	External Clock Enabled		
	10	External Clock Enabled		
	11	Disabled		
9,8	InC Polarity / External Trigger			
	00	Disabled (Default)		
	01	Active LOW Trigger		
	10	Active HIGH Trigger		
	11	Disabled		
12,11,10	Clock Source[2]			
	Carrier Operational Freq.		8MHz	32MHz
	000	Internal @ (Default)	0.5MHz	2MHz
	001	Internal @	1MHz	4MHz
	010	Internal @	2MHz	8MHz
	011	Internal @	4MHz	16MHz
	100	Internal @	8MHz	32MHz
	101	External Clock	Up to 2MHz	Up to 8MHz
13	Input Debounce Enable			
	0	Disabled (Default) – No Debounce Applied to any Input.		
	1	Enabled – Reject Gate-Off or Trigger Pulses (noise) less than or equal to 2.5μs.		
14	Not Used (bit reads back as 0)			
15	Interrupt Enable			
	0	Disable Interrupt Service (Default)		
	1	Enable Interrupt Service		

1. The default state of the output pin is high (output has pullup installed). Bit 3 specifies the active output polarity when the output is driven.

2. The available clock sources are determined by the operational frequency of the carrier board. For an 8MHz carrier, bit 0 of the Board Control Register located at the base address plus an offset of 0H must be set low. For a 32MHz, carrier the bit must be set high.

PROGRAMMING EXAMPLES

The following section provides sample applications for each of the counter modes of operation. This includes I/O pin assignments, register settings, required calculations, and waveform diagrams. All examples assume 8MHz carrier operation, even addressing, and that all values are read and written in hex. These assumptions may differ depending on the system and software being used.

Quadrature Position Measurement Example

The objective for this example is to employ Quadrature Position Measurement using 16-bit Counter 1. Suppose that an encoder, connected to the shaft of a motor, provides three signals. Two of the signals (A and B) are out of phase by 90° and provide directional information. For this example, Channel A will always lead B. The third signal C is an Index pulse that is active every four revolutions (A pulses). Assume that X2 encoding is used and on the index pulse, when Channel A and B are equal to one, an active high output and interrupt are generated, and the counter is reloaded to zero. Additionally, debounce is enabled.

1. Connect the inputs/output to the following pins (unpowered):

Table 3.18: *Quadrature Pin Assignments for Counter 1*

Pin #	Connection	Pin #	Connection	Description
1	In1_A(+)	2	In1_A(-)	Channel A
11	In1_B(+)	12	In1_B(-)	Channel B
29	In1_C(+)	30	In1_C(-)	Index
17	Out1(+)	18	Out1(-)	Output

2. Write the following information, A9E9H, to Counter 1 Control Register located at base address plus an offset of 08H.

Table 3.19: *Quadrature Counter Control Register 1 Settings*

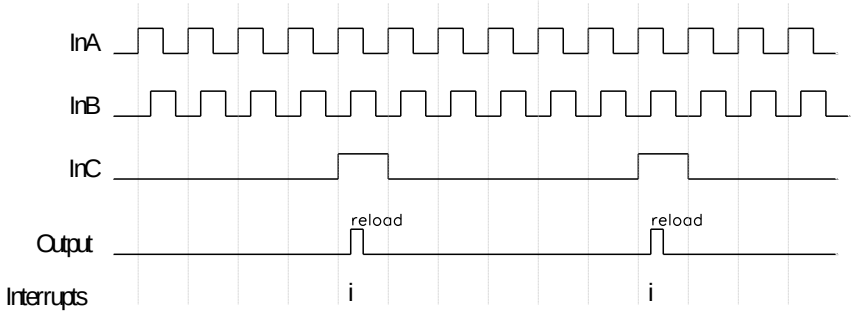
Bits	Logic	Operation
2,1,0	001	Sets the counter to Quadrature Position Measurement.
3	1	Sets the output to active high.
5,4	10	Sets encoding to X2 and enables Channel A (InA).
6	1	Enables Channel B (InB).
9,8,7	011	Sets the Index condition to occur when A=1 and B=1.
11,10	10	Provides for interrupt and reload to occur on index.
12	0	Not used.
13	1	Enables input debounce on InA, InB, and InC.
14	0	Not used.
15	1	Enables interrupts.

3. Write the 32-bit value 0H to Counter 1 Constant B Register located at base address plus an offset 44H for the counter reload value.

The Constant B Register contains the reload value of the counter. Therefore, in this example, when an index pulse occurs and Channel A and B are equal to one, the counter loads zero. This value relies on the specific application.

While Counter Constant A is not used in this example, it has other applications in Quadrature Position Measurement. Refer to the description of Quadrature mode for further information.

4. The following is a waveform diagram of this example. Since Quadrature mode does not accept external triggers, assume that a software trigger has already occurred.



PROGRAMMING EXAMPLES

Figure 3.2: *Quadrature waveform*

In the figure each "i" represents an interrupt

When the index condition is true the counter will reload the value in Counter Constant B register, and an interrupt is generated. The output remains active for as long as the Index condition holds true. For further information on encoder counting, index pulse conditions, interrupts, and outputs, see the Quadrature Position Measurement description.

Pulse Width Modulation Example

The objective for this example is to create a pulse width modulated with an active high pulse of 2μs and a low pulse of 6μs using 16-bit Counter 3. The counter has an external active high gate-off, trigger, and clock signals. The output is active high. Assume the external clock has a frequency of 500KHz. The Gate-Off signal will become active after 2 PWM cycles. Additionally, debounce and interrupts are enabled.

1. Connect the inputs/output to the following pins (unpowered):

Pin #	Connection	Pin #	Connection	Description
5	In3_A(+)	6	In3_A(-)	Gate-Off
15	In3_B(+)	16	In3_B(-)	Ext. Clock
33	In3_C(+)	34	In3_C(-)	Ext. Trigger
21	Out3(+)	22	Out3(-)	Output

Table 3.20: *PWM Pin Assignments for Counter 3*

2. Write the following information, B66AH, to Counter 3 Control Register located at base address plus an offset of 0CH.

Bits	Logic	Operation
2,1,0	010	Sets the counter to Pulse Width Modulation mode.
3	1	Sets the output to active high.
5,4	10	Enable the Gate-Off input (InA) to active high.
7,6	01	Enables the external clock input (InB).
9,8	10	Enables the external Trigger Input (InC) to active high.
12,11,10	101	Sets the clock to an external source.
13	1	Enables input debounce on InA and InC.
14	0	Not used.
15	1	Enables interrupts.

Table 3.21: *PWM Counter Control Register 3 Settings*

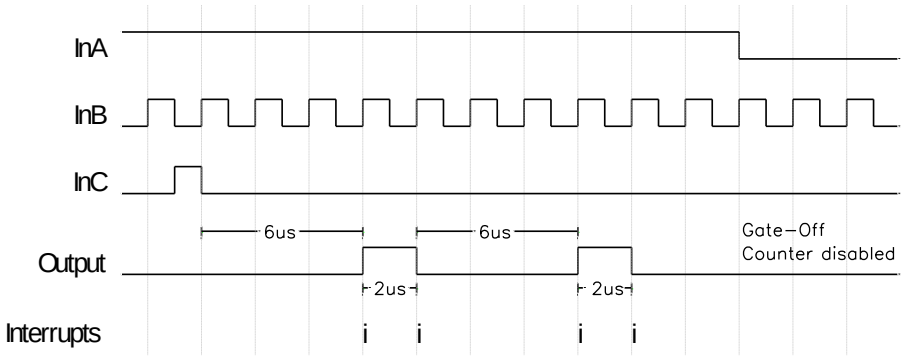
PROGRAMMING EXAMPLES

3. Write the 16-bit value 3H to Counter 3 Constant A Register located at base address plus an offset 34H for the non-active portion of the pulse, and 1H to Counter 3 Constant B Register located at base address plus an offset 48H for the active portion of the pulse.

In order to determine the necessary Counter Constant values first calculate the period of the selected clock (internal or external). The period is calculated by taking the inverse of the clock frequency. In this case, 1/500KHz is equal to 2μs. Then take the total time for the low portion of the pulse and divide it by the clock period. For this example, 6μs/2μs is equal to 3. Convert this value to Hex and the result is the total count that is placed in the appropriate Counter Constant Register. Since it has been stipulated that the pulse is active high, 3H is written to Counter 3 Constant A Register, which contains the value for the non-active (low) portion of the pulse. The same procedure is used to calculate the Constant B value. Take the total period of the high portion of the pulse and divide it by the period of the clock. Here 2μs/2μs is equal to 1. Converting to hex, 1H is written to Counter 3 Constant B Register since it contains the active (high) portion of the pulse.

4. The following is a waveform diagram of this example.

Figure 3.3: *PWM waveform*



In the figure an "i" represents an interrupt

Note that the InA and InC inputs run off the internal 8MHz (or 32MHz) clock. Those signals may not be synchronous with the selected clock. For further information, see the Pulse Width Modulation Operation description.

Watchdog Timer Operation Example

The objective for this example is to create a Watchdog Timer with a countdown length of 10μs using 16-bit Counter 5 with an external active high counter reload, clock, and active low trigger signals. The output is active high. Assume the external clock has a frequency of 500KHz. The counter reload and trigger signals are periodic. Additionally, debounce and interrupts are enabled.

PROGRAMMING EXAMPLES

1. Connect the inputs/output to the following pins (unpowered):

Pin #	Connection	Pin #	Connection	Description
9	In5_A(+)	10	In5_A(-)	Reload
27	In5_B(+)	28	In5_B(-)	Ext. Clock
37	In5_C(+)	38	In5_C(-)	Ext. Trigger
41	Out5(+)	42	Out5(-)	Output

Table 3.22: *Watchdog Pin Assignments for Counter 5*

2. Write the following information, B56BH, to Counter 5 Control Register located at base address plus an offset of 10H.

Bits	Logic	Operation
2,1,0	011	Sets the counter to Watchdog mode.
3	1	Sets the output to active high.
5,4	10	Enable the Counter Reload input (InA) to active high.
7,6	01	Enables the external clock input (InB).
9,8	01	Enables the external Trigger Input (InC) to active low.
12,11,10	101	Sets the clock to an external source.
13	1	Enables input debounce on InA and InC.
14	0	Not used.
15	1	Enables interrupts.

Table 3.23: *Watchdog Counter Control Register 5 Settings*

3. Write the 16-bit value 5H to Counter 5 Constant A Register located at the base address plus an offset of 38H.

In order to determine the correct Constant A Register value, first calculate the period of the selected clock. The period is calculated by taking the inverse of the clock frequency. In this case, 1/500KHz is equal to 2μs. Then take the total duration of the watchdog timer and divide it by the clock period. For this example, 10μs/2μs is equal to five. Converted to Hex, this is the number to write to the Counter 5 Constant A Register.

Counter Constant B Register is not used in Watchdog mode.

4. The following is a waveform diagram of this example.

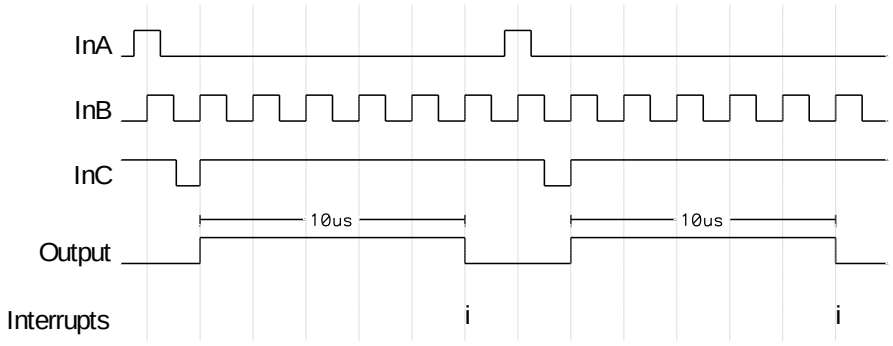


Figure 3.4: *Watchdog waveform*

In the figure each "i" represents an interrupt

In Watchdog mode, the counter must be loaded (InA) and then triggered (InC) for each cycle. While this can be done internally or externally, failure to follow this procedure will cause unpredictable results.

PROGRAMMING EXAMPLES

Note that the InA and InC inputs run off the internal 8MHz (or 32MHz) clock. Those signals may not be synchronous with the selected clock. For further information, see the Watchdog Timer Operation description.

Event Counting Operation Example

The objective for this example is to create an Event Counter that will count the number of active high events on InB using 16-bit Counter 5. The output is active low. Additionally the counter has an active low Gate-Off and an active low External Trigger. After every five events, the event counter interrupts.

1. Connect the inputs/output to the following pins (unpowered):

Table 3.24: *Event Counting Pin Settings for Counter 5*

Pin #	Connection	Pin #	Connection	Description
9	In5_A(+)	10	In5_A(-)	Gate-Off
27	In5_B(+)	28	In5_B(-)	Event Input
37	In5_C(+)	38	In5_C(-)	Ext. Trigger
41	Out5(+)	42	Out5(-)	Output

2. Write the following information, 8194H, to Counter 5 Control Register located at base address plus an offset of 10H.

Table 3.25: *Event Counter Control Register 5 Settings*

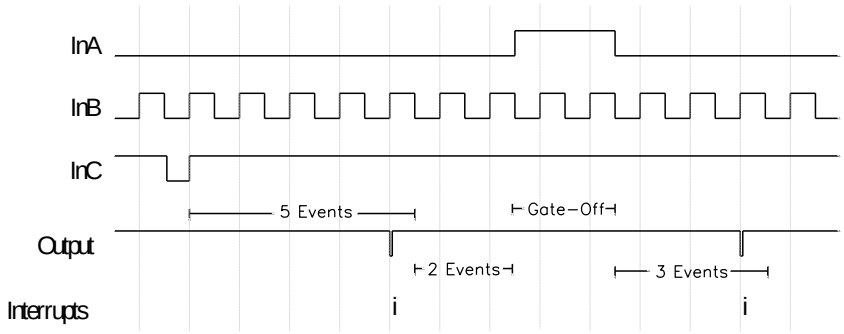
Bits	Logic	Operation
2,1,0	100	Sets the counter to Event Counting mode.
3	0	Sets the output to active low.
5,4	01	Enable the Gate-Off input (InA) to active low.
7,6	10	Enables the Event input (InB) to active high.
9,8	01	Enables the external Trigger Input (InC) to active low.
12,11,10	000	Sets the counter to Event Counting mode.
13	0	Disables input debounce on InA, InB, and InC.
14	0	Not used.
15	1	Enables interrupts.

3. Write the 16-bit value 5H to Counter 5 Constant A Register located at the base address plus an offset of 38H.

Counter Constant B Register is not used in Event Counting mode.

In Event Counting, when the Constant A Register is equal to the value in the Counter 5 Read Back Register, in this case located at base address plus an offset of 24H, there is an output pulse and an interrupt. Furthermore, when this condition occurs, the counter resets to zero and starts incrementing again. For this example, an interrupt and output pulse will occur every five events. Therefore 5H is written to the Counter 5 Constant A Register. Note that all values are stored and read in Hex.

4. The following is a waveform diagram of this example.



PROGRAMMING EXAMPLES

Figure 3.5: *Event Counting waveform*

In the figure each "i" represents an interrupt

The Gate-Off signal is used in this example to pause the counter. While the Gate-Off signal is non-active (logic high), the counter and output will remain constant. Additionally, the output pulse is active for 1.75μs upon the detection of the final event. For further information, see the Event Counting Operation description.

Frequency Measurement Operation Example

The objective for this example is to use the Frequency Measurement Operation using 16-bit Counter 4. The enable signal and the signal measured are active high. Additionally, the counter has an active low External Trigger. The output of the counter is active low and interrupts and debounce are enabled. Assume the enable pulse has a duration of 50μs.

1. Connect the inputs/output to the following pins (unpowered):

Pin #	Connection	Pin #	Connection	Description
7	In4_A(+)	8	In4_A(-)	Enable Input
25	In4_B(+)	26	In4_B(-)	Signal Input
35	In4_C(+)	36	In4_C(-)	Ext. Trigger
23	Out4(+)	24	Out4(-)	Output

Table 3.26: *Frequency Measurement Pin Assignments for Counter 4*

2. Write the following information, BDA4H, to Counter 4 Control Register located at base address plus an offset of 0EH.

Bits	Logic	Operation
2,1,0	100	Sets the counter to Frequency Measurement.
3	0	Sets the output to active low.
5,4	10	Sets the Enable Pulse input (InA) to active high.
7,6	10	Enables the Signal input (InB) to active high.
9,8	01	Enables the external Trigger Input (InC) to active low.
12,11,10	111	Sets the counter to Frequency Measurement mode.
13	1	Enables input debounce on InA, InB, and InC.
14	0	Not used.
15	1	Enables interrupts.

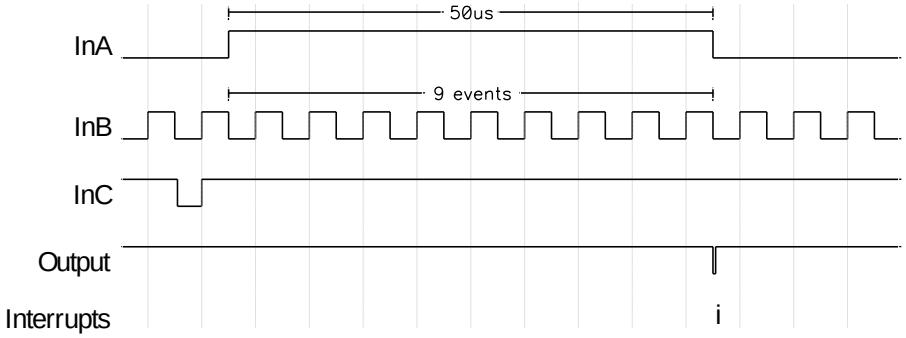
Table 3.27: *Frequency Measurement Control Register 4 Settings*

PROGRAMMING EXAMPLES

3. Do *not* write to either of the Counter 4 Constant Registers. They are not required for frequency measurement and writing to them can cause errors.

4. The following is a waveform diagram of this example.

Figure 3.6: *Frequency Measurement waveform*



In the figure each "i" represents an interrupt

The frequency of the signal is calculated by dividing the value in the Counter 4 Read Back Register, located at base address plus an offset of 22H, by the duration of the InA enable signal. Note that the value in the Read Back Register is stored in Hex and requires conversion to decimal for calculations. In this case the pulse length is 50μs. The value in the Read Back Register is 9, since there were nine high pulses during the enable signal. Therefore, the frequency is 9/50μs, which is equal to 180KHz.

Note that the counter must be re-triggered before the next frequency measurement can take place. Additionally, the output pulse is active for 1.75μs. Since debounce was enabled the output pulse will occur 2.5μs after the completion of the enable signal. For further information, see the Frequency Measurement Operation description.

Input Pulse-Width Measurement Example

The objective for this example is to use the Pulse-Width Measurement Operation using 16-bit Counter 2. The pulse to be measured is active low. Additionally the counter has an external clock and an active low External Trigger. The output of the counter is active high and interrupts are enabled. Assume the external clock has a frequency of 100KHz.

1. Connect the inputs/output to the following pins (unpowered):

Table 3.28: *Pulse-Width Measurement Pin Assignments for Counter 2*

Pin #	Connection	Pin #	Connection	Description
3	In2_A(+)	4	In2_A(-)	Pulse Input
13	In2_B(+)	14	In2_B(-)	Ext. Clock
31	In2_C(+)	32	In2_C(-)	Ext. Trigger
19	Out2(+)	20	Out2(-)	Output

PROGRAMMING EXAMPLES

2. Write the following information, 959DH, to Counter 2 Control Register located at base address plus an offset of 0AH.

Table 3.29: *Pulse-Width Measurement Control Register 2 Settings*

Bits	Logic	Operation
2,1,0	101	Sets the counter to Pulse-Width Measurement.
3	1	Sets the output to active high.
5,4	01	Sets the Pulse input (InA) to active low.
7,6	10	Enables the external clock input (InB).
9,8	01	Enables the external Trigger Input (InC) to active low.
12,11,10	101	Sets the clock to an external source.
13	0	Disables input debounce on InA and InC.
14	0	Not used.
15	1	Enables interrupts.

3. Do *not* write to either of the Counter 2 Constant Registers. They are not required for pulse-width measurement and writing to them can cause errors.

4. The following is a waveform diagram of this example.

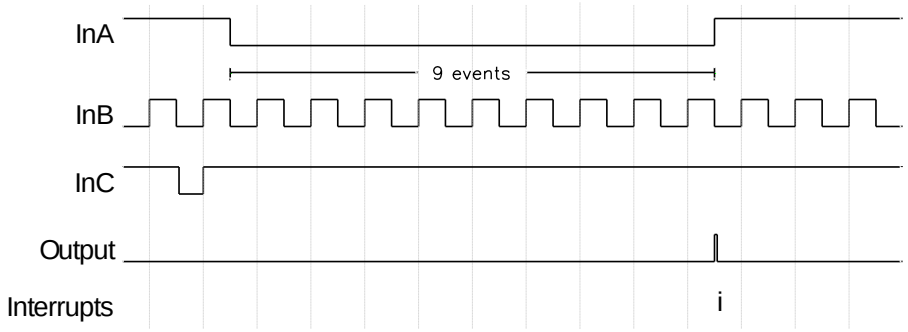


Figure 3.7: *Pulse-Width Measurement waveform*

In the figure each "i" represents an interrupt

The length of the low portion of the InA pulse is calculated by multiplying the number in the Counter 2 Read Back Register, located at base address plus an offset of 1EH, by the period of the selected clock. Note that the value in the Read Back Register is stored in Hex and requires conversion to decimal for calculations. In this case the value in the Read Back Register is 9, since there were nine high pulses during the active InA signal. The period of the clock is calculated by taking the inverse of the frequency of the clock. For this example, the frequency was 100KHz. Therefore the clock period is 1/100KHz, which is equal to 10μs. The clock period multiplied by the Read Back Register 10μs x 9, is equal to 90μs, the duration of the active low InA pulse. This value may be in error by ± 1 clock period.

Note that the InA and InC inputs run off the internal 8MHz (or 32MHz) clock. Those signals may not be synchronous with the selected clock. The output pulse is active for 1.75μs. If debounce was enabled, the output pulse will occur 2.5μs after the completion of the input pulse. Additionally, the counter must be re-triggered before any further measurements take place. For more information, see the Pulse-Width Measurement description.

PROGRAMMING EXAMPLES

Input Period Measurement Example

The objective for this example is to use the Input Period Measurement operation using 16-bit Counter 1. The high-to-low transition of the input signal will begin measurement. Additionally, the counter has an external clock and an active high External Trigger. The output of the counter is active high and interrupts are enabled. Assume the external clock has a frequency of 250KHz.

1. Connect the inputs/output to the following pins (unpowered):

Table 3.30: *Input Period Measurement Pin Assignments for Counter 1*

Pin #	Connection	Pin #	Connection	Description
1	In1_A(+)	2	In1_A(-)	Pulse Input
11	In1_B(+)	12	In1_B(-)	Ext. Clock
29	In1_C(+)	30	In1_C(-)	Ext. Trigger
17	Out1(+)	18	Out1(-)	Output

2. Write the following information, 965EH, to Counter 1 Control Register located at base address plus an offset of 08H.

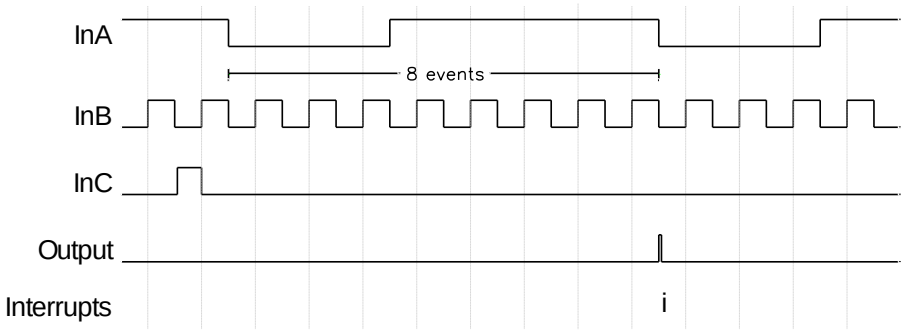
Table 3.31: *Input Period Measurement Control Register 1 Settings*

Bits	Logic	Operation
2,1,0	110	Sets the counter to Input Period Measurement.
3	1	Sets the output to active high.
5,4	01	Sets the Pulse input (InA) to active low.
7,6	01	Enables the external clock input (InB).
9,8	10	Enables the external Trigger Input (InC) to active high.
12,11,10	101	Sets the clock to an external source.
13	0	Disables input debounce on InA and InC.
14	0	Not used.
15	1	Enables interrupts.

3. Do *not* write to either of the Counter 1 Constant Registers. They are not required for input period measurement and writing to them can cause errors.

4. The following is a waveform diagram of this example.

Figure 3.8: *Input Period Measurement waveform*



In the figure each "i" represents an interrupt

PROGRAMMING EXAMPLES

The period of one cycle of the InA waveform is calculated by multiplying the number in the Counter 1 Read Back Register, located at the base address plus an offset of 1CH, by the period of the selected clock. Note that the value in the Read Back Register is stored in Hex and requires conversion to decimal for calculations. In this case the value in the Counter 1 Read Back Register is 8, since there were eight high pulses during one InA period. The period of the clock is calculated by taking the inverse of the frequency of the clock. For this example, the frequency was 250KHz. Therefore, the clock period is 1/250KHz, which is equal to 4μs. The clock period multiplied by the Read Back Register 4μs x 8, is equal to 32μs (the period of the InA waveform). This value may be in error by ± 1 clock period.

Note that the InA and InC inputs run off the internal 8MHz (or 32MHz) clock. Those signals may not be synchronous with the selected clock. The output pulse is active for 1.75μs. If debounce was enabled, the output pulse will occur 2.5μs after the completion of the input signal. Additionally, the counter must be re-triggered before any further measurements take place. For more information, see the Input Period Measurement description.

One-Shot Pulse Mode Example

The objective for this example is to use the One-Shot Pulse mode using 16-bit Counter 2. The output pulse is active high with the low portion 20μs long and the high portion 5 μs long. Additionally, the counter has an external clock, an active high Gate-off signal, and an active high External Trigger. Interrupts are enabled. Assume the external clock has a frequency of 200KHz.

1. Connect the inputs/output to the following pins (unpowered):

Pin #	Connection	Pin #	Connection	Description
3	In2_A(+)	4	In2_A(-)	Gate-Off
13	In2_B(+)	14	In2_B(-)	Ext. Clock
31	In2_C(+)	32	In2_C(-)	Ext. Trigger
19	Out2(+)	20	Out2(-)	Output

Table 3.32: *One-Shot Pulse Pin Assignments for Counter 2*

2. Write the following information, 966FH, to Counter 2 Control Register located at base address plus an offset of 0AH.

Bits	Logic	Operation
2,1,0	111	Sets the counter to One-Shot Pulse generation mode.
3	1	Sets the output to active high.
5,4	10	Sets the Gate-Off input (InA) to active high.
7,6	01	Enables the external clock input (InB).
9,8	10	Enables the external Trigger Input (InC) to active high.
12,11,10	101	Sets the clock to an external source.
13	0	Disables input debounce on InA and InC.
14	0	Not used.
15	1	Enables interrupts.

Table 3.33: *One-Shot Pulse Control Register 2 Settings*

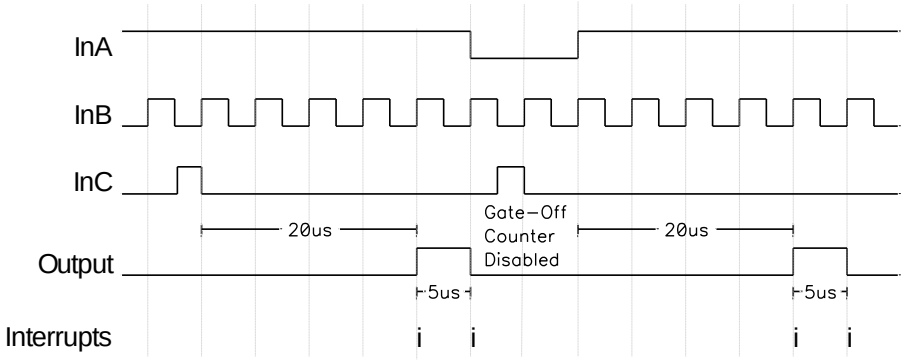
PROGRAMMING EXAMPLES

3. Write the 16-bit value 4H to Counter 2 Constant A Register located at base address plus an offset 32H for the non-active portion of the pulse, and 1H to Counter 2 Constant B Register located at base address plus an offset 46H for the active portion of the pulse.

In order to determine the necessary Counter Constant values first calculate the period of the selected clock (internal or external). The period is calculated by taking the inverse of the clock frequency. In this case, 1/200KHz is equal to 5μs. Then take the total time for the low portion of the pulse and divide it by the clock period. For this example, 20μs/5μs is equal to 4. Convert this value to Hex and the result is the total count that is placed in the appropriate Counter Constant Register. Since it has been stipulated that the pulse is active high, 4H is written to the Counter 2 Constant A Register, which contains the value for the non-active (low) portion of the pulse. The same procedure is used to calculate the Constant B value. Take the total period of the high portion of the pulse and divide it by the period of the clock. For this example 5μs/5μs is equal to 1. Converting to hex, 1H is written to Counter 2 Constant B Register since it contains the active (high) portion of the pulse.

4. The following is a waveform diagram of this example.

Figure 3.9: *One-Shot Pulse waveform*



In the figure each "i" represents an interrupt

The Gate-Off signal (InA) is used as a pause mechanism. The counter register and output remain constant while the Gate-Off signal is active. In this example, this occurs when InA is logic low.

Note that the InA and InC inputs run off the internal 8MHz (or 32MHz) clock. Those signals may not be synchronous with the selected clock. For further information, see the One-Shot Pulse Mode description.

Table 3.34: Counter Timer Modes Overview

Function Description	Pulse Width Modulation/ One-Shot	Watchdog	Event Counting	Frequency Measure	Pulse Measure	Period Measure	Quadrature Position Measure
InA Input	Gate-Off for start/stop control	Counter Reload	Gate-Off for start/stop control	Enable Frequency Measurement for Set Duration	Next complete pulse after trigger is measured.	Next complete period after trigger is measured.	Channel A
InB Input	External Clock	External Clock	Event Input	Signal Measured/ Counted	External Clock	External Clock	Channel B
InC Input	External Trigger	External Trigger or Gate-Off for start/stop control	External Trigger or Up/Down Count Control	External Trigger	External Trigger	External Trigger	Index
Internal Software Trig	Starts Waveform Generation	Starts Count Down	Start Event Counting	Start Frequency Measurement on next active edge of InA signal.	Next complete pulse after trigger is measured.	Next complete period after trigger is measured.	Starts Quadrature Measurement
Counter Timer Output	Output Waveform	Output is active from trigger until terminal count.	1.75µs pulse is output upon reaching the count limit	1.75µs pulse is output upon end of frequency measurement	1.75µs pulse is output upon end of pulse measurement	1.75µs pulse is output upon end of period measurement	Output pulse while index or programmed count limit remains true.
Constant A Reg	Count down from value loaded. Defines duration until active pulse	Counts down from value loaded. Must always load before trigger. Note that InA input can be used to reload.	Count Limit. Input events are counted up to the count limit.				An interrupt can be generated when the counter equals the Constant A value.
Constant B Reg	Count down from value loaded. Defines duration of active pulse						Constant B can be reloaded on occurrence of an Index signal.
Counter Read Back Reg		Gives the Count value at the time of the read.	Gives the Count value at the time read.	Gives count value reflecting measurement	Gives count value reflecting pulse measured	Gives count value reflecting period measured	Gives count value reflecting position measurement
Interrupt	On Edge Transitions	On Terminal Count of 0	Upon reach of count limit	Upon end of enable pulse	Upon end of pulse measurement	Upon end of period measurement	On Index or Constant A count limit.

4.0 THEORY OF OPERATION

This section contains information regarding the hardware of the IP484. A description of the basic functionality of the circuitry used on the board is also provided. Refer to the Block Diagram shown in Drawing 4501-977 as you review this material.

A Field Programmable Gate-Array (FPGA) installed on the IP Module provides an interface to the carrier board per IP Module specification ANSI/VITA 4 1995. The interface to the carrier board allows complete control of all board functions.

LOGIC/POWER INTERFACE

The FPGA installed on the IP Module provides the control signals required to operate the board. It decodes the selected addresses in the I/O, Interrupt, and ID spaces and produces the chip selects, control signals, and timing required by the control registers, as well as, the acknowledgment signal required by the carrier board per the IP specification. It also stores the interrupt vector.

The ID space (read only) is also implemented in the FPGA and provides the identification for the individual module per the IP specification. The ID space and the configuration and control registers are all accessed through a 16-bit data bus interface to the carrier board.

The I/O space (read/write) is implemented in the FPGA and provides software controls for the Counter/Timer modules.

FIELD INPUT/OUTPUT SIGNALS

The field I/O interface to the IP module is provided through connector P2 (refer to Table 2.1). These pins are tied to the inputs and outputs of EIA RS485/RS422 line transceivers or TTL transceivers. RS485 signals received are converted from the required EIA RS485/RS422 voltages signals to the TTL levels required by the FPGA. Likewise TTL signals are converted to the EIA RS485/RS422 voltages for data output transmission. The FPGA provides the necessary interface to the RS485/RS422 transceivers or TTL transceivers for control of data.

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.1). Field I/O points are NON-ISOLATED. This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring this effect may cause operational errors, and with extreme abuse, possible circuit damage.

COUNTER/TIMERS

Differential RS485/RS422 input control signals In_A±, In_B±, and In_C± are available for the five 16-bit counters of the board. See Table 2.1 for the list of these signals and their corresponding pin assignments.

Counter timer out signals OUT1± to OUT5± are differential RS485/RS422 signals output from the five 16-bit counters. See Table 2.1 for the output signals and their corresponding pin assignments.

DIGITAL I/O

Digital input/output signals DIN1± and DOut1± to 3 are differential RS422 signals. The signals are available via the P1 field I/O connector. See Table 2.1 for the list of these signals and their corresponding pin assignments.

5.0 SERVICE AND REPAIR

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

SERVICE AND REPAIR ASSISTANCE

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier/CPU board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

www.acromag.com

Go to the "Support" tab to access:

- Application Notes
- Frequently Asked Questions (FAQ's)
- Product Knowledge Base
- Tutorials
- Software Updates/Drivers

An email question can also be submitted from within the Knowledge Base of directly from the "Contact Us" tab.

Acromag's application engineers can also be contacted directly for technical assistance via telephone or FAX through the numbers listed at the bottom of this page. If needed, complete repair services are also available.

6.0 SPECIFICATIONS

PHYSICAL

Physical Configuration	**Single Industrial Pack Module**
Length	3.880 in. (98.5 mm)
Width	1.780 in. (45.2 mm)
Board Thickness	0.062 in. (1.59 mm)
Max Component Height	0.290 in. (7.37 mm)

Connectors

- IP Logic Interface: 50-pin female receptacle header (AMP 173279-3 or equivalent).
- Field I/O: 50-pin female receptacle header (AMP 173279-3 or equivalent).

Table 6.1: *Power Requirements*

5V Maximum rise time of 100m seconds

Power Requirements		**Module IP484**
5V (±5%)	Typical	410mA
	Max.	480mA
+/-12V (±5%)	Not used	

ENVIRONMENTAL

Operating Temperature: Standard Unit 0 to +70°C.
E Version -40 to 85°C.

Relative Humidity: 5-95% Non-Condensing.

Storage Temperature: -55°C to +125°C.

Non-Isolated: Logic and field commons have a direct electrical connection.

Resistance to RFI: Complies with EN61000-4-3 (3 V/m, 80 to 1000MHz AM & 900MHz. Keyed) and European Norm EN50082-1 with no digital upsets.

Conducted R F Immunity (CRFI): Complies with EN61000-4-6 (3V/rms, 150kHz to 80MHz) and European Norm EN50082-1 with no digital upsets.

Electromagnetic Interference Immunity (EMI): No register upsets under the influence of EMI from switching solenoids, commutator motors, and drill motors.

Surge Immunity: Not required for signal I/O per European Norm EN50082-1.

Electric Fast Transient Immunity EFT: Complies with EN61000-4-4 Level 2 (0.5KV at field input and output terminals) and European Norm EN50082-1.

Electrostatic Discharge (ESD) Immunity: Complies with EN61000-4-2 Level 3, (8KV enclosure port air discharge) Level 2, (4KV enclosure port contact discharge) Level 1, (2KV I/O terminal contact discharge) and European Norm EN50082-1.

Radiated Emissions: Meets or exceeds European Norm EN50081-1 for class B equipment. Shielded cable with I/O connections in a shielded enclosure is required to meet compliance.

SPECIFICATIONS

COUNTER/TIMERS

Counter Functions: Quadrature Position Measurement, Pulse Width Modulation, Watchdog Timer, Event Counting, Frequency Measurement, Period Measurement, Pulse-Width Measurement, and One Shot/Repetitive

Counter Type: - The IP484 has a total of five counter/timers available for use with differential RS485/RS422 I/O.

RS485/RS422 Counter Input

Counters 1 through 5 have Differential RS485/RS422 input signals of InA±, InB±, and InC±. These differential input ports are used to control Start/Stop, Reload, Event Input, External Clock, Trigger, and Up/Down operations.

Fail-Safe: When differential inputs are left floating, receiver output is logic high.

RS485/RS422 Input Electrical Characteristics

- -0.2 Min to 0.2 Max: Differential Input Threshold Voltage with $-7V \leq V_{CM} \leq 12V$
- 70mV Typical: Input Hysteresis
- 12KΩ Minimum Input Resistance

Termination Resistors: Termination Resistors are not provided. Termination resistors are recommended at network end points only (see Drawing 4501-702 for location).

RS485/RS422 Counter Output

Counters 1 through 5 each have a Differential RS485/RS422 Output. The Differential output ports 6 and 7 are used for waveform output, watchdog active indicator, or 1.75μs pulse upon counter function completion. Counter output is programmable as active high or low.

RS485/RS422 Output Electrical Characteristics

- 1.5 V Minimum: Differential Driver Output Voltage with 27Ω load.
- 3 V Maximum: Common Mode Output Voltage.

8MHz IP Carrier Operation

Selectable Counter Clock Frequencies: 8MHz, 4MHz, 2MHz, 1MHz, 0.5MHz or External up to 2MHz.
Minimum I/P Event: 125ns
Minimum Pulse Measurement: 125ns
Minimum Period Measurement: 300ns
Minimum Gate/Trigger Pulse: 125ns

SPECIFICATIONS

32MHz IP Carrier Operation

Selectable Counter Clock Frequencies : 32MHz, 16MHz, 8MHz, 4MHz, 2Mhz or External up to 8MHz.
Minimum I/P Event: 31.25ns
Minimum Pulse Measurement: 31.25ns
Minimum Period Measurement: 150ns
Minimum Gate/Trigger Pulse: 31.25ns

DIGITAL I/O

Digital I/O: Specifications for RS485/RS422 Digital Input 1 and RS485/RS422 Digital Outputs 1-3 are the same as the counter inputs and outputs. See the "RS485/RS422 Input Electrical Characteristics" and "RS485/RS422 Output Electrical Characteristics" sections on the previous page.

INDUSTRIAL I/O PACK COMPLIANCE

Specification: This device meets or exceeds all written Industrial I/O Pack specifications per ANSI/VITA 4 1995 for 8MHz or 32MHz operation for Type I Modules.

Electrical/Mechanical Interface: Single-Size IP Module.

I/O Space: 16-bit and 8-bit

ID Space: 16 and 8-bit; Supports Type 1, 32 bytes per IP (consecutive odd byte addresses). IPAH is used to indicate 32MHz operation (8MHz operation is also supported).

Memory Space: Not implemented in design.

Interrupts: The INTREQ0 signal is used to request interrupts provided by the Counter/Timers.

DMA: Not implemented in design.

APPENDIX

CABLE: MODEL 5025-551-x (Shielded)

Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet (12 feet maximum). Choose shielded cable according to model number. The shielded cable is highly recommended for optimum performance with analog input or output modules.

Application: Used to connect a Model 5025-552 termination panel to the AVME9630/9660 or APC8620/1 non-intelligent carrier board connectors (both have 50-pin connectors).

Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.

Cable: 50-wire flat ribbon cable, 28 gage. Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).

Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).

Keying: Headers at both ends have polarizing key to prevent improper installation.

Schematic and Physical Attributes: See Drawing 4501-463.

Shipping Weight: 1.0 pound (0.5Kg) packaged.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For AVME9630/9660 or APC8620 Boards Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660 3U/6U or APC8620/1 non-intelligent carrier boards (field connectors only) via a flat ribbon cable (Model 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.

Schematic and Physical Attributes: See Drawing 4501-464.

Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.

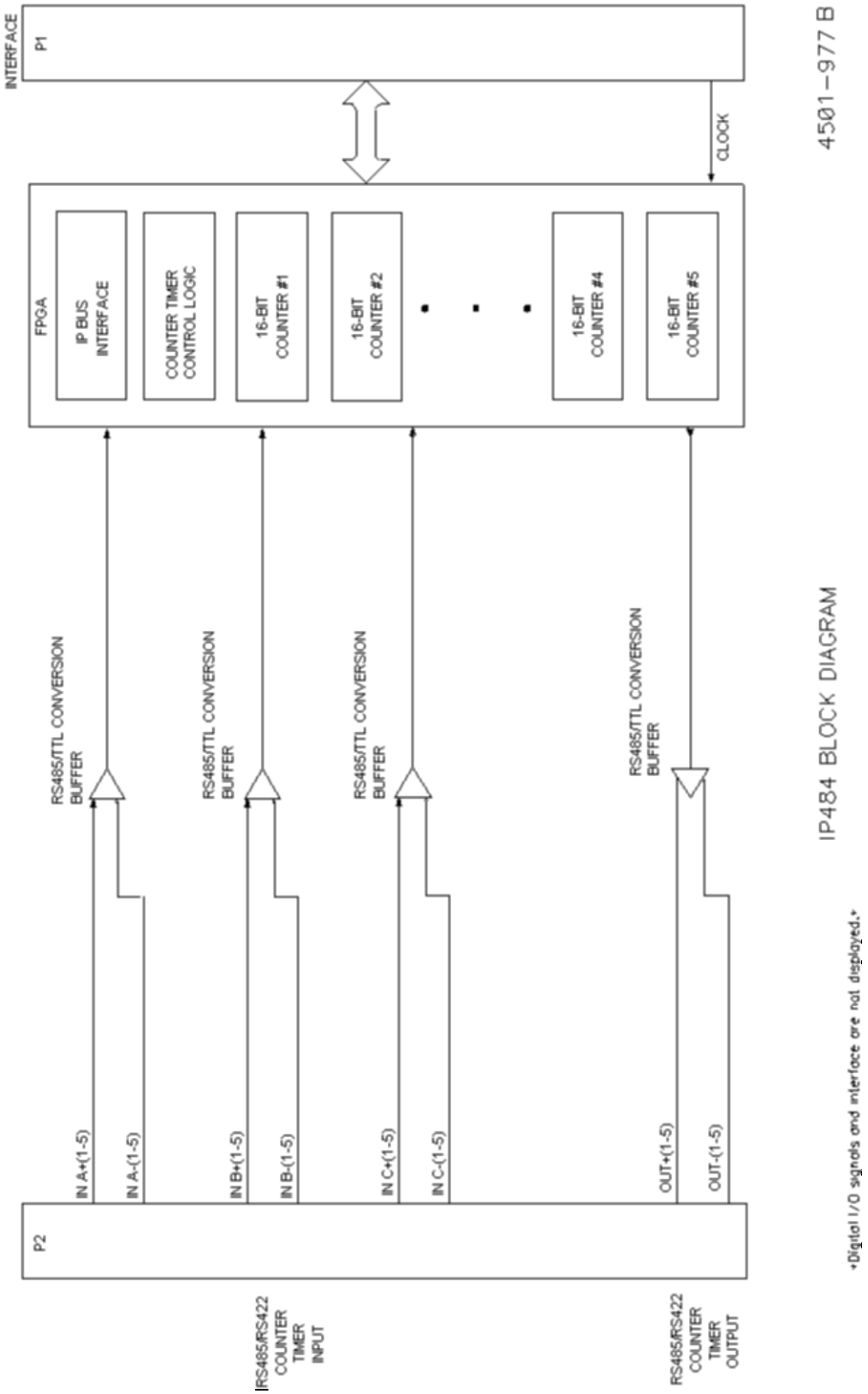
Connections to AVME9630/9660 or APC8620/1: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.

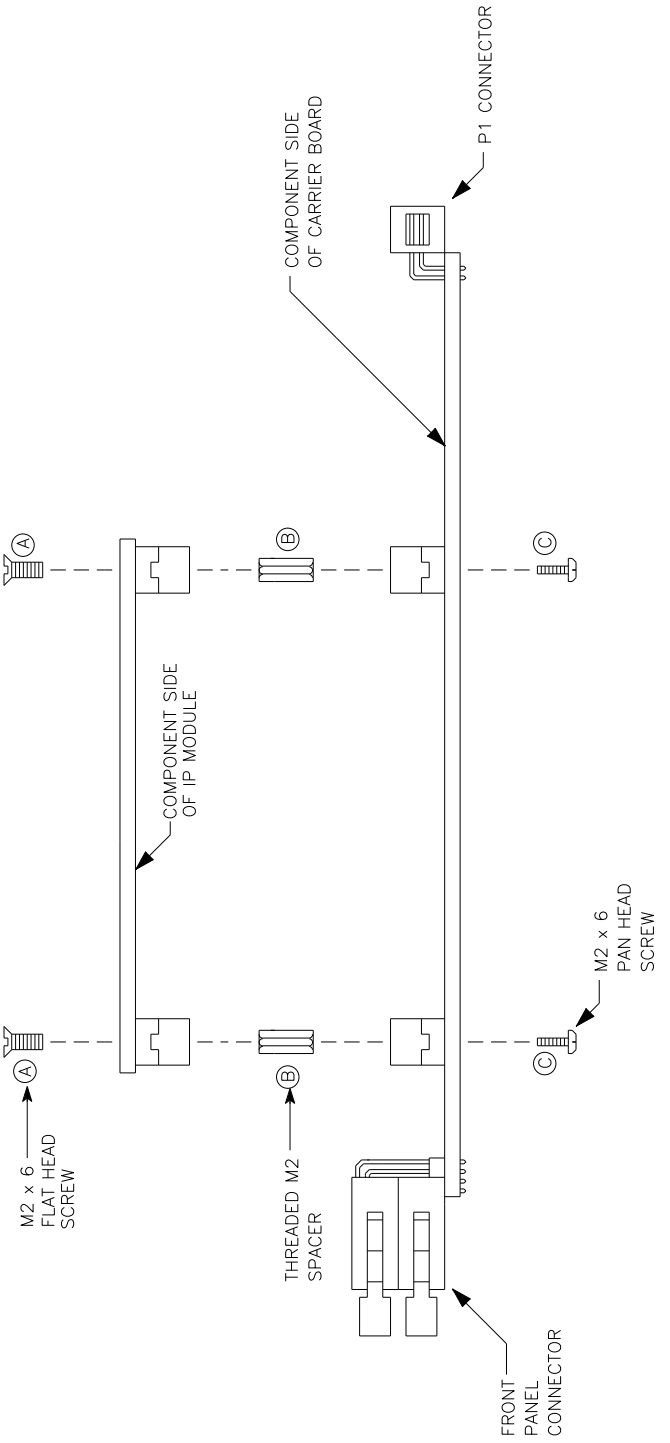
APPENDIX

Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: 0 to +70°C.
Storage Temperature: -25°C to +85°C.
Shipping Weight: 1.25 pounds (0.6kg) packaged.

TRANSITION MODULE: MODEL TRANS-GP

Type: Transition module for AVME9630/9660 boards.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-551-X).
Schematic and Physical Attributes: See Drawing 4501-465.
Field Wiring: 100-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-551-X).
Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-551-X).
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Printed Circuit Board: Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: 0 to +70°C.
Storage Temperature: -25°C to +85°C.
Shipping Weight: 1.25 pounds (0.6Kg) packaged.


INTERFACE
P1
CLOCK
4501-977 B
FPGA
IP BUS INTERFACE
COUNTER TIMER CONTROL LOGIC
16-BIT COUNTER #1
16-BIT COUNTER #2
16-BIT COUNTER #4
16-BIT COUNTER #5
RS485/TTL CONVERSION BUFFER
RS485/TTL CONVERSION BUFFER
RS485/TTL CONVERSION BUFFER
RS485/TTL CONVERSION BUFFER
IN A+(1-5)
IN A-(1-5)
IN B+(1-5)
IN B-(1-5)
IN C+(1-5)
IN C-(1-5)
OUT+(1-5)
OUT-(1-5)
P2
RS485/RS422 COUNTER TIMER INPUT
RS485/RS422 COUNTER TIMER OUTPUT
IP484 BLOCK DIAGRAM
Digital I/O signals and interface are not displayed.



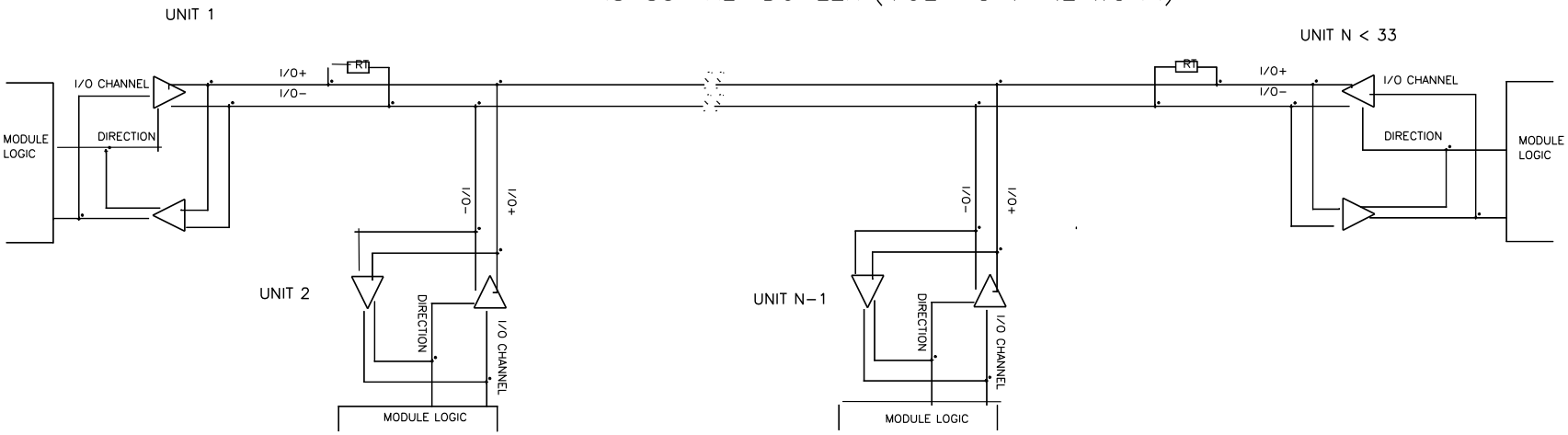
ASSEMBLY PROCEDURE:

1. THREADED SPACERS ARE PROVIDED FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED. THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES). THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.

IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY

4501-434C

RS485 HALF DUPLEX (MULTIPOINT NETWORK)



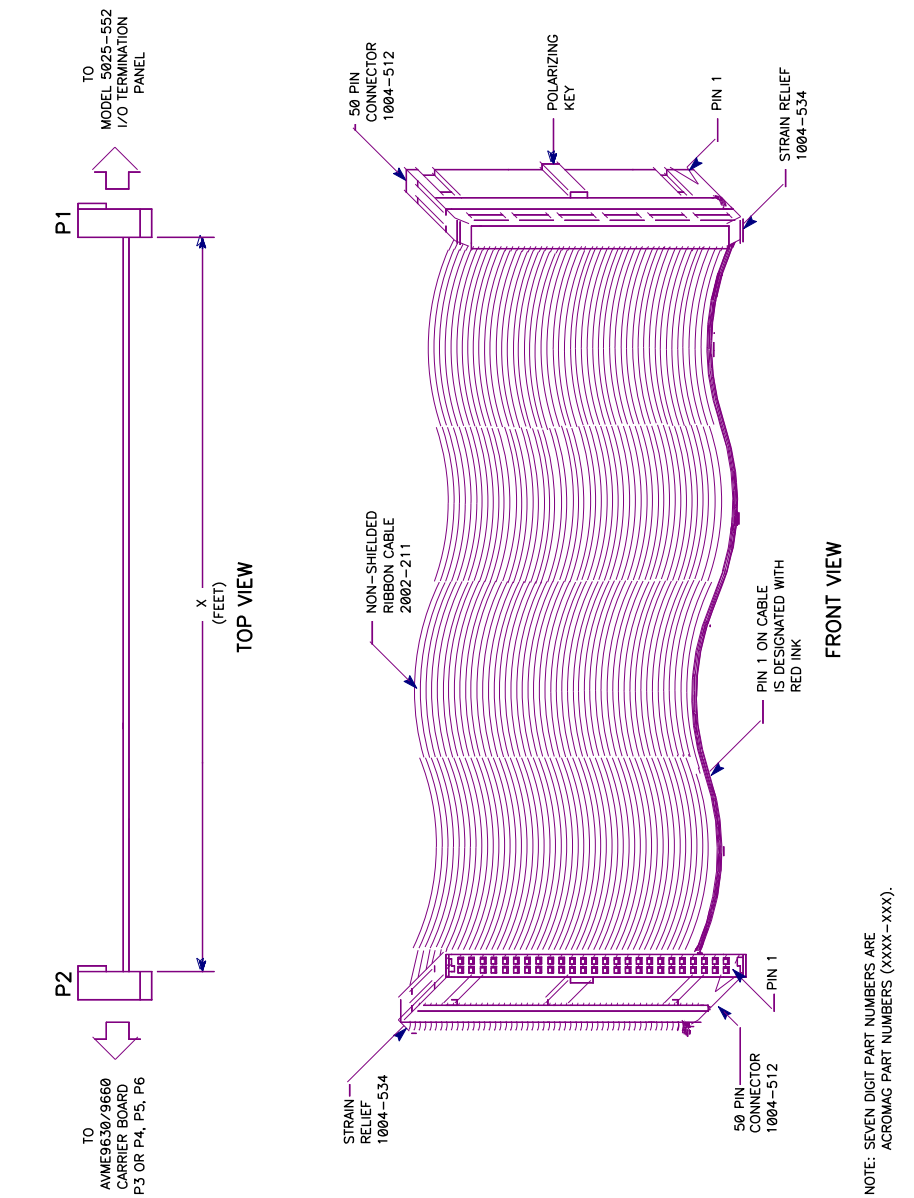
NOTES:

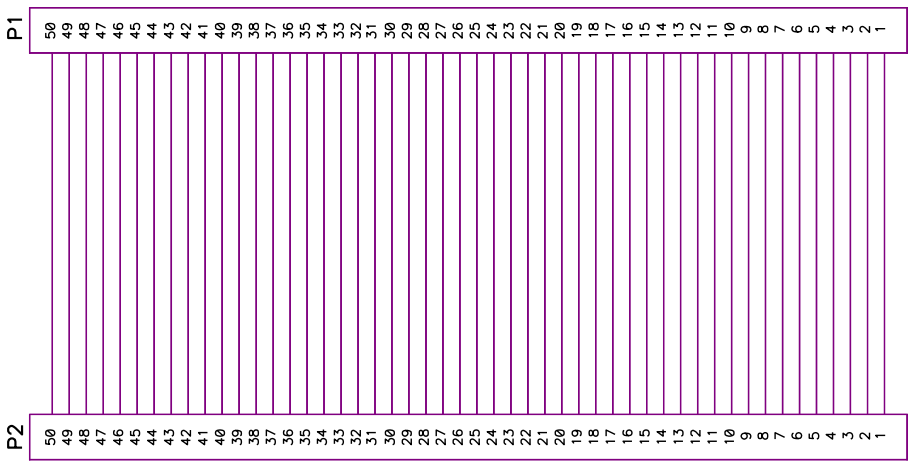
THE RS−485 STANDARD ALLOWS UP TO 32 DRIVER/RECEIVERS TO BE CONNECTED TO A SINGLE BUS. THE BUS IS A HALF DUPLEX BI−DIRECTIONAL BUS, BUT ONLY ONE DRIVER SHOULD BE ACTIVE AT A TIME.

TERMINATION SHOULD BE USED AND ONLY LOCATED AT THE TWO EXTREME ENDS OF THE BUS (NOT AT EACH NODE). THE PURPOSE OF THE TERMINATION IS TO PREVENT ADVERSE TRANSMISSION−LINE REFLECTIONS. TO MINIMIZE POWER DISSIPATION THE TERMINATION RESISTORS CAN BE LEFT OFF. THIS IS POSSIBLE IF THE CABLE IS SHORT AND THE DATA RATE IS LOW. IT IS ALSO POSSIBLE TO MINIMIZE POWER DISSIPATION BY USING AN RC TERMINATION IN PLACE OF THE RESISTOR TERMINATION.

TO MINIMIZE TRANSMISSION−LINE PROBLEMS, ALL NODES CONNECTED TO THE CABLE MUST USE MINIMUM STUB LENGHT CONNECTIONS. IDEALLY ALL NODES SHOULD BE CONNECTED IN A DAISY CHAIN FASHION.

TO MINIMIZE HIGH LEVEL OF EMI THE GROUND WIRE (ON PIN 50) MUST BE USED TO PROVIDE A PATH FOR INDUCED COMMON−MODE NOISE AND CURRENTS. THE GROUND PROVIDES A LOW−IMPEDANCE PATH TO REDUCE EMMISSIONS.

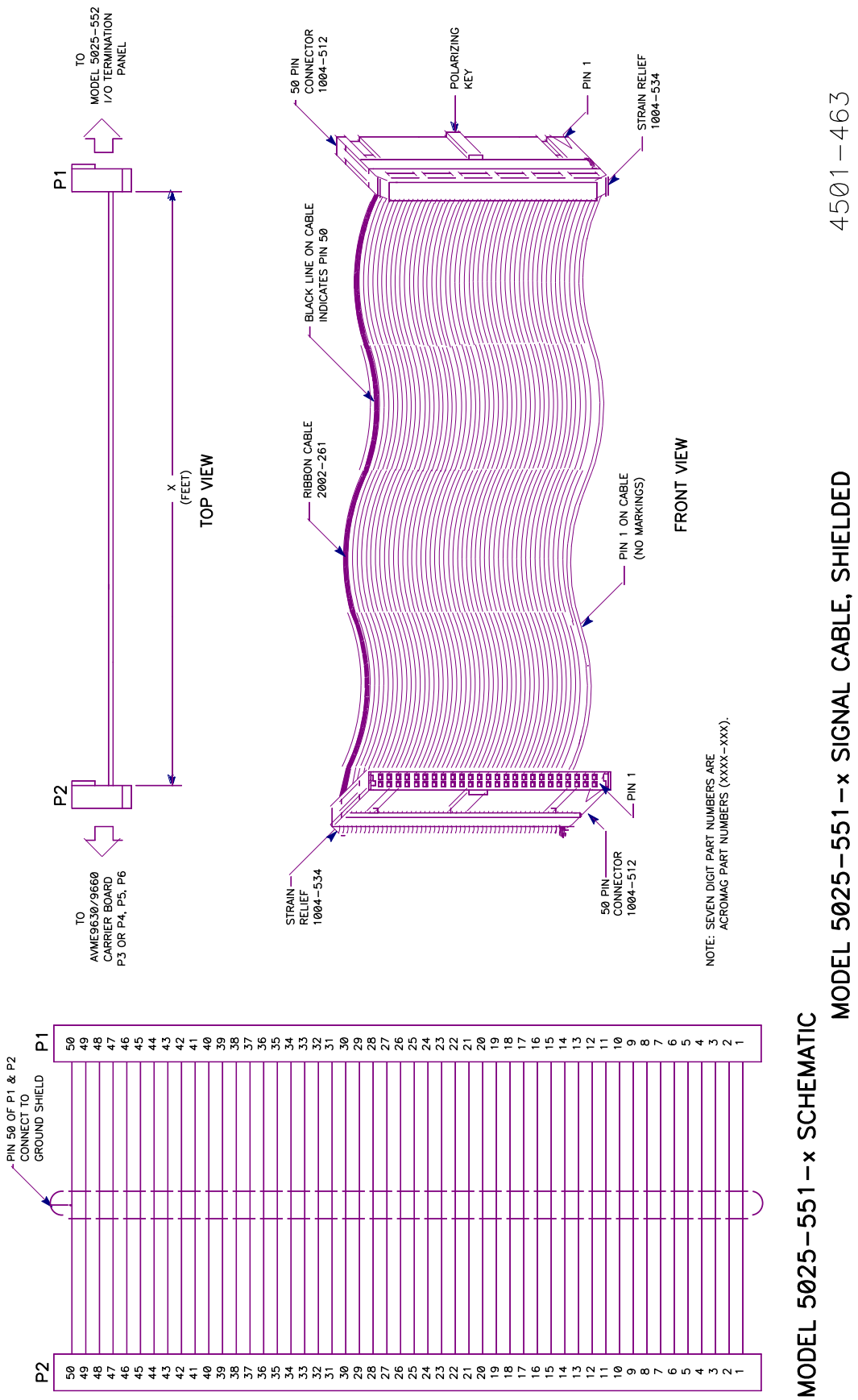


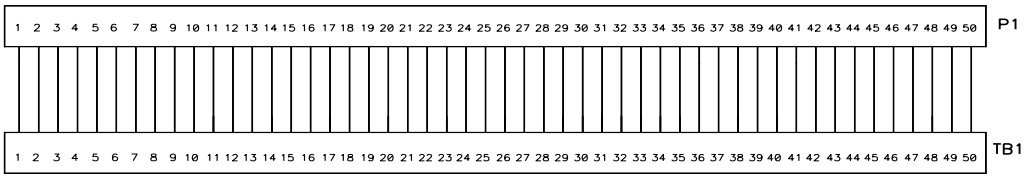


MODEL 5025-550-x SCHEMATIC

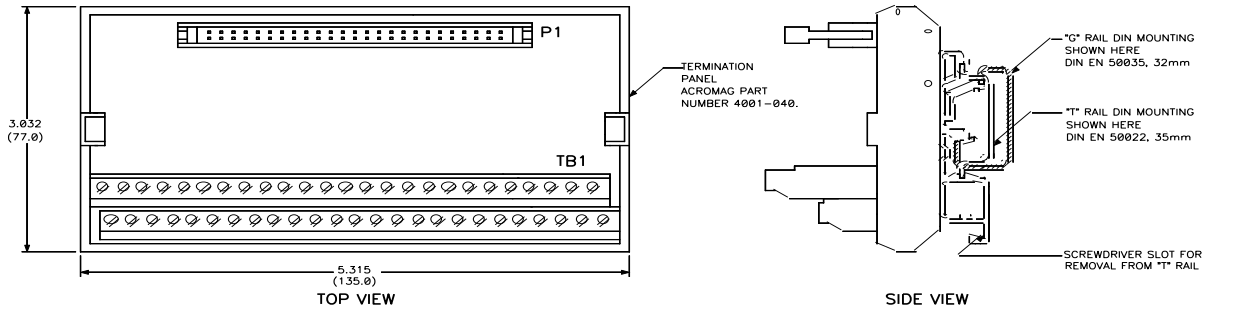
MODEL 5025-550-x SIGNAL CABLE, NON-SHIELDED

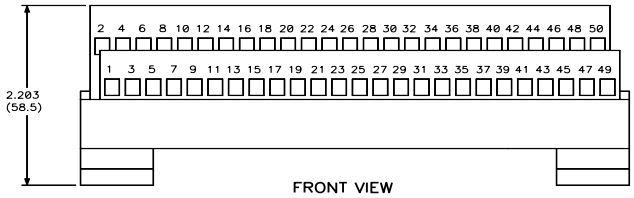
4501-462


TO
MODEL 5025-552
I/O TERMINATION
PANEL
P1
P2
X
(FEET)
TOP VIEW
TO
AVME9630/9660
CARRIER BOARD
P3 OR P4, P5, P6
50 PIN
CONNECTOR
1004-512
POLARIZING
KEY
PIN 1
STRAIN RELIEF
1004-534
BLACK LINE ON CABLE
INDICATES PIN 50
RIBBON CABLE
2002-261
PIN 1 ON CABLE
(NO MARKINGS)
FRONT VIEW
STRAIN
RELIEF
1004-534
50 PIN
CONNECTOR
1004-512
PIN 1
NOTE: SEVEN DIGIT PART NUMBERS ARE
ACROMAG PART NUMBERS (XXXX-XXX).
4501-463
MODEL 5025-551-x SIGNAL CABLE, SHIELDED
MODEL 5025-551-x SCHEMATIC
PIN 50 OF P1 & P2
CONNECT TO
GROUND SHIELD
P1
P2



MODEL 5025-552 TERMINATION PANEL SCHEMATIC

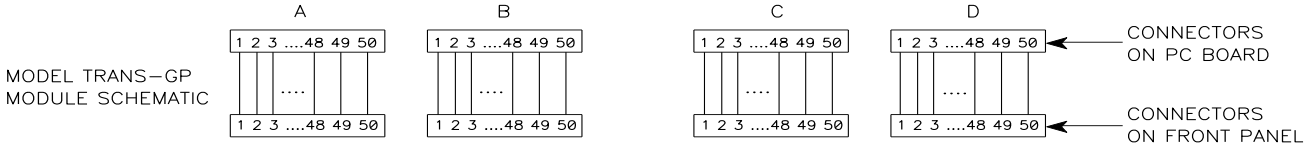


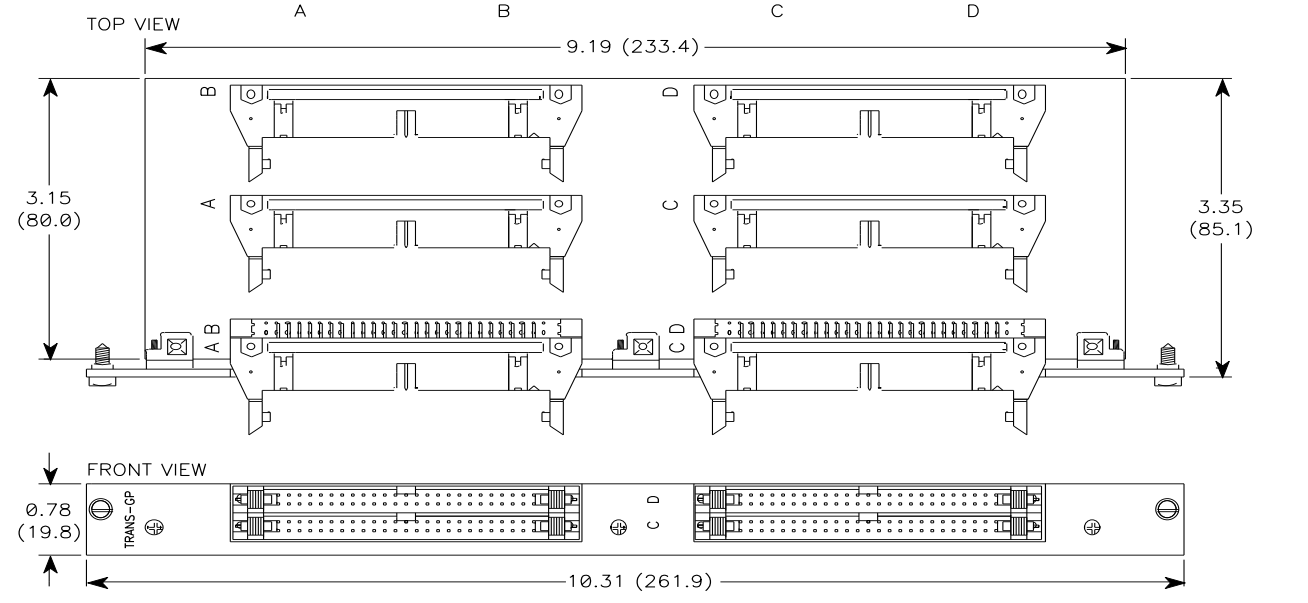


NOTES:
DIMENSIONS ARE IN INCHES (MILLIMETERS).
TOLERANCE: ±0.020 (±0.5).

MODEL 5025-552 TERMINATION PANEL

4501-464A





TRANS-GP MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC

NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).

4501-465A