Series IP445A Industrial I/O Pack
32 Channel Isolated SSR Output Module

USER'S MANUAL

ACROMAG INCORPORATED
30765 South Wixom Road
P.O. BOX 437
Wixom, MI 48393-7037 U.S.A.
Tel: (248) 624-1541
Fax: (248) 624-9234

8501-029

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP445A module is a bus isolated 32-channel output module. The IP445A provides control for 32 solid state relays which are bipolar and may be used to switch positive or negative voltages. Four units may be mounted on a carrier board to provide up to 128 channels of output control in a single system slot. The IP445A offers a variety of features which make it an ideal choice for many industrial and scientific applications as described below.

MODEL	OPERATING TEMPERATURE RANGE
IP445A	0 to +70°C
IP445AE	-40 to +85°C

KEY IP445A FEATURES

- **High Channel Count** - Individual control of up to 32 (SPST-NO) bipolar Solid State Relays (SSR's) is provided. Four units mounted on a carrier board provide 128 channels in a single system slot.
- **High-Speed/0 Wait States -** No wait states are required for all read/write cycles (all cycles complete in 250nS.) and hold states are supported.
- **Optically Isolated -** Individual bipolar SSR's provide isolation. The IP445A contains four groups (ports) of eight channels which include separate port commons to ensure port to port isolation. Individual ports are isolated from each other and from the IP logic.
- **Low-Side or High-Side Switch Configuration -** Each group of eight channels can be connected directly to positive or negative supplies for high (hot) side switching. Alternatively, each group of eight channels can be connected to common for low side switching. Socketed pull-up resistors are provided for low side switching applications.
- **TTL Compatible -** When configured as a low side switch will sink 27mA at 0.4 volts. Sourcing is controlled by the installed pull-up resistor.
- **Power Up & System Reset is Fail-safe** - For safety, the outputs are turned OFF upon power-up and a system reset. Thus, the SSR's will be disabled after a power-up or system reset.
- **Wide Range Bipolar Voltage Outputs -** Outputs are rated from 0 to ±60 volts. The bipolar solid state relays allow both AC and DC switching.
- **Output Readback Function -** Readback buffers are provided that allow the output channel registers to be read back.
- **Loopback Compatible with IP440A Digital Input Module -** The P2 field I/O pin assignments of the IP445A output module correspond with those of the Acromag IP440A Bus Isolated Input module. This provides direct closed-loop monitoring of the output states.

- **No Configuration Jumpers or Switches -** All configuration is performed through software commands with no internal jumpers to configure or switches to set.

INDUSTRIAL I/O PACK INTERFACE FEATURES

- **High density -** Single-size, industry standard, IP module footprint. Four units mounted on a carrier board provide up to 128 isolated output points in a single system slot. Both VMEbus and ISA bus (PC/AT) carriers are supported.
- **Local ID** - Each IP module has its own 8-bit ID signature which can be read via access to the ID space.
- **8-bit I/O** - Port register Read/Write is performed through 8 or 16-bit data transfer cycles in the IP module I/O space.
- **High Speed with No Wait States** - Access times for all data transfer cycles are described in terms of "wait" states - 0 wait states are required for all read and write operations of this model. See Specification section for detailed information.

SIGNAL INTERFACE PRODUCTS

(See Appendix for more information on compatible products)

This IP module will mate directly to any industry standard IP carrier board (including Acromag AVME9630/9660 3U/6U non-intelligent VMEbus carrier boards). Additionally, Acromag's APC8600 ISA bus (PC/AT) carrier board is also supported. A wide range of other Acromag IP modules are also available to serve your signal conditioning and interface needs.

The following cables and termination panels are also available. Consult your carrier board documentation for the correct interface product part numbers to ensure compatibility with your carrier board.

Cables

Model 5025-551-X (Shielded Cable), or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9630/9660, or other compatible carrier boards, to Model 5025-552 termination panels. The "-X" suffix of the model number is used to indicate the length in feet.

The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.

Termination Panels:

Model 5025-552: A DIN-rail mountable panel that provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9630/9660, or other compatible carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

Transition Module:

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from a VMEbus card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. It connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within the card cage, via flat 50-pin ribbon cable (cable Model 5025-550 or 5025-551).

INDUSTRIAL I/O PACK SOFTWARE LIBRARY

Acromag provides an Industrial I/O Pack Software Library diskette (Model IPSW-LIB-M03, MSDOS format) to simplify communication with the board. Example software functions are provided for both VMEbus and ISA bus (PC/AT) applications. All functions are written in the "C" programming language and can be linked to your application. For more details, refer to the "README.TXT" file in the root directory on the diskette and the "INFO445.TXT" file in the appropriate "IP445" subdirectory off of "\VMEIP" or "\PCIP", according to your carrier.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, Inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-434 and your IP module documentation for configuration and assembly instructions. Module IP445A digital output boards have no hardware jumpers or switches to configure. Software configurable control registers are provided for control of all modes of operation. Refer to section 3 for programming details.

This module is built with socketed output pull-up resistors installed. These may be used when the SSR's are applied as low side switches. Resistor values may be changed if needed, and the resistors may be removed for high side switching (see IP445A Resistor Location Figure 1).

CONNECTORS

IP Field I/O Connector (P2)

P2 provides the field I/O interface connections for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly.

P2 pin assignments are unique to each IP model (see Table 2.1) and normally correspond to the pin numbers of the field I/O interface connector on the carrier board (you should verify this for your carrier board).

Table 2.1: IP445A Field I/O Pin Connections (P2)

Pin Description	Number		Pin Description	Number	
OD00	1		OD20	26	**P**
OD01	2		OD21	27	**O**
OD02	3	**P**	OD22	28	**R**
OD03	4	**O**	OD23	29	**T**
User Supply 0	5	**R**	User Com Out 2	30	**2**
OD04	6	**T**	OD24	31	
OD05	7		OD25	32	
OD06	8	**0**	OD26	33	**P**
OD07	9		OD27	34	**O**
User Com Out 0	10		User Supply 3	35	**R**
OD08	11		OD28	36	**T**
OD09	12		OD29	37	
OD10	13	**P**	OD30	38	**3**
OD11	14	**O**	OD31	39	
User Supply 1	15	**R**	User Com Out 3	40	
OD12	16	**T**	Not Used	41	
OD13	17		Not Used	42	
OD14	18	**1**	Not Used	43	
OD15	19		Not Used	44	
User Com Out 1	20		Not Used	45	
OD16	21	**P**	Not Used	46	
OD17	22	**O**	Not Used	47	
OD18	23	**R**	Not Used	48	
OD19	24	**T**	Not Used	49	
User Supply 2	25	**2**	Not Used	50	

The output channels of this module are divided into four ports of eight channels each. All channels within a port share a common signal connection with each other. Isolation is provided between the ports and the IP logic. In addition, bus isolation is provided between ports.

P2 pin assignments are arranged to be compatible with similar Acromag models. This model is directly loopback compatible with the Acromag Model IP440A 32-Channel Digital Input Board. Likewise, pin assignments are identical to those of Acromag Model IP405 40-Channel Digital Output Boards for channels 0-31, except for the user supply connections. This model (remove socketed pull-up resistors) may also interface with industry accepted I/O panels, termination panels, and relay racks when used with the Acromag Model 5025-655 I/O Adapter Card. However, relay racks are usually isolated in which case it would probably be more efficient to use the non-isolated IP405 module. Consult the factory for information on these and other compatible products.

Refer to Figure 2 for example field output connections. See Figure 3 for loopback connections to Acromag Model IP440A Input Modules.

Note that the outputs of this module are bipolar, and may be connected in any direction with respect to the port common. Further, do not confuse port commons with signal ground. For the IP445A, port common only infers that this lead is connected common to the 8 outputs of the port (a separate common for each port). **The port commons of the IP445A output module and IP440A input module are normally not connected together for loopback interconnection (see Figure 3).**

Grounding and Noise Considerations

Output lines of the IP445A are optically isolated between the logic and field output connections. Likewise, separate port commons ensure port-to-port isolation. Consequently, the field I/O connections are isolated from the carrier board and backplane, thus minimizing the negative effects of ground bounce, impedance drops, and switching transients. However, care should be taken in designing installations to avoid inadvertently compromising isolation, or creating ground loops which can cause noise pickup and reduce overall system reliability.

IP Logic Interface Connector (P1)

P1 of the IP module provides the logic interface to the mating connector on the carrier board. The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.2). The IP Logic Interface connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly.

Table 2.2: Standard Logic Interface Connections (P1)

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSEL*	29
D01	5	***DMAReq0****	30
D02	6	MEMSEL*	31
D03	7	***DMAReq1****	32
D04	8	IntSel*	33
D05	9	***DMAck0****	34
D06	10	IOSEL*	35
D07	11	***RESERVED***	36
D08	12	A1	37
D09	13	***DMAEnd****	38
D10	14	A2	39
D11	15	***ERROR****	40
D12	16	A3	41
D13	17	***INTReq0****	42
D14	18	A4	43
D15	19	***INTReq1****	44
BS0*	20	A5	45
BS1*	21	***STROBE****	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	***RESERVED***	49
GND	25	GND	50

An Asterisk (*) is used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by this IP Model.

3.0 PROGRAMMING INFORMATION

IP IDENTIFICATION SPACE - (Read Only, 32 Odd-Byte Addresses)

Each IP module contains identification (ID) information that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID space. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP445A ID information does not contain any variable (e.g. unique calibration) information. ID space bytes are addressed using only the odd addresses in a 64 byte block (on the “Big Endian” VMEbus). Even addresses are used on the “Little Endian” PC ISA bus. The IP445A ID space contents are shown in Table 3.1. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID space. Execution of an ID space read requires 0 wait states.

Table 3.1: IP445A ID Space Identification (ID) ROM

Hex Offset From ID ROM Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All IP's have 'IPAC'
03	P	50	
05	A	41	
07	C	43	
09		A3	Acromag ID Code
0B		09	IP Model Code[1]
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		0C	Total Number of ID ROM Bytes
17		8C	CRC
19 to 3F		yy	Not Used

Notes (Table 3.1):

1. The IP model number is represented by a two-digit code within the ID space (the IP445A model is represented by 09 Hex).
2. Execution of an ID space read requires 0 wait states.

I/O SPACE ADDRESS MAP

This board is addressable in the Industrial Pack I/O space to control the 32 channels of digital output to the field.

The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1 to A6, but the IP445A uses only a portion of this space. The I/O space address map for the IP445A is shown in Table 3.2. Note that the base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space. Accesses may be performed on an 8 or 16-bit basis but only D0-D7 are driven. D08-D15 are not used but will normally read high due to pull-up resistors on the carrier board.

The following table shows the memory map for the IP445. Data is read and written to one of four groups (ports) as designated by the address.

Table 3.2: IP445A I/O Space Address (Hex) Memory Map[2]

Base Addr +	MSB D15 D08	LSB D07 D00	Base Addr +
00	Not Used	Control Register	**01**
02	Not Used	Output Port 0 CH07 ↔ CH00	**03**
04	Not Used	Output Port 1 CH15 ↔ CH08	**05**
06	Not Used	Output Port 2 CH23 ↔ CH16	**07**
08	Not Used	Output Port 3 CH31 ↔ CH24	**09**
0A	Not Used ⇓		**0B**
7E	Not Used		**7F**

Notes (Table 3.2):

1. The IP will not respond to addresses that are "Not Used".
2. All Register accesses implement 0 wait state data transfers.

This memory map reflects byte accesses using the “Big Endian” byte ordering format. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses. The Intel x86 family of microprocessors uses the opposite convention, or “Little Endian” byte ordering. Little Endian uses even-byte addresses to store the low-order byte. As such, installation of this module on a PC carrier board will require the use of the even address locations to access the lower 8 data bits while on a VMEbus carrier use of odd address locations are required.

REGISTER DEFINITIONS

Control Register, (Write) - (Base + 00H)

This write only register is used to reset all output ports to 0 (SSR switches OFF).

Table 3.3: Control Register

BIT	FUNCTION
0	1 = Software Reset
1 to 7	Not Used

Port Output Registers (Read/Write, 03H, 05H, 07H, and 09H)

Four registers are provided to control 32 possible output points. Data can be read from or written to one of four groups of eight output lines (Ports 0-3), as designated by the address and read/write signals. Each port assigns the least significant data line (D0) to the least significant output line of the port grouping (e.g. OD00 for port 0 to D0).

REGISTER 0 (OUTPUT SWITCHES 00 THROUGH 07):

MSB							LSB
07	06	05	04	03	02	01	00
CH07							CH00

REGISTER 1 (OUTPUT SWITCHES 08 THROUGH 15):

MSB							LSB
07	06	05	04	03	02	01	00
CH15							CH08

REGISTER 2 (OUTPUT SWITCHES 16 THROUGH 23):

MSB							LSB
07	06	05	04	03	02	01	00
CH23							CH16

REGISTER 3 (OUTPUT SWITCHES 24 THROUGH 31):

MSB							LSB
07	06	05	04	03	02	01	00
CH31							CH24

Write a zero to each channel’s position to turn the corresponding SSR OFF. Write a one to each channel’s position to turn the corresponding SSR ON.

Each output channel register can be conveniently read back for verification purposes. For critical control applications, it is recommended that outputs be directly fed back to an input point and the input point monitored (loopback I/O). Acromag Model IP440A 32-channel isolated input modules can be used to implement loopback output monitoring with this model (see Figure 3).

On power-up, hardware reset, or software reset, the ports are reset to 0 forcing the outputs (SSR’s) to be OFF.

IP445A PROGRAMMING

Acromag provides you with the Industrial I/O Pack Software Library diskette (Model IPSW-LIB-M03, MSDOS format) to make communication with the board easy. Example software functions are provided for both ISAbus (PC/AT) and VMEbus applications. All functions are written in the “C” programming language and can be linked to your application. For more details, refer to the “README.TXT” file in the root directory on the diskette and the “INFO445.TXT” file in the appropriate “IP445” subdirectory off of “\VMEIP” or “\PCIP”, according to your carrier.

4.0 THEORY OF OPERATION

This section contains information regarding the basic functionality of the circuitry used on the IP445. Refer to the Block Diagram shown in Figure 4 as you review this material.

LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1 (refer to Table 2.2). The P1 interface also provides +5V power to the module. Note that data lines D08..D15, BS1*, the DMA control, interrupt requests (INTREQ0∗ and INTREQ1∗), ERROR∗, STROBE∗ and +/-12V power signals are not used.

A Field Programmable Gate-Array (FPGA) installed on the IP Module provides an interface to the carrier board per IP Module specification revision 0.7.1. The interface to the carrier board allows complete control of all IP445A functions. This logic includes: address decoding, I/O and ID read/write control circuitry, and ID space implementation. With regard to throughput, 0 wait states are required for read and write operations.

Address decoding of the six IP address signals A(1:6) is implemented in the FPGA, in conjunction with the IP select signals, to identify access to the IP module's ID or I/O space. In addition, the byte strobe BS0∗ is decoded to identify a low byte data transfer.

OUTPUT PORTS

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.1). Individual Solid State Relays (SSR's) for each channel isolate the field from the control logic for the IP445. Channels are isolated from each other in groups of eight. There are eight channels to a group or port. Because the output lines of a single port share a common connection, individual outputs are not isolated from each other within the same port. However, separate port commons are provided to facilitate port-to-port isolation.

32 Single Pole Single Throw - Normally Open (SPST-NO, "1 Form A") SSR outputs are controlled by this module. Each group of eight channels can be connected directly to positive or negative supplies for high (hot) side switching. Alternatively, each group of eight channels can be connected to common for low side switching. Socketed pull-up resistors are provided for low side switching applications. These resistors should be removed if high side switching is needed. In low side switching applications the resistor values can be changed (e.g. lower values will provide a faster pull-up while a higher values will keep power dissipation from becoming a problem at higher voltages) - see Specifications in Chapter 6 for details.

The SSR's are controlled by output registers within the FPGA. Writing a '1' to the output register will turn the switch ON (closed-circuit) while writing a '0' will turn it OFF (open-circuit). Readback of the output state is accomplished by reading the output registers. However, for complete confidence in output control, loopback should be performed. This may be accomplished using the IP440A isolated digital input module (refer to Figure 3).

The SSR's employed are rated for a much higher voltage than specified. However, the field connector and printed circuit board foil spacings limit applied voltages to +/-60VDC or AC peak. Each port (group of eight channels) has a single common. Since the connectors and cables are rated to 1A maximum per pin, then each port is limited to that total current. Thus, the sum of currents conducted by the 8 channels must stay below that total (see specifications in Chapter 6 for details). The low on resistance of the SSR's helps reduce their power dissipation when they conduct high currents; however, given the large number of channels on the board adequate air circulation must be maintained. The SSR's used in the IP445A are very rugged and contain built-in current limiting for their protection. They provide clean, bounce free switching and can replace electromechanical relays in many applications. SSR switching speeds are comparable to electromechanical relays (1mS. typical) but are slow compared to high speed optocouplers.

Output operation is "Fail-safe". That is, the outputs are always OFF upon power-up reset, and are automatically cleared following a software (control register) or system software reset. This is done for safety reasons to ensure reliable control of the output state under all conditions.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

GENERAL SPECIFICATIONS

Operating Temperature.....0 to +70°C.
-40 to +85°C (E Version)
Relative Humidity.....5-95% non-condensing.
Storage Temperature.....-40 to +150°C.

Physical Configuration.....Single Industrial I/O Pack Module.
Length.....3.880 inches (98.5 mm).
Width.....1.780 inches (45.2 mm).
Board Thickness.....0.062 inches (1.59 mm).
Max Component Height.....0.314 inches (7.97 mm).

Connectors:
P1 (IP Logic Interface).....50-pin female receptacle header (AMP 173279-3 or equivalent).
P2 (Field I/O).....50-pin female receptacle header (AMP 173279-3 or equivalent).

Power Requirements:
+5 Volts (±5%) All On.....150mA, Typical
200mA, Maximum.
+5 Volts (±5%) All Off.....5mA, Typical
8mA, Maximum.
±12 Volts (±5%) from P1.....0mA (Not Used).

Isolation.....Logic and field connections are optically isolated by SSR's. Individual ports are also isolated from each other. However, output lines of individual ports share a common connection and are not isolated from each other. Separate port commons are provided to facilitate port-to-port isolation. IP Logic and field lines are isolated from each other for voltages up to 250VAC, or 354V DC on a continuous basis (unit will withstand a 1500V AC dielectric strength test for one minute without breakdown). This complies with test requirements outlined in ANSI/ISA-S82.01-1988 for the voltage rating specified. Port to port isolation is less critical and is specified as 100V DC.
Isolation Spacing.....Printed circuit board minimum isolation spacings are as follows:
Port-to-Logic:
0.024" Minimum (inner layer),
0.071" Minimum (external layer).
Port-to-Port:
0.012" Minimum (inner layer),
0.040" Minimum (external layer).

DIGITAL (SSR) OUTPUTS

Output Channel Configuration.....32 isolated Solid State Relay (SSR) outputs supporting AC or DC (high or low side switching) operation.
SPST-NO, "1 Form A" contacts.
"OFF" Voltage Range.....0 to +/-60V DC or peak AC.
Output "OFF" Leakage Current....1uA Maximum (over temp.).
Output "ON" Current Range.....140mA Maximum continuous (up to 1A total per port)
No deration required at elevated ambients.
Output ON Resistance.....15Ω, Maximum (25°C).
Output Current Limiting.....480mA Maximum.
Turn-ON Time.....1mS. Typical, 2mS. Maximum.
Turn-OFF Time.....1mS. Typical, 2mS. Maximum.
Reset Condition.....All output SSR's OFF.
Output Pull-up Resistors.....Socketed 4.7KΩ (used in low side switching applications).
See Figure 1: Res. Loc. Dwg.
Calculate resistor power for user supplied voltage (Power = V^2/R).
Limit power to 0.1 Watt per resistor (21.7V max. @ 4.7KΩ).
Remove or insert higher value (consult factory) for higher voltages. Install lower value (check power) to obtain faster, stronger pull-up. Remove for high side switching applications.
TTL Compatibility.....Yes, used as low side switch can sink 27mA. @ 0.4V Maximum; source 500uA @ 2.4V Min. with 4.7KΩ pull-up to 5V supply.
Resistance to RFI.....No digital upsets occur for field strengths up to 10V per meter at 27MHz, 151MHz, & 460MHz per SAMA PMC 33.1 test procedures.
Resistance to EMI.....Unit has been tested with no digital upsets under the influence of EMI from switching solenoids, commutator motors, and drill motors.
ESD Protection.....Output lines are protected from ESD voltages to ± 4KV**,** typical. May degrade 4.7K pullups by approximately 5%.

INDUSTRIAL I/O PACK COMPLIANCE

Specification.....This module meets or exceeds all written Industrial I/O Pack specifications per revision 0.7.1.
Electrical/Mechanical Interface...Single-Size IP Module.
IP Data Transfer Cycle Types Supported:
Input/Output (IOSel*).....D16 or D08 least significant read/write of port data.
ID Read (IDSel*).....32 x 8 ID ROM read on D0..D7.
Access Times (8MHz Clock):
ID ROM Read.....0 wait states (250ns cycle).
Port Registers (R/W).....0 wait states (250ns cycle).

APPENDIX

CABLE: MODEL 5025-550-x (Non-Shielded)
MODEL 5025-551-x (Shielded)

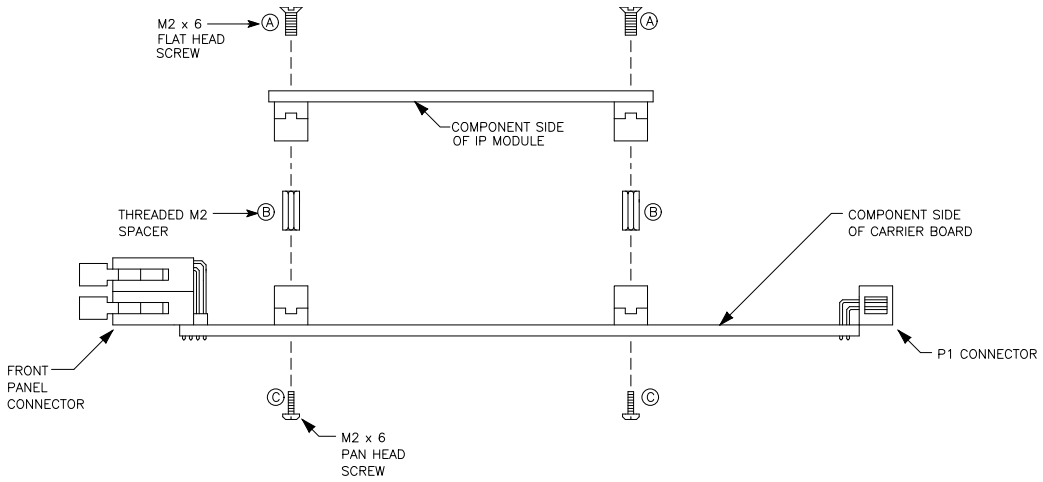
Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet (12 feet maximum). Choose shielded or unshielded cable according to model number. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.
Application: Used to connect a Model 5025-552 termination panel to the AVME9630/9660 non-intelligent carrier board A-D connectors (both have 50-pin connectors).
Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50-wire flat ribbon cable, 28 gage. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent). Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).
Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).
Keying: Headers at both ends have polarizing key to prevent improper installation.
Schematic and Physical Attributes: For Non-Shielded cable model, see Drawing 4501-462. For Shielded cable model, see Drawing 4501-463.
Shipping Weight: 1.0 pound (0.5Kg) packaged.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For AVME9630/9660 Boards
Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660 3U/6U non-intelligent carrier boards (A-D connectors only) via a flat ribbon cable (Model 5025-550-x or 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Connections to AVME9630/9660: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-550-x or 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight : 1.25 pounds (0.6kg) packaged.

TRANSITION MODULE: MODEL TRANS-GP

Type: Transition module for AVME9630/9660 boards.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-551-X).
Schematic and Physical Attributes: See Drawing 4501-465.
Field Wiring: 100-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-551-X).
Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-551-X).
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Printed Circuit Board: Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +85°C.
Storage Temperature: -55°C to +105°C.
Shipping Weight: 1.25 pounds (0.6Kg) packaged.



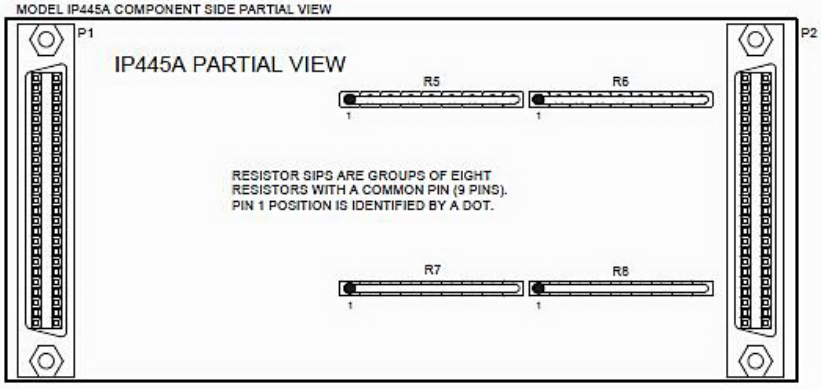
ASSEMBLY PROCEDURE:

1. THREADED SPACERS ARE PROVIDED FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED. THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES). THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.

IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY 4501-434C

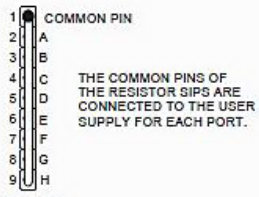
IP445A PULLUP RESISTOR LOCATION DRAWING
FOR REMOVAL AND REPLACEMENT WHERE REQUIRED

MODEL IP445A COMPONENT SIDE PARTIAL VIEW



PULL-UP RESISTOR SIPS ARE MOUNTED IN SOCKETS AND CAN BE REMOVED IF REQUIRED.

RESISTOR SIPS ARE DIVIDED AS SHOWN



DETAIL "A"

MODULE IS SHIPPED WITH ALL PULL-UP SIP RESISTORS INSTALLED

NOTES CONCERNING SOCKETED PULLUP RESISTORS R5-R8:

1. ALL OUTPUT PORTS INCLUDE 4.7K OHM PULLUP RESISTORS TO THE USER SUPPLY FOR EACH PORT IN THE FORM OF SIP RESISTORS AS SHOWN. THESE SIP RESISTORS ARE INSTALLED IN SOCKETS AND MAY BE MODIFIED AS REQUIRED.
2. R5-R8 ARE USED IN LOW SIDE SWITCHING APPLICATIONS ONLY (REMOVE WHEN SSR's ARE USED IN HIGH (HOT) SIDE SWITCHING APPLICATIONS).
3. SEE CHAPTER 6 "SPECIFICATIONS" FOR MORE INFORMATION ON PULL-UP RESISTOR VALUE CHANGES.

SIP RESISTOR IDENTIFICATION

SIP	VALUE	FUNCTION	PORT
R5:A...R5:H	4.7K OHM	OD07...OD00 PULLUP	PORT 0
R6:A...R6:H	4.7K OHM	OD08...OD15 PULLUP	PORT 1
R7:A...R7:H	4.7K OHM	OD23...OD16 PULLUP	PORT 2
R8:A...R8:H	4.7K OHM	OD24...OD31 PULLUP	PORT 3

Figure 1

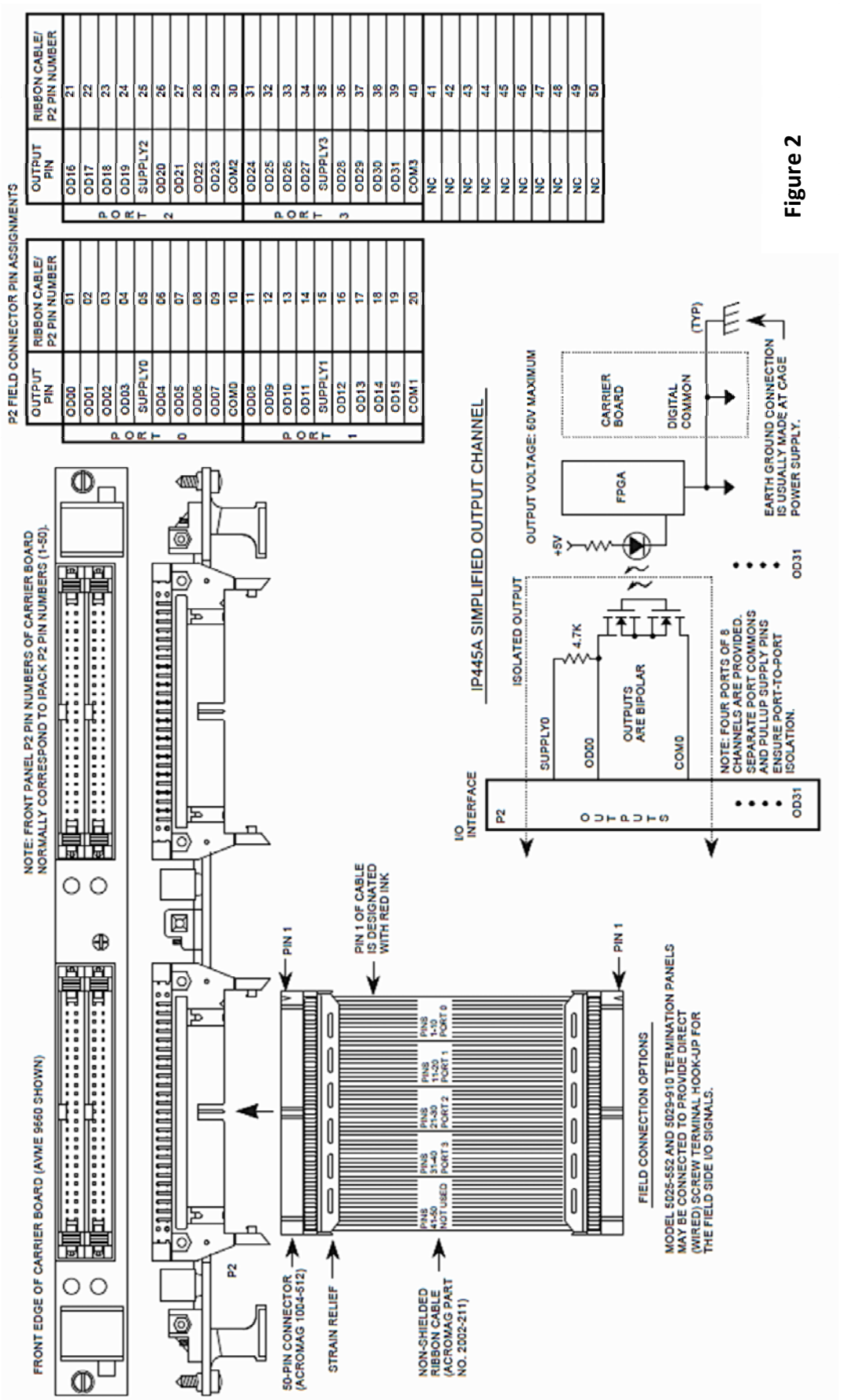

P2 FIELD CONNECTOR PIN ASSIGNMENTS
PORT 0
OUTPUT PIN
RIBBON CABLE/ P2 PIN NUMBER
OD00 01
OD01 02
OD02 03
OD03 04
SUPPLY0 05
OD04 06
OD05 07
OD06 08
OD07 09
COM0 10
PORT 1
OD08 11
OD09 12
OD10 13
OD11 14
SUPPLY1 15
OD12 16
OD13 17
OD14 18
OD15 19
COM1 20
PORT 2
OD16 21
OD17 22
OD18 23
OD19 24
SUPPLY2 25
OD20 26
OD21 27
OD22 28
OD23 29
COM2 30
PORT 3
OD24 31
OD25 32
OD26 33
OD27 34
SUPPLY3 35
OD28 36
OD29 37
OD30 38
OD31 39
COM3 40
NC 41
NC 42
NC 43
NC 44
NC 45
NC 46
NC 47
NC 48
NC 49
NC 50
NOTE: FRONT PANEL P2 PIN NUMBERS OF CARRIER BOARD NORMALLY CORRESPOND TO IPACK P2 PIN NUMBERS (1-50).
FRONT EDGE OF CARRIER BOARD (AVME 9660 SHOWN)
P2
50-PIN CONNECTOR (ACROMAG 1004-512)
STRAIN RELIEF
NON-SHIELDED RIBBON CABLE (ACROMAG PART NO. 2002-211)
PIN 1
PIN 1 OF CABLE IS DESIGNATED WITH RED INK
PINS 1-10 PORT 0
PINS 11-20 PORT 1
PINS 21-30 PORT 2
PINS 31-40 PORT 3
PINS 41-50 NOT USED
PIN 1
FIELD CONNECTION OPTIONS
MODEL 5025-552 AND 5029-910 TERMINATION PANELS MAY BE CONNECTED TO PROVIDE DIRECT (WIRED) SCREW TERMINAL HOOK-UP FOR THE FIELD SIDE I/O SIGNALS.
IP445A SIMPLIFIED OUTPUT CHANNEL
I/O INTERFACE
P2
OUTPUTS
SUPPLY0
OD00
COM0
OD31
ISOLATED OUTPUT
4.7K
OUTPUTS ARE BIPOLAR
NOTE: FOUR PORTS OF 8 CHANNELS ARE PROVIDED. SEPARATE PORT COMMONS AND PULLUP SUPPLY PINS ENSURE PORT-TO-PORT ISOLATION.
OUTPUT VOLTAGE: 60V MAXIMUM
+5V
FPGA
CARRIER BOARD
DIGITAL COMMON
(TYP)
EARTH GROUND CONNECTION IS USUALLY MADE AT CAGE POWER SUPPLY.

Figure 2

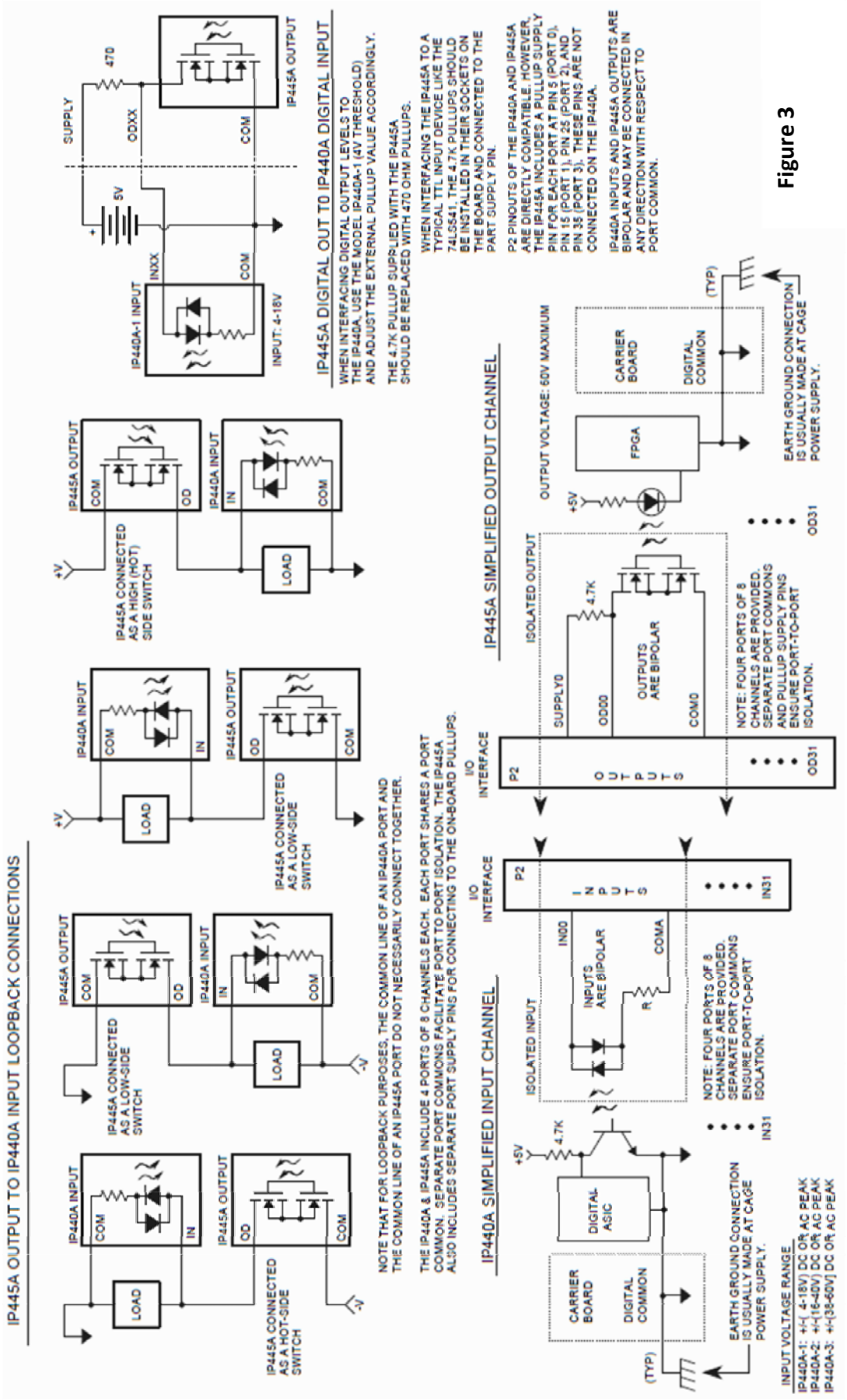

IP445A OUTPUT TO IP440A INPUT LOOPBACK CONNECTIONS
IP440A INPUT
IP445A OUTPUT
LOAD
IP445A CONNECTED AS A HOT-SIDE SWITCH
IP445A CONNECTED AS A LOW-SIDE SWITCH
-V
NOTE THAT FOR LOOPBACK PURPOSES, THE COMMON LINE OF AN IP440A PORT AND THE COMMON LINE OF AN IP445A PORT DO NOT NECESSARILY CONNECT TOGETHER.
THE IP440A & IP445A INCLUDE 4 PORTS OF 8 CHANNELS EACH. EACH PORT SHARES A PORT COMMON. SEPARATE PORT COMMONS FACILITATE PORT TO PORT ISOLATION. THE IP445A ALSO INCLUDES SEPARATE PORT SUPPLY PINS FOR CONNECTING TO THE ON-BOARD PULLUPS.
+V
IP445A CONNECTED AS A HIGH (HOT) SIDE SWITCH
IP440A SIMPLIFIED INPUT CHANNEL
I/O INTERFACE
P2
ISOLATED INPUT
INPUTS ARE BIPOLAR
IN00
COMA
R
4.7K
+5V
DIGITAL ASIC
CARRIER BOARD
DIGITAL COMMON
(TYP)
EARTH GROUND CONNECTION IS USUALLY MADE AT CAGE POWER SUPPLY.
IN31
NOTE: FOUR PORTS OF 8 CHANNELS ARE PROVIDED. SEPARATE PORT COMMONS ENSURE PORT-TO-PORT ISOLATION.
INPUT VOLTAGE RANGE
IP440A-1: +/-[4-18V] DC OR AC PEAK
IP440A-2: +/-[16-40V] DC OR AC PEAK
IP440A-3: +/-[36-60V] DC OR AC PEAK
IP445A SIMPLIFIED OUTPUT CHANNEL
OUTPUT VOLTAGE: 60V MAXIMUM
ISOLATED OUTPUT
OUTPUTS ARE BIPOLAR
SUPPLY0
OD00
COM0
OD31
FPGA
+5V
IP445A DIGITAL OUT T0 IP440A DIGITAL INPUT
WHEN INTERFACING DIGITAL OUTPUT LEVELS TO THE IP440A, USE THE MODEL IP440A-1 (4V THRESHOLD) AND ADJUST THE EXTERNAL PULLUP VALUE ACCORDINGLY.
THE 4.7K PULLUP SUPPLIED WITH THE IP445A SHOULD BE REPLACED WITH 470 OHM PULLUPS.
WHEN INTERFACING THE IP445A TO A TYPICAL TTL INPUT DEVICE LIKE THE 74LS541, THE 4.7K PULLUPS SHOULD BE INSTALLED IN THEIR SOCKETS ON THE BOARD AND CONNECTED TO THE PART SUPPLY PIN.
P2 PINOUTS OF THE IP440A AND IP445A ARE DIRECTLY COMPATIBLE. HOWEVER, THE IP445A INCLUDES A PULLUP SUPPLY PIN FOR EACH PORT AT PIN 5 (PORT 0), PIN 15 (PORT 1), PIN 25 (PORT 2), AND PIN 35 (PORT 3). THESE PINS ARE NOT CONNECTED ON THE IP440A.
IP440A INPUTS AND IP445A OUTPUTS ARE BIPOLAR AND MAY BE CONNECTED IN ANY DIRECTION WITH RESPECT TO PORT COMMON.
IP440A-1 INPUT
INPUT: 4-18V
INXX
COM
SUPPLY
470
ODXX
5V
IP445A OUTPUT

Figure 3

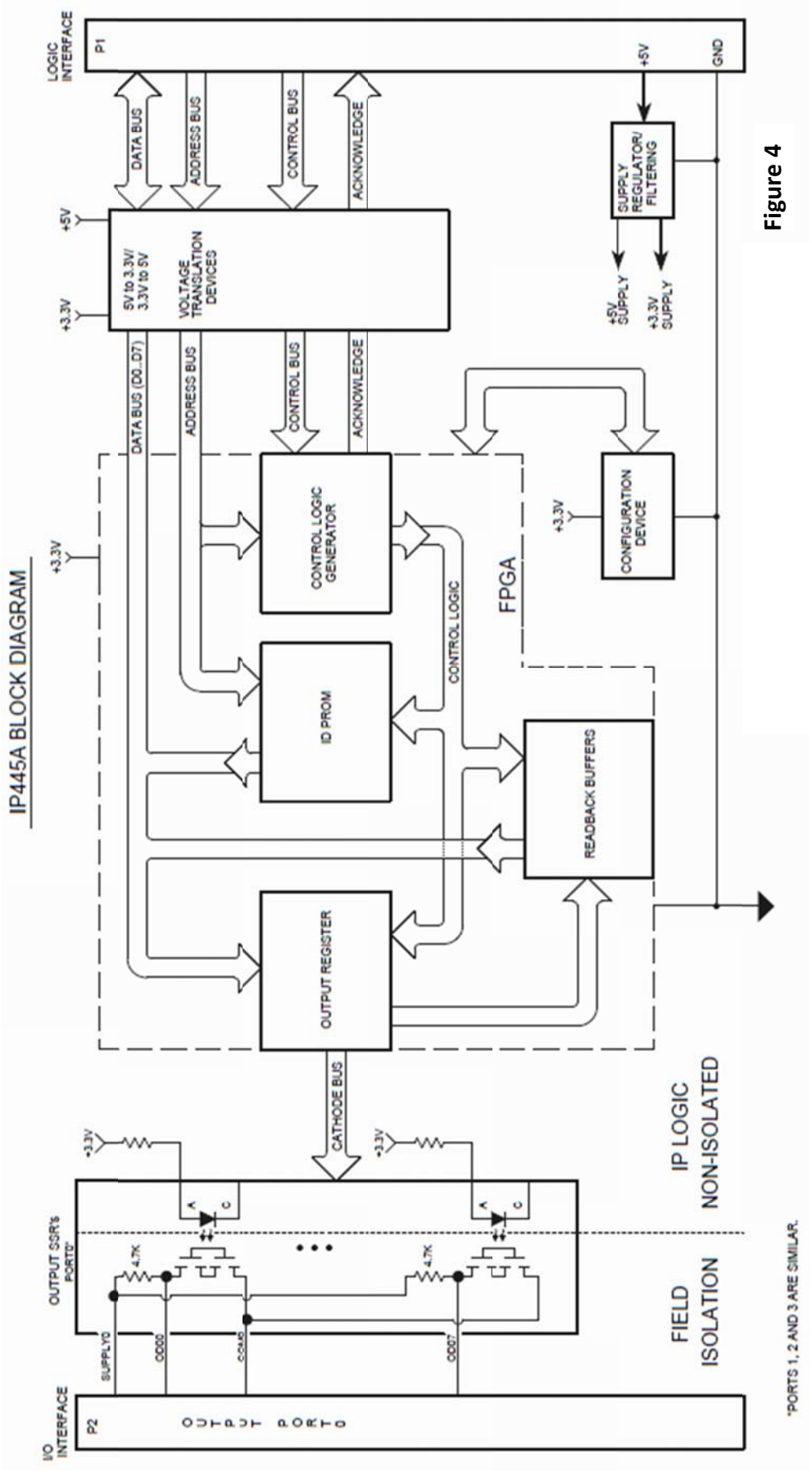
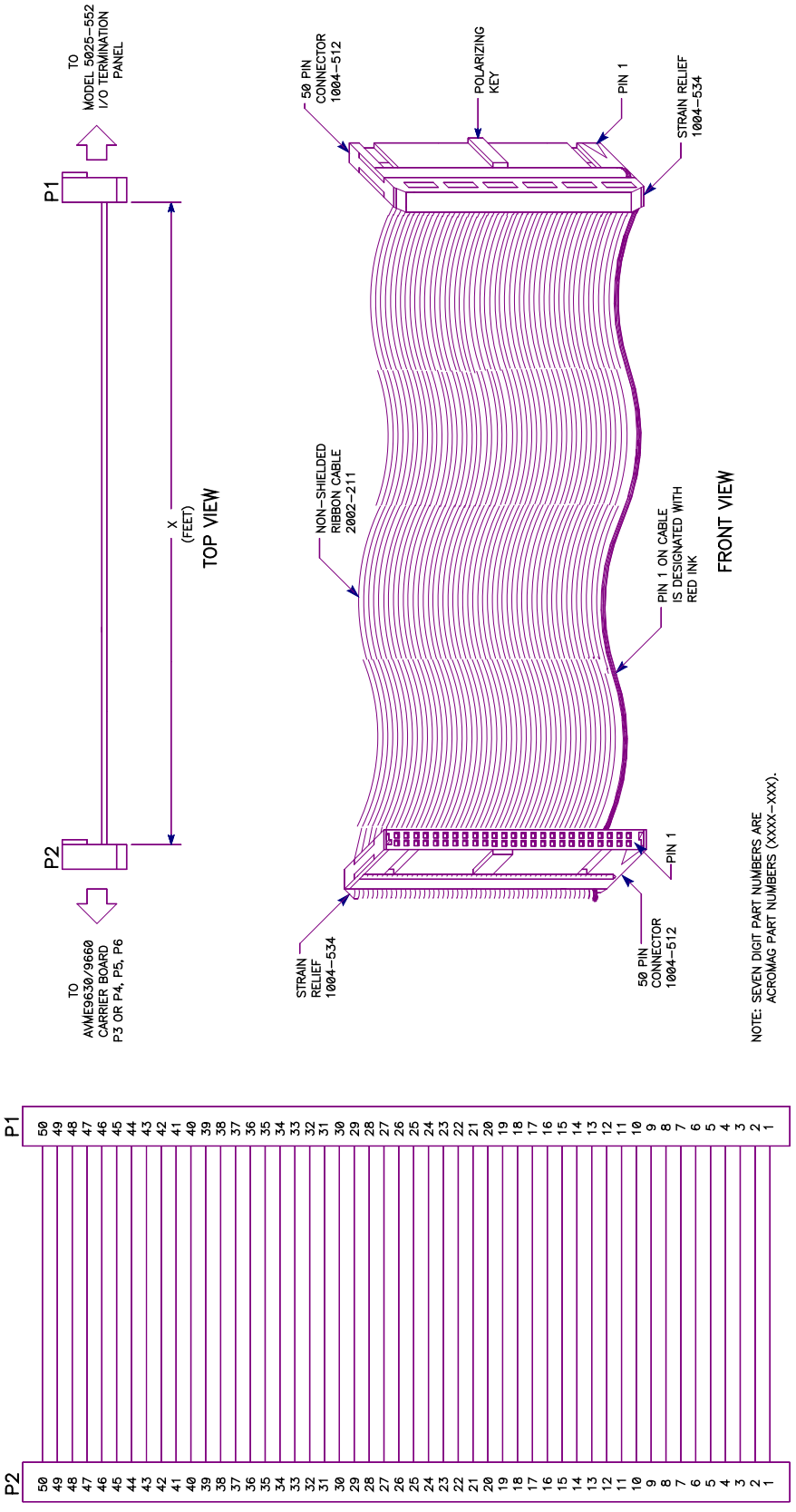

IP445A BLOCK DIAGRAM
LOGIC INTERFACE
P1
+5V
GND
DATA BUS
ADDRESS BUS
CONTROL BUS
ACKNOWLEDGE
SUPPLY REGULATOR/ FILTERING
+5V SUPPLY
+3.3V SUPPLY
5V to 3.3V/ 3.3V to 5V VOLTAGE TRANSLATION DEVICES
DATA BUS (D0..D7)
FPGA
CONTROL LOGIC GENERATOR
CONFIGURATION DEVICE
ID PROM
CONTROL LOGIC
READBACK BUFFERS
OUTPUT REGISTER
CATHODE BUS
IP LOGIC
NON-ISOLATED
FIELD
ISOLATION
OUTPUT SSR's PORT0*
4.7K
SUPPLY0
COM0
COM5
COM7
I/O INTERFACE
P2
OUTPUT PORT 0
*PORTS 1, 2 AND 3 ARE SIMILAR.

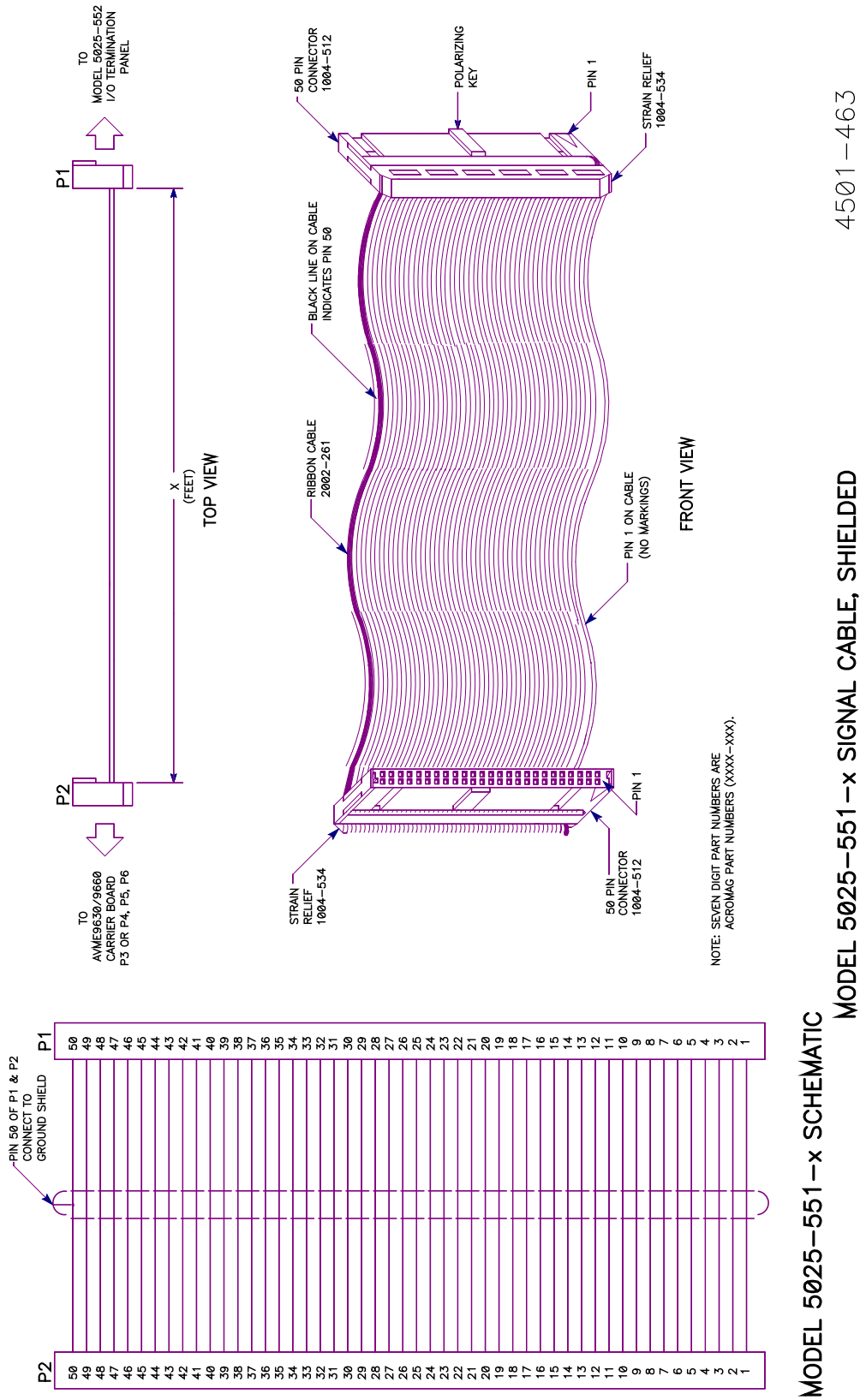
Figure 4



MODEL 5025-550-x SCHEMATIC

MODEL 5025-550-x SIGNAL CABLE, NON-SHIELDED

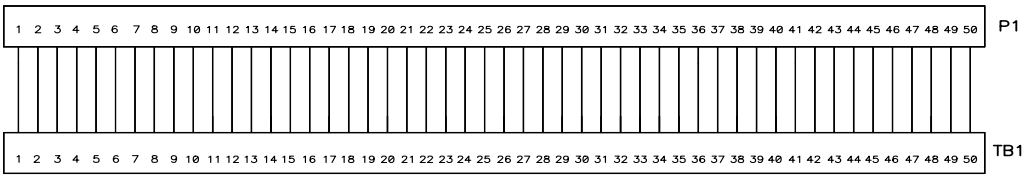
4501-462



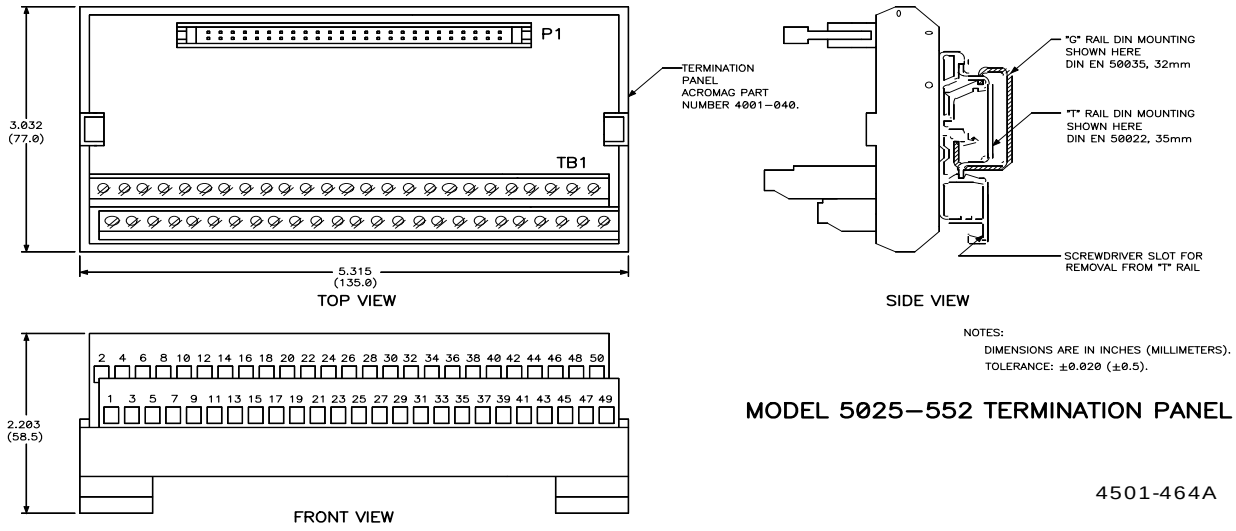
MODEL 5025-551-x SCHEMATIC

MODEL 5025-551-x SIGNAL CABLE, SHIELDED

4501-463



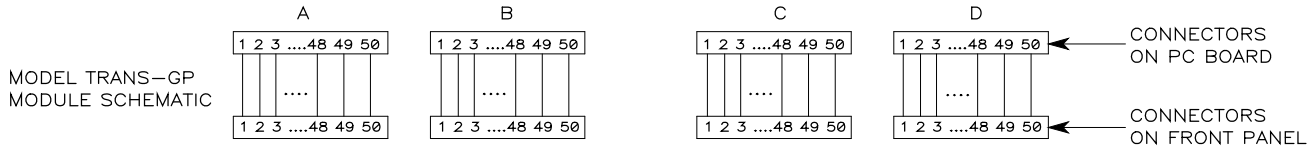
MODEL 5025–552 TERMINATION PANEL SCHEMATIC

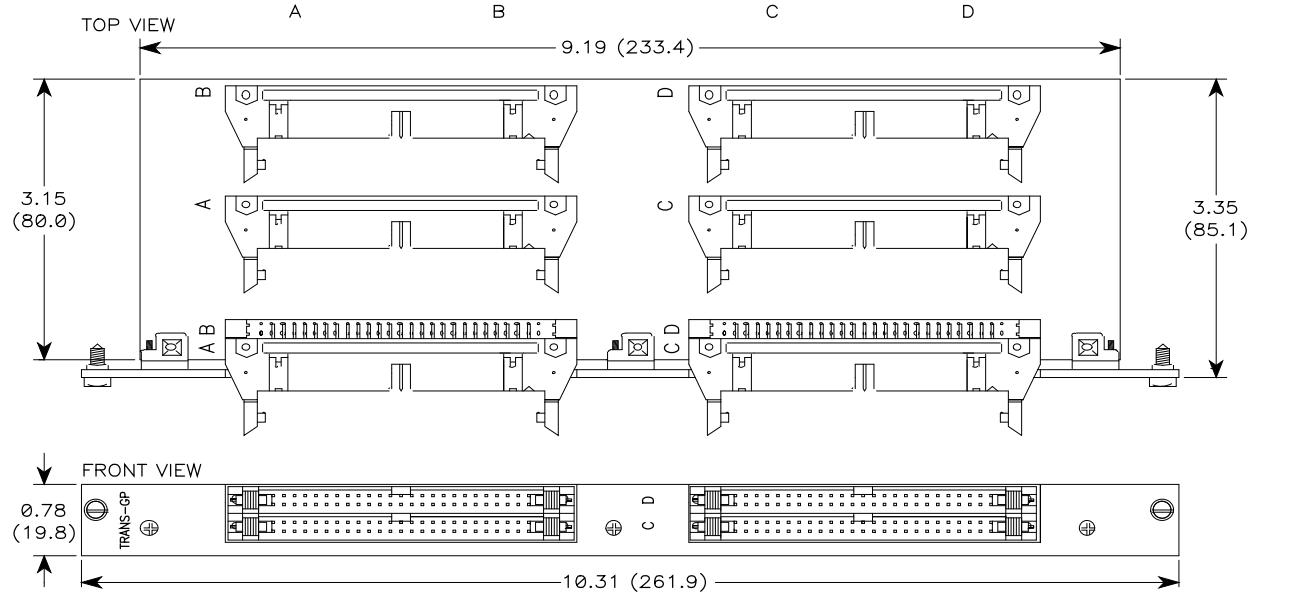


NOTES:
DIMENSIONS ARE IN INCHES (MILLIMETERS).
TOLERANCE: ±0.020 (±0.5).

MODEL 5025–552 TERMINATION PANEL

4501-464A





TRANS–GP MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC

NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).

4501–465A