Acromag®

Series IP405 Industrial I/O Pack
40-Channel Digital Output Board

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP405 module is a 40-channel, open-drain output board. This model provides control for 40 low-side switches (open-drain MOSFETS), with up to 160 switches per 6U-VMEbus system slot. The IP405 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its high channel density and is an ideal choice for a wide range of industrial control applications that require high-density, high-reliability, and high-performance at a low cost.

MODEL	OPERATING TEMPERATURE RANGE
IP405	0 to +70°C
IP405E	-40 to +85°C

KEY IP405 FEATURES

- **High Channel Count** - Individual control of up to 40 low-side switches (open-drain) is provided. Four units mounted on a carrier board provide 160 channels in a single system slot.
- **Power Up & System Reset is Failsafe** - For safety, the outputs are always OFF upon power-up and cleared after a system reset. Unlike some competitive units, gate pulldowns are included to ensure that the outputs will not turn on momentarily when load power is applied with no power to the IP module.
- **True Logic** - Outputs operate using True-Logic (1=ON/SWITCH CLOSED, 0=OFF/SWITCH OPEN).
- **Low R_{dsON} (0.2Ω Maximum) -** Low drain-to-source ON resistance ensures TTL logic-low compatibility at high currents and reduces power dissipation.
- **High Voltage Outputs** - Outputs are rated for operation up to 60V DC. Output drivers are internally voltage-clamped.
- **High Output Current** - individual output channels may sink up to 1A DC continuous (up to 10A total, all channels combined), or 250mA DC (with all 40 channels ON). No deration of output current is required at elevated ambient temperatures.
- **Output Readback Function** - Readback buffers are provided that allow the output channel registers to be read back.
- **Loopback Compatible with IP400** - The P2 field I/O pin assignments of the IP405 output module correspond with those of the Acromag IP400 input module. This provides direct interface “loopback“ capability between these models.

INDUSTRIAL I/O PACK INTERFACE FEATURES

- **High density -** Single-size, industry standard, IP module footprint. Four units mounted on a carrier board provide up to 160 open drain outputs in a single system slot.
- **Local ID** - Each IP module has its own 8-bit ID PROM which is accessed via data transfers in the "ID Read" space.

- **16-bit I/O** - Channel register Read/Write is performed through 16-bit data transfer cycles in the IP module I/O space.
- **High Speed** - Access times for all data transfer cycles are described in terms of "wait" states - 0 wait states are required for readback, 1 wait state for a write (see specifications for detailed information).

SIGNAL INTERFACE PRODUCTS
(See Appendix for more information on compatible products)

This IP module will mate directly to any industry standard IP carrier board (including Acromag AVME9630/9660 3U/6U non-intelligent carrier boards). Consult the documentation of your carrier board to ensure compatibility with the following interface products (since all connections to field signals are made through the carrier board which passes them to the individual IP modules).

Cables:

Model 5025-551-X (Shielded Cable), or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9630/9660, or other compatible carrier boards, to Model 5025-552 termination panels. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.

Termination Panel:

Model 5025-552: A DIN-rail mountable panel that provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9630/9660, or other compatible carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

Transition Module:

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from the card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. It connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within the card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).

INDUSTRIAL I/O PACK SOFTWARE LIBRARY

Acromag provides an Industrial I/O Pack Software Library diskette (Model IPSW-LIB-M03, MSDOS format) to simplify communication with the board. All functions are written in the “C” programming language and can be linked to your application. Refer to the “README.TXT” file in the root directory and the “INFO405.TXT” file in the “IP405” subdirectory on the diskette for more details.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, Inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-434 and your IP module documentation for configuration and assembly instructions. Model IP405 Output Boards have no jumpers or switches to configure.

CONNECTORS

IP Field I/O Connector (P2)

P2 provides the field I/O interface connector for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly. P2 pin assignments are unique to each IP model (see Table 2.1) and normally correspond to the pin numbers of the front-panel, field I/O interface connector on the carrier board (you should verify this for your carrier board).

Table 2.1: IP405 Field I/O Pin Connections (P2)

Pin Description	Number	Pin Description	Number
OD00	1	OD25	32
OD01	2	OD26	33
OD02	3	OD27	34
OD03	4	OD28	36
OD04	6	OD29	37
OD05	7	OD30	38
OD06	8	OD31	39
OD07	9	OD32	41
OD08	11	OD33	42
OD09	12	OD34	43
OD10	13	OD35	44
OD11	14	OD36	46
OD12	16	OD37	47
OD13	17	OD38	48
OD14	18	OD39	49
OD15	19	COMMON	5
OD16	21	COMMON	10
OD17	22	COMMON	15
OD18	23	COMMON	20
OD19	24	COMMON	25
OD20	26	COMMON	30
OD21	27	COMMON	35
OD22	28	COMMON	40
OD23	29	COMMON	45
OD24	31	COMMON	50

Model IP405 output modules share the same P2 field I/O pin assignments as Acromag Model IP400 40-channel input modules and IP408 32-channel I/O modules (for channels 0-31 & common), making these models directly compatible for “loopback” output control.

Output Noise and Grounding Considerations

The output channels of this model are the open drains of mosfets with a common source connection. The IP405 is non-isolated between the logic and field I/O grounds since output common is electrically connected to the IP module ground. Consequently, the field I/O connections are not isolated from the carrier board and backplane. Two ounce copper ground plane foil has been employed in the design of this model to help minimize the effects of ground bounce, impedance drops, and switching transients. However, care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

This device is capable of switching many channels at high currents. Additionally, the nature of the IP interface is inherently inductive. The outputs of this model are protected to voltages up to 60V. As such, when switching inductive loads, it is important that careful consideration be given to the use of snubber devices to shunt the reverse emf that develops when the current through an inductor is interrupted. Filtering and bypassing at the load may also be necessary. Additionally, proper grounding with thick conductors is essential. Interface cabling and ground wiring should be kept as short as possible. The use of an interposing relay may also be desireable for isolating the load, raising the drive capability, or providing additional system protection. Please refer to Drawing 4501-516 for examples of these connections and proper output and grounding connections.

IP Logic Interface Connector (P1)

P1 of the IP module provides the logic interface to the mating connector on the carrier board. This connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly.

The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.2).

Table 2.2: Standard Logic Interface Connections (P1)

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSEL*	29
D01	5	***DMAReq0****	30
D02	6	MEMSEL*	31
D03	7	***DMAReq1****	32
D04	8	IntSel*	33
D05	9	***DMAck0****	34
D06	10	IOSEL*	35
D07	11	***RESERVED***	36
D08	12	A1	37
D09	13	***DMAEnd****	38
D10	14	A2	39
D11	15	***ERROR****	40
D12	16	A3	41
D13	17	***INTReq0****	42
D14	18	A4	43
D15	19	***INTReq1****	44
BS0*	20	A5	45
BS1*	21	***STROBE****	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	***RESERVED***	49
GND	25	GND	50

Asterisk (*) is used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by this IP Model.

3.0 PROGRAMMING INFORMATION

ADDRESS MAPS

This board is addressable in the Industrial Pack I/O space to control the ON/OFF states of 40 individual low-side switches. The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1..A6, but the IP405 only uses a portion of this space. The I/O space address map for the IP405 is shown in Table 3.1. Note the base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space. All accesses are performed on a 16-bit word basis (D0..D15).

Table 3.1: IP405 R/W Space Address (Hex) Memory Map

Hex Base Address+	DATA WORD D15 - - - - - - - - - - - - - - - - D00
00	R/W - Digital Output Channel Register A CH15 ↔ CH0
02 ↓ 0E	Repeated Digital Output Channel Register A[1]
10	R/W - Digital Output Channel Register B CH31 ↔ CH16
12 ↓ 1E	Repeated Digital Output Channel Register B[1]
20	R/W - Digital Output Channel Register C (See Note 2) CH39 ↔ CH32
22 ↓ 2E	Repeated Digital Output Channel Register C[1,2]
30 ↓ 7E	NOT USED[3]

Notes (Table 3.1):

1. Registers appear in multiple locations in the memory map because of simplified address decoding (these locations can be ignored).
2. The upper 8 bits of Digital Output Channel Register C are “Don’t Care” - it makes no difference what is written to it. Pull-ups on the carrier board data bus will cause these bits to always read High (1’s).
3. The IP will not respond to addresses that are "Not Used".
4. All Reads are 0 wait states. All Writes are 1 wait state.

IP Digital Output Registers A, B, & C (Read/Write)

When the digital output channel data registers are written to, the value written is represented at the corresponding output channels. A “0” bit means that the corresponding output switch is OPEN (OFF). Writing a “1” bit CLOSES the corresponding output switch (turns it ON).

Read/Write control for 40 output channels numbered 0 through 39 is provided. Channel state Read/Write operations use 16-bit words with the lower ordered bits corresponding to the lower-numbered channels for the register of interest (see below). Register A controls output channels 0 through 15. Register B controls output channels 16 through 31. Register C controls output channels 32 through 39 (the upper 8 bits of register C are “Don’t Care”).

REGISTER A (OUTPUT SWITCHES 0 THROUGH 15):

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CH15							CH8	CH7							CH0

REGISTER B (OUTPUT SWITCHES 16 THROUGH 31):

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
CH31							CH24	CH23							CH16

REGISTER C (OUTPUT SWITCHES 32 THROUGH 39):

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
X	X	X	X	X	X	X	X	CH39							CH31

Each output channel register can be conveniently read back for verification purposes. Pullups on the carrier board data bus will cause the unused upper 8 bits of register C to read back as high (1’s). For critical control applications, it is recommended that outputs be directly fed back to an input point and the input point monitored (loopback I/O). Acromag Model IP400 40-channel input modules can be used to implement loopback output control with this model.

All outputs are OFF (switch OPEN) following a power-on reset, and are immediately cleared (OFF) following a system reset.

IP Identification PROM - (Read Only, 32 Odd-Byte Addresses)

Each IP module contains an identification (ID) PROM that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID PROM. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP405 ID PROM does not contain any variable (e.g. unique calibration) information. ID PROM bytes are addressed using only the odd addresses in a 64 byte block. The IP405 ID PROM contents are shown in Table 3.2. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID PROM. Execution of an ID PROM Read requires 0 wait states.

Table 3.2: IP405 ID Space Identification (ID) PROM

Hex Offset From ID PROM Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All IP's have 'IPAC'
03	P	50	
05	A	41	
07	C	43	
09		A3	Acromag ID Code
0B		01	IP Model Code[1]
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		0C	Total Number of ID PROM Bytes
17		21	CRC
19 to 3F		yy	Not Used

Notes (Table 3.2):

1. The IP model number is represented by a two-digit code within the ID PROM (the IP405 model is represented by 01 Hex).

IP405 PROGRAMMING

Acromag provides you with the Industrial I/O Pack Software Library diskette to make communication with the board easy. The functions provided are written in the "C" programming language and can be linked into your application. Refer to the "README.TXT" file in the root directory and the "INFO405.TXT" file in the "IP405" subdirectory on the diskette for details.

4.0 THEORY OF OPERATION

This section describes the basic functionality of the circuitry used on the board. Refer to the Block Diagram shown in Drawing 4501-517 as you review this material.

OUTPUTS

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.1). Field outputs are NON-ISOLATED. This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage. Refer to Drawing 4501-516 for example output and grounding connections.

Up to 40 open-drain outputs may be controlled. The outputs are the open drains of individual mosfets. The sources of these mosfets are connected in common. This configuration provides 40 low-side switches for digital control. Writing a '1' to the output will turn the switch ON (closed-circuit), a '0' will turn it OFF (open-circuit).

The gates of the mosfets are controlled by D-flip/flop registers operating off the data bus. Readback of the output state configuration is accomplished through line drivers on the data bus fed by the D-flip/flop registers. Read/Write data is transferred using 16-bit words. With regard to throughput, 0 wait states are required for readback, 1 wait state for write operations.

Output operation is 'Fail-safe'. That is, the outputs are always OFF upon power-up reset, and are automatically cleared following a system software reset. This is done for safety reasons to ensure reliable control of the output state under all conditions. Further, unlike some competitive units, gate pulldowns are included to ensure that the outputs do not turn on momentarily if power is applied to the output drain circuit while the IP module power is off.

The output mosfets employed are rated for a much higher current than specified. However, the field connector and cabling used are only rated to 1A per pin (limiting a single channel to 1A). Since 40 output channels are provided and only 50-pins are available, the balance of 10 pins is used to provide ground return (hence; the 10A total current limitation placed on this module). The low R_{dsON} of the output mosfets will ensure TTL-level compatible logic-low output signals even at high (1A) output currents.

The output mosfets include an integrated zener diode between the drain and the source. This provides output voltage clamp protection to 60V. It also helps protect aginst damage due to high frequency surges and ESD. However, when driving inductive loads such as relay coils, you should always place a snubber diode across the load to shunt the reverse EMF that develops across the coil when the current through it is turned off (refer to Drawing 4501-516 for an example of this type of protection).

LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1 (refer to Table 2.2). Not all of the IP logic P1 pin functions are used. P1 also provides +5V to power the module (±12V is not used).

A programmable logic device installed on the IP Module provides the control signals required to operate the board. It decodes the selected addresses in the I/O and ID spaces and produces the chip selects, control signals, and timing required by the output registers, readback buffers, and ID PROM, as well as, the acknowledgement signal required by the carrier board per the IP specification.

The ID PROM (read only) installed on the IP module provides the identification for the individual module per the IP specification. The ID PROM, output registers, and readback buffers are all accessed through the 16-bit data bus interface to the carrier board.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

GENERAL SPECIFICATIONS

Operating Temperature.....0 to +70°C.
-40 to +85°C (E version).
Relative Humidity.....5-95% non-condensing.
Storage Temperature.....-55°C to +125°C.
Physical Configuration.....Single Industrial I/O Pack Module.
Length.....3.880 in. (98.5 mm).
Width.....1.780 in. (45.2 mm).
Board Thickness.....0.062 in. (1.59 mm).
Max Component Height.....0.314 in. (7.97 mm).
Connectors:
P1 (IP Logic Interface).....50-pin female receptacle header (AMP 173279-3 or equivalent).
P2 (Field I/O).....50-pin female receptacle header (AMP 173279-3 or equivalent).
Power:
+5 Volts (±5%).....180mA, Typical with outputs ON; 240mA, Typical with outputs OFF; 350mA, Maximum.
+12 Volts (±5%) from P1.....0mA (Not Used).
-12 Volts (±5%) from P1.....0mA (Not Used).
Non-Isolated.....Logic and field commons have a direct electrical connection.

DIGITAL OUTPUTS

Output Channel Configuration.....40 open-drain DMOS Mosfets with common source connection. For DC voltage applications only, observe proper polarity.
Output "OFF" Voltage Range.....0 to +60V DC, Maximum.
Output "OFF" Leakage Current.....25uA Maximum (55°C, 48V).
Output "ON" Current Range.....0 to +1A DC, continuous (up to 10A total for all channels combined), or 250mA DC continuous (all channels ON). No deration required at elevated ambients.
Output R_{ds} ON Resistance.....0.2Ω, Maximum (25°C).
Turn-ON Time.....Varies with load, 320ns Typical, with 330Ω pull-up to +5V and 12-inch ribbon cable (Measured from IOSEL line assertion to output drain state transfer to TTL 0.8V level).
Turn-OFF Time.....Varies with load, 500ns Typical, with 330Ω pull-up to +5V and 12-inch ribbon cable (Measured from IOSEL line assertion to output drain state transfer to TTL 2.0V level).
Resistance to RFI.....No digital upsets occur for field strengths up to 10V per meter at 27MHz, 151MHz, & 460MHz per SAMA PMC 33.1 test procedures.
Resistance to EMI.....Unit has been tested with no digital upsets under the influence of EMI from switching solenoids, commutator motors, and drill motors.
Surge Withstand Capability.....Outputs exhibit no damage when tested with a standardized test waveform representative of surges (high frequency transient electrical interference) per ANSI/IEEE C37.90-1978.
ESD Protection.....Outputs exhibit no degradation of performance with repeated ESD induced voltages to ± 6KV per DOD-STD-1686.

OUTPUT MOSFETS

(These specifications are included for reference and apply to the output driver only. See DIGITAL OUTPUTS above for module specifications).

Manufacturer/Part Number.....National NDS9945, Siliconix Si9945DY.
Voltage V_{DSS}.....60V DC, Maximum.
Current I_D.....3.5A, Continuous (25°C), 2.8A, Continuous (70°C).
ON Resistance R_{DS}.....0.2Ω Max (VGS=4.5V, 25°C).
Power Dissipation P_D.....2W (25°C).
Output "OFF" Leakage Current.....25uA Maximum (55°C, 48V).

INDUSTRIAL I/O PACK COMPLIANCE

Specification.....This module meets or exceeds all written Industrial I/O Pack specifications per revision 0.7.1.
Electrical/Mechanical Interface.....Single-Size IP Module.
IP Data Transfer Cycle Types Supported:
Input/Output (IOSel*).....16-bit word (D16) read/write of channel data.
ID Read (IDSel*).....32 x 8 ID PROM read on D0..D7.
Access Times (8MHz Clock):
ID PROM Read.....0 wait states (250ns cycle).
Channel Register Read.....0 wait states (250ns cycle).
Channel Register Write.....1 wait state (375ns cycle).

APPENDIX

CABLE: MODEL 5025-550-x (Non-Shielded)
MODEL 5025-551-x (Shielded)

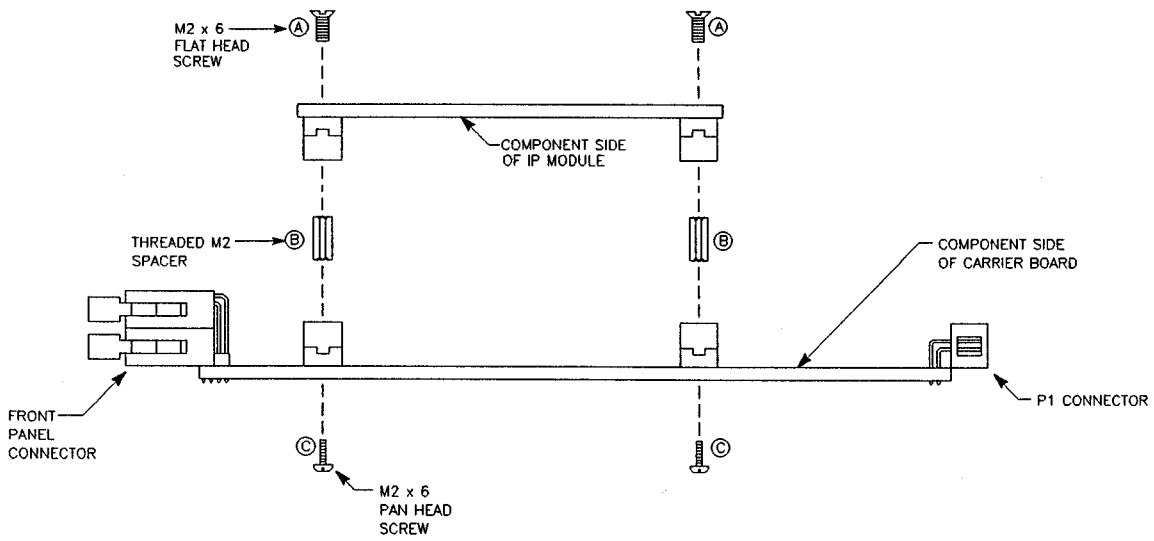
Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet (12 feet maximum). Choose shielded or unshielded cable according to model number. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.
Application: Used to connect a Model 5025-552 termination panel to the AVME9630/9660 non-intelligent carrier board A-D connectors (both have 50-pin connectors).
Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50-wire flat ribbon cable, 28 gage. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent). Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).
Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).
Keying: Headers at both ends have polarizing key to prevent improper installation.
Schematic and Physical Attributes: For Non-Shielded cable model, see Drawing 4501-462. For Shielded cable model, see Drawing 4501-463.
Shipping Weight: 1.0 pound (0.5Kg) packaged.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For AVME9630/9660 Boards
Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660 3U/6U non-intelligent carrier boards (A-D connectors only) via a flat ribbon cable (Model 5025-550-x or 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Connections to AVME9630/9660: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-550-x or 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight: 1.25 pounds (0.6kg) packaged.

TRANSITION MODULE: MODEL TRANS-GP

Type: Transition module for AVME9630/9660 boards.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Schematic and Physical Attributes: See Drawing 4501-465.
Field Wiring: 100-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Printed Circuit Board: Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +85°C.
Storage Temperature: -55°C to +105°C.
Shipping Weight: 1.25 pounds (0.6Kg) packaged.



ASSEMBLY PROCEDURE:

1. THREADED SPACERS ARE PROVIDED IN TWO DIFFERENT LENGTHS. THE SHORTER LENGTH IS FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES).

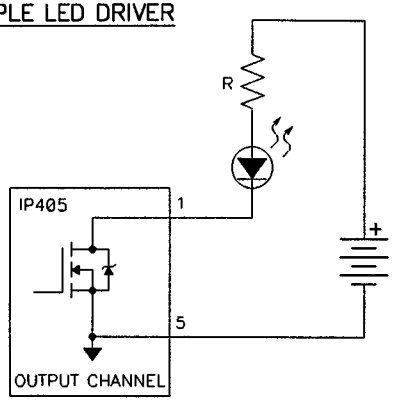
IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY

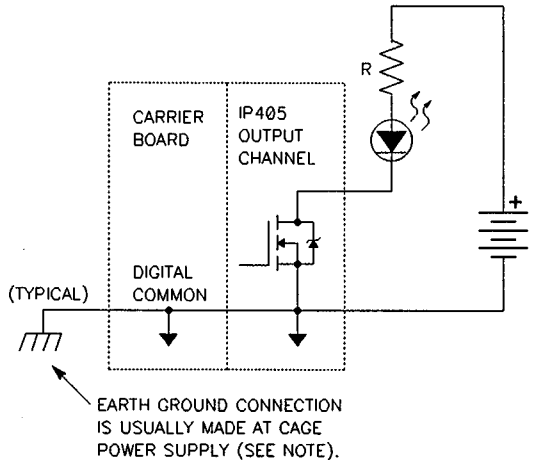
Acromag WIXOM, MICH.						
29 JUL 94	B	94C911	TAV	JGV	BC
21 DEC 93	A	——	TAV	JGV	BC
DATE	REV	ECN	DR	ENG	CLP

TITLE: IP MECHANICAL ASSEMBLY

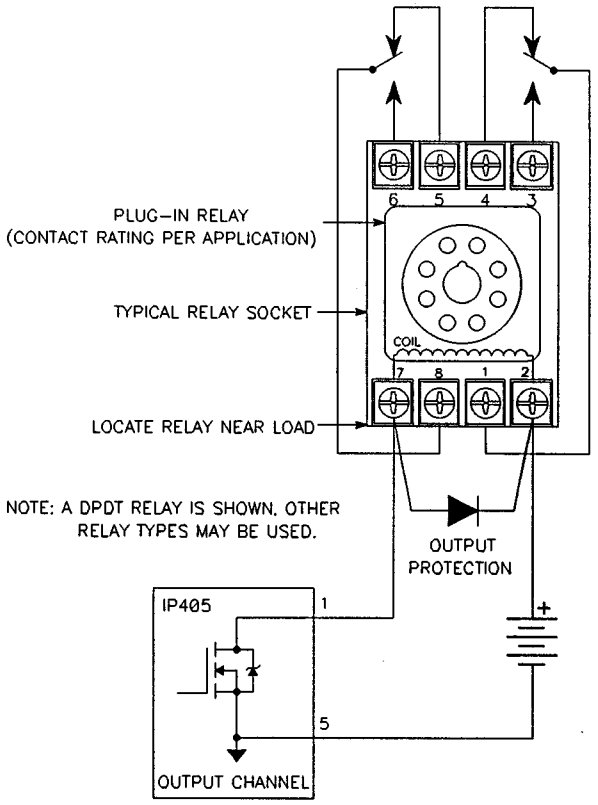
SIZE	SERIES		DWG NO.	REV
D	IP	1 of 1	4501-434	B

EXAMPLE LED DRIVER

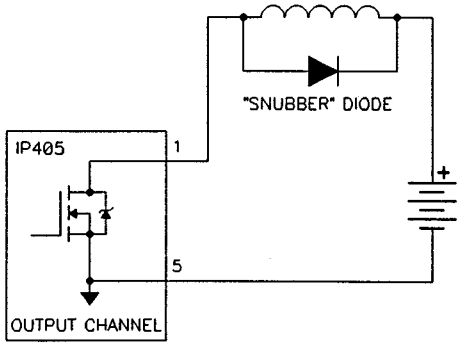




CONNECTION TO AN INTERPOSING RELAY FOR GREATER DRIVE CAPABILITY

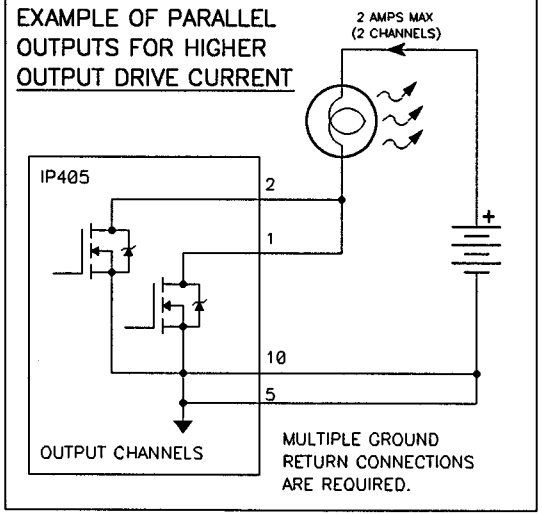


EXAMPLE RELAY/COIL DRIVER



NOTE: THE "SNUBBER" DIODE IS USED TO SHUNT THE REVERSE EMF THAT DEVELOPS WHEN THE CURRENT THROUGH THE COIL IS TURNED OFF. THIS WILL HELP PROLONG THE LIFE OF THE OUTPUT CHANNEL.

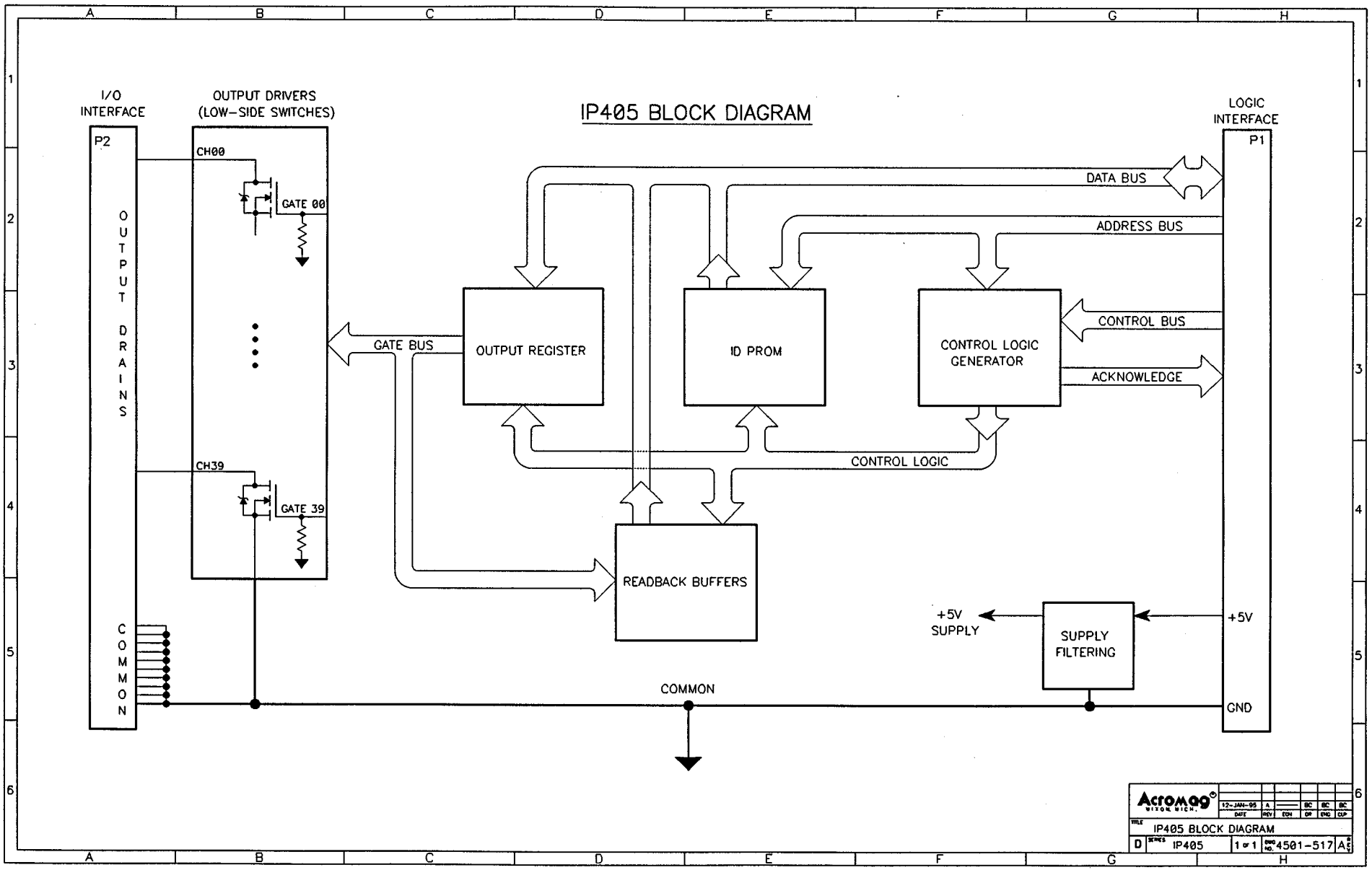
EXAMPLE OF PARALLEL OUTPUTS FOR HIGHER OUTPUT DRIVE CURRENT

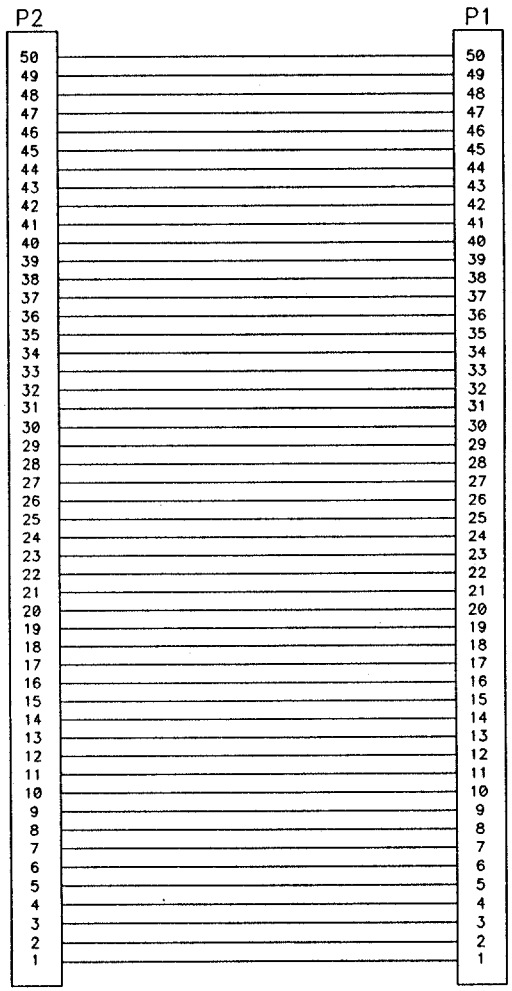


NOTE: MULTIPLE EARTH GROUNDS CAUSE GROUND LOOPS AND MUST BE AVOIDED.

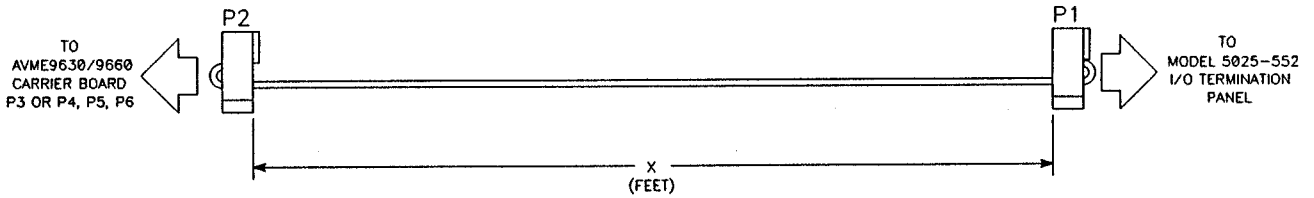
IP405 EXAMPLE OUTPUT CONNECTIONS

Acromag WIXOM MICH.						
08-AUG-94	A		BC	BC	BC	
DATE	REV	SCN	DR	ENG	SUP	
TITLE: IP405 EXAMPLE OUTPUT CONNECTIONS						
D	SIZE: IP405	1 of 1	DWG NO. 4501-516	A	REV	

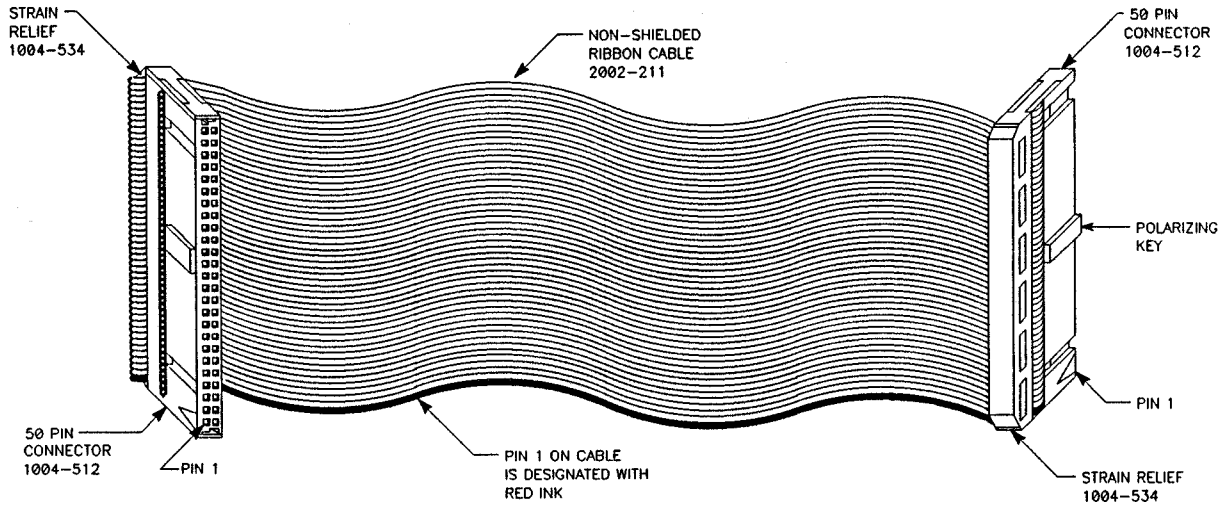

IP405 BLOCK DIAGRAM
I/O INTERFACE
OUTPUT DRIVERS (LOW-SIDE SWITCHES)
LOGIC INTERFACE
P2
P1
OUTPUT DRAINS
COMMON
CH00
CH39
GATE 00
GATE 39
GATE BUS
OUTPUT REGISTER
ID PROM
CONTROL LOGIC GENERATOR
READBACK BUFFERS
DATA BUS
ADDRESS BUS
CONTROL BUS
ACKNOWLEDGE
CONTROL LOGIC
+5V SUPPLY
SUPPLY FILTERING
+5V
GND
COMMON
Acromag
12-JAN-95
IP405 BLOCK DIAGRAM
IP405
1 of 1
4501-517



MODEL 5025-550-x SCHEMATIC



TOP VIEW

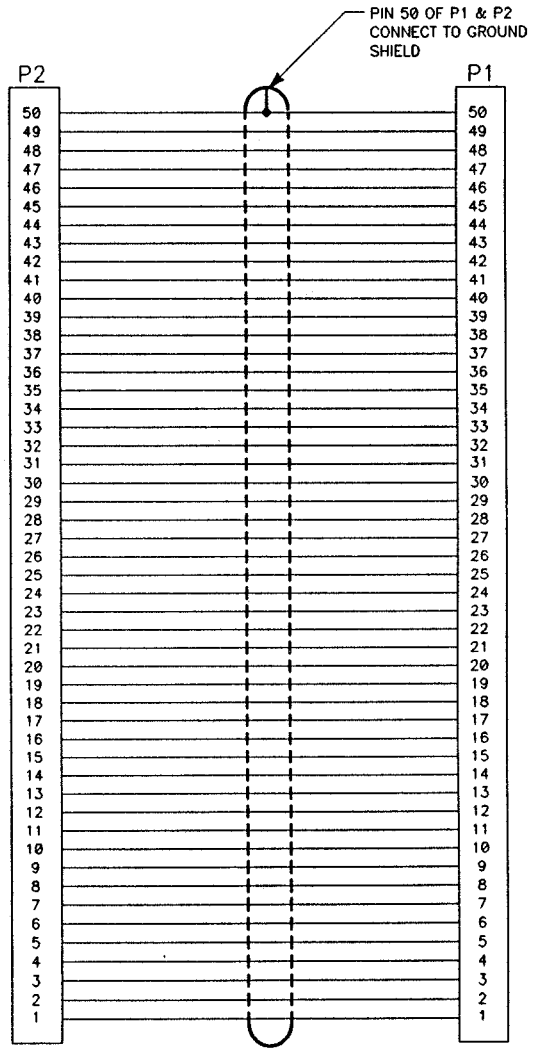


FRONT VIEW

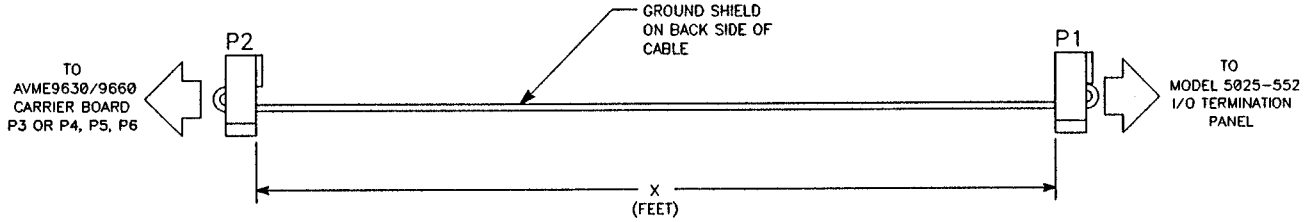
NOTE: SEVEN DIGIT PART NUMBERS ARE
ACROMAG PART NUMBERS (XXXX-XXX).

MODEL 5025-550-x SIGNAL CABLE, NON-SHIELDED

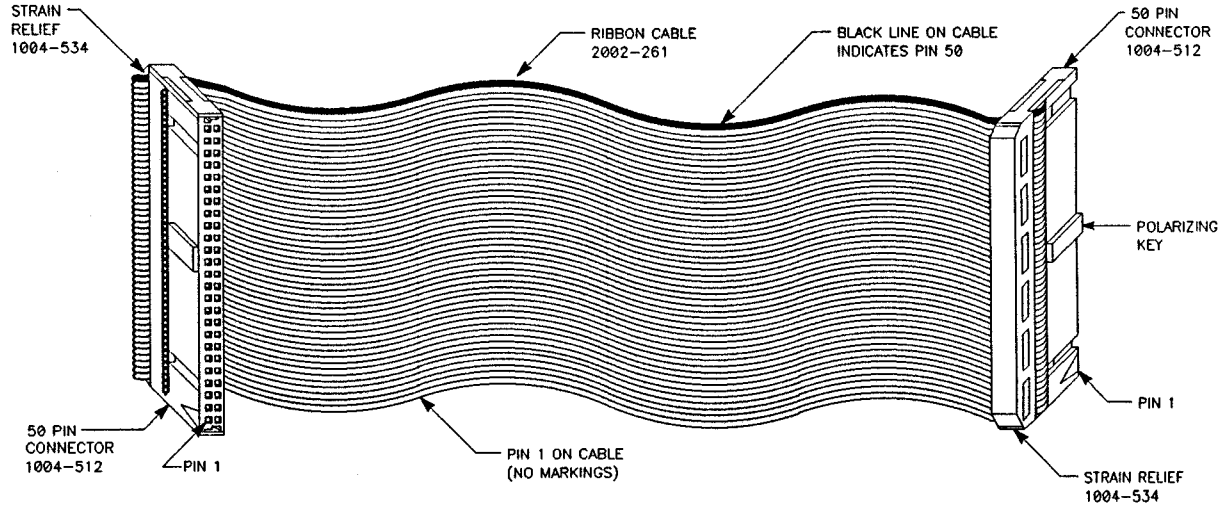
Acromag WIXOM, MICH.
09 FEB 94 A
DATE REV ECN DR ENG CLP
TITLE CABLE 5025-550-x, NON-SHIELDED
D SERIES 1 OF 1 DWG NO. 4501-462 A



MODEL 5025-551-x SCHEMATIC



TOP VIEW

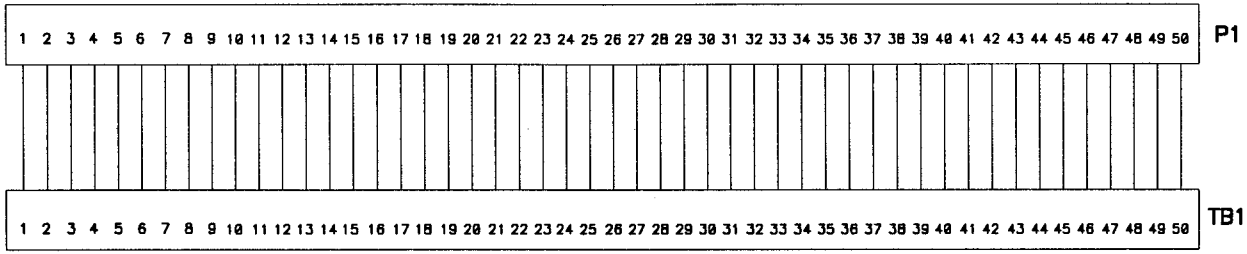


FRONT VIEW

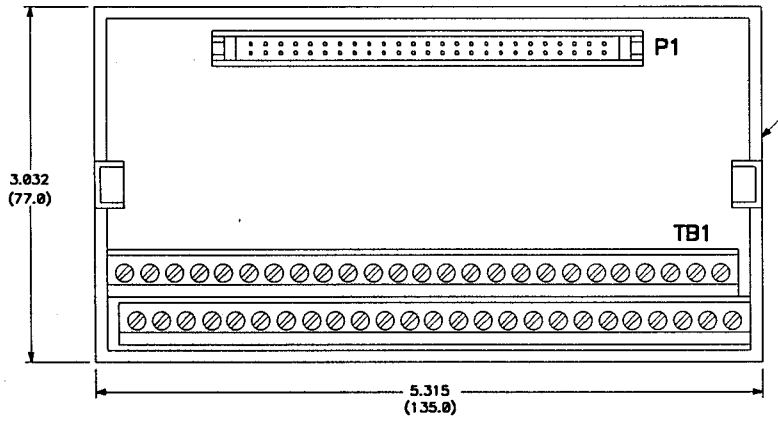
NOTE: SEVEN DIGIT PART NUMBERS ARE
ACROMAG PART NUMBERS (XXXX-XXX).

MODEL 5025-551-x SIGNAL CABLE, SHIELDED

Acromag WIXOM, MICH.
95 FEB 94 | A | — | T&V | CAP | BC
DATE | REV | ECN | DR | CHG | CLP
TITLE: CABLE 5025-551-x, SHIELDED
D | SERIES | 1 OF 1 | DWG NO. 4501-463 | A

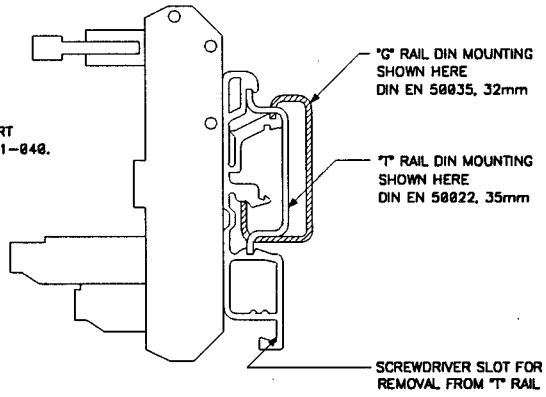


MODEL 5025-552 TERMINATION PANEL SCHEMATIC

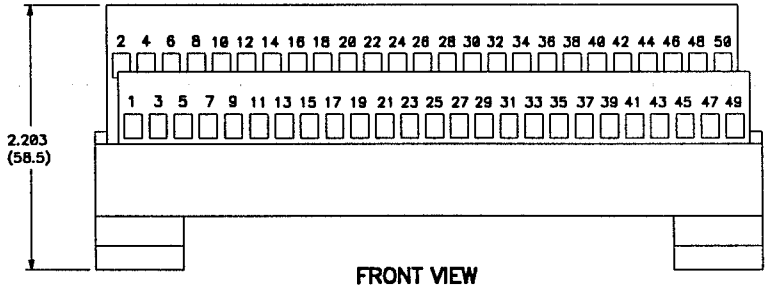


TOP VIEW

TERMINATION PANEL ACROMAG PART NUMBER 4001-040.



SIDE VIEW



FRONT VIEW

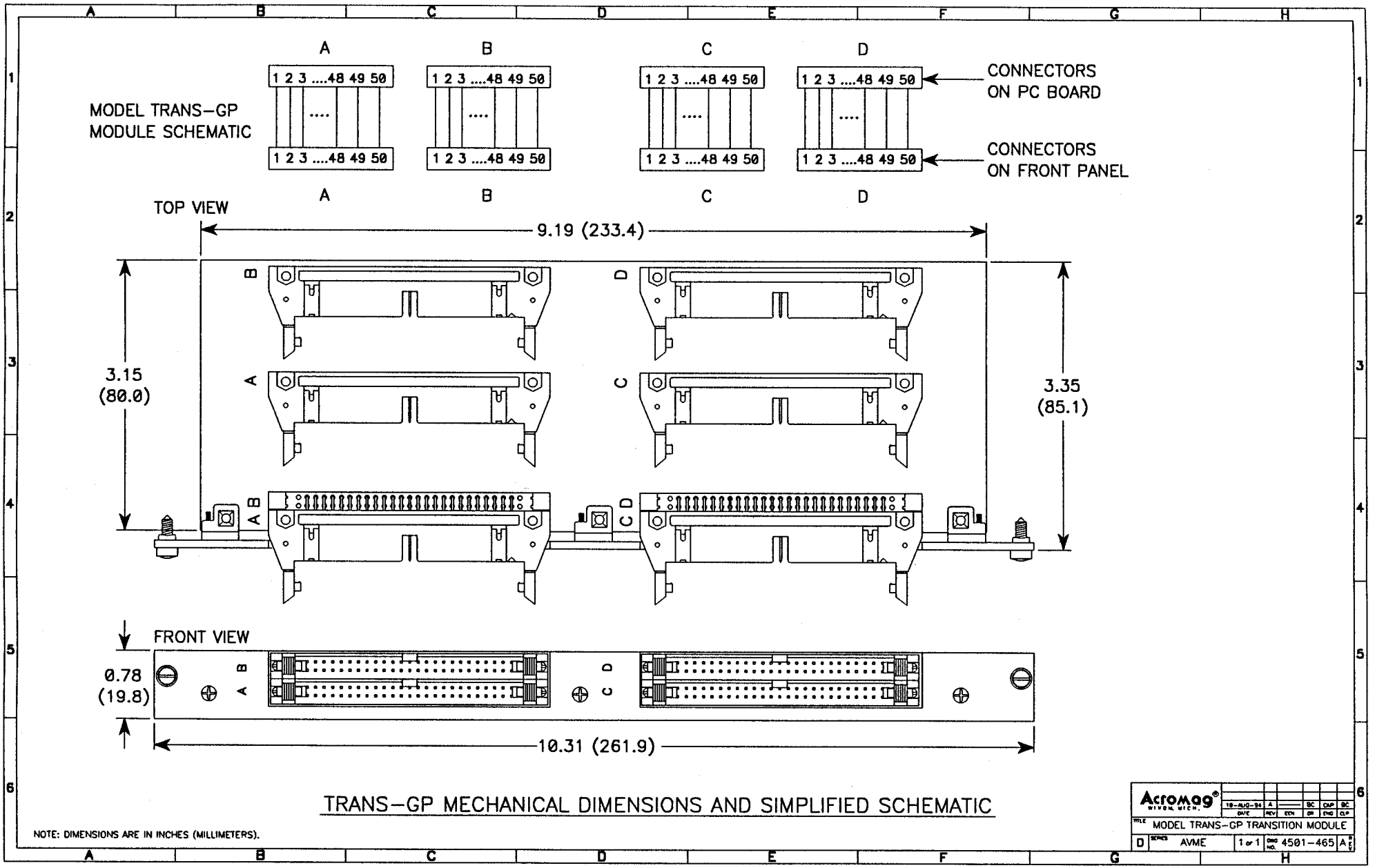
NOTES:

DIMENSIONS ARE IN INCHES (MILLIMETERS).

TOLERANCE: ±0.020 (±0.5).

MODEL 5025-552 TERMINATION PANEL

Acromag® WIXOM, MICH.						
	09 FEB 94	A	—	TAV	CAP	BC
	DATE	REV	ECN	DR	ENG	CLP
TITLE: MODEL 5025-552 TERMINATION PANEL						
D SERIES	1 OF 1	DWG NO. 4501-464		A REV		



TRANS–GP MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC

NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).

Acromag® WIXOM, MICH.

DATE	REV	ECN	DR	ENG	CLP
18-AUG-94	A	——	BC	CAP	BC

TITLE: MODEL TRANS–GP TRANSITION MODULE

D | SERIES: AVME | 1 of 1 | DWG NO. 4501–465 | A REV