XMCAP2020/XMCAP2021 XMC AcroPack Carrier Boards

USER'S MANUAL

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1. GENERAL INFORMATION

Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the AcroPack module.

Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag.

Trademark, Trade Name and Copyright Information

Radio Frequency Interference Statement

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

XMCAP2020/XMCAP2021 OVERVIEW

The XMCAP2020/XMCAP2021 is a carrier for mini-PCIe or AcroPack mezzanine modules in an air-cooled XMC form factor. This carrier board provides a modular approach to system assembly, since each carrier can be populated with any combination of analog input/output, digital input/output, communication, etc. AcroPack modules. Thus, the user can create a board which is customized to the application. This saves money and space - a single carrier board populated with AcroPack modules may replace several dedicated function XMC modules.

Ordering Information

There are two models of this board available. The only difference is whether the Field I/O from the attached AcroPack modules are available through connectors on the front panel or through the rear P14 and P16 XMC connectors.

Model	I/O Type
XMCAP2020-LF	Front Panel
XMCAP2021-LF	Rear (P14 & P16)

KEY XMCAP2020/XMCAP2021 FEATURES

Interface for AcroPack modules – The XMCAP2020/XMCAP2021 provides an electrical and mechanical interface for up to two industry standard mini-PCIe or AcroPack modules. AcroPack modules are available from Acromag. Mini-PCIe cards are available from other vendors in a wide variety of input/output configurations to meet the needs of varied applications.

PCI Express Version 2.1 Compliant Carrier: - Includes a PCIe switch to allow two PCIe devices (AcroPack or mini-PCIe) to share a single XMC slot on the XMC carrier.

Board Identification – A unique carrier and site number can be set for each AcroPack site automatically by geographical address bits or by DIP switch. This feature provides the capability to distinguish a particular AcroPack module from others when multiple instances of the same module are used in a system.

JTAG Programming Header – JTAG programming is supported both through the XMC P15 connector, as well as through a Molex 78171-5006 6-pin micro connector (J3). This connection is provided for programming and debugging the FPGA on some AcroPack modules. The JTAG ports of the two AcroPack modules are daisy-chained.

SIGNAL INTERFACE PRODUCTS

This AcroPack carrier board will mate directly to most industry standard mini-PCIe and AcroPack modules. Acromag provides the following interface products (all connections to field signals are made through the carrier board which passes them to the individual AcroPack modules):

Field I/O Cable

Model 5028-420 Round cable, shielded, 34 twisted pairs, male SCSI-3 connector to 68 pin CHAMP 0.8mm, 2 meters long.

Termination Panel

Model 5025-288 DIN-rail mountable panel provides 68 screw terminals for universal field I/O termination, SCSI-3 connector.

JTAG Adapter Cable

Model 5028-564 JTAG Adapter Cable connects between J3 and a Xilinx USB programmer. This cable is only required if JTAG is not available on the XMC carrier through the P15 XMC connector.

SOFTWARE SUPPORT

The AcroPack series products require support drivers specific to your operating system. Supported operating systems include: Linux®, Windows®, and VxWorks®.

Windows®

Acromag provides software products (sold separately) to facilitate the development of Windows® applications interfacing with AcroPack modules. This software (model APSW-API-WIN) consists of low-level drivers and Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

VxWorks®

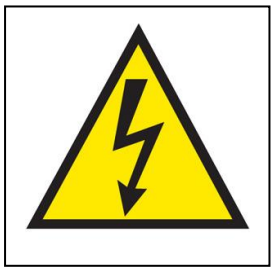
Acromag provides a software product (sold separately) consisting of VxWorks® software. This software (Model APSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of “C” functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

Linux®

Acromag provides a software product consisting of Linux® software. This software (Model APSW-API-LNX) is composed of Linux® libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of “C” functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

2. PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.

WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened, and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

BOARD CONFIGURATION

Power should be removed from the board when changing switch configurations or when installing AcroPack modules, cables, and field wiring.

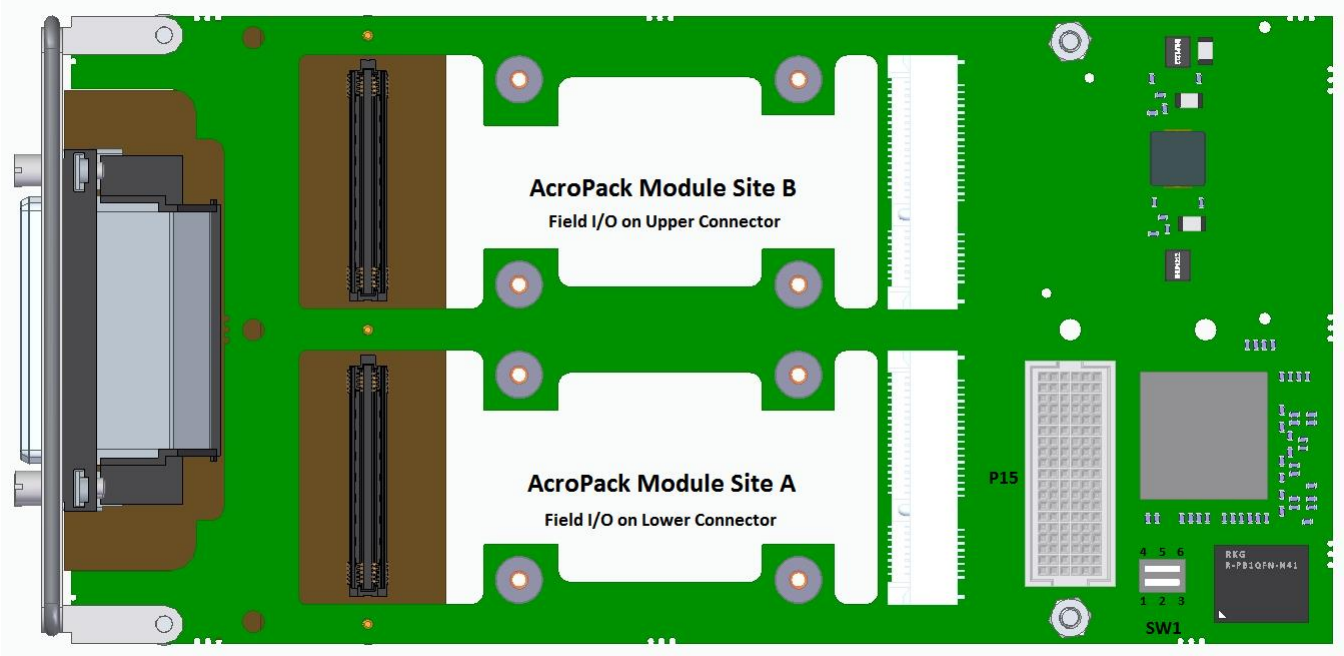


Figure 1 XMCAP2020 Primary Side

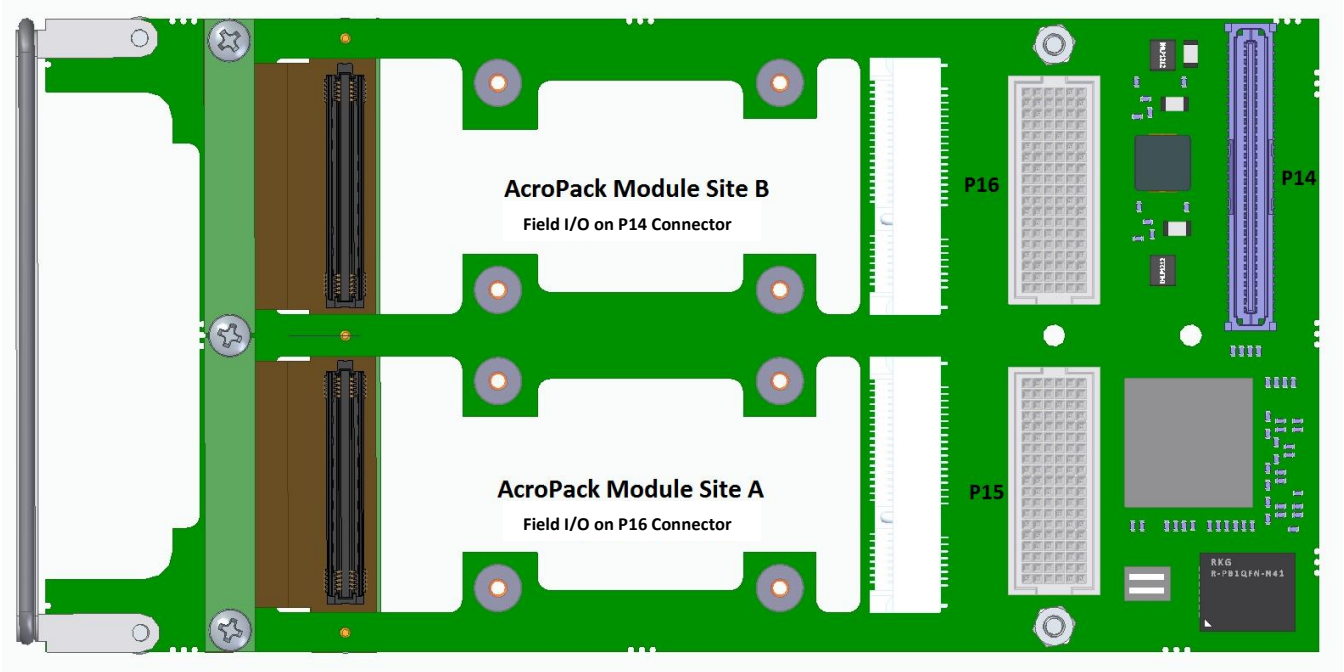


Figure 2 XMCAP2021Primary Side

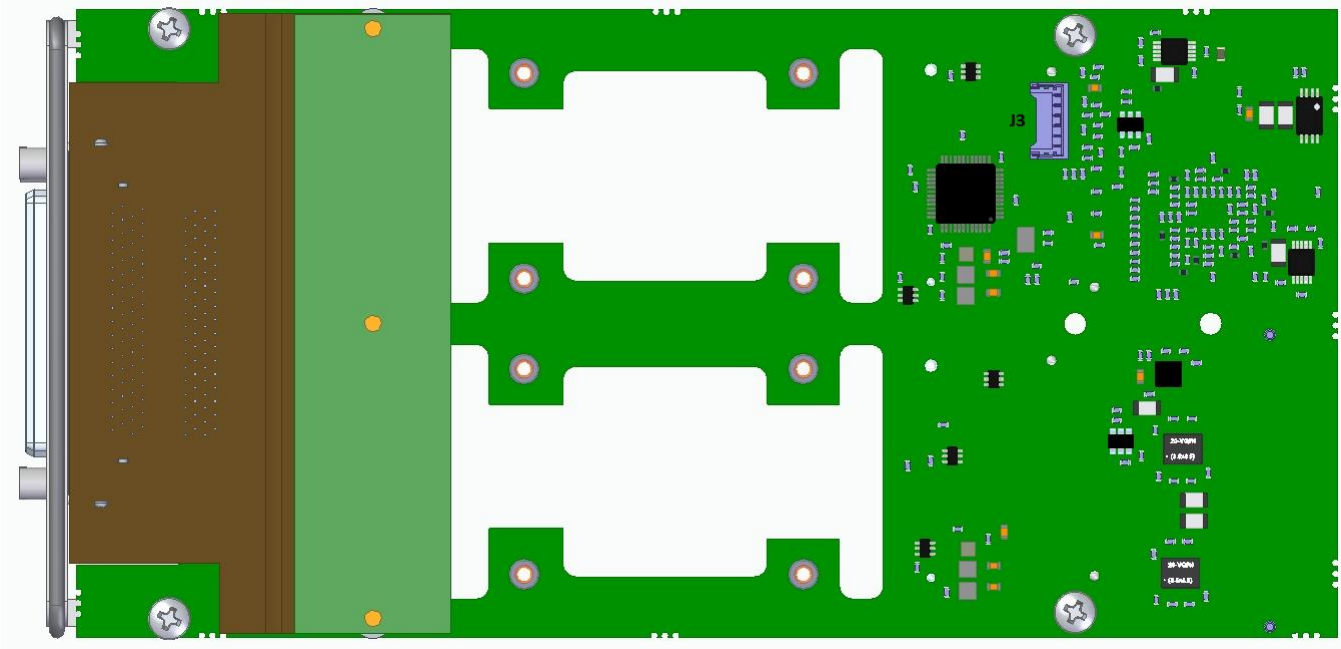


Figure 3 XMCAP2020/XMCAP2020 Secondary Side

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed AcroPack modules within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The lack of air circulation across the XMC carrier could be a cause for some concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

Isolation Considerations

WARNING: *This AcroPack carrier is designed to provide isolation between the AcroPack Field I/O signals and the host. The AcroPack module must also be an isolated AcroPack module to maintain the isolation between the logic and field I/O signals. Unless isolation is provided on the AcroPack module itself, the field I/O connections are not isolated from the PCIe bus.*

When this carrier is used with isolated AcroPack modules, both AcroPacks in slots A and B should be isolated AcroPacks. Non-isolated AcroPacks sharing the same Connector will compromise the isolation integrity of the other AcroPack.

For the XMCAP2021 model using Rear I/O Isolation may be violated by the carrier onto which the XMCAP2021 board is installed. See XMC carrier documentation for available isolation ratings for Rear I/O.

Refer to Specifications for Isolation ratings.

CARRIER ADDRESS ASSIGNMENT

Following are the instructions for setting the slot address of the carrier. By assigning a unique address to each carrier, system software can distinguish this carrier from other similarly configured carriers installed in a system.

Address bits A0, A1, and A2 are connected to the corresponding Geographical Addressing (GA) bits of the XMC P15 connector. This should automatically assign a unique address to the XMCAP2020/XMCAP2021 board.

If the GA bits are not supplied by the XMC carrier onto which the XMCAP2020/XMCAP2021 board is installed, SW1 may be used to select address bits A3 and A4. Figure 1 shows the location of switch SW1. Set the switch state as shown in Table 1 below to assign a unique slot address to this carrier.

Table 1 Switch SW1 assignments

SW1 Position	Address Bit	Value
1-2	A3	1
2-3		0
4-5	A4	1
5-6		0

ACROPACK MODULE INSTALLATION

Power should be removed from the carrier board when installing AcroPack modules, cables, termination panels, and field wiring. Refer to Figure 4 while reading this section. Place the XMCAP2020/XMCAP2021 flat on an anti-static surface for support. To install, first insert the edge of the AcroPack module into the carrier connector at an angle similar to that shown in the figure. Next, using a rocking motion while gently applying force to keep the edge of the board against the back of the carrier connector, position the module such that the field I/O connector is just above the mating connector. Verify that the two connectors are properly aligned. Once alignment is achieved, you can fully seat the connector. It will snap into place. Install four M2.5 screws as shown.

***Note: AcroPack/mini-PCIe modules with component height greater than 2.1mm will cause the XMCAP2020/XMCAP2021 to violate the 4.7mm maximum XMC module height specification. Taller Acropack/mini-PCIe modules may fit if component height under the XMCAP2020/XMCAP2021 on the carrier is less than 4.7mm.**

Current list of AcroPack modules taller than 2.1mm:
AP323E-LF (2.21mm)
AP445E-LF (2.184mm)
AP512E-LF (2.65mm)
AP513E-LF (2.82mm)
AP560E-LF (2.65mm)
AP571-000 (4.6mm)
AP572-000 (4.6mm)
AP580E-LF (4.35mm)
AP580E-POE-LF (6.5mm)

Note: AP441E-LF is not recommended for use with the XMC AcroPack carrier.

WARNING: When installing a commercial mini-PCIe module onto the XMCAP2020/XMCAP2021 board be sure that pin 45 on the module's mini-PCIe connector is not grounded or damage to the module may result.

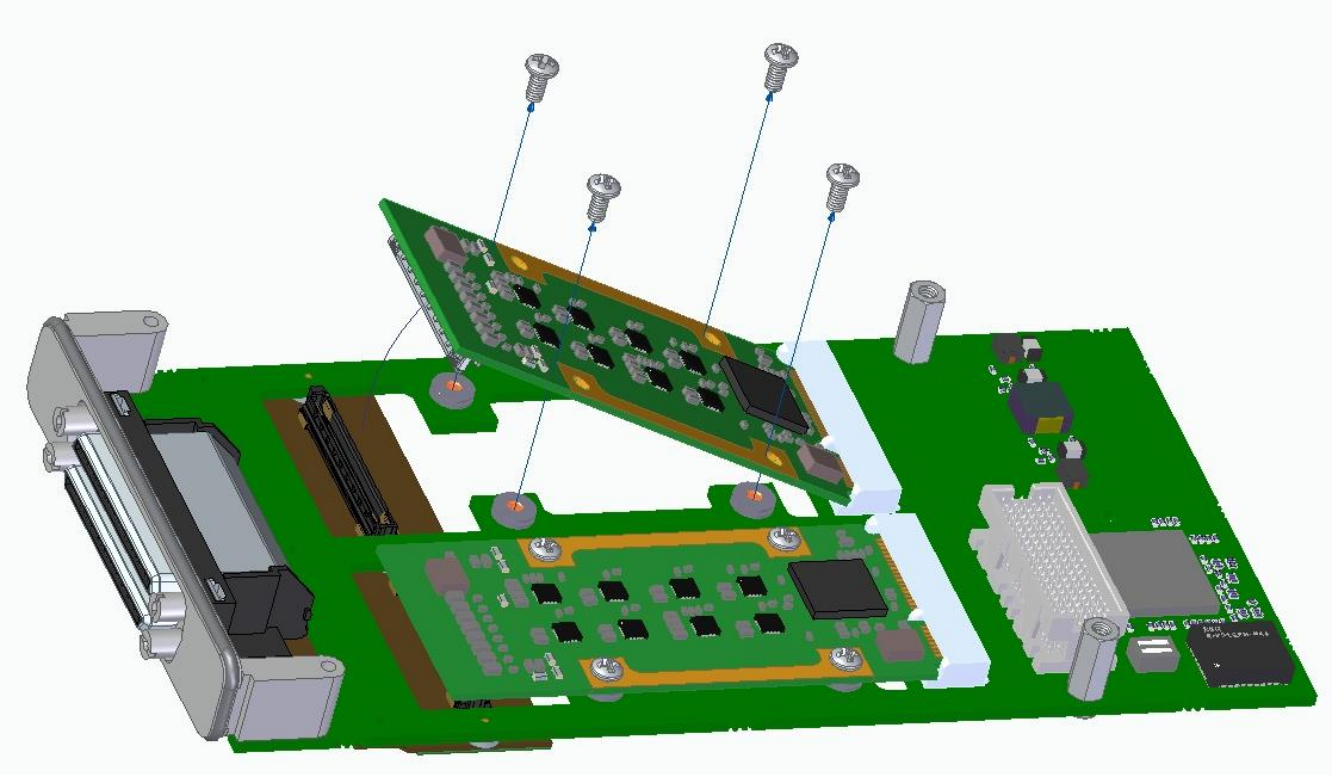


Figure 4 AcroPack Module Installation

FIELD GROUNDING CONSIDERATIONS

The Field I/O signals are isolated from chassis and system ground on the carrier. However, some non-isolated AcroPack modules connect Field I/O ground to system ground. Care should be taken in designing installations without isolation to avoid ground loops and noise pickup. This is particularly important for analog I/O applications when a high level of accuracy/resolution is needed (12-bits or more). Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the AcroPack input/output modules.

CONNECTORS

The XMCAP2020/XMCAP2021 carrier uses two AcroPack module field I/O connectors, two mini-PCIe connectors, two field I/O connectors (front panel for XMCAP2020 and rear P14 & P16 connectors for XMCAP2021) and one XMC bus interface connector. These are discussed in the following sections.

Front Panel Field I/O Connectors (XMCAP2020 only)

Field I/O connections on the XMCAP2020 model are made via two 68 pin, Stacked, 0.8 mm Champ cable connectors mounted on the front panel. The AcroPack module identifier (A or B) is marked on Figure 5 for easy identification. Cables and termination panels (or user defined terminations) can be quickly mated to the field I/O connectors.

See Table 2 below for pin assignments.

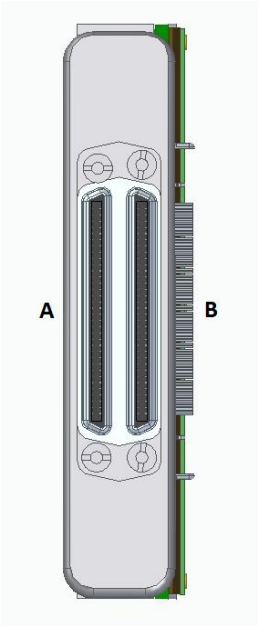


Figure 5 Front panel Field I/O Connector Location (XMCAP2020 only)

Rear Field I/O Connectors (XMCAP2021 only)

Field I/O connections on the XMCAP2021 model are made via the XMC P14 and P16 connectors. The Field I/O connections from the AcroPack module in Site A are available through the XMC P16 connector, using X24s+X8d+X12d Rear I/O mapping.

The Field I/O connections from the AcroPack module in Site B are available through the XMC P14 connector, using P64s Rear I/O mapping.

See Table 2 below for pin assignments.

AcroPack Field I/O Connectors

The field side connector of AcroPack modules mate to Samtec SS5-50-3.00-L-D-K-TR socket connectors on the carrier board.

This provides excellent connection integrity due to the gold plating in the mating area. M2.5 screws and spacers provide additional stability for harsh environments.

The functions of each of the Field I/O signals are defined by the installed AcroPack model.

Table 2 Field I/O Pin Assignments

XMCAP2020 Front Panel I/O Connectors	XMCAP2021 Rear I/O Connection (Site A - P16)	XMCAP2021 Rear I/O Connection (Site B - P14)	Carrier P1, P2 Samtec SS5-50-3.00-L-D-K-TR	Module Pin Number	Field I/O Signal
1	A1	1	2	2	Field I/O 1
35	B1	3	1	1	Field I/O 2
			4	4	Reserved/isolation
			3	3	Reserved/isolation
2	D1	2	6	6	Field I/O 3
36	E1	4	5	5	Field I/O 4
			8	8	Reserved/isolation
			7	7	Reserved/isolation
3	A3	5	10	10	Field I/O 5
37	B3	7	9	9	Field I/O 6
			12	12	Reserved/isolation
			11	11	Reserved/isolation
4	D3	6	14	14	Field I/O 7
38	E3	8	13	13	Field I/O 8
			16	16	Reserved/isolation
			15	15	Reserved/isolation
5	A5	9	18	18	Field I/O 9
39	B5	11	17	17	Field I/O 10
			20	20	Reserved/isolation
			19	19	Reserved/isolation
6	D5	10	22	22	Field I/O 11
40	E5	12	21	21	Field I/O 12
			24	24	Reserved/isolation
			23	23	Reserved/isolation
7	A7	13	26	26	Field I/O 13
41	B7	15	25	25	Field I/O 14
			28	28	Reserved/isolation
			27	27	Reserved/isolation
8	D7	14	30	30	Field I/O 15
42	E7	16	29	29	Field I/O 16
			32	32	Reserved/isolation
			31	31	Reserved/isolation
9	C9	17	34	34	Field I/O 17
43	C8	19	33	33	Field I/O 18
			36	36	Reserved/isolation

XMCAP2020 Front Panel I/O Connectors	XMCAP2021 Rear I/O Connection (Site A - P16)	XMCAP2021 Rear I/O Connection (Site B - P14)	Carrier P1, P2 Samtec SS5-50-3.00-L-D-K-TR	Module Pin Number	Field I/O Signal
			35	35	Reserved/isolation
10	C11	18	38	38	Field I/O 19
44	C10	20	37	37	Field I/O 20
			40	40	Reserved/isolation
			39	39	Reserved/isolation
11	F11	21	42	42	Field I/O 21
45	F10	23	41	41	Field I/O 22
			44	44	Reserved/isolation
			43	43	Reserved/isolation
12	A11	22	46	46	Field I/O 23
46	B11	24	45	45	Field I/O 24
			48	48	Reserved/isolation
			47	47	Reserved/isolation
13	D11	25	50	50	Field I/O 25
47	E11	27	49	49	Field I/O 26
			52	52	Reserved/isolation
			51	51	Reserved/isolation
14	C13	26	54	54	Field I/O 27
48	C12	28	53	53	Field I/O 28
			56	56	Reserved/isolation
			55	55	Reserved/isolation
15	F13	29	58	58	Field I/O 29
49	F12	31	57	57	Field I/O 30
			60	60	Reserved/isolation
			59	59	Reserved/isolation
16	A13	30	62	62	Field I/O 31
50	B13	32	61	61	Field I/O 32
			64	64	Reserved/isolation
			63	63	Reserved/isolation
17	D13	33	66	66	Field I/O 33
51	E13	35	65	65	Field I/O 34
			68	68	Reserved/isolation
			67	67	Reserved/isolation
18	C15	34	70	70	Field I/O 35
52	C14	36	69	69	Field I/O 36

XMCAP2020 Front Panel I/O Connectors	XMCAP2021 Rear I/O Connection (Site A - P16)	XMCAP2021 Rear I/O Connection (Site B - P14)	Carrier P1, P2 Samtec SS5-50-3.00-L-D-K-TR	Module Pin Number	Field I/O Signal
			72	72	Reserved/isolation
			71	71	Reserved/isolation
19	F15	37	74	74	Field I/O 37
53	F14	39	73	73	Field I/O 38
			76	76	Reserved/isolation
			75	75	Reserved/isolation
20	A15	38	78	78	Field I/O 39
54	B15	40	77	77	Field I/O 40
			80	80	Reserved/isolation
			79	79	Reserved/isolation
21	D15	41	82	82	Field I/O 41
55	E15	43	81	81	Field I/O 42
			84	84	Reserved/isolation
			83	83	Reserved/isolation
22	C17	42	86	86	Field I/O 43
56	C16	44	85	85	Field I/O 44
			88	88	Reserved/isolation
			87	87	Reserved/isolation
23	F17	45	90	90	Field I/O 45
57	F16	47	89	89	Field I/O 46
			92	92	Reserved/isolation
			91	91	Reserved/isolation
24	A17	46	94	94	Field I/O 47
58	B17	48	93	93	Field I/O 48
			96	96	Reserved/isolation
			95	95	Reserved/isolation
25	D17	49	98	98	Field I/O 49
59	E17	51	97	97	Field I/O 50
			100	100	Reserved/isolation
			99	99	Reserved/isolation

Mini-PCIe Connectors

The AcroPack Mini-PCIe connectors mate to TE Connectivity 1759457-1 connectors on the carrier board. AcroPack locations A and B are labeled on the board for easy identification.

Pin assignments for these connectors are based on the Mini-PCIe specification with the exceptions noted in Table 3.

WARNING: When installing a commercial mini-PCIe module onto the XMCAP2020/XMCAP2021 board be sure that pin 45 on the module's mini-PCIe connector is not grounded or damage to the module may result.

Table 3 Mini-PCIe Connectors J1 and J2 Pin Assignments

Pin #	Name	Pin #	Name
51	**+5V**[3]	52	+3.3V[4]
49	**+12V**[3]	50	GND
47	**-12V**[3]	48	+1.5V
45	**Present***[3]	46	N.C. (LED_WPAN#)[1]
43	GND	44	N.C. (LED_WLAN#)[1]
41	+3.3V[4]	42	N.C. (LED_WWAN#)[1]
39	+3.3V[4]	40	GND
37	GND	38	N.C. (USB_D+)[1]
35	GND	36	N.C. (USB_D-)[1]
33	PETX0_P	34	GND
31	PETX0_N	32	SMB_DATA[5]
29	GND	30	SMB_CLK[5]
27	GND	28	+1.5V
25	PERX0_P	26	GND
23	PERX0_N	24	+3.3V[4]
21	GND	22	PERST#
19	**TDI** (UIM_C4)[1,2]	20	N.C. (W_DISABLE#)[1]
17	**TDO** (UIM_C8)[1,2]	18	GND
15	GND	16	N.C. (UIM_VPP)[1]
13	REFCLK_P	14	N.C. (UIM_RESET)[1]
11	REFCLK_N	12	N.C. (UIM_CLK)[1]
9	GND	10	N.C. (UIM_DATA)[1]
7	CLKREQ#	8	N.C. (UIM_PWR)[1]
5	**TCK** (COEX2)[1]	6	+1.5V
3	**TMS** (COEX1)[1]	4	GND
1	N.C. (WAKE#)[1]	2	+3.3V[4]

Notes:

1. The following mini-PCIe signals are not supported: USB_D+, USB_D-, WAKE#, LED_WPAN#, LED_WLAN#, LED_WWAN#, W_DISABLE#, COEX1, COEX2, UIM_C4, UIM_C8, UIM_VPP, UIM_RESET, UIM_CLK, UIM_DATA, UIM_PWR. The following signals UIM_C4, UIM_C8, COEX2 and COEX1 are repurposed for JTAG.
2. TDI is tied to TDO on modules that do not use JTAG.
3. +5, +12, and -12 Volt power supplies and their control signal have been assigned to pins that are reserved in the mini-PCIe specification. This power is switched and only supplied when The Present* Pin (45) of the AcroPack module is seen to be grounded.
4. All +3.3Vaux power pins are changed to system +3.3V power.
5. The SM bus signals SMB_CLK and SMB_DATA are used to communicate with a CPLD on the carrier that reports slot ID. These signals will be under the control of the AcroPack module.

XMC/PCIe Bus Connections

Table4 indicates the pin assignments for the PCIe bus signals at the XMC VITA 42.3 connector P15.

Refer to the PCI Express bus specification for additional information on the PCI Express bus signals.

Table 4 XMC/PCIe Bus P15 CONNECTIONS

	A	B	C	D	E	F
1	PET00_P	PET00_N	+3.3V	PET01_P	PET01_N	VPWR
2	GND	GND	No Connect	GND	GND	PERST*
3	PET02_P	PET02_N	+3.3V	PET03_P	PET03_N	VPWR
4	GND	GND	TCK	GND	GND	No Connect
5	No Connect	No Connect	+3.3V	No Connect	No Connect	VPWR
6	GND	GND	TMS	GND	GND	+12V_AUX (NC)[3]
7	No Connect	No Connect	+3.3V	No Connect	No Connect	VPWR
8	GND	GND	TDI	GND	GND	-12V_AUX (NC)[3]
9	No Connect	No Connect	No Connect	No Connect	No Connect	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	PER00_P	PER00_N	No Connect	PER01_P	PER01_N	VPWR
12	GND	GND	GA1	GND	GND	GND
13	PER02_P	PER02_N	+3.3V_AUX (NC)[2]	PER03_P	PER03_N	VPWR
14	GND	GND	GA2	GND	GND	SMDAT(NC)
15	No Connect	No Connect	No Connect	No Connect	No Connect	VPWR
16	GND	GND	MVMRO*	GND	GND	SMCLK(NC)
17	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
18	GND	GND	No Connect	GND	GND	No Connect
19	REFCLK0_P	REFCLK0_N	No Connect	WAKE	No Connect	No Connect

Notes:

1. Asterisk (*) is used to indicate an active-low signal.
2. +3.3Vaux power is not used by the carrier. Contact Acromag to enable +3.3Vaux power to AcroPack modules and/or ID EEPROM. The carrier provides +3.3V power to the modules.
3. +12V_AUX and -12V_AUX are not used by the carrier. +12V and -12V are created from +3.3V to support XMC carriers that do not supply these voltages.

JTAG Programming/Debug Connector

JTAG programming/debug is supported through the JTAG signals of the XMC P15 connector. An alternate header is supplied if JTAG is not available from the XMC carrier (See reference designator J3 in Figure 3). JTAG is provided for developing applications that use Acromag's FPGA AcroPack modules. An adapter cable is available to connect to a Xilinx Platform USB II programming device (or equivalent). See Signal Interface Products for ordering information.

The pin assignment for J3 is shown below. A bypass circuit is included that will detect a vacant AcroPack site and close a switch to bypass the TDI and TDO signals. A CPLD on the carrier is included in the JTAG chain. The Xilinx Vivado

tools can detect the presence of the CPLD in the JTAG chain, and skip it when accessing the FPGAs on the AcroPack modules.

Table 1 JTAG Programming/Debug Connector (J3) Pin Assignment

Signal	Pin
TDI	1
TDO	2
GND	3
TCK	4
TMS	5
VREF (3.3V)	6

Notes:

TMS – **JTAG Test Mode Select**. This pin is the JTAG mode signal establishing appropriate TAP state transitions for target ISP devices sharing the same data stream.

TCK – **JTAG Test Clock**. This pin is the clock signal for JTAG operations and should be connected to the TCK pin on all target ISP devices sharing the same data stream.

TDO – **JTAG Test Data Out**. This pin is the serial data stream received from the TDO pin on the last device in a JTAG chain.

TDI – **JTAG Test Data In**. This pin outputs the serial data stream transmitted to the TDI pin on the first device in a JTAG chain.

V_{REF} – The target reference voltage V_{REF} is 3.3 Volts

GND – Signal Return

3. PROGRAMMING INFORMATION

This XMCAP2020/XMCAP2021 carrier board has no end user programmable components. The PCIe switch on the carrier is transparent to the end user.

4. THEORY OF OPERATION

This section describes the functionality of the circuitry used on the carrier board. Refer to Figure 6 as you read this section.

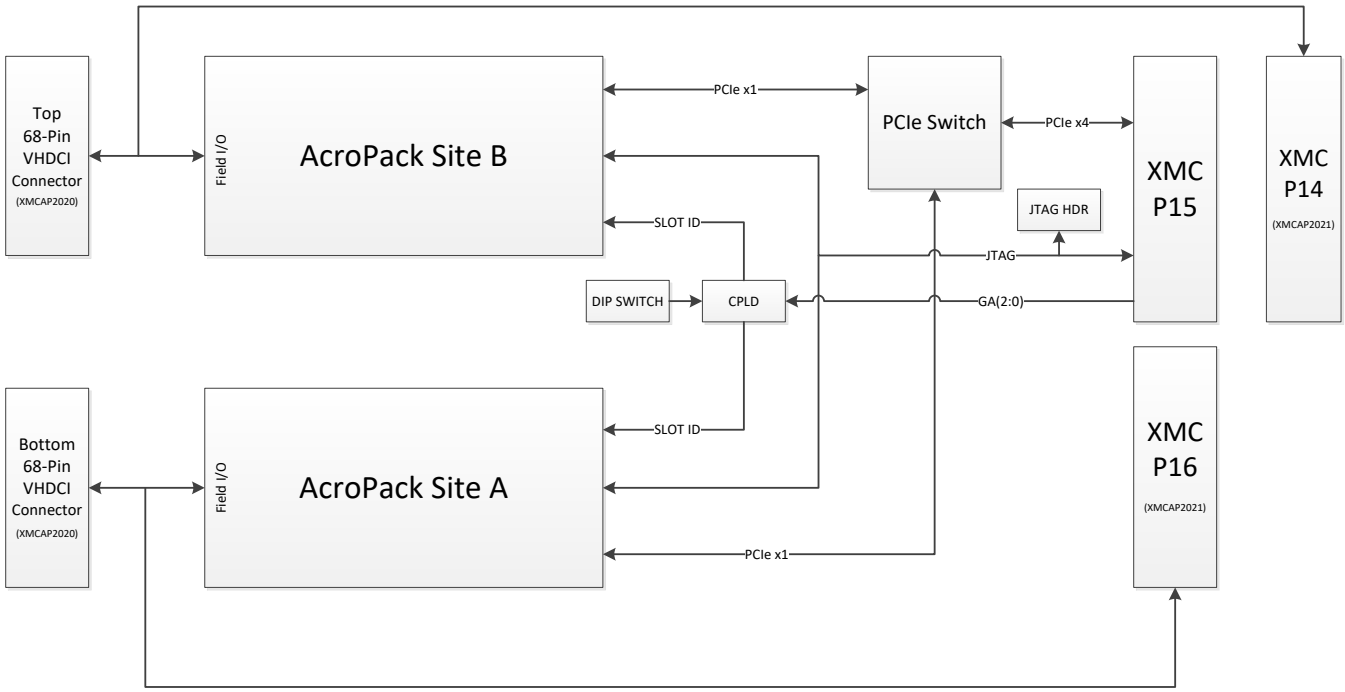


Figure 6 XMCAP2020/XMCAP2021 AcroPack Carrier Block Diagram

PCIe SWITCH

The PCIe switch is a 6 port 8 lane PCIe Gen 2 switch. It expands the single host PCIe port to two ports, one for each AcroPack site. The host port consists of four PCIe lanes, each of the AcroPack sites have one lane each.

Important Note: The XMCAP2020/XMCAP2021 board is not hot-swappable.

DC/DC CONVERTERS

The XMCAP2020/XMCAP2021 has four DC/DC converters to provide the power supply voltages to the AcroPack modules that are not present at the host interface. The +1.5V supply is sourced from the VPWR host power. The +5 Volt, +12 Volt, and -12V supplies are sourced from +3.3 Volt host power.

SLOT ADDRESSING

The XMCAP2020/XMCAP2021 carrier can be assigned by a combination of host supplied Geographical Addressing bits and/or by selecting the appropriate combination of SW1 switch settings. The slot address is 8 bits long and consists of 3 bits to identify the site on the carrier where the AcroPack module is installed and 5 bits that are determined by host's Geographical Address bits (A0-A2) and the SW1 switch settings on the carrier (A3,A4). The CPLD will serialize the slot address and transmit the address to the AcroPack module as requested by the AcroPack module. The processes of reading the slot address is typically initiated by host software. See CARRIER ADDRESS ASSIGNMENT in section 2 for details regarding slot address selection.

JTAG

A JTAG interface is provided for programming and debugging FPGAs on AcroPack modules. It is intended to be used with a Xilinx Platform USB II programming device. A bypass circuit is included that will detect a vacant AcroPack site and close a switch to complete the JTAG chain. The slot address CPLD is included first in the JTAG chain for factory programming. When two AcroPack modules with Xilinx FPGAs are installed on the carrier the module in slot A appears next in the chain followed by the module in slot B.

POWER SUPPLY FET SWITCHES

The +5V, +12V, and -12V power supplies to each AcroPack module are individually switched by onboard FETs. When the AcroPack PRESENT* signal, Pin 45 on the mini-PCIe connector, is seen to be grounded these supplies are turned on to supply voltage to the AcroPack module(s).

WARNING: When installing a commercial mini-PCIe module onto the XMCAP2020/XMCAP2021 board be sure that pin 45 on the module's mini-PCIe connector is not grounded or damage to the module may result.

5. SERVICE AND REPAIR

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Before beginning repair, be sure that all of the procedures in Section 2, PREPARATION FOR USE, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Verify that there are no blown fuses. Replacement of the carrier and/or AcroPack with one that is known to work correctly is a good technique to isolate a faulty board.

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at https://acromag.com. Our web site contains the most up-to-date product and software information.

Go to the “Support” tab to access:

- Application Notes/White Papers
- I/O Questions Answered

Acromag’s application engineers can also be contacted directly for technical assistance via email or telephone through the contact information listed below. Note that an email question can also be submitted from within the “I/O Questions Answered” or directly from the “Contact Us” tab. When needed, complete repair services are also available.

- Email: solutions@acromag.com
- Phone: 248-295-0310

6. SPECIFICATIONS

PHYSICAL

Physical Configuration (conforms to VITA 42 air-cooled XMC Specification)

Length.....5.866 inches (149 mm)
Width.....2.9134 inches (74 mm)
Board thickness .....0.066” +/-0.0066” (1.676 mm)
Max AcroPack module height .....0.083 inches (2.1 mm)*
Weight .....XMC2020-LF: 2.33 oz. (66 g); XMC2021-LF: 2.26 oz (64 g)

***Note: AcroPack/mini-PCIe modules with component height greater than 2.1mm will cause the XMCAP2020/XMCAP2021 to violate the 4.7mm maximum XMC module height specification. Taller Acropack/mini-PCIe modules may fit if component height under the XMCAP2020/XMCAP2021 on the carrier is less than 4.7mm.**

Current list of AcroPack modules taller than 2.1mm:

AP323E-LF (2.21mm)
AP445E-LF (2.184mm)
AP512E-LF (2.65mm)
AP513E-LF (2.82mm)
AP560AE-ISO-LF (2.65mm)
AP571-000 (4.6mm)
AP572-000 (4.6mm)
AP580E-LF (4.35mm)
AP580E-POE-LF (6.5mm)

Note: AP441E-LF is not recommended for use with the XMC AcroPack carrier.

Connectors

P15 (XMC/PCIe Bus) .....114-pin plug (Samtec ASP-103614-5)
Front I/O (Carrier Field I/O).....68-pin, Stacked, Champ (TE Connectivity 5787962), XMCAP2020 ONLY
P16 Rear I/O (Carrier Field I/O) .....114-pin plug (Samtec ASP-103614-5), XMCAP2021 ONLY
P14 Rear I/O (Carrier Field I/O) .....64-pin plug (Molex 71436-2464), XMCAP2021 ONLY
P1, P2 (AcroPack Field I/O).....100-pin socket (Samtec SS5-50-3.00-L-D-K-TR)
J1, J2 (Mini-PCIe) .....52-pin socket (TE Connectivity 1759547-1)
J3 (JTAG) .....6-pin micro connector (Molex 78171-5006)

ISOLATION

This AcroPack carrier is designed to provide isolation between the AcroPack Field I/O signals and the host. The AcroPack module must also be an isolated AcroPack module to maintain the isolation between the logic and field I/O signals. Unless isolation is provided on the AcroPack module itself, the field I/O connections are not isolated from the PCIe bus. The carrier onto which the XMCAP2020/XMCAP2021 board is installed must also provide isolation. Consult the XMC carrier board's documentation regarding this.

The isolation between different signal types is dependent on model and shown in Table 8

Table 8 Module Isolation Specifications

Model	Field I/O to Host Logic	Field I/O A to Field I/O B	Field I/O A pin to pin	Field I/O B pin to pin
XMCAP2020-LF	250V[1]	100V[2]	30V or 60V[3]	60V[4]
XMCAP2021-LF	60V[5]	60V[4]	60V[4]	60V[4]

Notes:

1. Isolated from each other for voltages up to 250VAC or DC on a continuous basis (unit will withstand a 1500VAC dielectric strength test for one minute without breakdown).
2. Isolated from each other for voltages up to 100VAC or DC on a continuous basis between the signals of different AcroPack modules (unit will withstand a 750VAC dielectric strength test for one minute without breakdown).
3. Designed to be isolated from each other for voltages up to 30VAC or DC on a continuous basis between pins of the Site A Front Panel I/O connector:

   Field I/O 3 - Field I/O 6
   Field I/O 7 - Field I/O 10
   Field I/O 11 - Field I/O 14
   Field I/O 15 - Field I/O 18
   Field I/O 19 - Field I/O 22
   Field I/O 23 - Field I/O 26
   Field I/O 27 - Field I/O 30
   Field I/O 31 - Field I/O 34
   Field I/O 35 - Field I/O 38
   Field I/O 39 - Field I/O 42
   Field I/O 43 - Field I/O 46
   Field I/O 47 - Field I/O 50

   All other Field I/O pins for the Site A front panel connectors are designed to be isolated from each other for voltages up to 60VAC or DC on a continuous basis between pins of the Site A Front Panel I/O connector.
4. Designed to be isolated from each other for voltages up to 60VAC or DC on a continuous basis between pins of the Site A Front Panel I/O connector.
5. Designed to be isolated from each other for voltages up to 60VAC or DC on a continuous basis (unit will withstand a 600VAC dielectric strength test for one minute without breakdown).

When this carrier is used with isolated AcroPack modules, both AcroPacks in slots A and should be isolated AcroPacks. Non-isolated AcroPacks sharing the same Connector will compromise the isolation integrity of the other AcroPack.

POWER

Board power requirements are a function of the installed AcroPack modules.

The current specified below is for the XMCAP2020/XMCAP2021 carrier board only.

+3.3 Volts (±5 %)	140 mA Typical
VPWR = +5V (±5 %)	200 mA Typical
VPWR = +12V (±8 %)	<100 mA Typical

Add the current for each of the AcroPack modules to calculate the total current required from each supply.

The carrier is designed to provide the voltages and currents to the AcroPack modules as shown in Table 9. Note the rated current is *combined* for both AcroPack modules.

Table 8 Module Isolation Specifications

Supply Voltage	Shared Current (Max)
+12V +/- 5% (max)	1 A[1]
-12V +/- 5% (max)	0.8 A[2]
+5V +/- 5% (max)	2 A[3]
+3.3V +/- 5% (max)	3 A[4]
+1.5V +/- 5% (max)	2 A[5]

Notes:

1. +12V is created from the host's +3.3V supply. This 1A current also supplies the -12V, so combined +12V and -12V current cannot exceed 1A.
2. -12V is created from the onboard +12V supply, which is fed from the host's +3.3V supply. Since the maximum output of the +12V supply is 1A, the combined +12V and -12V current cannot exceed 1A.
3. +5V is created from the host's +3.3V supply.
4. +3.3V is fed directly from the host's +3.3V supply.
5. +1.5V is created from the host's VPWR supply.

PCIe BUS COMPLIANCE

Specification .....This device meets or exceeds all written PCI Express specifications per revision 2.1. PCIe bus switch supports PCIe Gen 2 signals but rates exceed the rated bandwidth of the AcroPack connect.

ENVIRONMENTAL

Operating Temperature .....-40 to +70°C (with 200 LFM airflow)
Relative Humidity .....5-95% non-condensing
Storage Temperature .....-55 to +125°C.

EMC Compliance

The XMCAP2020/XMCAP2021 is designed to comply with EMC Directive 2004/108/EC.

Immunity	per EN 61000-6-2
	Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2
	Radiated Field Immunity (RFI), per IEC 61000-4-3
	Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4
	Surge Immunity, per IEC 61000-4-5
	Conducted RF Immunity (CRFI), per IEC 61000-4-6
Emissions	per EN61000-6-4
	Enclosure Port, per CISPR 16
	Low Voltage AC Mains Port, per CISPR 16
	Note: This is a Class A product

Vibration and Shock Standard

The XMCAP2020/XMCAP2021 is designed to pass the following Vibration and Shock standards.

Vibration, Sinusoidal Operating...Designed to comply with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis

Vibration, Random Operating.....Designed to comply with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis

Shock, Operating .....Designed to comply with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3mS half sine, 18 shocks at 6 orientations for both test levels

Reliability Prediction

XMCAC2020 MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled, G_BG_C*

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	1.991,980	227.4	502.0
40°C	1,252,395	143.0	798.5

[1] FIT is Failures in 10^9 hours.

XMCAC2021 MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled, G_BG_C*

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	1,676,654	191.4	596.4
40°C	1,064,183	121.5	939.7

[1] FIT is Failures in 10^9 hours.

7. CERTIFICATE OF VOLATILITY

Certificate of Volatility				
Acromag Model XMCAP2020/XMCAP2021	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) □ Yes ■ No				
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No				
Type (EEPROM, FLASH etc.)	Size:	User Modifiable	Function:	Process to Sanitize:
EEPROM	16K bytes	Yes	PCIe switch configuration	Overwrite EEPROM contents.
EEPROM	256 bytes	Yes	FRU Data	Overwrite EEPROM contents.

Acromag Representative				
Name: Russ Nieves	Title: Director of Sales and Marketing	Email: rnieves@acromag.com	Office Phone: 248-295-0838	Office Fax: 248-624-9234

8. REVISION HISTORY

Release Date	Version	EGR/DOC	Description of Revision
24-MAR-2017	A	DWR/ARP	Initial Release
4 JAN 2019	B	ENZ/ARP	Added modules that violate XMC height restrictions, added AP441E-LF note, cleaned up isolation specs.
4 NOV 2020	C	ENZ/AMM	Added MTBF numbers.
16 DEC 2022	D	AS/MJO	Correct Field I/O Connector Callouts on XMCAP2021 Primary Side figure, pg 8.
18 JAN 2024	E	AS/MJO	Correct Information in Table 4.