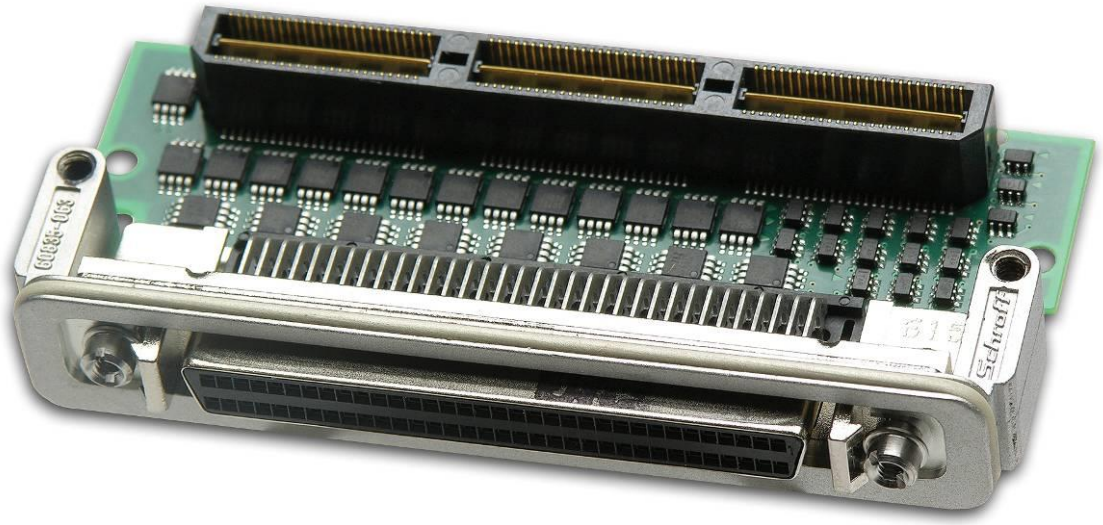
AXM-D Series and AXM-EDK
Digital I/O Mezzanine Modules

USER'S MANUAL



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IMPORTANT SAFETY CONSIDERATIONS

You must consider the possible negative effects of power, wiring, component, sensor, or software failure in the design of any type of control or monitoring system. This is very important where property loss or human life is involved. It is important that you perform satisfactory overall system design and it is agreed between you and Acromag, that this is your responsibility.

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1.0 GENERAL INFORMATION

The AXM-D series of daughter boards offer numerous digital options for Front I/O to Acromag's line of re-configurable PMC/XMC modules. The AXM-D03/AXM-DX03 provides 22/24 differential & 16 CMOS input/output channels on the Front I/O for compatible Acromag PMC/XMC modules. The data direction, input/output, for each channel can be independently controlled. Eight change-of-state interrupt channels are provided on the least significant eight differential channels.

The AXM-EDK board (sold with the PMC/XMC base boards' Engineering Design Kit) provides the standard Xilinx JTAG header as well as direct connections to the Xilinx FPGA. These general purpose LVTTL (Low Voltage TTL) I/O points allow the user to emulate AXM-D modules while using ChipScope®.

Table 1.1: *AXM-D Series and AXM-EDK Models*

MODEL	Front I/O Type	Front I/O Connector	OPERATING TEMPERATURE RANGE
AXM-D01	64 LVTTL	68 SCSI	-40°C to +85°C
AXM-D02	30 Differential	68 SCSI	-40°C to +85°C
AXM-D02-JTAG	30 Differential	68 SCSI	-40°C to +85°C
AXM-D03	22 Differential & 16 CMOS	68 SCSI	-40°C to +85°C
AXM-DX03	24 Differential & 16 CMOS	68 SCSI	-40°C to +85°C
AXM-D04	30 LVDS	68 SCSI	-40°C to +85°C
AXM-D04-JTAG	30 LVDS	68 SCSI	-40°C to +85°C
AXM-EDK	JTAG & LVTTL	Xilinx Std JTAG & 34-Pin 0.1" Header	-40°C to +85°C

KEY FEATURES

- **Multifunction Modules** – Various modules allows users to select the Front I/O required for their application.
- **Differential Input/Output Channels** – Differential RS485/RS422 can be configured for input or output with independent direction control.
- **Digital Input/Output Channels** – Interface with 5V compliant input/output CMOS channels which can be configured as input or output with independent direction control.
- **LVDS Input/Output Channels** – Low voltage differential signaling can be configured for input or output with independent direction control.
- **Xilinx JTAG Interface** – The AXM-D02-JTAG, AXM-D04-JTAG, and EDK boards provides the standard Xilinx JTAG interface to allow direct programming of the FPGA and an interface with ChipScope®.
- **Programmable Change of State/Level Interrupts –** Example code provides interrupts that are software programmable for any bit Change-Of-State or level on 8 channels.

- **Example Design –** The example VHDL design, provided in the base board EDK, includes control of all I/O, and eight Change-Of-State interrupts.

SIGNAL INTERFACE PRODUCTS

The AXM-D models' I/O is accessed via a 68 pin SCSI front panel connector.

Cables and a termination panel are available to interface with these boards.

See the Appendix for further information on these products.

Cable:

Model 5028-432: A 2-meter, round 68 conductor shielded cable with a male SCSI-3 connector at both ends and 34 twisted pairs. This cable is used for connecting the board to Model 5025-288 termination panels. For optimum performance, use the shortest possible length of shielded cable.

Termination Panel:

Model 5025-288: DIN-rail mountable panel provides 68 screw terminals for universal field I/O termination. Connects to Acromag board, via SCSI-3 to twisted pair cable described above.

ENGINEERING DESIGN KIT

Acromag does not provide an engineering design kit specifically for the AXM-D modules. However, an example design for each module is included in the Engineering Design Kit of the PMC/XMC base board. Furthermore, the AXM-EDK is included with the Engineering Design Kit of the PMC/XMC base board to allow for programming via the JTAG interface. Refer to the PMC/XMC base board's manual for further information on the available Engineering Design Kit.

BOARD CONTROL SOFTWARE

Acromag does not provide board control software specifically for the AXM-EDK and AXM-D series boards. However, the AXM-EDK and each AXM-D module can be accessed via the control software for the base PMC/XMC module. These products (sold separately) facilitate the product interface in the following operating systems: Windows® DLL, VxWorks®, and QNX®. Refer to the PMC/XMC base board's manual for further information.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation.

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

CARD CAGE CONSIDERATIONS

IMPORTANT: *Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.*

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Remove power from the system before installing board, cables, termination panels, and field wiring.

Default Hardware Configuration

The AXM-EDK and AXM-D Series boards cannot stand-alone and must be mated with a compatible Acromag PMC/XMC module. The default configuration of the control register bits at power-up is described in section 3.

Front Panel Field I/O Connector

The front panel connector provides the field I/O interface connections. For the AXM-D series, it is a SCSI-3 68-pin female connector (AMP 5787394-7 or equivalent) employing latch blocks and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-288 from the front panel via round shielded cable (Model 5028-432).

The AXM-EDK board has two front I/O connectors. The first is a double row 14-pin 2mm header (male) for JTAG programming. This is the standard Xilinx JTAG Header. The other I/O interface is a double row 34-pin 0.1" header (male). A standard floppy drive cable can be used to connect to the interface. Note neither cables are available from Acromag.

AXM-D01 Front I/O

The AXM-D01 module has 64 LVTTL I/O channels (connecting directly to the FPGA - can be other I/O standards). This module is for straight thru I/O (no pull-ups or pull-downs). Custom modules are available for optional pull-ups, pull downs, JTAG, and fused power for front I/O use. The pin out is shown in Table 2.1.

***Table 2.1: AXM-D01** Board Field I/O Pin Connections*

SCSI-3 68-Pin Female Connector			
Pin Description	**Pin**	**Pin Description**	**Pin**
[Fused +5V]	1	COMMON	35
[Fused +3.3V]	2	COMMON	36
LVTTL IO 0 (TMS)	3	LVTTL IO 1 (TDI)	37
LVTTL IO 2 (TCK)	4	LVTTL IO 3 (TDO)	38
LVTTL IO 4	5	LVTTL IO 5	39
LVTTL IO 6	6	LVTTL IO 7	40
LVTTL IO 8	7	LVTTL IO 9	41
LVTTL IO 10	8	LVTTL IO 11	42
LVTTL IO 12	9	LVTTL IO 13	43
LVTTL IO 14	10	LVTTL IO 15	44
LVTTL IO 16	11	LVTTL IO 17	45
LVTTL IO 18	12	LVTTL IO 19	46
LVTTL IO 20	13	LVTTL IO 21	47
LVTTL IO 22	14	LVTTL IO 23	48
LVTTL IO 24	15	LVTTL IO 25	49
LVTTL IO 26	16	LVTTL IO 27	50
LVTTL IO 28	17	LVTTL IO 29	51
LVTTL IO 30	18	LVTTL IO 31	52
LVTTL IO 32	19	LVTTL IO 33	53
LVTTL IO 34	20	LVTTL IO 35	54
LVTTL IO 36	21	LVTTL IO 37	55
LVTTL IO 38	22	LVTTL IO 39	56
LVTTL IO 40	23	LVTTL IO 41	57
LVTTL IO 42	24	LVTTL IO 43	58
LVTTL IO 44	25	LVTTL IO 45	59
LVTTL IO 46	26	LVTTL IO 47	60
LVTTL IO 48	27	LVTTL IO 49	61
LVTTL IO 50	28	LVTTL IO 51	62
LVTTL IO 52	29	LVTTL IO 53	63
LVTTL IO 54	30	LVTTL IO 55	64
LVTTL IO 56	31	LVTTL IO 57	65
LVTTL IO 58	32	LVTTL IO 59	66
LVTTL IO 60	33	LVTTL IO 61	67
LVTTL IO 62	34	LVTTL IO 63	68

[ ] Optional fused power for front I/O use.
( ) Optional JTAG for front panel use.

AXM-D02 Front I/O

The AXM-D02 module has 30 differential I/O channels. The data direction of the differential channels numbered 0 to 29 are independently controlled via the Differential Direction Register. The pinout is shown in Table 2.2.

***Table 2.2: AXM-D02** Board Field I/O Pin Connections*

SCSI-3 68-Pin Female Connector			
Pin Description	**Pin**	**Pin Description**	**Pin**
COMMON	1	COMMON	35
Differential Ch0+	2	Differential Ch0-	36
Differential Ch1+	3	Differential Ch1-	37
Differential Ch2+	4	Differential Ch2-	38
Differential Ch3+	5	Differential Ch3-	39
Differential Ch4+	6	Differential Ch4-	40
Differential Ch5+	7	Differential Ch5-	41
Differential Ch6+	8	Differential Ch6-	42
Differential Ch7+	9	Differential Ch7-	43
Differential Ch8+	10	Differential Ch8-	44
Differential Ch9+	11	Differential Ch9-	45
COMMON	12	COMMON	46
Differential Ch10+	13	Differential Ch10-	47
Differential Ch11+	14	Differential Ch11-	48
Differential Ch12+	15	Differential Ch12-	49
Differential Ch13+	16	Differential Ch13-	50
Differential Ch14+	17	Differential Ch14-	51
Differential Ch15+	18	Differential Ch15-	52
Differential Ch16+	19	Differential Ch16-	53
Differential Ch17+	20	Differential Ch17-	54
Differential Ch18+	21	Differential Ch18-	55
Differential Ch19+	22	Differential Ch19-	56
COMMON	23	COMMON	57
Differential Ch20+	24	Differential Ch20-	58
Differential Ch21+	25	Differential Ch21-	59
Differential Ch22+	26	Differential Ch22-	60
Differential Ch23+	27	Differential Ch23-	61
Differential Ch24+	28	Differential Ch24-	62
Differential Ch25+	29	Differential Ch25-	63
Differential Ch26+	30	Differential Ch26-	64
Differential Ch27+	31	Differential Ch27-	65
Differential Ch28+	32	Differential Ch28-	66
Differential Ch29+	33	Differential Ch29-	67
COMMON	34	COMMON	68

AXM-D02-JTAG Front I/O

The AXM-D02-JTAG module has 30 differential I/O channels. The data direction of the differential channels numbered 0 to 29 are independently controlled via the Differential Direction Register. The pinout is shown in Table 2.3.

Table 2.3: AXM-D02-JTAG *Board Field I/O Pin Connections*

SCSI-3 68-Pin Female Connector			
Pin Description	**Pin**	**Pin Description**	**Pin**
SCSI_TCK	1	COMMON	35
Differential Ch0+	2	Differential Ch0-	36
Differential Ch1+	3	Differential Ch1-	37
Differential Ch2+	4	Differential Ch2-	38
Differential Ch3+	5	Differential Ch3-	39
Differential Ch4+	6	Differential Ch4-	40
Differential Ch5+	7	Differential Ch5-	41
Differential Ch6+	8	Differential Ch6-	42
Differential Ch7+	9	Differential Ch7-	43
Differential Ch8+	10	Differential Ch8-	44
Differential Ch9+	11	Differential Ch9-	45
SCSI_TMS	12	COMMON	46
Differential Ch10+	13	Differential Ch10-	47
Differential Ch11+	14	Differential Ch11-	48
Differential Ch12+	15	Differential Ch12-	49
Differential Ch13+	16	Differential Ch13-	50
Differential Ch14+	17	Differential Ch14-	51
Differential Ch15+	18	Differential Ch15-	52
Differential Ch16+	19	Differential Ch16-	53
Differential Ch17+	20	Differential Ch17-	54
Differential Ch18+	21	Differential Ch18-	55
Differential Ch19+	22	Differential Ch19-	56
SCSI_TDI	23	COMMON	57
Differential Ch20+	24	Differential Ch20-	58
Differential Ch21+	25	Differential Ch21-	59
Differential Ch22+	26	Differential Ch22-	60
Differential Ch23+	27	Differential Ch23-	61
Differential Ch24+	28	Differential Ch24-	62
Differential Ch25+	29	Differential Ch25-	63
Differential Ch26+	30	Differential Ch26-	64
Differential Ch27+	31	Differential Ch27-	65
Differential Ch28+	32	Differential Ch28-	66
Differential Ch29+	33	Differential Ch29-	67
SCSI_TDO	34	SCSI_JTAG_PWR	68

AXM-D03 Front I/O

The AXM-D03 module has 22 differential I/O channels and 16 digital (CMOS) channels. The data direction of the differential channels numbered 8 to 29 and digital channels numbered 0 to 15 are independently controlled via the Differential and Digital Direction Registers. The pinout is shown in Table 2.4.

***Table 2.4: AXM-D03** Board Field I/O Pin Connections*

DIFFERENTIAL CHANNELS ARE NUMBERED 8 to 29. THERE ARE NO DIFFERENTIAL CHANNELS 0 to 7 ON THIS MODULE.

SCSI-3 68-Pin Female Connector			
Pin Description	**Pin**	**Pin Description**	**Pin**
COMMON	1	COMMON	35
Digital Channel 0	2	*Digital Channel 8*	36
Digital Channel 1	3	*Digital Channel 9*	37
Digital Channel 2	4	*Digital Channel 10*	38
Digital Channel 3	5	*Digital Channel 11*	39
Digital Channel 4	6	*Digital Channel 12*	40
Digital Channel 5	7	*Digital Channel 13*	41
Digital Channel 6	8	*Digital Channel 14*	42
Digital Channel 7	9	*Digital Channel 15*	43
Differential Ch8+	10	Differential Ch8-	44
Differential Ch9+	11	Differential Ch9-	45
COMMON	12	COMMON	46
Differential Ch10+	13	Differential Ch10-	47
Differential Ch11+	14	Differential Ch11-	48
Differential Ch12+	15	Differential Ch12-	49
Differential Ch13+	16	Differential Ch13-	50
Differential Ch14+	17	Differential Ch14-	51
Differential Ch15+	18	Differential Ch15-	52
Differential Ch16+	19	Differential Ch16-	53
Differential Ch17+	20	Differential Ch17-	54
Differential Ch18+	21	Differential Ch18-	55
Differential Ch19+	22	Differential Ch19-	56
COMMON	23	COMMON	57
Differential Ch20+	24	Differential Ch20-	58
Differential Ch21+	25	Differential Ch21-	59
Differential Ch22+	26	Differential Ch22-	60
Differential Ch23+	27	Differential Ch23-	61
Differential Ch24+	28	Differential Ch24-	62
Differential Ch25+	29	Differential Ch25-	63
Differential Ch26+	30	Differential Ch26-	64
Differential Ch27+	31	Differential Ch27-	65
Differential Ch28+	32	Differential Ch28-	66
Differential Ch29+	33	Differential Ch29-	67
COMMON	34	COMMON	68

AXM-DX03 Front I/O

The AXM-DX03 module has 24 differential I/O channels and 16 digital (CMOS) channels. The data direction of the differential channels numbered 16 to 39 and digital channels numbered 0 to 15 are independently controlled via the Differential and Digital Direction Registers. The pinout is shown in Table 2.5.

SCSI-3 68-Pin Female Connector			
Pin Description	**Pin**	**Pin Description**	**Pin**
Digital Channel 0	1	COMMON	35
Digital Channel 1	2	COMMON	36
Digital Channel 2	3	Differential Ch24+	37
Digital Channel 3	4	Differential Ch24-	38
Digital Channel 4	5	Differential Ch25+	39
Digital Channel 5	6	Differential Ch25-	40
Digital Channel 6	7	Differential Ch26+	41
Digital Channel 7	8	Differential Ch26-	42
Digital Channel 8	9	Differential Ch27+	43
Digital Channel 9	10	Differential Ch27-	44
Digital Channel 10	11	Differential Ch28+	45
Digital Channel 11	12	Differential Ch28-	46
Digital Channel 12	13	Differential Ch29+	47
Digital Channel 13	14	Differential Ch29-	48
Digital Channel 14	15	Differential Ch30+	49
Digital Channel 15	16	Differential Ch30-	50
COMMON	17	Differential Ch31+	51
COMMON	18	Differential Ch31-	52
Differential Ch16+	19	Differential Ch32+	53
Differential Ch16-	20	Differential Ch32-	54
Differential Ch17+	21	Differential Ch33+	55
Differential Ch17-	22	Differential Ch33-	56
Differential Ch18+	23	Differential Ch34+	57
Differential Ch18-	24	Differential Ch34-	58
Differential Ch19+	25	Differential Ch35+	59
Differential Ch19-	26	Differential Ch35-	60
Differential Ch20+	27	Differential Ch36+	61
Differential Ch20-	28	Differential Ch36-	62
Differential Ch21+	29	Differential Ch37+	63
Differential Ch21-	30	Differential Ch37-	64
Differential Ch22+	31	Differential Ch38+	65
Differential Ch22-	32	Differential Ch38-	66
Differential Ch23+	33	Differential Ch39+	67
Differential Ch23-	34	Differential Ch39-	68

Table 2.5: AXM-DX03 *Board Field I/O Pin Connections*

DIFFERENTIAL CHANNELS ARE NUMBERED 8 to 29. THERE ARE NO DIFFERENTIAL CHANNELS 0 to 7 ON THIS MODULE.

AXM-D04 Front I/O

The AXM-D04 module has 30 Low Voltage Differential Signaling (LVDS) channels. The data direction of the differential channels numbered 0 to 29 are independently controlled via the Differential Direction Registers. The pinout is shown in Table 2.6.

***Table 2.6: AXM-D04** Board Field I/O Pin Connections*

SCSI-3 68-Pin Female Connector			
Pin Description	**Pin**	**Pin Description**	**Pin**
COMMON	1	COMMON	35
LVDS Ch0+	2	LVDS Ch0-	36
LVDS Ch1+	3	LVDS Ch1-	37
LVDS Ch2+	4	LVDS Ch2-	38
LVDS Ch3+	5	LVDS Ch3-	39
LVDS Ch4+	6	LVDS Ch4-	40
LVDS Ch5+	7	LVDS Ch5-	41
LVDS Ch6+	8	LVDS Ch6-	42
LVDS Ch7+	9	LVDS Ch7-	43
LVDS Ch8+	10	LVDS Ch8-	44
LVDS Ch9+	11	LVDS Ch9-	45
COMMON	12	COMMON	46
LVDS Ch10+	13	LVDS Ch10-	47
LVDS Ch11+	14	LVDS Ch11-	48
LVDS Ch12+	15	LVDS Ch12-	49
LVDS Ch13+	16	LVDS Ch13-	50
LVDS Ch14+	17	LVDS Ch14-	51
LVDS Ch15+	18	LVDS Ch15-	52
LVDS Ch16+	19	LVDS Ch16-	53
LVDS Ch17+	20	LVDS Ch17-	54
LVDS Ch18+	21	LVDS Ch18-	55
LVDS Ch19+	22	LVDS Ch19-	56
COMMON	23	COMMON	57
LVDS Ch20+	24	LVDS Ch20-	58
LVDS Ch21+	25	LVDS Ch21-	59
LVDS Ch22+	26	LVDS Ch22-	60
LVDS Ch23+	27	LVDS Ch23-	61
LVDS Ch24+	28	LVDS Ch24-	62
LVDS Ch25+	29	LVDS Ch25-	63
LVDS Ch26+	30	LVDS Ch26-	64
LVDS Ch27+	31	LVDS Ch27-	65
LVDS Ch28+	32	LVDS Ch28-	66
LVDS Ch29+	33	LVDS Ch29-	67
COMMON	34	COMMON	68

AXM-D04-JTAG Front I/O

The AXM-D04-JTAG module has 30 Low Voltage Differential Signaling (LVDS) channels. The data direction of the differential channels numbered 0 to 29 are independently controlled via the Differential Direction Registers. The pinout is shown in Table 2.7.

Table 2.7: AXM-D04-JTAG *Board Field I/O Pin Connections*

SCSI-3 68-Pin Female Connector			
Pin Description	**Pin**	**Pin Description**	**Pin**
SCSI_TCK	1	COMMON	35
LVDS Ch0+	2	LVDS Ch0-	36
LVDS Ch1+	3	LVDS Ch1-	37
LVDS Ch2+	4	LVDS Ch2-	38
LVDS Ch3+	5	LVDS Ch3-	39
LVDS Ch4+	6	LVDS Ch4-	40
LVDS Ch5+	7	LVDS Ch5-	41
LVDS Ch6+	8	LVDS Ch6-	42
LVDS Ch7+	9	LVDS Ch7-	43
LVDS Ch8+	10	LVDS Ch8-	44
LVDS Ch9+	11	LVDS Ch9-	45
SCSI_TMS	12	COMMON	46
LVDS Ch10+	13	LVDS Ch10-	47
LVDS Ch11+	14	LVDS Ch11-	48
LVDS Ch12+	15	LVDS Ch12-	49
LVDS Ch13+	16	LVDS Ch13-	50
LVDS Ch14+	17	LVDS Ch14-	51
LVDS Ch15+	18	LVDS Ch15-	52
LVDS Ch16+	19	LVDS Ch16-	53
LVDS Ch17+	20	LVDS Ch17-	54
LVDS Ch18+	21	LVDS Ch18-	55
LVDS Ch19+	22	LVDS Ch19-	56
SCSI_TDI	23	COMMON	57
LVDS Ch20+	24	LVDS Ch20-	58
LVDS Ch21+	25	LVDS Ch21-	59
LVDS Ch22+	26	LVDS Ch22-	60
LVDS Ch23+	27	LVDS Ch23-	61
LVDS Ch24+	28	LVDS Ch24-	62
LVDS Ch25+	29	LVDS Ch25-	63
LVDS Ch26+	30	LVDS Ch26-	64
LVDS Ch27+	31	LVDS Ch27-	65
LVDS Ch28+	32	LVDS Ch28-	66
LVDS Ch29+	33	LVDS Ch29-	67
SCSI_TDO	34	SCSI_JTAG_PWR	68

AXM-EDK Front I/O

The AXM-EDK has a standard 34 pin double row 0.1" header for front I/O. The I/O are LVTTL compatible. These pin connections can emulate the 30 differential channels on the AXM-D02 and AXM-D04 models and the 22/24 differential channels on the AXM-D03/AXM-DX03 model using LVTTL signaling. Refer to the Differential I/O Register section for further information. Front I/O connections are listed in Table 2.8a.

The AXM-EDK front I/O also includes the standard Xilinx 14-pin 2mm JTAG header. This header can be used to directly program the FPGA or to interface with the FPGA debug software ChipScope®. The pin connections are shown in table 2.8b.

In addition, the AXM-EDK contains 16 auxiliary pins that are routed to two 8 pin SIP patterns on the board. *Note that these are not front panel I/O connections.* Due to height restrictions SIP sockets are not installed. This allows for full end user customization. These pins correspond to the 16 channels of Digital I/O on the AXM-D03/AXM-DX03 module. Refer to the Digital I/O Register section for further information. The connections are listed in table 2.8c.

Refer to drawing 4502-056, located at the end of this manual, for I/O pin locations on the AXM-EDK.

***Table 2.8a: AXM-EDK** Board Field I/O Pin Connections*

34-Pin Double Row 0.1" I/O Header			
Pin Description	**Pin**	**Pin Description**	**Pin**
COMMON	1	COMMON	2
LVTTL Channel 0	3	LVTTL Channel 1	4
LVTTL Channel 2	5	LVTTL Channel 3	6
LVTTL Channel 4	7	LVTTL Channel 5	8
LVTTL Channel 6	9	LVTTL Channel 7	10
LVTTL Channel 8	11	LVTTL Channel 9	12
LVTTL Channel 10	13	LVTTL Channel 11	14
LVTTL Channel 12	15	LVTTL Channel 13	16
LVTTL Channel 14	17	LVTTL Channel 15	18
LVTTL Channel 16	19	LVTTL Channel 17	20
LVTTL Channel 18	21	LVTTL Channel 19	22
LVTTL Channel 20	23	LVTTL Channel 21	24
LVTTL Channel 22	25	LVTTL Channel 23	26
LVTTL Channel 24	27	LVTTL Channel 25	28
LVTTL Channel 26	29	LVTTL Channel 27	30
LVTTL Channel 28	31	LVTTL Channel 29	32
COMMON	33	COMMON	34

***Table 2.8b: AXM-EDK** Board Field JTAG Pin Connections*

14-Pin 2mm Double Row JTAG Header			
Pin Description	**Pin**	**Pin Description**	**Pin**
COMMON	1	+3.3V	2
COMMON	3	TMS	4
COMMON	5	TCK	6
COMMON	7	TDO	8
COMMON	9	TDI	10
COMMON	11	Not Connected	12
COMMON	13	Not Connected	14

AXM-EDK Front I/O

Auxiliary (LVTTL) I/O Pin Connections (SIP)			
SIP 1 (S1)		SIP 2 (S2)	
Pin Description	**Pin**	**Pin Description**	**Pin**
AUX Channel 0	1	AUX Channel 8	1
AUX Channel 1	2	AUX Channel 9	2
AUX Channel 2	3	AUX Channel 10	3
AUX Channel 3	4	AUX Channel 11	4
AUX Channel 4	5	AUX Channel 12	5
AUX Channel 5	6	AUX Channel 13	6
AUX Channel 6	7	AUX Channel 14	7
AUX Channel 7	8	AUX Channel 15	8

Table 2.8c: AXM-EDK
Auxiliary I/O Pin Connections

Non-Isolation Considerations

The board is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the boards.

These models are daughter cards intended only for use on specific Acromag PMC/XMC modules. As such only a small portion of I/O memory space is currently reserved for operation of the daughter card. The remaining memory space is defined in the base boards User's Manual.

AXM-EDK & AXM-D GENERIC MEMORY MAP

The generic memory space address map for the board is shown in Table 3.2. The actual bit mapping in the individual registers varies by the mezzanine module and are detailed in the register descriptions later in this manual. Note that the base address from the base PMC/XMC module in memory space must be added to the addresses shown to properly access the board registers. Register accesses as 32, 16, and 8-bits in memory space are permitted.

Table 3.2: Memory Map

Base Addr+	D31 D16	D15 D00	Base Addr+
0003 ↓ 7FFF	Reserved for base PMC/XMC Module[1]		0000 ↓ 7FFC
8003	Board Status Register and Software Reset[2]		8000
8007	31-0 Differential & EDK I/O Register[3]		8004
800B	Direction Register Differential & EDK Channels 31-0[3]		8008
800F	31-0 Digital I/O Register[3]		800C
8013	Direction Register Digital Channels 31-0[3]		8010
8017	Not Used[4]	Interrupt Enable Differential Ch. 15-8	8014
801B	Not Used[4]	Interrupt Type Differential Ch. 15-8	8018
801F	Not Used[4]	Interrupt Polarity Differential Ch. 15-8	801C
8023	Not Used[4]		8020
8027	Not Used[4]		8024
802B	Not Used[4]		8028
802F ↓ 1FFFFF	Reserved for base PMC/XMC Module[1]		802C ↓ 1FFFFC

1. This address space is not defined for this module. This space may be used on the base PMC/XMC Module. Refer to the base PMC/XMC module User's Manual for further information

2. These registers have bits that are reserved for the base PMC/XMC module. See the register definition later in this manual for further details.

3. The bits used in these registers varies for each model. Refer to the register descriptions in the following pages for specific module mapping.

4. The board will return 0 for all addresses that are "Not Used".

This memory map reflects byte accesses using the "Little Endian" byte ordering format. Little Endian uses even-byte addresses to store the low-order byte. The Intel x86 family of microprocessors uses "Little Endian" byte ordering. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses.

Board Status and Software Reset Register (Read/Write) – (Base Addr + 8000H)

BOARD STATUS AND RESET REGISTER

This read/write register is used the issue a software reset, view and clear pending interrupts, and to identify the attached AXM module. It may also provide other functions that are defined by the base board. Writing a "1" to bit 31 of this register will cause a software reset effecting both the PMC/XMC base board and all of the AXM series registers. Bits 15 to 13 are used for AXM identification code.

Bits 0 to 7 or this register reflect the status of each of the Differential I/O channels 8 to 15. A **Read** of this bit reflects the interrupt pending status. Read of a "1" indicates that an interrupt is pending for the corresponding differential channel. **Write** of a logic "1" to this bit will release the corresponding differential channel's pending interrupt. Writing "0" to a bit location has no effect, a pending interrupt will remain pending.

BIT	FUNCTION	
0	Differential Channel 8 Interrupt Pending/Clear	
1	Differential Channel 9 Interrupt Pending/Clear	
2	Differential Channel 10 Interrupt Pending/Clear	
3	Differential Channel 11 Interrupt Pending/Clear	
4	Differential Channel 12 Interrupt Pending/Clear	
5	Differential Channel 13 Interrupt Pending/Clear	
6	Differential Channel 14 Interrupt Pending/Clear	
7	Differential Channel 15 Interrupt Pending/Clear	
12-8	Reserved for PMC/XMC base board[3]	
15-13	AXM Identification bits[1,2] (Read Only)	
	AXM-D01	"100"
	AXM-D02	"001"
	AXM-D03	"001"
	AXM-D03-JTAG	"001"
	AXM-DX03	"001"
	AXM-D04	"001"
	AXM-D04-JTAG	"001"
	AXM-EDK	"001"
30-16	Reserved for PMC/XMC base board[3]	
31	Software Reset (Write Only)	

1. Note that if no AXM module is attached the register will still read "001". It is up to the end user to differentiate if no mezzanine module is attached.
2. All other 3 bit values are reserved for future use.
3. Bit function is defined by the base PMC/XMC Module.

This register can be written with either 8-bit, 16-bit, or 32-bit data transfers.

DIFFERENTIAL INPUT/OUTPUT REGISTERS

Differential & EDK Input/Output Registers (Read/Write) – (Base Addr + 8004H)

AXM-D2/3/4 differential channels and the AXM-D01 and AXM-EDK LVTTL channels may be individually accessed via this register at the carrier base address +8004H. This includes all 30 differential channels on the AXM-D02(AXM-D02-JTAG), 22/24 differential channels on the AXM-D03/AXM-DX03, 30 LVDS channels on the AXM-D04(AXM-D04-JTAG), 32 general purpose LVTTL channel on the AXM-D01, and 30 general purpose LVTTL channels on the AXM-EDK. Each channel is controlled by its corresponding data bit, as shown in the register mapping table below. Channel input signal levels are determined by reading this register. Likewise, channel output signal levels are set by writing to this register. Note that the data direction, input or output, must first be set via theDifferential Direction register at base address plus 8008H.

Model	Differential I/O Register Mapping							
	D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**
AXM-EDK	Not Used		I/O 29	I/O 28	I/O 27	I/O 26	I/O 25	I/O 24
AXM-D01	I/O 31	I/O 30	I/O 29	I/O 28	I/O 27	I/O 26	I/O 25	I/O 24
AXM-D02[1]	Not Used		Diff 29	Diff 28	Diff 27	Diff 26	Diff 25	Diff 24
AXM-D03	Not Used		Diff 29	Diff 28	Diff 27	Diff 26	Diff 25	Diff 24
AXM-DX03	Diff 39	Diff 38	Diff 37	Diff 36	Diff 35	Diff 34	Diff 33	Diff 32
AXM-D04[2]	Not Used		LVDS 29	LVDS 28	LVDS 27	LVDS 26	LVDS 25	LVDS 24

	D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
AXM-EDK	I/O 23	I/O 22	I/O 21	I/O 20	I/O 19	I/O 18	I/O 17	I/O 16
AXM-D01	I/O 23	I/O 22	I/O 21	I/O 20	I/O 19	I/O 18	I/O 17	I/O 16
AXM-D02[1]	Diff 23	Diff 22	Diff 21	Diff 20	Diff 19	Diff 18	Diff 17	Diff 16
AXM-D03	Diff 23	Diff 22	Diff 21	Diff 20	Diff 19	Diff 18	Diff 17	Diff 16
AXM-DX03	Diff 31	Diff 30	Diff 29	Diff 28	Diff 27	Diff 26	Diff 25	Diff 24
AXM-D04[2]	LVDS 23	LVDS 22	LVDS 21	LVDS 20	LVDS 19	LVDS 18	LVDS 17	LVDS 16

	D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
AXM-EDK	I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9	I/O 8
AXM-D01	I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9	I/O 8
AXM-D02[1]	Diff 15	Diff 14	Diff 13	Diff 12	Diff 11	Diff 10	Diff 9	Diff 8
AXM-D03	Diff 15	Diff 14	Diff 13	Diff 12	Diff 11	Diff 10	Diff 9	Diff 8
AXM-DX03	Diff 23	Diff 22	Diff 21	Diff 20	Diff 19	Diff 18	Diff 17	Diff 16
AXM-D04[2]	LVDS 15	LVDS 14	LVDS 13	LVDS 12	LVDS 11	LVDS 10	LVDS 9	LVDS 8

	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
AXM-EDK	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
AXM-D01	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
AXM-D02[1]	Diff 7	Diff 6	Diff 5	Diff 4	Diff 3	Diff 2	Diff 1	Diff 0
AXM-D03	Diff Channels 0-7 are not used in this module.							
AXM-DX03	Diff Channels 0-15 are not used in this module.							
AXM-D04	LVDS 7	LVDS 6	LVDS 5	LVDS 4	LVDS 3	LVDS 2	LVDS 1	LVDS 0

1. This register definition also applies to the AXM-D02-JTAG.
2. This register definition also applies to the AXM-D04-JTAG

Channel read/write operations use 8-bit, 16-bit, or 32-bit data transfers with the lower ordered bits corresponding to the lower-numbered channels for the register of interest. All input/output channels are configured as inputs following a power-on or software reset. Data-bits 30 and 31 are not used and will return 0 when read for all but the AXM-D01/AXM-DX03 module. Data bits 0 through 7 in the AXM-D03/AXM-DX03 module will read back the last data values written to those bits, except for bits 0 & 1 will always read 0.

DIFFERENTIAL INPUT/OUTPUT REGISTERS

Differential Direction Control Register (Read/Write) – (Base Addr + 8008H)

The data direction (input or output) of the differential channels is selected via this register at the carrier base address +8008H. This includes the direction of all 32 differential channels on the AXM-D01, 30 differential channels on the AXM-D02(AXM-D02-JTAG), 22/24 differential channels on the AXM-D03/AXM-DX03, 30 LVDS channels on the AXM-D04(AXM-D04-JTAG), and 30 general purpose LVTTL channels on the AXM-EDK. The direction of each channel is controlled by its corresponding data bit. Data bit use varies depending on the module selected. The bit mapping corresponds to the Differential and EDK I/O Register.

Independent channel direction control is provided for each differential channel. Setting a bit low configures the corresponding channel data direction for input. Setting the control bit high configures the corresponding channel data direction for output.

The default power-up state of these registers is logic low. Thus, all channels are configured as inputs following system reset or power-up. Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers. Data-bits 30 and 31 are not used and will return 0 when read for all but the AXM-D01/AXMDX03 module. Data bits 0 through 7 in the AXM-D03/AXM-DX03 module will read back the last data values written to those bits, except for bits 0 & 1 will always read 0.

DIGITAL INPUT/OUTPUT REGISTERS

Digital Input/Output Registers (Read/Write) – (Base Addr + 800CH)

Digital CMOS input/output channels may be individually accessed via this register at the carrier base address +800CH. This includes the sixteen CMOS Channels on the AXM-D03/AXM-DX03, 32 upper data channels for the AXM-D01 and the sixteen auxiliary LVTTL I/O on the AXM-EDK module. Channel input signal levels are determined by reading this register. Likewise, channel output signal levels are set by writing to this register. The data bits are mapped according to the following table. Note that the data direction, input or output, must first be set via the Digital Direction register at base address plus 8010H

Model	Digital I/O Register Mapping							
	D31	D30	D29	D28	D27	D26	D25	D24
AXM-EDK	Not Used							
AXM-D01	I/O 63	I/O 62	I/O 61	I/O 60	I/O 59	I/O 58	I/O 57	I/O 56
AXM-D02[1]	Not Used							
AXM-D03	Not Used							

AXM-DX03	Not Used
AXM-D04[2]	Not Used

	D23	D22	D21	D20	D19	D18	D17	D16
AXM-EDK	Not Used							
AXM-D01	I/O 55	I/O 54	I/O 53	I/O 52	I/O 51	I/O 50	I/O 49	I/O 48
AXM-D02[1]	Not Used							
AXM-D03	Not Used							
AXM-DX03	Not Used							
AXM-D04[2]	Not Used							

	D15	D14	D13	D12	D11	D10	D9	D8
AXM-EDK	AUX 15	AUX 14	AUX 13	AUX 12	AUX 11	AUX 10	AUX 9	AUX 8
AXM-D01	I/O 47	I/O 46	I/O 45	I/O 44	I/O 43	I/O 42	I/O 41	I/O 40
AXM-D02[1]	Not Used							
AXM-D03	DIG 15	DIG 14	DIG 13	DIG 12	DIG 11	DIG 10	DIG 9	DIG 8
AXM-DX03	DIG 15	DIG 14	DIG 13	DIG 12	DIG 11	DIG 10	DIG 9	DIG 8
AXM-D04[2]	Not Used							

	D7	D6	D5	D4	D3	D2	D1	D0
AXM-EDK	AUX 7	AUX 6	AUX 5	AUX 4	AUX 3	AUX 2	AUX 1	AUX 0
AXM-D01	I/O 39	I/O 38	I/O 37	I/O 36	I/O 35	I/O 34	I/O 33	I/O 32
AXM-D02[1]	Not Used							
AXM-D03	DIG 7	DIG 6	DIG 5	DIG 4	DIG 3	DIG 2	DIG 1	DIG 0
AXM-DX03	DIG 7	DIG 6	DIG 5	DIG 4	DIG 3	DIG 2	DIG 1	DIG 0
AXM-D04[2]	Not Used							

1. This register definition also applies to the AXM-D02-JTAG.
2. This register definition also applies to the AXM-D04-JTAG

DIGITAL INPUT/OUTPUT REGISTERS

Channel read/write operations use 8-bit, 16-bit, or 32-bit data transfers with the lower ordered bits corresponding to the lower-numbered channels for the register of interest. All input/output channels are configured as inputs following a power-on or software reset. Data bits 0 through 15 on the AXM-D02(AXM-D02-JTAG) and AXM-D04(AXM-D04-JTAG) modules are not used and will read back the last data value written to them.

Digital Direction Control Register (Read/Write) – (Base Addr + 8010H)

The data direction (input or output) of the digital channels is selected via this register at the carrier base address +8010H. This includes the 32 data channels on the AXM-D01, sixteen CMOS Channels on the AXM-D03/AXM-DX03 and the sixteen auxiliary LVTTL I/O on the AXM-EDK module. The direction of each channel is controlled by its corresponding data bit. The register mapping is the same as the Digital I/O Register. Data bits 0 through 15 on the AXM-D02(AXM-D02-JTAG) and AXM-D04(AXM-D04-JTAG) modules are not used and will read back the last data value written to them.

Independent channel direction control is provided for each digital channel. Setting a bit low configures the corresponding channel data direction for input. Setting the control bit high configures the corresponding channel data direction for output.

The default power-up state of these registers is logic low. Thus, all channels are configured as inputs following system reset or power-up. Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers.

Interrupt Enable Register (Read/Write) – (Base Addr + 8014H)

DIFFERENTIAL INTERRUPT REGISTERS

The Interrupt Enable Register provides a map bit for each differential channel from 8 to 15. A "0" bit will prevent the corresponding input channel from generating an external interrupt. A "1" bit will allow the corresponding channel to generate an interrupt.

The Interrupt Enable register at the base address + offset 8014H is used to control channels 8 through 15 via data bits 0 to 7. Bits 8 to 15 are not used and will always read as "0".

All channel interrupts are disabled (set to "0") following a power-on or software reset. Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers. Additional steps may be required to enable interrupts. Refer to the PMC/XMC base module's User's Manual for further information.

Model	Interrupt Register Mapping							
	D7	D6	D5	D4	D3	D2	D1	D0
AXM-EDK	I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9	I/O 8
AXM-D01	I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9	I/O 8
AXM-D02[1]	Diff 15	Diff 14	Diff 13	Diff 12	Diff 11	Diff 10	Diff 9	Diff 8
AXM-D03	Diff 15	Diff 14	Diff 13	Diff 12	Diff 11	Diff 10	Diff 9	Diff 8
AXM-DX03	Diff 23	Diff 22	Diff 21	Diff 20	Diff 19	Diff 18	Diff 17	Diff 16
AXM-D04[2]	LVDS 15	LVDS 14	LVDS 13	LVDS 12	LVDS 11	LVDS 10	LVDS 9	LVDS 8

1. This register definition also applies to the AXM-D02-JTAG.
2. This register definition also applies to the AXM-D04-JTAG

Interrupt Type (COS or H/L) Configuration Register (Read/Write) - (Base Addr + 8018)

DIFFERENTIAL INTERRUPT REGISTERS

The Interrupt Type Configuration Register determines the type of input channel transition that will generate an interrupt for each of the eight possible interrupting channels. A "0" bit selects interrupt on level. An interrupt will be generated when the input channel level specified by the Interrupt Polarity Register occurs (i.e. Low or High level transition interrupt). A "1" bit means the interrupt will occur when a Change-Of-State (COS) occurs at the corresponding input channel (i.e. any state transition, low to high or high to low).

The Interrupt Type Configuration register at base address +8018H is used to control channels 8 through 15 as mapped in the Interrupt Enable

Register. For example, channel 8 is controlled via data bit-0. Bits 8 to 15 are not used and will always read as "0".

All bits are set to "0" following a reset which means that, if enabled, the inputs will cause interrupts for the levels specified by the Interrupt Polarity Register.

Channel read or write operations use 8-bit, 16-bit, or 32-bit data transfers. Note that no interrupts will occur unless they are enabled by the Interrupt Enable Register.

Interrupt Polarity Register (Read/Write) – (Base Addr + 801C)

The Interrupt Polarity Register determines the level that will cause a channel interrupt to occur for each of the channels enabled for level interrupts. A "0" bit specifies that an interrupt will occur when the corresponding input channel is low (i.e. a "0" in the differential input channel data register). A "1" bit means that an interrupt will occur when the input channel is high (i.e. a "1" in the differential input channel data register). Note that no interrupts will occur unless they are enabled by the Interrupt Enable Register. Further, the Interrupt Polarity Register will have no effect if the Change-of-State (COS) interrupt type is configured by the Interrupt Type Configuration Register.

The Interrupt Polarity register at the base address + offset 801CH is used to control differential channels 8 through 15 as mapped in the Interrupt Enable Register. For example, channel 8 is controlled via data bit-0. Bits 8 to 15 are not used and will always read as "0".

All bits are set to "0" following a reset, which means that the inputs will cause interrupts when they are logic low (provided they are enabled for interrupt on level).

4.0 THEORY OF OPERATION

This section contains information regarding the hardware of the board. A description of the basic functionality of the circuitry used on the board is also provided. Note that each section does not necessarily apply to every model. Refer to table below to determine the appropriate sections.

MODEL	I/O Type	Interrupts	JTAG Support
AXM-D01	64 LVTTL	8 Channels	Optional
AXM-D02[1]	30 Differential	8 Channels	No
AXM-D03	22 Differential & 16 CMOS Digital	8 Channels	No
AXM-DX03	24 Differential & 16 CMOS Digital	8 Channels	No
AXM-D04[2]	30 LVDS	8 Channels	No
AXM-EDK	30 LVTTL	8 Channels	Yes

1. This register definition also applies to the AXM-D02-JTAG.

2. This register definition also applies to the AXM-D04-JTAG

DIFFERENTIAL INPUT/OUTPUT LOGIC

Differential I/O are provided on the AXM-D02, AXM-D03 and AXM-DX03 models through the Field I/O Connector (refer to Table 2.2 to 2.5). *Field I/O points are NON-ISOLATED.* This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops. Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage.

Differential channels to the FPGA are buffered using EIA RS485/RS422 line transceivers. The transceivers are considered failsafe as a open or short circuit on the I/O will not damage the board. Field input lines are not terminated. **External 120 Ohm resistors are recommended on all receivers.** Signals received are converted from the required EIA RS485/RS422 voltages to the LVTTL levels required by the FPGA. Likewise, LVTTL signals are converted to the EIA RS485/RS422 voltages for data output transmission. The direction control of the differential channels is independently controlled.

CMOS DIGITAL INPUT/OUTPUT LOGIC

Digital field I/O are provided on the AXM-D03/AXM-DX03 model through the Field I/O Connector (refer to Table 2.4 and 2.5). *Field I/O points are NON-ISOLATED.* This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops. Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage.

Digital input/output signals to the FPGA are buffered using a dual voltage digital transceiver. Signals received are converted from 5V CMOS to LVTTL as required by the FPGA. Likewise LVTTL signals are converted to 5V CMOS voltages for data output transmission. The direction control of the digital channels is independently controlled.

Each field line has a 10K pullup resistor to +5V. Output operation is considered 'Fail-safe'. That is, the Digital Input/Output signals are always configured as inputs following a power-up or software reset. This is done for safety reasons to ensure reliable control under all conditions.

LVDS INPUT/OUTPUT LOGIC

LVDS I/O on the AXM-D04 are provided through the Field I/O Connector (refer to Table 2.6 and 2.7). *Field I/O points are NON-ISOLATED.* This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops. Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage.

LVDS channels (0-31) to the FPGA are buffered using multidrop LVDS line drivers and receivers. The drivers and receivers are standard LVDS signaling characteristics (TIA/EIA-644) with double the current for multipoint applications. Field inputs to these receivers include a 100 ohm termination resistor. Signals received are converted from the LVDS voltages to the LVTTL levels required by the FPGA. Likewise, LVTTL signals are converted to the TIA/EIA-644 LVDS voltages for data output transmission. The direction control of the LVDS channels is independently controlled.

LVTTL DIRECT INTERFACE

The AXM-EDK has a total of 46 (30 General Purpose and 16 auxiliary) channels of LVTTL. These I/O provide a direct connection through the mezzanine connector to the adjoining FPGA. There are no intermediate buffers on the I/O. As such care must be taken to limit overshoot (to 3.6V) and to prevent ESD, or the FPGA on the PMC/XMC base board may be damaged.

The I/O on the AXM-EDK are mapped to simulate the various types of I/O that can be found on the AXM-D series modules. Therefore the same registers can be used to simulate the Field I/O on the AXM-EDK. The 30 general purpose I/O map to the 30 differential I/O on the AXM-D02(AXM-D02-JTAG), the 22/24 differential I/O on the AXM-D03/AXM-DX03, and 30 LVDS I/O on the AXM-D04(AXM-D04-JTAG). The 16 auxiliary I/O map to the 16 differential signal on the AXM-D03/AXM-DX03. Note that regardless of which AXM-D module is being emulated, the AXM-EDK I/O are all 3.3V LVTTL.

The AXM-D01 module has 64 LVTTL I/O channels (connecting directly to the FPGA - can be other I/O standards). This module is for straight thru I/O (no pull-ups or pull-downs). Custom modules are available for optional pull-ups, pull downs, JTAG, and fused power for front I/O use.

JTAG INTERFACE

The AXM-EDK model has a front field I/O Xilinx JTAG header. It readily connects to any compatible Xilinx programming system such as the MULTIPro Tool® or Parallel Cable programming system. In general, the JTAG interface pins connect only to the Xilinx FPGA. See the PMC base board for further information. The JTAG interface is powered by 3.3V.

INTERRUPT LOGIC

Eight Channels in each model can be configured to generate interrupts for Change-Of-State (COS) and input level (polarity) match conditions. The interrupt is released via a write to the corresponding bit of the Interrupt Status/Clear register. The channels enabled for interrupt in the example design are Differential Channels 8 to 15 on the AXM-D02(AXM-D02-JTAG), AXM-D03 and AXM-DX03, LVDS Channels 8 to 15 on the AXM-D04(AXM-D04-JTAG), LVTTL Channels 8-15 on the AXM-EDK, and LVTTL Channels 8-15 on the AXM-D01.

PMC/XMC BASE BOARD CONNECTION

The AXM-EDK and AXM-D series of extension I/O modules are attached to the PMC/XMC base board via a high speed 150 pin header. The connector provides power to the extension board and multiple logic connections to the base board. Note that any PMC/XMC base board with a re-configurable FPGA will require the pin definitions provided in the EDK to properly operate the AXM-EDK and AXM-D series boards.

5.0 SERVICE AND REPAIR

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

SERVICE AND REPAIR ASSISTANCE

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier/CPU board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

www.acromag.com

Acromag's application engineers can also be contacted directly for technical assistance via telephone or email. Contact information is located at the bottom of this page. When needed, complete repair services are also available.

6.0 SPECIFICATIONS

PHYSICAL

Single AXM Board

Height	11.5 mm (0.453 in)
Stacking Height	8.0 mm (0.315 in)
Depth	31.0 mm (1.220 in)
Width	74.0 mm (2.913 in)
Board Thickness	0.8 mm (0.031 in)

Unit Weight (Including all mounting hardware)

AXM-EDK: 0.43oz (0.01218Kg)
AXM-D01: 1.36oz (0.0386Kg)
AXM-D02/AXM-D02-JTAG: 1.36oz (0.0386Kg)
AXM-D03: 1.39oz (0.0395Kg)
AXM-DX03: 1.39oz (0.0395Kg)
AXM-D04/AXM-D04-JTAG: 1.39oz (0.0394Kg)

Connectors

- **AXM-D Front Field I/O:** 68-pin, SCSI-3, female receptacle male header (AMP 5787394-7 or equivalent)
- **AXM-EDK Front Field I/O:** 14-pin, 2mm double row male header (standard Xilinx JTAG header). 34-pin, 0.1" double row header.

Table 6.1: Power Requirements for Example Design

Power Requirements			
		TYP[2]	**MAX[4]**
3.3V (±5%)[1]	AXM-D01	Not Used[3]	
	AXM-D02	460mA	900mA
	AXM-D03[5]	370mA	700mA
	AXM-DX03	370mA	700mA
	AXM-D04[6]	162mA	330mA
	AXM-EDK	Not Used[3]	
5V (±5%)[1]	AXM-D01	Not Used[3]	
	AXM-D02	Not Used	
	AXM-D03[5]	32mA	80mA
	AXM-DX03	32mA	80mA
	AXM-D04[6]	Not Used	
	AXM-EDK	Not Used[3]	

1. Power source is the base board. Current draw is for AXM module only.
2. With ½ of I/O as inputs, ½ as outputs, and at 25°C.
3. The AXM-EDK and AXM-D01 has no components that draw power. It is simply a pass though board.
4. Floating or shorted I/O will have higher current draw.
5. Power also applies to the AXM-D02-JTAG model
6. Power also applies to the AXM-D04-JTAG model

ENVIRONMENTAL

Operating Temperature: -40°C to +85°C
Relative Humidity: 5-95% Non-Condensing.
Storage Temperature: -55°C to 150°C. (AXM-D01: -40°C to +85°C)
Non-Isolated: Logic and field commons have a direct electrical connection.

Radiated Field Immunity (RFI): Complies with EN61000-4-3 (3V/m, 80 to 1000MHz AM & 900MHz. keyed) and European Norm EN50082-1 with no register upsets.

Conducted R F Immunity (CRFI): Complies with EN61000-4-6 (3V/rms, 150KHz to 80MHz) and European Norm EN50082-1 with no register upsets.

Electromagnetic Interference Immunity (EMI): No register upsets occur under the influence of EMI from switching solenoids, commutator motors, and drill motors.

Surge Immunity: Not required for signal I/O per European Norm EN50082-1.

Electric Fast Transient (EFT) Immunity: Complies with EN61000-4-4 Level 2 (0.5KV at field I/O terminals) and European Norm EN50082-1.

Electrostatic Discharge (ESD) Immunity: Complies with EN61000-4-2 Level 3 (8KV enclosure port air discharge) Level 2 (4KV enclosure port contact discharge) Level 1 (2KV I/O terminals contact discharge) and European Norm EN50082-1.

Radiated Emissions: Meets or exceeds European Norm EN50081-1 for class B equipment. Shielded cable with I/O connections in shielded enclosure are required to meet compliance.

Reliability Prediction

Mean Time Between Failure: MIL-HDBK-217F, Notice 2, at 25°C
AXM-D01: TBD Hours
AXM-D02/AXM-D02-JTAG: 3,559,276 Hours
AXM-D03: 3,921,522 Hours
AXM-DX03: TBD Hours
AXM-D04/AXM-D04-JTAG: 6,534,197 Hours
AXM-EDK: N/A No active components..

DIFFERENTIAL I/O

Channel Configuration: 30 (AXM-D02/AXM-D02-JTAG) or 22 (AXM-D04/AXM-D04-JTAG) Bi-directional EIA 485/422 differential signals are independently direction controlled.

EIA 485/422 Differential I/O Electrical Characteristics

- 1.5 V Min., 3.3V Max.: Differential Driver Output Voltage with 54Ω load
- 3 V Max.: Common Mode Output Voltage.

- -0.2 Min to -0.05 Max: Differential Input Threshold Voltage $-7V \le V_{CM} \le 12V$
- 15mV Typical: Input Hysteresis
- 96KΩ Minimum Input Resistance

The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating) or shorted.

Differential Propagation Delay

- Driver Input to Output Delay = 27ns Typical, 40ns Maximum
- Receiver Input to Output Delay = 33ns Typical, 60ns Maximum

Termination Resistors

Termination Resistors: Termination resistor are not provided. External 120 Ohm termination resistors for EIA RS485/422 differential receivers are recommended.

DIGITAL I/O

CMOS Channel Configuration: 16 Channels (AXM-D02/AXM-D02-JTAG) of Bi-directional CMOS Transceivers Direction controlled as pairs of channels.

Reset/Power Up Condition: All Digital Channels Default to Input.

CMOS Digital I/O DC Electrical Characteristics

- Digital I/O DC Electrical Characteristics
- $V_{OH:}$ 3.8V minimum
- V_{OL}: 0.55V maximum
- I_{OH}: -32.0mA
- I_{OL}: 32.0mA
- V_{IH}: 3.5V minimum
- V_{IL}: 1.5V maximum

Digital Propagation Delay

- Driver/Receiver Input to Output Delay = 4ns Typical

Pull-up Resistors: 10K pull-up resistors to +5V are installed on each CMOS I/O line.

LVDS I/O

Channel Configuration: 30 Channels (AXM-D04/AXM-D04-JTAG) Bi-directional LVDS signals are independently direction controlled.

LVDS I/O Electrical Characteristics

- 247m V Min., 454mV Max.: LVDS Driver Output Voltage with 50Ω load.
- 1.37 V Max.: Common Mode Output Voltage.
- -50 mV Min to +50mV Max: LVDS Input Threshold Voltage
- Interface with either standard LVDS TIA/EIA-644 or M-LVDS TIA/EIA-899 for Multipoint Data Interchange

LVDS Propagation Delay

- Driver Propagation Delay Time = 2.7ns Maximum
- Driver Output Signal Transition Time = 1.0ns Maximum
- Receiver Propagation Delay Time = 4.5ns Maximum
- Receiver Output Signal Transition Time = 1.5ns Maximum

Maximum Data Rate

Maximum Data Rate 150MHz (4 Meters shielded cable at 25°C)

Termination Resistors

Termination Resistors: Non-removable 100Ω termination resistors are in place for each of the differential channels.

LVTTL I/O

Channel Configuration: 46 Channels (AXM-EDK) and 64 Channels (AXM-D01) Bi-directional LVTTL signals are independently direction controlled.

Reset/Power Up Condition: All Digital Channels Default to Input.

LVTTL I/O Characteristics: Due to the direct connections from the Field I/O to the FPGA, all I/O characteristics for LVTTL are determined by the FPGA. Refer to the FPGA documentation for 3.3V signaling for further information.

APPENDIX

CABLE: MODEL 5028-432 (SCSI-3 to Round, Shielded)

Type: Round shielded cable, 34 twisted pairs (SCSI-3 male connector at both ends). The cable length is 2 meters (6.56 feet). This shielded cable is recommended for all I/O applications (both digital I/O and precision analog I/O).

Application: Used to connect Model 5025-288 termination panel to the board.

Length: Standard length is 2 meters (6.56 feet). Consult factory for other lengths. It is recommended that this length be kept to a minimum to reduce noise and power loss.

Cable: 68 conductors, 28 AWG on 0.050 inch centers (permits mass termination for IDC connectors), foil/braided shield inside a PVC jacket.

Connectors: SCSI-3, 68-pin male connector with backshell.

Keying: The SCSI-3 connector has a "D Shell".

Schematic and Physical Attributes: See Drawing 4501-919.

Electrical Specifications: 30 VAC per UL and CSA (SCSI-3 connector spec.'s). 1 Amp maximum at 50% energized (SCSI-3 connector spec.'s).

Operating Temperature: -30°C to +80°C.

Storage Temperature: -40°C to +85°C.

Shipping Weight: 1.0 pound (0.5Kg), packed.

TERMINATION PANEL: MODEL 5025-288

Type: Termination Panel For 68 Pin SCSI-3 Cable Connection

Application: To connect field I/O signals to the board. *Termination Panel:* Acromag Part 4001-066. The 5025-288 termination panel facilitates the connection of up to 68 field I/O signals and connects to the board (connectors only) via a round shielded cable (Model 5028-432). Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-68) correspond to field I/O (pins 1-68) on the board. Each board has its own unique pin assignments. Refer to the board manual for correct wiring connections to the termination panel.

Schematic and Physical Attributes: See Drawing 4501-920.

Field Wiring: 68-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.

Mounting: Termination panel is snapped on the DIN mounting rail.

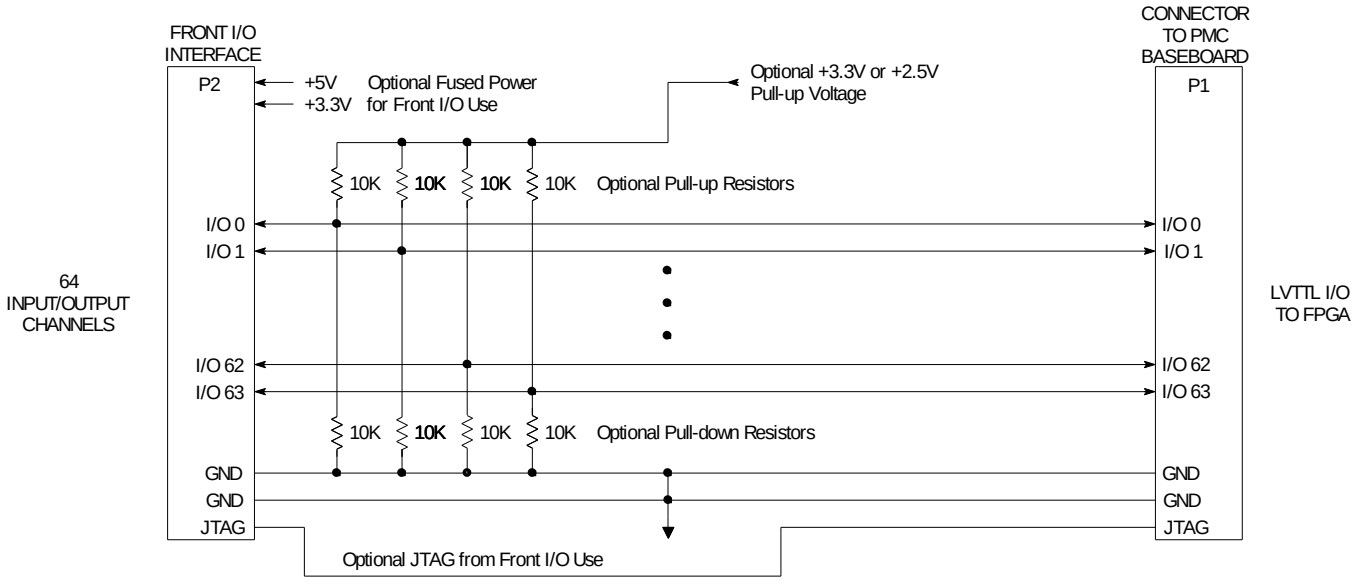
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.

Operating Temperature: -40°C to +100°C.

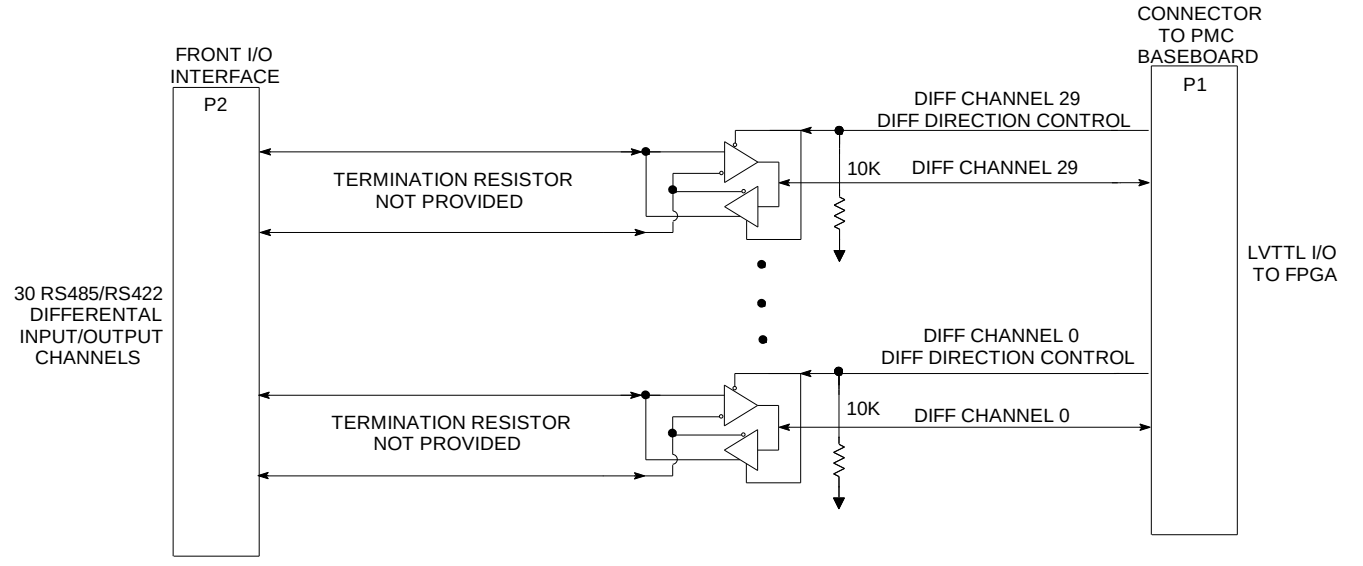
Storage Temperature: -40°C to +100°C.

Shipping Weight: 1.0 pounds (0.5kg) packaged.

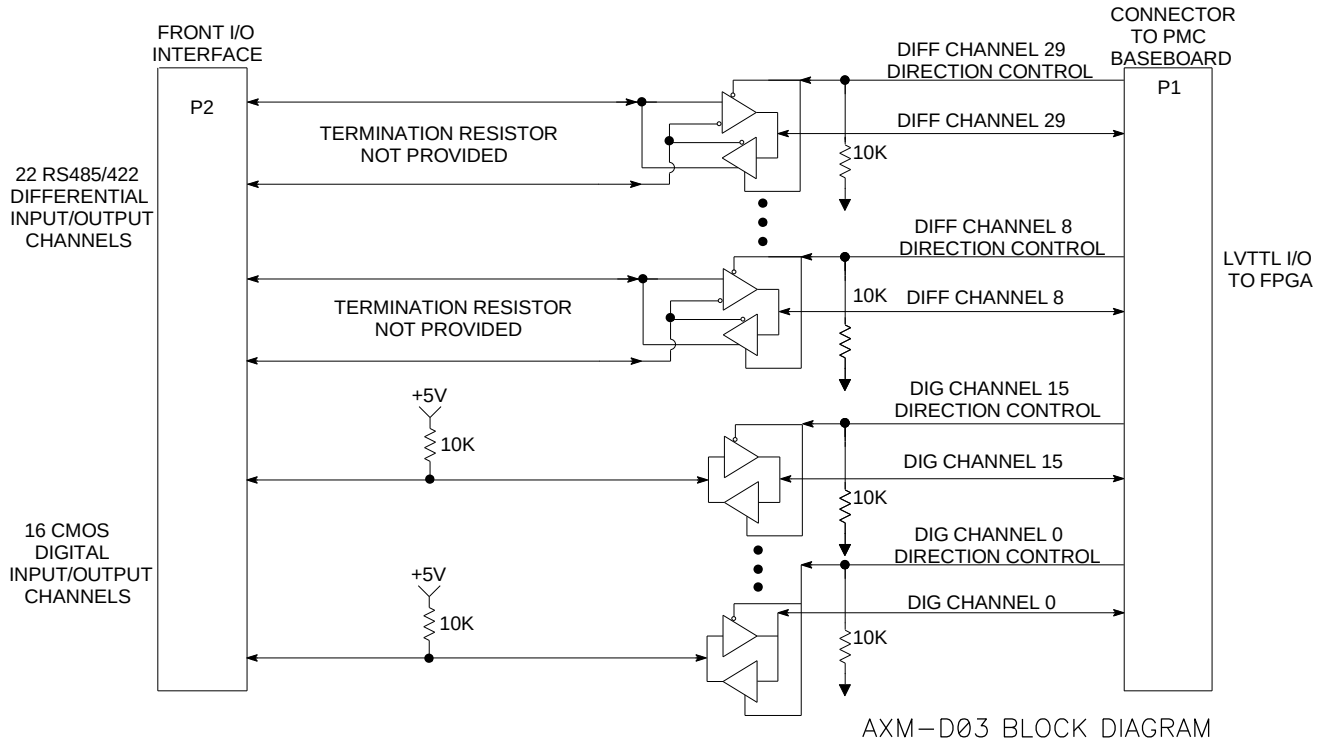
DRAWINGS



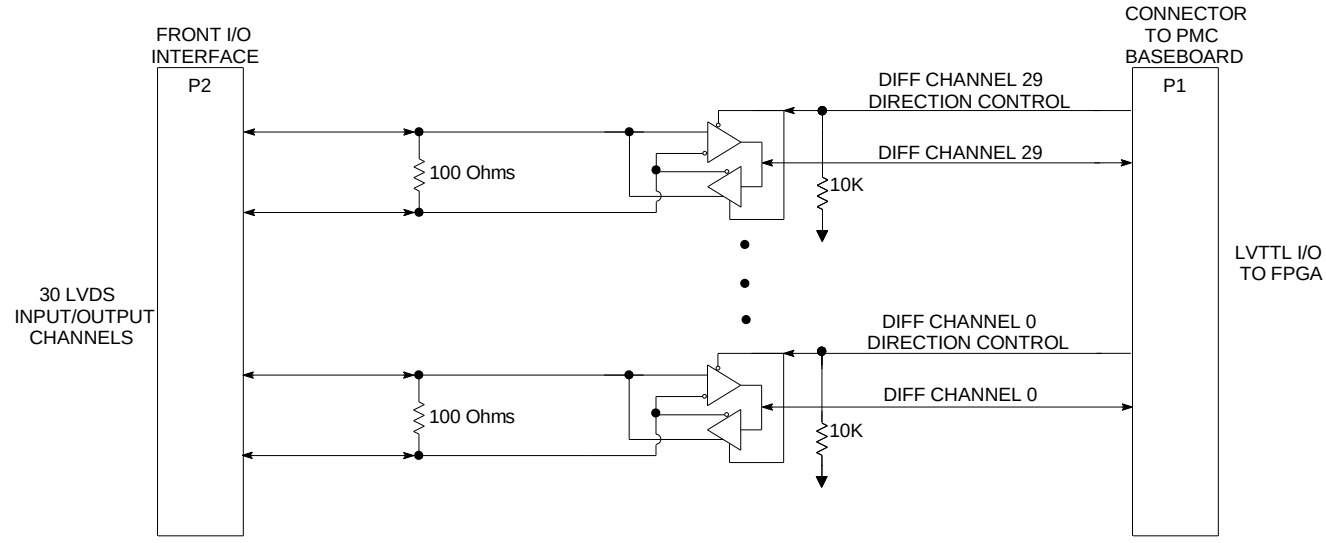
AXM-D01 BLOCK DIAGRAM
4502-156A



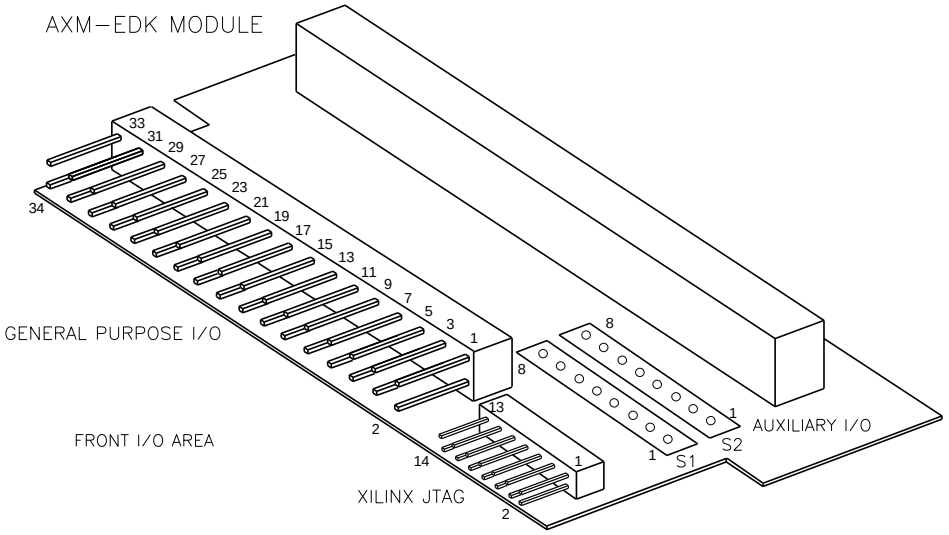
AXM-D02 BLOCK DIAGRAM
4502-051A, P1



AXM-D03 BLOCK DIAGRAM
4502-051A, P2



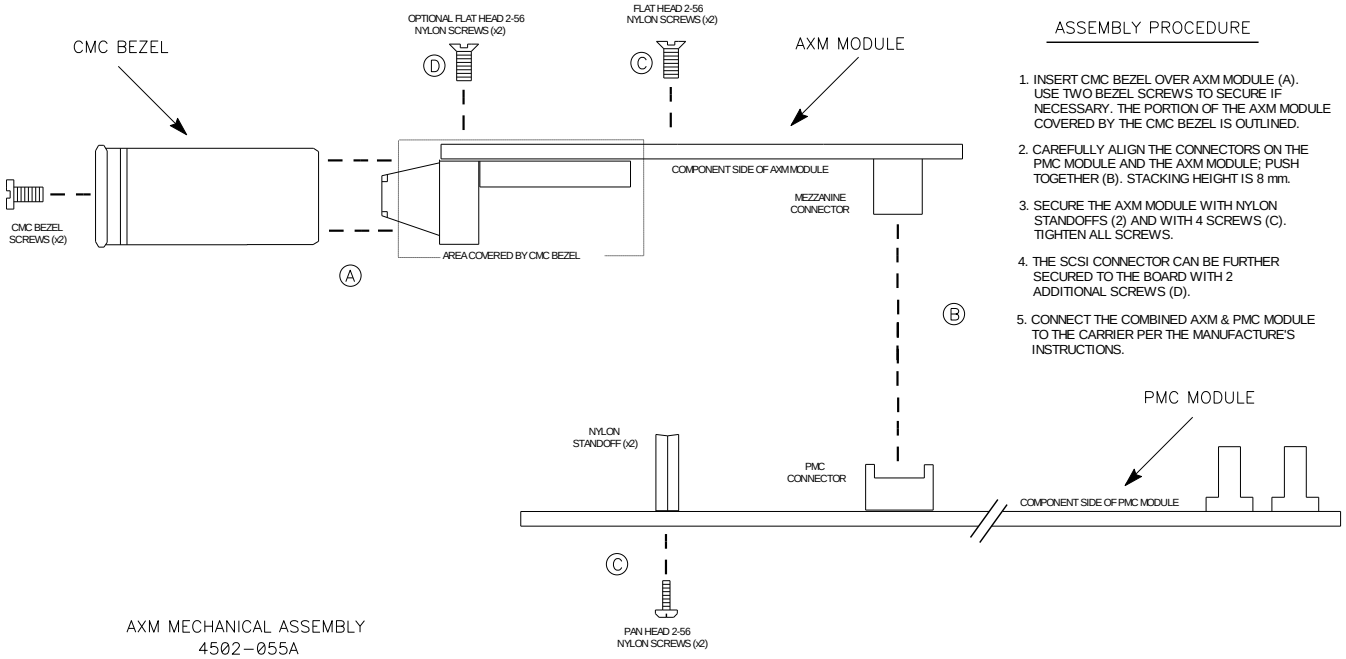
AXM-D04 BLOCK DIAGRAM
4502-051A, P3



JTAG PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION
1	GND	2	+3.3V
3	GND	4	TMS
5	GND	6	TCK
7	GND	8	TDO
9	GND	10	TDI
11	GND	12	NC
13	GND	14	NC

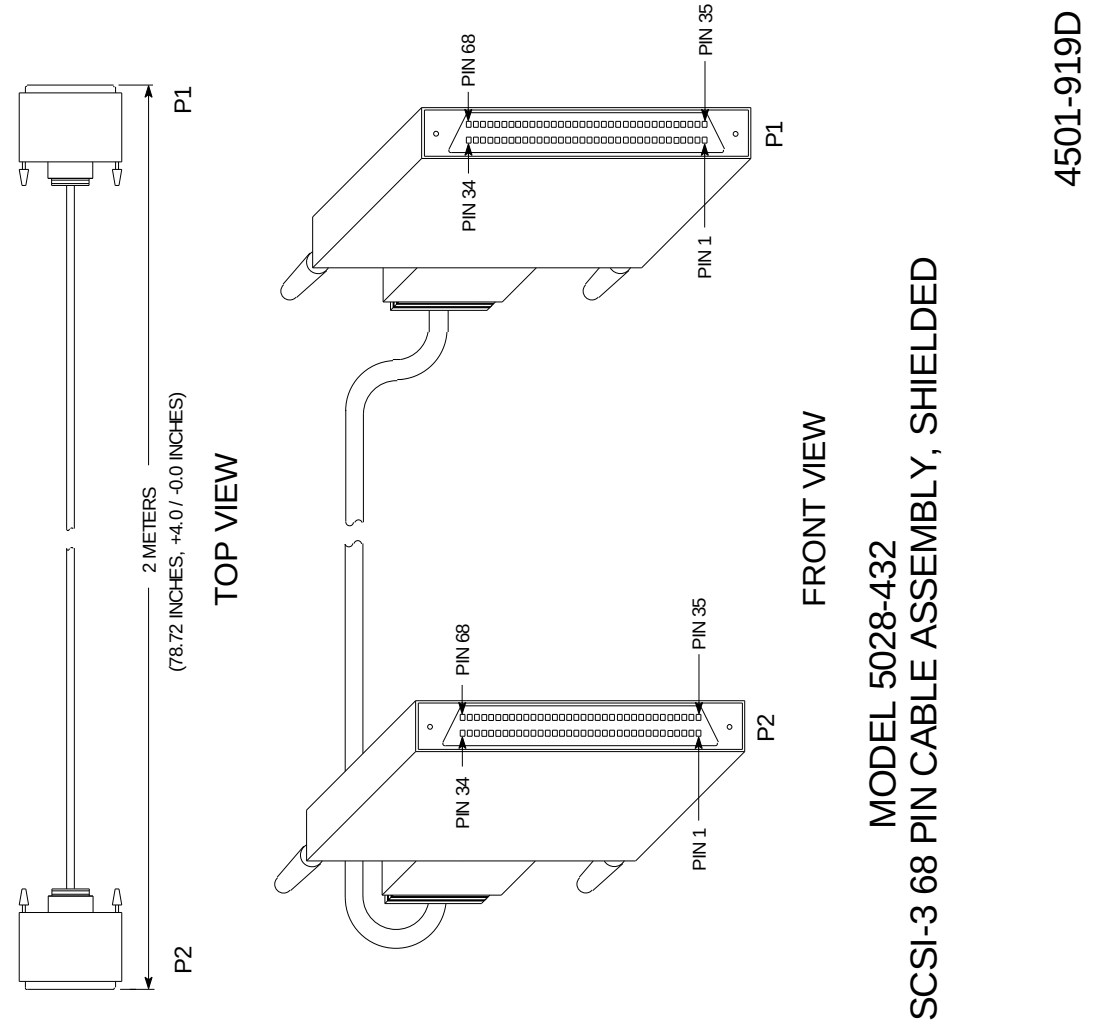
AXM–EDK I/O LOCATION DRAWING
4502–056A

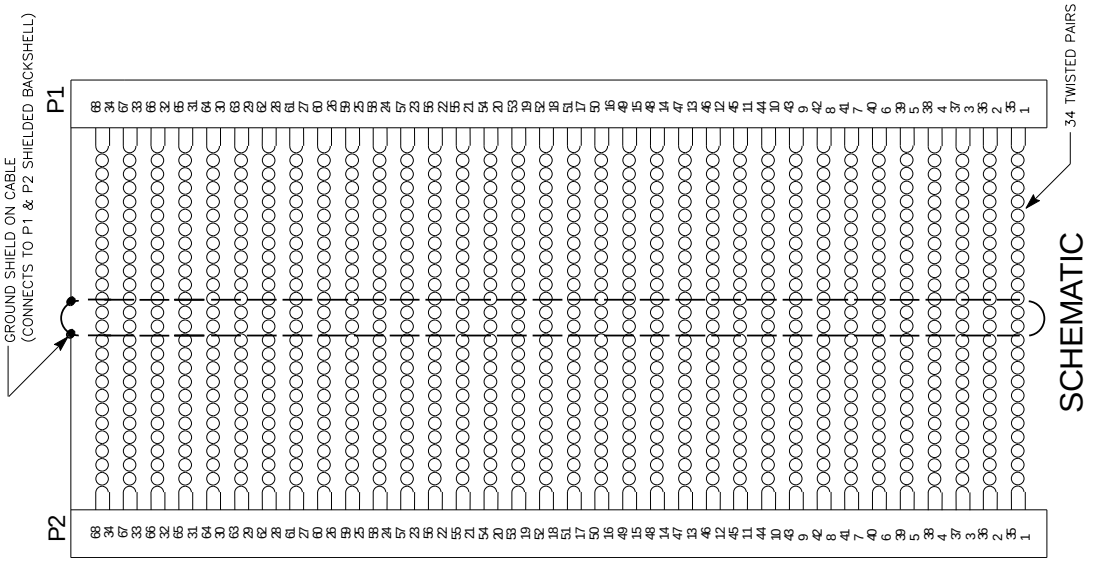


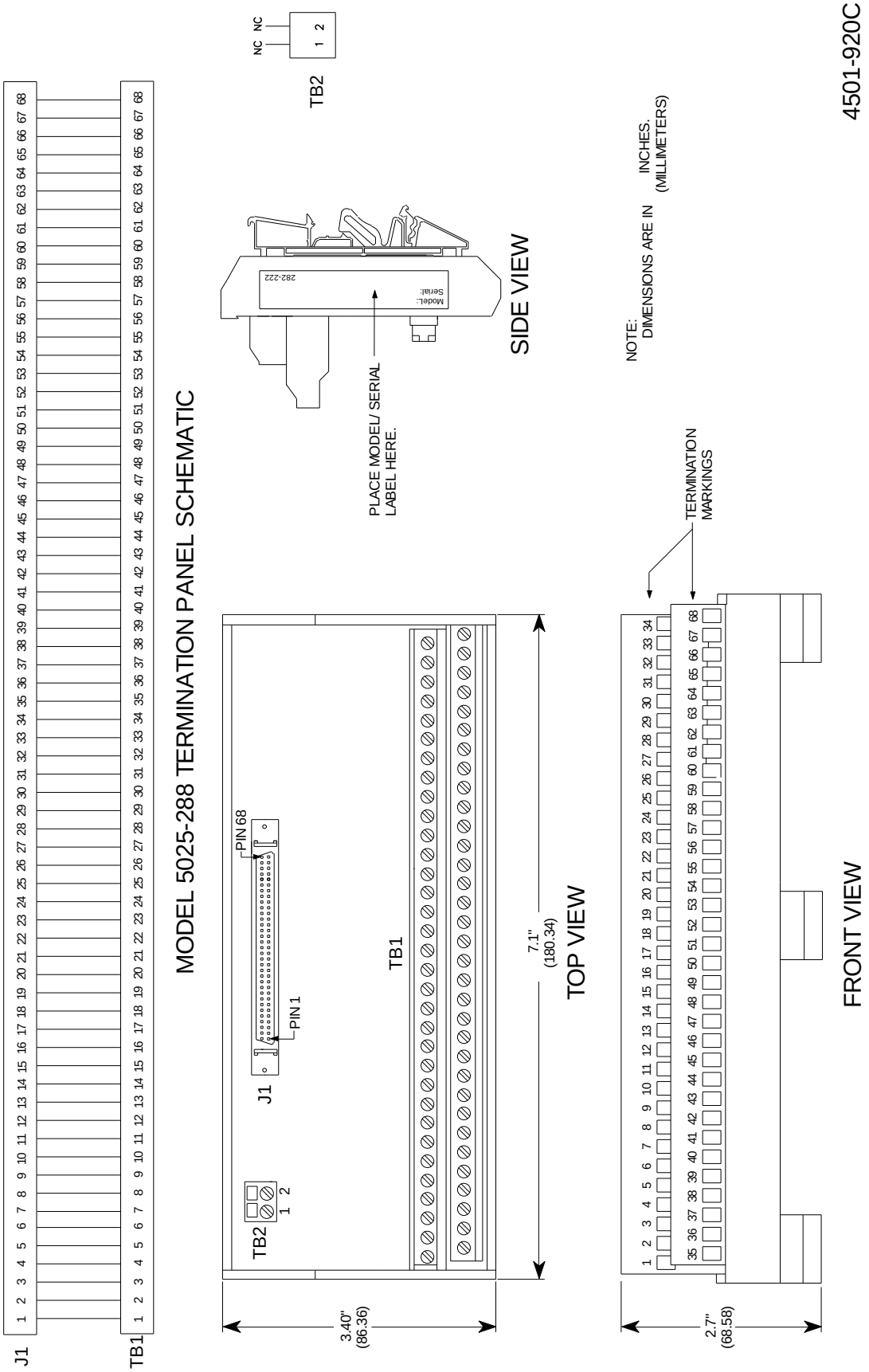
ASSEMBLY PROCEDURE

1. INSERT CMC BEZEL OVER AXM MODULE (A). USE TWO BEZEL SCREWS TO SECURE IF NECESSARY. THE PORTION OF THE AXM MODULE COVERED BY THE CMC BEZEL IS OUTLINED.
2. CAREFULLY ALIGN THE CONNECTORS ON THE PMC MODULE AND THE AXM MODULE; PUSH TOGETHER (B). STACKING HEIGHT IS 8 mm.
3. SECURE THE AXM MODULE WITH NYLON STANDOFFS (2) AND WITH 4 SCREWS (C). TIGHTEN ALL SCREWS.
4. THE SCSI CONNECTOR CAN BE FURTHER SECURED TO THE BOARD WITH 2 ADDITIONAL SCREWS (D).
5. CONNECT THE COMBINED AXM & PMC MODULE TO THE CARRIER PER THE MANUFACTURE'S INSTRUCTIONS.

AXM MECHANICAL ASSEMBLY
4502–055A


4501-919D
MODEL 5028-432
SCSI-3 68 PIN CABLE ASSEMBLY, SHIELDED
TOP VIEW
FRONT VIEW
P1
P2
2 METERS
(78.72 INCHES, +4.0 / -0.0 INCHES)
PIN 68
PIN 35
PIN 34
PIN 1


SCHEMATIC
P1
P2
GROUND SHIELD ON CABLE
(CONNECTS TO P1 & P2 SHIELDED BACKSHELL)
34 TWISTED PAIRS


MODEL 5025-288 TERMINATION PANEL SCHEMATIC
J1
TB1
TB2
NC NC
1 2
SIDE VIEW
PLACE MODEL/ SERIAL LABEL HERE.
Model:
Serial:
282-222
NOTE:
DIMENSIONS ARE IN INCHES.
(MILLIMETERS)
4501-920C
TOP VIEW
PIN 68
PIN 1
J1
TB1
TB2
1 2
7.1"
(180.34)
3.40"
(86.36)
TERMINATION MARKINGS
FRONT VIEW
2.7"
(68.58)

REVISION HISTORY

Release Date	Version	EGR/DOC	Description of Revision
28-JAN-14	H	LMP	Added tables and registers information corresponding to the AXM-D02-JTAG and AXM-D04-JTAG models.