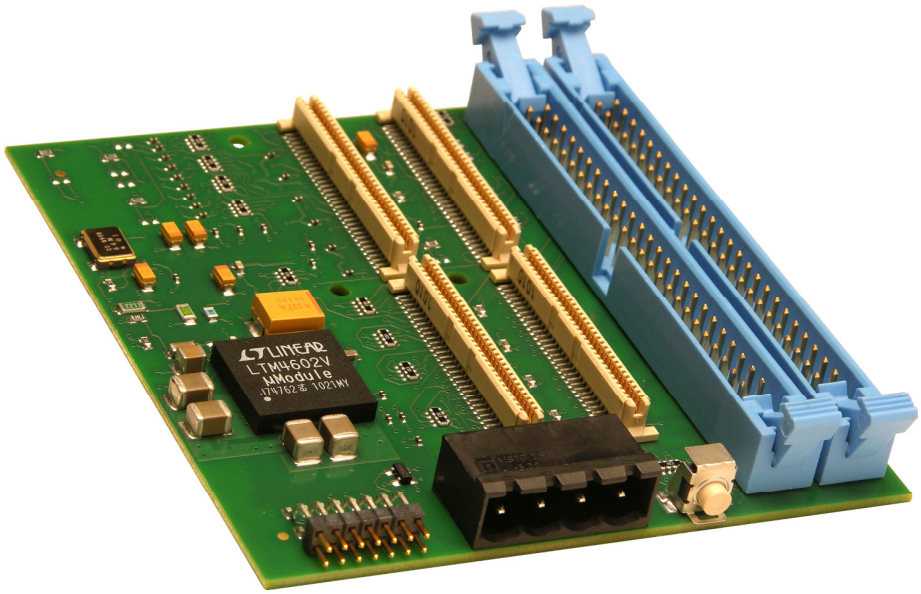
APMC4110 POWERED PMC CARRIER
STANDALONE PCI INTERFACE MODULE

USER'S MANUAL



ACROMAG INCORPORATED
30765 South Wixom Road
P.O. BOX 437
Wixom, MI 48393-7037 U.S.A.

Tel: (248) 295-0310
Fax: (248) 624-9234

8500-899-A10L000

TABLE OF CONTENTS

IMPORTANT SAFETY CONSIDERATIONS
You must consider the possible negative effects of power, wiring, component, sensor, or software failure in the design of any type of control or monitoring system. This is very important where property loss or human life is involved. It is important that you perform satisfactory overall system design and it is agreed between you and Acromag, that this is your responsibility.

1.0 General Information

The Acromag APMC4110 Powered PMC Carrier is a board that functions as a stand-alone PCI interface. Using an external power supply, the carrier allows any industry standard PMC module to be mounted without an accompany processor. The user has full access to the field I/O via two 50-pin ribbon cable connectors, P1 and P2. A 14-pin Xilinx JTAG connector is also available for utilizing boundary scan debugging. A manual reset button allows the user to force a RST# signal when needed. An on-board DC-DC converter creates +3.3VDC from the external +5VDC source, lowering the number of external power connections required.

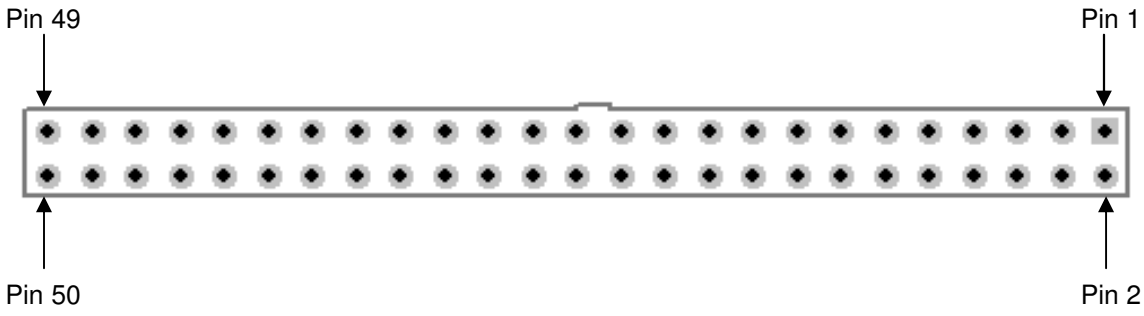
1.1 FIELD I/O CONNECTORS

The PMC module's connections are made to the Acromag APMC4110 carrier field I/O connections through the P1 and P2 50-pin connectors. The connections are terminated as defined within the PCI specification. The reset and clock signals are sourced from the APMC4110. In addition, power is provided to the PMC module through the APMC4110 Carrier board.

The field I/O connections are made via two 50 pin ribbon cable connectors. Table 1.1 indicates the pin assignments for the field I/O signal mapping of the Powered PMC Carrier board for connector P1. Table 1.2 indicates the pin assignments for the field I/O signal mapping of the Powered PMC Carrier board for connector P2. The field I/O signals are split equally between the two connectors.

The diagram below shows how the pins on the I/O pins in the tables correspond to the P1 and P2 connectors on the Powered PMC Carrier module.

Note: Notice the notch on the top side of the connector. Pin 1 is indicated with a square pad. The odd pins are in order on the top row from right to left, as shown. The even pins are in order on the bottom row from right to left.



Connector P1			
Pin Description	**Pin**	**Pin Description**	**Pin**
Differential Ch0+ (1)	1	Differential Ch0- (2)	2
COMMON	3	COMMON	4
Differential Ch1+ (3)	5	Differential Ch1- (4)	6
Differential Ch2+ (5)	7	Differential Ch2- (6)	8
COMMON	9	COMMON	10
Differential Ch3+ (7)	11	Differential Ch3- (8)	12
COMMON	13	COMMON	14
Differential Ch4+ (9)	15	Differential Ch4- (10)	16
Differential Ch5+ (11)	17	Differential Ch5- (12)	18
COMMON	19	COMMON	20
Differential Ch6+ (13)	21	Differential Ch6- (14)	22
COMMON	23	COMMON	24
Differential Ch7+ (15)	25	Differential Ch7- (16)	26
Differential Ch16+ (33)	27	Differential Ch16- (34)	28
COMMON	29	COMMON	30
Differential Ch17+ (35)	31	Differential Ch17- (36)	32
COMMON	33	COMMON	34
Differential Ch18+ (37)	35	Differential Ch18- (38)	36
Differential Ch19+ (39)	37	Differential Ch19- (40)	38
COMMON	39	COMMON	40
Differential Ch20+ (41)	41	Differential Ch20- (42)	42
Differential Ch21+ (43)	43	Differential Ch21- (44)	44
COMMON	45	COMMON	46
Differential Ch22+ (45)	47	Differential Ch22- (46)	48
Differential Ch23+ (47)	49	Differential Ch23- (48)	50

Table 1.1: Powered PMC Carrier Board Field I/O Pin Connections for P1

Note that the number in parenthesis corresponds to rear I/O PMC P4 pin number.

Connector P2			
Pin Description	**Pin**	**Pin Description**	**Pin**
Differential Ch8+ (17)	1	Differential Ch8- (18)	2
COMMON	3	COMMON	4
Differential Ch9+ (19)	5	Differential Ch9- (20)	6
Differential Ch10+ (21)	7	Differential Ch10- (22)	8
COMMON	9	COMMON	10
Differential Ch11+ (23)	11	Differential Ch11- (24)	12
COMMON	13	COMMON	14
Differential Ch12+ (25)	15	Differential Ch12- (26)	16
Differential Ch13+ (27)	17	Differential Ch13- (28)	18
COMMON	19	COMMON	20
Differential Ch14+ (29)	21	Differential Ch14- (30)	22
COMMON	23	COMMON	24
Differential Ch15+ (31)	25	Differential Ch15- (32)	26
Differential Ch24+ (49)	27	Differential Ch24- (50)	28
COMMON	29	COMMON	30
Differential Ch25+ (51)	31	Differential Ch25- (52)	32
COMMON	33	COMMON	34
Differential Ch26+ (53)	35	Differential Ch26- (54)	36
Differential Ch27+ (55)	37	Differential Ch27- (56)	38
COMMON	39	COMMON	40
Differential Ch28+ (57)	41	Differential Ch28- (58)	42
Differential Ch29+ (59)	43	Differential Ch29- (60)	44
COMMON	45	COMMON	46
Differential Ch30+ (61)	47	Differential Ch30- (62)	48
Differential Ch31+ (63)	49	Differential Ch31- (64)	50

Table 1.2: Powered PMC Carrier Board Field I/O Pin Connections for P2

Note that the number in parenthesis corresponds to rear I/O PMC P4 pin number.

1.2 POWER

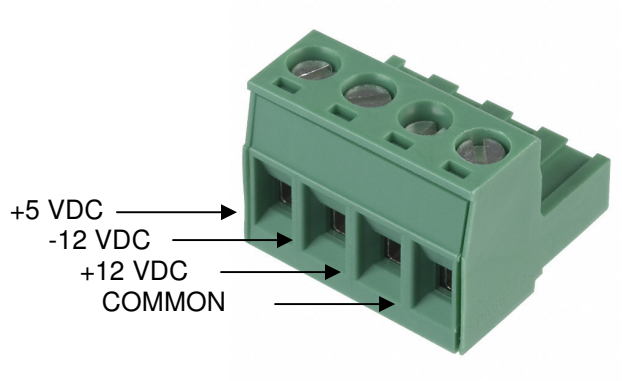
The APMC4110 module features a 4-pin power connection. An external power supply is used to provide the proper voltage and current to the board. Use the table and figure below to make the appropriate connections. An external +3.3VDC connection is not needed; this voltage is generated on-board via a high-current DC-DC converter.

CAUTION: Ensure your power connections are correct BEFORE turning on your power supply. Incorrect power connections may cause hazardous conditions and damage the board.

Pin	Voltage	Current
1	COMMON	N/A
2	+12 VDC ±10%	0.5A Max
3	-12 VDC ±10%	0.5A Max
4	+5 VDC ±5%	6.0A Max

Table 1.3: APMC4110 Power Connections

The 4-pin male connector shown below mates with the 4-pin female header P3 on the board.



1.3 MANUAL RESET

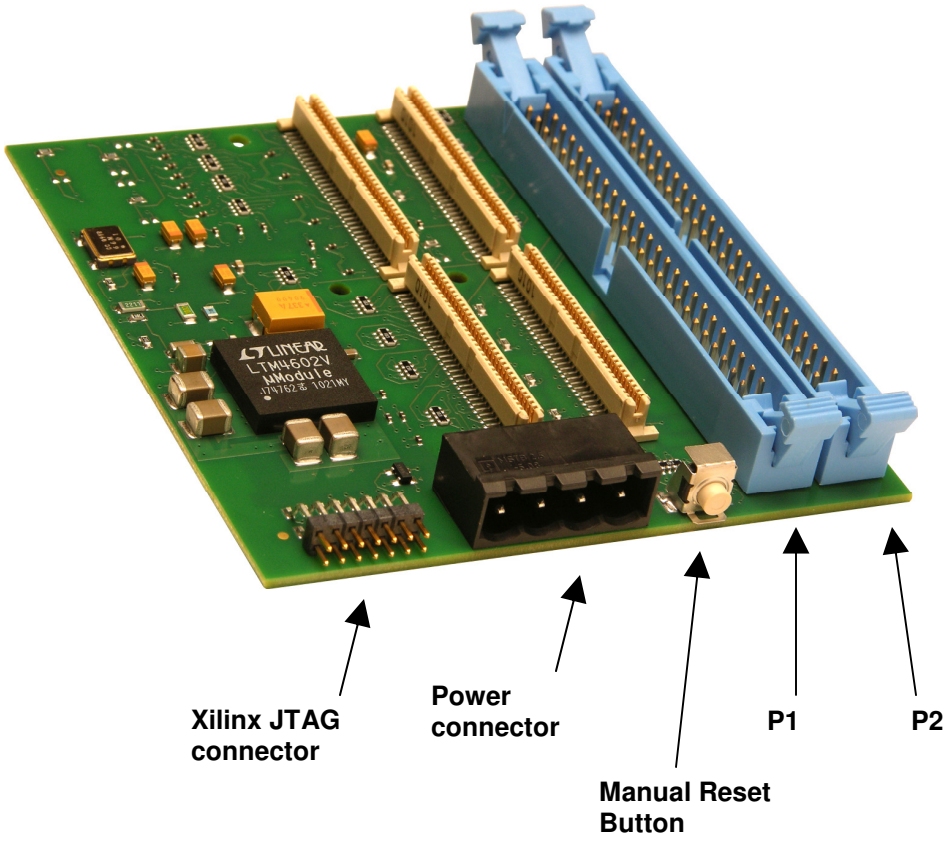
The APMC4110 module features a manual reset button. This is a SPST switch which can be pressed to assert the active-low RST# signal and reset the PMC module. A reset delay chip is used on the board to keep RST# asserted for a minimum of 140ms after the +5VDC rail has risen above 1V. This is designed to prevent code execution errors during power-up, power-down, or potential brown-out conditions when +5VDC dips too low.

1.4 XILINX JTAG PORT

A standard 14-pin Xilinx JTAG connection is available for utilizing the TDI, TDO, TCK, and TMS signals routed through the PMC connectors. The pin out for this connector (P4) is shown in the table below.

Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	COMMON	5	COMMON	9	COMMON	13	COMMON
2	+3.3VDC	6	TCK	10	TDI	14	N.C.
3	COMMON	7	COMMON	11	COMMON		
4	TMS	8	TDO	12	N.C.		

Figure 1.1: APMC4110 Feature Location



2.0 PREPARATION FOR USE

2.1 UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

2.2 INSTALLATION CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

IMPORTANT: *Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.*

Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

2.3 NON-ISOLATION CONSIDERATIONS

The board is non-isolated, since there is electrical continuity between the PCI interface and PMC module grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

3.0 SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at an elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

3.1 PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier/CPU board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique to isolate a faulty board. Use the unmodified example we provide.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

3.2 WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

Acromag's application engineers can also be contacted directly for technical assistance via telephone or FAX through the numbers listed below. When needed, complete repair services are also available.

Phone: 248-295-0310
Fax: 248-624-9234
Email: solutions@acromag.com

4.0 SPECIFICATIONS

4.1 PHYSICAL

Physical Configuration

Height	3.300 inches (83.820 mm)
Depth	3.520 inches (89.408 mm)
Board Thickness	0.063 inches (1.600 mm)
Unit Weight	0.117 lbs (0.053 kg)

Connectors

P1, P2 (Field I/O)	50-pin, ribbon cable, male receptacle headers
P3	4-pin power header
P4	14-pin Xilinx JTAG port

4.2 ENVIRONMENTAL

Operating Temperature: -40°C to 85°C
Relative Humidity: 5-95% Non-Condensing
Storage Temperature: -55°C to 120°C

PCI Bus Clock: On-board 66Mhz crystal oscillator.

PMC Compatibility: Pin assignment conforms to PCI Bus Specification Revision 3.0.

Non-Isolated: PCI interface and field commons have a direct electrical connection.

4.3 POWER REQUIREMENTS

5.0 VDC (±5%)	66 mA
12.0 VDC (±10%)	0 mA
-12.0 VDC(±10%)	0 mA

Note that these power requirements are for the APMC4110 only. The +3.3V is generated on the APMC4110 from 5V via a DC/DC converter.

±12.0 VDC is routed directly to the PMC module and must be provided only if required by the PMC module.

Certificate of Volatility				
Acromag Model: APMC4110	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) □ Yes ■ No				
Type (SRAM, SDRAM, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Type (SRAM, SDRAM, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Type (SRAM, SDRAM, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) □ Yes ■ No				
Type(EEPROM, Flash, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Type(EEPROM, Flash, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize: