Series APCe8650 Industrial I/O Pack

PCI Bus Non-Intelligent Carrier Board

USER'S MANUAL

ACROMAG INCORPORATED
30765 South Wixom Road
P.O. BOX 437
Wixom, MI 48393-7037 U.S.A.
Tel: (248) 295-0310
Fax: (248) 624-9234

8500-912 D

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1. GENERAL INFORMATION

The APCe8650 card is a Peripheral Component Interconnect Express (PCIe) bus card and is a carrier for the Industrial I/O Pack (IP) mezzanine board field I/O modules. The carrier board provides a modular approach to system assembly, since each carrier can be populated with any combination of analog input/output, digital input/output, communication, etc. IP modules. Thus, the user can create a board which is customized to the application. This saves money and space - a single carrier board populated with IP modules may replace several dedicated function PCI or PCIe bus boards. The APCe8650 non-intelligent carrier board provides impressive functionality at low cost.

Model	Board Size (Length)	Supported IP Slots	Operating Temperature Range
APCe8650	Long (12.283”)	4(A,B,C,D)	0 to +70°C
APCe8650E	Long (12.283”)	4(A,B,C,D)	-40 to +85°C

KEY APCe8650 FEATURES

PCI Express Version 1.1 Compliant Slave Carrier: - Provides a PCIe bus interface to control and communicate with industry standard IP modules.

Interface for IP Modules – The APCe8650 provides an electrical and mechanical interface for up to four industry standard IP modules. IP Modules are available from Acromag and other vendors in a wide variety of input/output configurations to meet the needs of varied applications.

Plug-And-Play PCIe bus Carrier - The carrier card contains standard PCI bus configuration memory. Upon power-up the system auto-configuration process assigns the carrier’s base address in memory space.

Plug-And-Play Interrupt Support - The personal computer system software will allocate one interrupt line to the carrier. The carrier’s interrupt pending register can be used to quickly identify IP module pending interrupts.

Supports Two Interrupt Channels per IP - Up to two interrupt requests are supported for each IP. Additional registers are associated with each interrupt request for control and status monitoring.

Full IP Register Access - Makes maximum use of logically organized programmable registers on the carrier boards to provide for easy configuration and control of IP modules. Supports accesses to IP input/output, interrupt, ID ROM, and Memory data spaces.

IP Module Access Time Out - Allows access to empty IP slots without system failure. If the IP module accessed does not respond within 32u seconds the bus access is terminated without system failure. This allows each IP slot to be probed to determine if an IP is installed. A control register bit will be set and/or issue of an interrupt request to indicate IP module time out access has occurred.

IP Module Selectable Clock - Allows for each IP module to be individually configured to an 8MHz or 32MHz clock.

Optional Screw Termination Panel - Model supports field connection via screw terminals using the optional DIN rail mount termination panels.

Connectors Access I/O - Access to field I/O signals is provided via 3M Low Profile 50-pin headers with cable ejector latches. A separate header is provided for each IP module.

Supervisory Circuit for Reset Generation - A microprocessor supervisor circuit provides power-on, power-off, and low power detection reset signals to the IP modules per the IP specification.

Individually Filtered Power - Filtered +5V, +12V, and -12V DC power is provided to the IP modules via passive filters present on each supply line serving each IP. This provides optimum filtering and isolation between the IP modules and the carrier board and allows analog signals to be accurately measured or reproduced on IP modules without signal degradation from the carrier board logic signals.

Individually Fused Power - Fused +5V, +12V, and -12V DC power is provided. A fuse is present on each supply line serving each IP module.

PCI Express BUS INTERFACE FEATURES

Slave Module- All read and write accesses are implemented as either a 32-bit, 16-bit or 8-bit single data transfer.

Interrupt Support - PCI bus INTA# interrupt request is supported. All IP module interrupts are mapped to INTA#. Carrier board software programmable registers are utilized as interrupt request control and status monitors. One MSI interrupt is also supported.

SIGNAL INTERFACE PRODUCTS

This IP carrier board will mate directly to all industry standard IP modules. Acromag provides the following interface products (all connections to field signals are made through the carrier board which passes them to the individual IP modules):

Cables

Model 5025-551-X (Shielded Cable) or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting carrier boards, to Model 5025-552 termination panels. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications. The cables are available in 4, 7, or 10 feet lengths. Custom lengths (12 feet maximum) are available upon request.

Termination Panel:

Model 5025-552: DIN-rail mountable panel provides 50 screw terminals for universal field I/O termination. Connects to carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

SUPPORTED OPERATING SYSTEMS

IP MODULE Windows Software

Acromag provides a software product (sold separately) to facilitate the development of Windows (2000/XP/Vista/7®) applications accessing Acromag Industry Pack models installed on Acromag PCI Carrier Cards and CompactPCI Carrier Cards. This software (Model IPSW-API-WIN) consists of low-level drivers and Windows 32 Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments including Visual C++™, Visual Basic .NET® and others. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

IP MODULE VxWORKS SOFTWARE

Acromag provides a software product (sold separately) consisting of board VxWorks® software. This software (Model IPSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all Acromag IP modules and Carriers, PCI I/O Cards, and CompactPCI I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag PCI boards.

IP MODULE LINUX SOFTWARE

Acromag provides a software product (available on website) consisting of board Linux® software. This software (Model IPSW-API-LINUX) is composed of Linux® libraries for all Acromag IP modules and carriers including the APCe8650. The software supports X86 PCI bus only and is implemented as library of "C" functions. These functions link with existing user code to make possible simple control of all Acromag IP CompactPCI BUS INTERFACE FEATURES

2. PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping

cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The lack of air circulation within the computer chassis is a cause for some concern. Most, if not all, computer chassis do not provide a fan for cooling of add-in boards. The dense packing of the IP modules to the carrier board alone results in elevated IP module and carrier board temperatures, and the restricted air flow within the chassis aggravates this problem. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

Board Configuration

The carrier board is plug-and-play compatible and, as such, its board addresses are automatically assigned by the system auto-configuration routine upon power-up. The base address of the carrier board's configuration registers in memory space and I/O space is assigned. In addition, the base addresses of the IP modules and carrier board registers are assigned in 32-bit memory space.

Power should be removed from the board when changing jumper configurations or when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4502-148 and your IP module documentation for specific configuration and assembly instructions.

See diagram 4502-135 located in the drawings portion of this manual for jumper location and settings. The jumper must be present in one of the two configurations for proper board operation. Factory default is memory space disabled.

Interrupt Configuration

No hardware jumper configuration is required for interrupts. Interrupt enables and status flags are configured or viewed via programmable registers on the carrier board (see Section 3 for programming details). The carrier board passes interrupt requests from the IP modules to the PCIe bus. Refer to the IP modules for their specific configuration requirements.

CONNECTORS

Connectors of the APCe8650 carrier consist of four carrier IP module field I/O connectors, four IP module logic connectors, four field I/O ribbon cable connectors, a peripheral power connector, a PCIe graphics power connector and one PCI Express bus interface connector. These interface connectors are discussed in the following sections.

Carrier Field I/O Connectors (IP modules A through D)

Field I/O connections are made via 50 pin ribbon cable connectors A, B, C, and D for IP modules in positions A through D. IP module assignment is marked on the board for easy identification (see IP location drawing 4502-135 for physical locations of the IP modules). Flat cable assemblies and termination panels (or user defined terminations) can be quickly mated to the field I/O connectors. Pin assignments are defined by the IP module employed since the pins from the IP module field side correspond identically to the pin numbers of the 50 pin connectors.

Carrier field I/O connectors A through D are TE Connectivity Low Profile 50-pin headers (TE P/N 1-1761685-5) and they mate to ejector equipped ribbon cable connectors (3M P/N 3425-6600).

IP Field I/O Connectors (IP modules A through D)

The field side connectors of IP modules A through D mate to AMP 173280-3 connectors, on the carrier board. IP locations are labeled on the board for easy identification. Field and logic side connectors are keyed to avoid incorrect assembly.

The AMP 173280-3 connectors mate to AMP 173279-3 connectors (or similar) on the IP modules. This provides excellent connection integrity and utilizes gold plating in the mating area. Threaded metric M2 screws and spacers (supplied with Acromag IP modules) provide additional stability for harsh environments (see Drawing 4502-148 for assembly details).

Pin assignments for these connectors are made by the specific IP model used and correspond identically to the pin numbers of the front panel connectors.

IP Logic Interface Connectors (IP modules A through D)

The logic interface sides of IP modules A through D mate to AMP 173280-3 connectors, on the carrier board. IP locations are labeled on the board for easy identification. Field and logic side connectors are keyed to avoid incorrect assembly.

The AMP 173280-3 connectors mate to AMP 173279-3 connectors (or similar) on the IP modules. This provides excellent connection integrity and utilizes gold plating in the mating area. Threaded metric M2 screws and spacers (supplied with Acromag IP modules) provide additional stability for harsh environments (see Drawing 4502-148 for assembly details).

Pin assignments for these connectors are defined by the IP module specification and are shown in Table 2-1.

Table 2-1 IP Bus Connectors

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSel*	29
D01	5	***DMAReq0****	30
D02	6	MEMSel*	31
D03	7	***DMAReq1****	32
D04	8	IntSel*	33
D05	9	***DMAck0****	34
D06	10	IOSEL*	35
D07	11	***RESERVED***	36
D08	12	A1	37
D09	13	***DMAEnd****	38
D10	14	A2	39
D11	15	ERROR*	40
D12	16	A3	41
D13	17	INTReq0*	42
D14	18	A4	43
D15	19	INTReq1*	44
BS0*	20	A5	45
BS1*	21	STROBE*	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	***RESERVED***	49
GND	25	GND	50

Notes(Table 2-1):

1. Asterisk (*) is used to indicate an active-low signal.
2. BOLD ITALIC Logic Lines are NOT USED by the carrier board.

PCI Express Bus Connections

Table 2-2 indicates the pin assignments for the PCIe bus signals at the card edge connector. Connector pins are designated by a letter and a number. The letter indicates which side of a particular connector the pin contact is on.

"B" is on the component side of the carrier board while "A" is on the solder side. Connector "gold finger" numbers increase with distance from the bracket end of the printed circuit board.

Refer to the PCI Express bus specification for additional information on the PCI Express bus signals

Table 2-2 PCIe Bus P1 CONNECTIONS

Signal	Pin	Pin	Signal
+12V	B01	A01	PRSNT1*
+12V	B02	A02	+12V
+12V	B03	A03	+12V
GND	B04	A04	GND
SMCLK	B05	A05	TCK
SMDAT	B06	A06	TDI
GND	B07	A07	TDO
+3.3V	B08	A08	TMS
TRST*	B09	A09	+3.3V
+3.3Vaux	B10	A10	+3.3V
WAKE*	B11	A11	PERST*
RSVD	B12	A12	GND
GND	B13	A13	REFCLKp
Tx0p	B14	A14	REFCLKn
Tx0n	B15	A15	GND
GND	B16	A16	Rx0p
PRSNT2*	B17	A17	Rx0n
GND	B18	A18	GND

Notes (Table 2-2):

1. Asterisk (*) is used to indicate an active-low signal.
2. BOLD ITALIC Logic Lines are NOT USED by the carrier board.

FIELD GROUNDING CONSIDERATIONS

Carrier boards are designed with passive filters on each supply line to each IP module. This provides maximum filtering and signal decoupling between the IP modules and the carrier board. However, the boards are considered non-isolated, since there is electrical continuity between the PCIe bus and the IP grounds. Therefore, unless isolation is provided on the IP module itself, the field I/O connections are not isolated from the PCI bus. Care should be taken in designing installations without isolation to avoid ground loops and noise pickup. This is particularly important for analog I/O applications when a high level of accuracy/resolution is needed (12-bits or more). Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the IP input/output modules.

DATA TRANSFER TIMING

The PCI express interface will treat all data transfers as 32 bits with the appropriate byte lanes enabled to support the actual requested number of bytes: 4, 2 or 1. The 32 bit transfer is broken into two back to back 16 bit accesses on the IP bus. The highest transfer rates will be achieved when accessing two 16 bit IP registers with consecutive addresses. The time to complete the 32 bit PCI express transaction is the same for 4, 2 or 1 byte(s) transferred. The time between PCI express transactions is system dependent. The APCe8650 does not insert any hold states.

3. PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the APCe8650 non-intelligent carrier board.

This Acromag APCe8650 is a PCIe Specification version 1.1 compliant PCIe bus slave carrier board. The carrier connects a PCIe host bus to the IP module's 16-bit data bus per the Industrial I/O Pack logic interface specification on the mezzanine (IP) boards that are installed on the carrier.

The PCI bus is defined to address three distinct address spaces: I/O, memory, and configuration space. **The IP modules can be accessed via the PCI bus memory space only.**

The PCIe card's configuration registers are initialized by system software at power-up to configure the card. The PCIe carrier is a Plug-and-Play PCI card. As a Plug-and-Play card the board's base address and system interrupt request line are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCIe bus configuration access is used to access a PCIe card's configuration registers.

PCI Configuration Address Space

When the computer is first powered-up, the computer's system configuration software scans the PCIe bus to determine what PCIe devices are present. The software also determines the configuration requirements of the PCIe card.

The system software accesses the configuration registers to determine how many blocks of memory space the carrier requires. It then programs the carrier's configuration registers with the unique memory address range assigned.

The configuration registers are also used to indicate that the PCI carrier requires an interrupt request line. The system software then programs the configuration registers with the interrupt request line assigned to the PCI carrier.

Since this PCI carrier is portable and not hardwired in address space, this carrier's device driver provided by Acromag uses the mapping information stored in the carrier's Configuration Space registers to determine where the carrier is mapped in memory space and which interrupt line will be used.

Configuration Transactions

The PCI bus is designed to recognize certain I/O accesses initiated by the host processor as a configuration access. Configuration uses two 32-bit I/O ports located at addresses 0CF8 and 0CFC hex. These two ports are:

32-bit configuration address port, occupying I/O addresses 0CF8 through 0CFB hex.

32-bit configuration data port, occupying I/O addresses 0CFC through 0CFF hex.

Configuration space, shown in Table 3-1,, is accessed by writing a 32-bit long-word into the configuration address port that specifies the PCI bus, the carrier board on the bus, and the configuration register on the carrier being accessed. A read or write to the configuration data port will then cause the configuration address value to be translated to the requested configuration cycle on the PCI bus. Accesses to the configuration data port determine the size of the access to the configuration register addressed and can be an 8, 16, or 32-bit operation.

Any access to the Configuration address port that is not a 32-bit access is treated like a normal computer I/O access. Thus, computer I/O devices using 8 or 16-bit registers are not affected because they will be accessed as expected.

Table 3-1 Configuration Address Port

BIT	FUNCTION
31	Enables accesses to Configuration Data to be translated to configuration cycles on the PCI bus.
30-24	Reserved, Return 0 when read.
23-16	Bus Number Choose a specific PCI bus in the system. Zero if only one PCI bus.
15-11	Device Number Choose a specific device/PCI board on the bus.
10-8	Function Number Choose a specific function in a device. Function number is zero for the APCe8650
7-2	Register Number Used to indicate which PCI Configuration Register to access. The Configuration Registers and their corresponding register numbers are given in Table 3.2.
1-0	Read Only bits that return 0.

Configuration Registers

The PCI specification requires software driven initialization and configuration via the Configuration Address space. This PCI carrier provides 256 bytes of configuration registers for this purpose. The PCI carrier contains the configuration registers, shown in Table 3-2, to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers and the Interrupt Line Register, which must be read to determine the base address, assigned to the carrier and the interrupt request line that goes active on a carrier interrupt request.

Table 3-2 Configuration Registers

REG	D31 D24	D23 D16	D15 D8	D7 D0
0	Device ID=5901		Vendor ID= 16D5	
1	Status		Command	
2	Class Code		Rev ID	
3	BIST	Header	Latency	Cache
4	Base Addr. Memory Mapped Configuration Registers			
5	Base Address for I/O Mapped Configuration Registers			
6	*PCIBar2:* Base Address for Carrier/IO/ID/INT/Memory Space			
7-10	Not Used			
11	Subsystem ID		Subsystem Vendor ID	
12	Not Used			
13	Reserved			
14	Reserved			
15	Max_Lat	Min_Gnt	Inter. Pin	Inter. Line

Memory Map

This board occupies a 64M byte block. The 64M byte block of memory consists of blocks of memory for the ID, I/O, INT and memory spaces corresponding to four IP modules. In addition, a small portion of the address space contains registers specific to the function of the carrier board.

The carrier is configured to map this 64M byte block of memory into 32-bit memory space. The system configuration software will allocate space by writing the assigned addresses into the corresponding Base Address registers of the Configuration Registers. The memory map for APCe8650 is shown in Table 3-3.

Table 3-3 APCe8650 Carrier Board Memory Map

PCIBar2 + (Hex)	High Byte D15 D08	Low Byte D07 D00	PCIBar2 + (Hex)
0001	Carrier Board Status / Control Register		**0000**
0003	IP Interrupt Pending Register		**0002**
0005	IP A Interrupt 0 Select Space		**0004**
0007	IP A Interrupt 1 Select Space		**0006**
0009	IP B Interrupt 0 Select Space		**0008**
000B	IP B Interrupt 1 Select Space		**000A**
000D	IP C Interrupt 0 Select Space		**000C**
000F	IP C Interrupt 1 Select Space		**000E**
0011	IP D Interrupt 0 Select Space		**0010**

PCIBar2 + (Hex)	High Byte D15 D08	Low Byte D07 D00	PCIBar2 + (Hex)
0013	IP D Interrupt 1 Select Space		**0012**
0015	Not Used[1]		**0014**
0017	Not Used[1]		**0016**
0019	Clock Control Register		**0018**
001B	ID Register		**001A**
001D ↓ **003F**	Not Used[1]		**001C** ↓ **003E**
0041 ↓ **007F**	IP A ID Space	IP A ID Space	**0040** ↓ **007E**
0081 ↓ **00BF**	IP B ID Space	IP B ID Space	**0080** ↓ **00BE**
00C1 ↓ **00FF**	IP C ID Space	IP C ID Space	**00C0** ↓ **00FE**
0101 ↓ **013F**	IP D ID Space	IP D ID Space	**0100** ↓ **013E**
0141 ↓ **017F**	Not Used[1]	Not Used[1]	**0140** ↓ **017E**
0181 ↓ **01FF**	IP A I/O Space	IP A I/O Space	**0180** ↓ **01FE**
0201 ↓ **027F**	IP B I/O Space	IP B I/O Space	**0200** ↓ **027E**
0281 ↓ **02FF**	IP C I/O Space	IP C I/O Space	**0280** ↓ **02FE**
0301 ↓ **037F**	IP D I/O Space	IP D I/O Space	**0300** ↓ **037E**
0381 ↓ **07FFFF**	Not Used[1]	Not Used[1]	**0380** ↓ **07FFFE**
0800001 ↓ **0FFFFFF**	IP A Memory Space		**0800000** ↓ **0FFFFFE**
1000001 ↓ **17FFFF**	IP B Memory Space		**1000000** ↓ **17FFFE**

PCIBar2 + (Hex)	High Byte D15 D08	Low Byte D07 D00	PCIBar2 + (Hex)
1800001 ↓ **1FFFFFF**	IP C Memory Space		**1800000** ↓ **1FFFFFE**
2000001 ↓ **27FFFFF**	IP D Memory Space		**2000000** ↓ **27FFFFE**
2800001 ↓ **3FFFFFF**	Not Used[1]		**2800000** ↓ **3FFFFFE**

Notes (Table 3-3):

1. Shaded areas not used by APCe8650A carrier.
2. The board will return "0" for all addresses that are not used.

The APCe8650 base addresses are determined through the PCI Configuration Registers. The addresses given in the memory map are relative to the base addresses PCIBar2 of the APCe8650 carrier as shown in Table 3-2. The addresses within each IP's own space are specific to that IP module. Refer to the IP module's User Manual for information relating to the IP specific addressing.

The Carrier registers, IP Identification (ID) spaces, IP Input/Output (IO), IP Interrupt spaces, and Memory (MEM) spaces are accessible via the PCI bus space as given in Table 3-3. A 32-bit PCI bus access will result in two 16-bit accesses to the IP module. A 16-bit or 8-bit PCI bus access results in a single 16-bit or 8-bit access to the IP module respectively.

Carrier Status/Control Register - (Read/Write, PCIBar2 + 00H)

The Carrier Board Status Register reflects and controls functions globally on the carrier board. This includes monitoring the IP Error signal, enabling, disabling, or monitoring IP and timeout interrupts and performing a software reset.

Table 3-4 Carrier Status / Control Register Bit Assignment

BIT	FUNCTION
15-9	Not Used (bits read as logic "0")
8 Write Only	Software Reset Writing a "1" to this bit causes a software reset. Writing a "0" or reading this bit has no effect. When set, the software reset pulse will have duration of 1 microsecond.
7	Not Used (bit reads as logic "0")
6 Read Only	FLASH Busy This bit will be "1" when a read or write to the ID FLASH is in progress. On initial application of power, a FLASH read sequence is automatically initiated to retrieve the ID bytes from the FLASH. The read sequence will take less than 5 microseconds. The ID bytes are stored in the ID register. Reading the ID register does not trigger a FLASH read sequence. A write to the ID register will initiate a FLASH write / read sequence that could take up to 3 seconds to complete. The busy bit will be "1" while the write / read sequence is in progress.
5 Read And Write	IP Module Access Time Out Interrupt Pending This bit will be "1" when there is an IP Module Access Time Out interrupt pending. This bit will be "0" when there is no interrupt pending. Reset condition: Set to "0". Writing a "1" to this bit will release the pending interrupt.
4 Read Only	IP Module Access Time Out Status Indicates the last IP module access has timed out. This bit only reflects the last IP module access. "0" if last IP module access did not time out. "1" if last IP module access did time out.
3 Read And Write	Time Out Interrupt Enable When set to "1", this bit will enable the carrier board to generate an interrupt upon time out of an IP module access. The default setting or reset condition is "0" (interrupt generation upon time out disabled). The interrupt service routine must set this bit to 0 to clear the pending interrupt request.
2 Read And Write	IP Module Interrupt Enable When set to "1", this bit will enable the generation of IP module interrupts. The reset condition is "0", (IP module interrupt generation disabled). Interrupts must also be supported and configured in the IP modules.

BIT	FUNCTION
1 Read Only	IP Module Interrupt Pending This bit will be "1" when there is an interrupt pending. This bit will be "0" when there is no interrupt pending. Polling this bit will reflect the IP Module's pending interrupt status, even if the IP Module Interrupt Enable bit is set to "0". Reset condition: Set to "0".
0 Read Only	IP Module Error This bit will be "1" when there is an active IP Module Error signal. This bit will be "0" when all IP module Error signals are inactive. This bit allows the user to monitor the Error signals of IP modules A through D. The IP specification states that the error signals indicate a non-recoverable error from the IP (such as a component failure or hard-wired configuration error). Refer to your IP specific documentation to see if the error signal is supported and what it indicates. Reset condition: Set to "0".

IP Interrupt Pending Register - (Read, PCIBar2 + 02H)

The IP Interrupt Pending Register is used to individually identify pending IP interrupts or a pending carrier generated interrupt as a result of IP module access time out. If multiple IP interrupts are pending, software must determine the order in which they are serviced.

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
IP D Int1 Pend	IP D Int0 Pend	IP C Int1 Pend	IP C Int0 Pend	IP B Int1 Pend	IP B Int0 Pend	IP A Int1 Pend	IP A Int0 Pend

MSB D15 -- D11	D10	LSB D9 -- D8
Not Used (bits read as logic "0")	Time Out Interrupt Pend	Not Used (bits read as logic "0")

A bit will be a "1" when the corresponding interrupt is pending. A bit will be a "0" when its corresponding interrupt is not pending. Polling this bit will reflect the IP module's pending interrupt status, even if the IP interrupt enable bit is set to "0".
Reset Condition: Set to "0". An IP module pending interrupt bit will be cleared if its corresponding interrupt request signal is inactive.

Clock Control Register - (Read/Write, PCIBar2 + 018H)

The Clock Control Register is used to select the clock frequency of the individual IP modules. A "0" (default) selects the 8MHz clock. A "1" selects the 32MHz clock. A reset will set all bits of this register to "0".

MSB D15 -- D4	D3	D2	D1	LSB D0
Not Used	IP D CLK	IP C CLK	IP B CLK	IP A CLK

ID Register - (Read/Write, PCIBar2 + 01AH)

The ID Register is used to store and retrieve a 16 bit non-volatile identifier that can be used to uniquely identify a particular carrier board. The ID register reflects the contents of the first two bytes of an on-board serial FLASH memory. On initial application of power, a FLASH read sequence is automatically initiated to retrieve the ID bytes from the FLASH. The read sequence will take less than 5 microseconds. Reading the ID register does not trigger a FLASH read sequence. A write to the ID register will initiate a FLASH write / read sequence that could take up to 3 seconds to complete. The busy bit will be "1" while the write / read sequence is in progress.

IP Module Interrupt Space - (Read Only)

The Interrupt space for each IP module is fixed at two 16-bit words. Interrupt 0 select space is read, typically by an interrupt service routine, to respond to an interrupt request via the IP Module's INTREQ0* signal. Likewise interrupt 1 select space is read to respond to an interrupt request via the IP Module's INTREQ1* signal. An access to an interrupt select space results in the IP module serving up an interrupt vector. In addition, access to the interrupt space will cause some IP modules to release their interrupt request. See each IP module's User Manual for details.

IP Module ID Space- (Read Only)

Each IP contains identification (ID) information that resides in the ID space per the IP specification. This area of memory contains either 32 bytes (Format I ID) or 64 bytes (Format II ID) of information, at most. Format I requires read of only the least significant byte. Format II requires read of a 16-bit value. The carrier will implement 16-bit reads to the ID space to allow support for either Format I or Format II. Both fixed and variable information may be present within the ID ROM. Variable information may include unique information required for the module. The identification Section for each IP module is located in the carrier board memory map per Table 3-3. Refer to the documentation of your IP module for specific information about each IP module's ID Space contents.

IP Module I/O Space - (Read/Write)

The I/O space on each IP module is fixed at 64, 16-bit words (128 bytes). The four IP module I/O spaces are accessible at fixed offsets from PCIBar2. IP modules may not fully decode their I/O space and may use byte or word only accesses. See each IP module's User Manual for details.

IP Module Memory Space - (Read/Write)

Each IP module may contain up to 8M bytes of Memory Space accessed as 16-bit words. The four IP module Memory spaces are accessible at fixed offsets from PCIBar2. IP modules may not fully decode their Memory space and may use only byte or word accesses. See each IP module's User Manual for details.

GENERATING INTERRUPTS

Interrupt requests originate from the carrier board in the case of an access time out and from the IP modules. Each IP may support 0, 1, or 2 interrupt requests. Upon an IP module interrupt request the carrier passes the interrupt request onto the host, provided that the carrier board is enabled for interrupts within the Carrier Board Status Register.

Sequence of Events for Processing an Interrupt

Perform any IP specific configuration required - do for each supported IP interrupt request.

Set the interrupt enable bit in the Carrier Board Status Register by writing a "1" to bit 2.

The IP module asserts an interrupt request to the carrier board (asserts interrupt request line IntReq0* or IntReq1*).

If the INTx virtual wire interrupt signaling method is being used, the carrier transmits an "Assert_INTx" message. When using MSI interrupts, a MSI interrupt message is sent.

The interrupt service routine determines which IP module caused the interrupt by reading the carrier interrupt pending register. If multiple interrupts are pending the interrupt service routine software determines which IP module to service first. If legacy PCI interrupts are used then the interrupts could be shared and can be from any slot on the backplane or from the mother board itself. The driver must first check that the interrupt came from the PCIe carrier by reading the carrier interrupt pending register. When using MSI interrupts, the interrupting carrier will be uniquely identified. A polling sequence to identify the interrupting carrier is not needed.

The interrupt service routine accesses the interrupt space of the IP module selected to be serviced. Note that the interrupt space accessed must correspond to the interrupt request signal driven by the IP module.

The carrier board will assert the INTSEL* signal to the appropriate IP together with (carrier board generated) address bit A1 to select which interrupt request is being processed (A1 low corresponds to INTREQ0*; A1 high corresponds to INTREQ1*).

The IP module receives an active INTSEL* signal from the carrier and supplies its interrupt vector to the host system during this interrupt acknowledge cycle. An IP module designed to release its interrupt request on acknowledge

will release its interrupt request upon receiving an active INTSEL* signal from the carrier. If the IP module is designed to release its interrupt request on register access the interrupt service routine must access the required register to clear the interrupt request.

If the IP interrupt stimulus has been removed and no other IP modules have interrupts pending, the interrupt cycle is completed (i.e. the carrier board transmits a "Deactivate_INTx" message).

4. THEORY OF OPERATION

This section describes the basic functionality of the circuitry used on the carrier board. Refer to Figure 1 APCe8650 Block Diagram as you review this material.

CARRIER BOARD OVERVIEW

The carrier board is a PCIe bus slave/target board providing up to four IP module interfaces. The carrier board's PCIe bus interface allows an intelligent single board computer (PCI bus Master) to control and communicate with IP modules that are present on the PCIe bus carrier. IP module field I/O connections link to field I/O connections on the carrier, which in turn connect to field electronic hardware connected to the carrier board via ribbon cable.

The PCIe bus and IP module logic commons have a direct electrical connection (i.e., they are not electrically isolated). However, the field I/O connections can be isolated from the PCIe bus if an IP module that provides this isolation (between the logic and field side) is utilized. A wide variety of IP modules are currently available (from Acromag and other vendors) that interface with many external devices for digital I/O, analog I/O, and communication applications.

PCIe Bus Interface

The carrier board's PCIe bus interface is used to program and monitor carrier board registers for configuration and control of the board's modes of operation (see section 3). In addition, the PCI bus interface is also used to communicate with and control external devices that are connected to an IP module's field I/O signals (assuming an IP module is present on the carrier board).

The PCI bus interface is implemented in the logic of the carrier board's PCIe bus target interface chip. The PCIe bus interface chip implements PCIe specification version 1.1 as an interrupting slave including 8-bit and 16-bit data transfers to the IP modules. 32-bit IP data transfers will be treated as two 16-bit data transfers.

Note that the APCe8650 board is not hot-swappable.

Carrier Board Registers

The carrier board registers (presented in section 3) are implemented in the logic of the carrier board's FPGA. An outline of the functions provided by the carrier board registers includes:

Selecting either an 8MHz or 32MHz clock for each IP module in the **Clock Control Register**.

Monitoring the error signal received from each IP module is possible via the **IP Error Bit**.

Enabling of PCI bus interrupt requests from each IP module is possible via the **IP Module Interrupt Enable Bit**.

Enabling of interrupt generation upon an IP module access time out is implemented via the **Time Out Interrupt Enable Bit.**

Monitoring an IP module access time out is possible via the **IP Module Access Time Out Status Bit.**

Identify pending interrupts via the carrier's **IP Module Interrupt Pending Bit**.

Pending interrupts can be individually monitored via the **IP Module Interrupt Pending register**.

A non-volatile ID can be written to and read from a serial FLASH memory by accessing the ID register.

IP Logic Interface

The IP logic interface is also implemented in the logic of the carrier board's FPGA. The carrier board implements ANSI/VITA 4 1995 Industrial I/O Pack logic interface specification and includes four IP logic interfaces. The PCIe bus is linked to the address and data of the IP bus interface. This link is implemented and controlled by the carrier board's FPGA.

The PCIe bus to IP bus interface allows a PCIe bus master to:

Access up to 64 ID Space bytes for IP module identification via 8-bit or 16-bit data transfers using PCIe bus.

Access up to 128 I/O Space bytes of IP data via 8-bit or 16-bit data transfers.

Access up to 8M byes of IP Memory Space data via 8-bit or 16-bit data transfers.

Access IP module interrupt space via 8-bit or 16-bit PCI bus data transfers.

Respond to two IP module interrupt requests per IP module.

When an IP module places data on the bus, for all data read cycles, any undriven data lines are read by the PCI bus as high because of pull-up resisters on the carrier board's data bus.

Carrier Board Clock Circuitry

An 80 MHz oscillator is used to clock the FPGA. The 32 MHz or 8 MHz IP bus clocks are generated from the 80 MHz clock by a phased locked loop internal to the FPGA. Clocks are then driven to each IP module via a high speed transceiver to allow for a module independent selectable clock. All clock lines include series damping resistors to reduce clock overshoot and undershoot.

PCI Interrupter

Interrupts are initiated from an interrupting IP module. However, the carrier board will only pass an interrupt generated by an IP module to the PCI bus if the carrier board has been first enabled for interrupts. Each IP module can initiate two interrupts which can be individually monitored on the carrier board. After interrupts are enabled on the carrier board via the Interrupt Enable Bits (see section 3 for programming details), an IP generated interrupt is recognized by the carrier board and is recorded in the carrier board's Interrupt Pending Register.

A carrier board pending interrupt will cause the board to pass the interrupt to the PCIe bus provided the Interrupt Enable bits of the carrier's Status Register have been enabled (see section 3 for programming details). The PC interrupt request line assigned by the system configuration software will then be asserted. The PC will respond to the asserted interrupt line by executing the interrupt service routine corresponding to the interrupt line asserted. The interrupt service routine is executed only if the IRQ on the PC's interrupt controller has been previously unmasked (see section 3 for programming details).

The interrupt service routine should respond to an interrupt by accessing IP Interrupt Select (INTSEL*) space. The interrupt service routine should also conclude the interrupt routine by writing the "End-Of-Interrupt" command to the PC's 8259 interrupt controller (see section 3 for more details).

Power Failure Monitor

The carrier board contains a 5 volt under voltage monitoring circuit which provides a reset to the IP modules when the 5 volt power drops below 4.5 volts typical / 4.37 volts minimum. This circuitry is implemented per the Industrial I/O Pack specification.

Power-On Reset

The carrier board will provide an asynchronous reset signal to all IP modules for at least 100ms following power-up. The IP reset signal will remain active until the FPGA is initialized.

Power Supply Fuses

The +5V supply lines to each of the IP modules are individually fused with a current limit of 2 amps minimum. In addition, the +12 V, and -12 V supply lines to each of the IP modules are individually fused with a current limit of 1

amp minimum. A blown fuse can be identified by visible inspection or by use of an ohm meter. The fuses are located under each IP slot near the "logic connectors" (see drawing 4502-135). Note that fuse type and current limit may vary. Contact Acromag for further details.

Power Supply Filters

Power line filters are dedicated to each IP module for filtering of the +5, +12, and -12 volt supplies. The power line filters are a "T" type filter circuit comprising ferrite bead inductors and a feed-through capacitor. The filters provide improved noise performance as is required on precision analog IP modules.

5. SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. .

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Verify that there are no blown fuses. Replacement of the carrier and/or IP with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

Go to the "Support" tab to access:

Application Notes

Frequently Asked Questions (FAQ's)

Product Knowledge Base

Tutorials

Software Updates/Drivers

An email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab.

Acromag's application engineers can also be contacted directly for technical assistance via telephone or FAX through the numbers listed below. When needed, complete repair services are also available.

Phone: 248-624-1541
Fax: 248-624-9234
Email: solutions@acromag.com

6. SPECIFICATIONS

PHYSICAL

Physical Configuration

Length (APCe8650) .....12.283 inches (312.0 mm)
Height.....4.200 inches (106.68 mm)
Board thickness.....0.063 inches (1.60 mm)
Max component height .....0.380 inches (9.65 mm)
Max component height under IP modules
0.180 inches (4.57 mm)

Connectors

P1 (PCIe Bus).....PCI Express V1.1 x1 lane
A-D (Carrier Field I/O) .....50-pin Low Profile Male Header (TE P/N 1-1761685-5).
P2, 5, 8, 11 (IP Field I/O) .....50-pin male plug header
P4, 7, 10, 13 (IP Logic).....50-pin male plug header (AMP 173280-3 or equivalent).

Power

Board power requirements are a function of the installed IP modules. This specification lists currents for the carrier board only. The carrier board provides +5V, +12V and -12V power to each IP module. Power for the IP modules can be supplied either from the PCIe bus +12V supply or from the auxiliary peripheral power connector or the PCIe graphics power connector. The +12V power source for the IP modules is selected by jumper J1. The APCe8650 contains DC/DC converters, which generate the +5V and -12V supplies from the selected +12V source. Each IP module supply line is individually filtered and fused. In addition the carrier board utilizes PCIe bus 3.3 volt power for logic. Note that the maximum amount of current provided to the carrier card via the PCIe bus varies with each system. Refer to your system documentation for more information on PCIe power specifications.

Fuses

+5 volts, 2 amps (minimum) per slot
±12 volts, 1 amp (minimum) per slot

The power failure monitor circuit provides a reset to IP modules when the 5 volt power drops below 4.5 volts typically / 4.37 volts minimum.

Currents specified are for the carrier board only for Model APCe8650(E), add the IP module currents for the total current required from each supply.

+3.3 Volts (±10%).....190 mA Typical
220 mA Maximum
+12 Volts (±5%).....130 mA Typical
150 mA Maximum

PCIe BUS COMPLIANCE

Specification.....This device meets or exceeds all written PCI Express specifications per revision 1.1 dated March 28, 2005.
Data Transfer Bus.....Slave with 32-bit, 16-bit, and 8-bit data transfer operation. 32-bit read or write accesses are implemented as two 16 bit transfers to the IP modules.

INDUSTRIAL I/O PACK COMPLIANCE

Specification.....This device meets or exceeds all written Industrial I/O Pack specifications per ANSI/VITA 4 1995 for 8MHz and 32MHz operation with a maximum of four IP modules. Supports Type I and Type II ID space formats.
Mechanical Interface .....Carrier supports four single-(For APCe8650) size IP modules.
Electrical Interface .....Carrier drivers use 5V CMOS logic
IP Clocks .....Support 8MHZ (default) or 32MHz IP clocks that are independently selected per each IP slot.
I/O Space.....16-bit and 8-bit: Supports 128 byte values per IP module.
ID Space .....16 and 8-bit; Supports Type 1 32 bytes per IP (consecutive odd byte addresses). Also supports Type II 32 words per IP via D16 data transfers.
Memory Space .....16 and 8-bit: Supports up to 8M bytes per IP.
Interrupts.....PCI bus INTA# interrupt signal
Up to two requests sourced from each IP are mapped to INTA#. Interrupt vectors come from IP modules via access to IP module INT space. One MSI interrupt is also supported.

ENVIRONMENTAL

Operating Temperature.....0 to +70°C (APCe8650)
-40 to +85°C (APCe8650E)
Relative Humidity.....5-95% non-condensing
Storage Temperature.....-55 to +125°C.
Non-Isolated .....The PCIe bus and the IP module commons have a direct electrical connection. As such unless the IP module provides isolation between the logic and field side, the field I/O signals are not isolated from the PCIe bus.
Radiated Field Immunity.....Designed to comply with IEC61000-4-3: 2006 Level A (10V/m, 80 to 1000MHz 80% AM modulation, 1 KHz).
Surge Immunity.....Not required for signal I/O per European Norm EN61000-6-1.
Electric Fast Transient Immunity
Designed to comply with IEC61000-4-4: 2007 Level 3 (1kV at field input and output terminals, capacitive coupling clamp used)
Radiated Emissions .....Designed to comply with CISPR 16-2-3 class A

Electrostatic Discharge .....Designed to comply with IEC6100-4-2: 2001 Level 2 (4kV contact discharge, 4kV air discharge)

Conducted Radio Frequency Interference

Designed to comply with IEC6100-4-6:2007 Level 3 (10 V/m, 150 KHz to 80 MHz 80% AM modulation, Bulk Current Injection method)

Certificate of Volatility

Certificate of Volatility				
Acromag Model APCe8650(E)	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) ■ Yes □ No				
Type(SRAM,SDRAM,etc.)	Size:	User Modifiable	Function:	Process to Sanitize:
FPGA based RAM	540 K bits	No	Short term data storage	Power Down
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No				
Type(EEPROM, FLASH etc.)	Size:	User Modifiable	Function:	Process to Sanitize:
FLASH	1 Mbit	Yes	Storage of 16 bit board identification code	Overwrite ID register.
Type(EEPROM, FLASH etc.)	Size:	User Modifiable	Function:	Process to Sanitize:
FLASH	4 Mbit	No	Storage of FPGA configuration data	Factory programmed, not accessible by user

Acromag Representative				
Name: Russ Nieves	Title: Dir. of Sales	Email: solutions@acromag.com	Office Phone: 248-295-0310	Office Fax: 248-624-9234

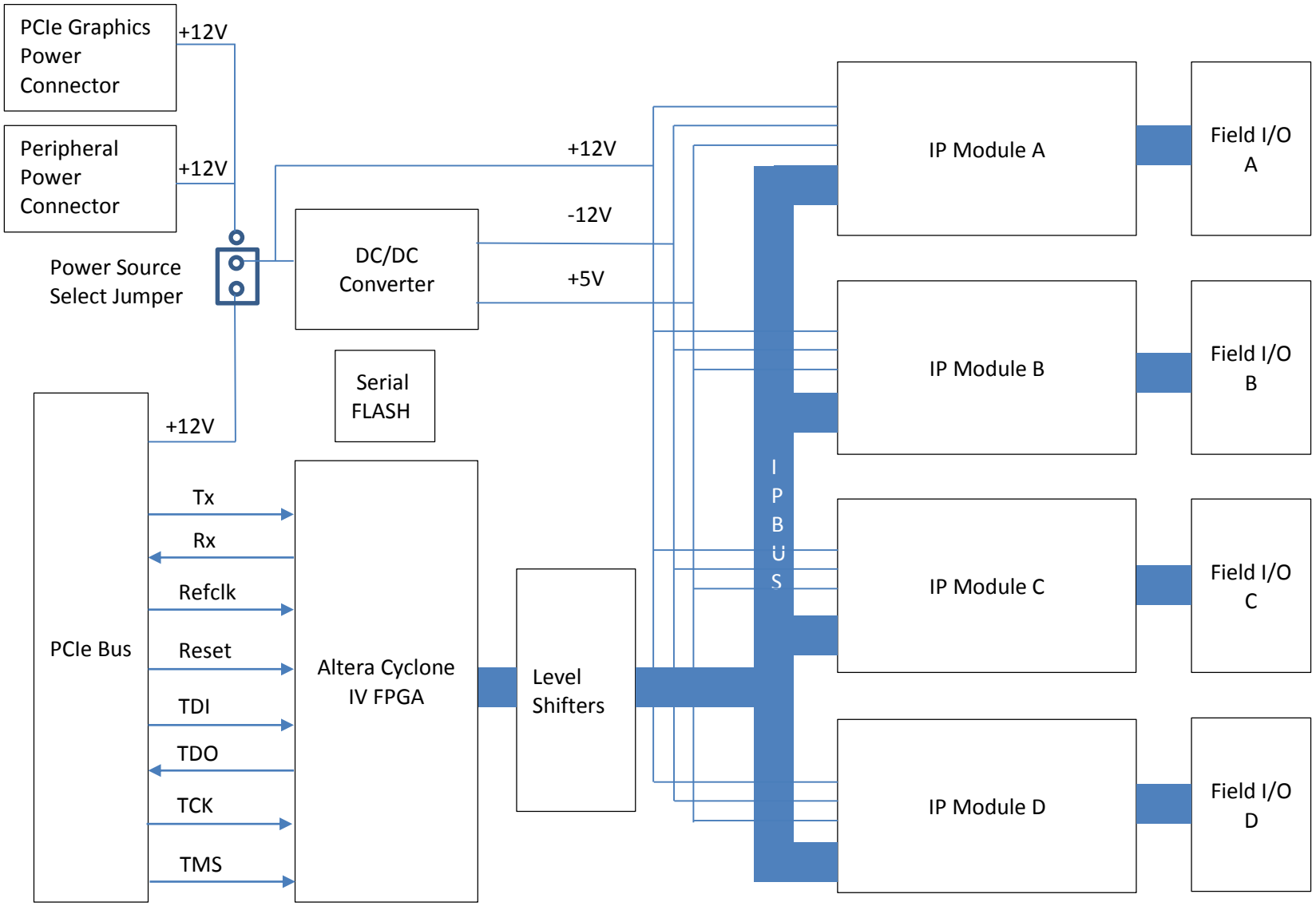
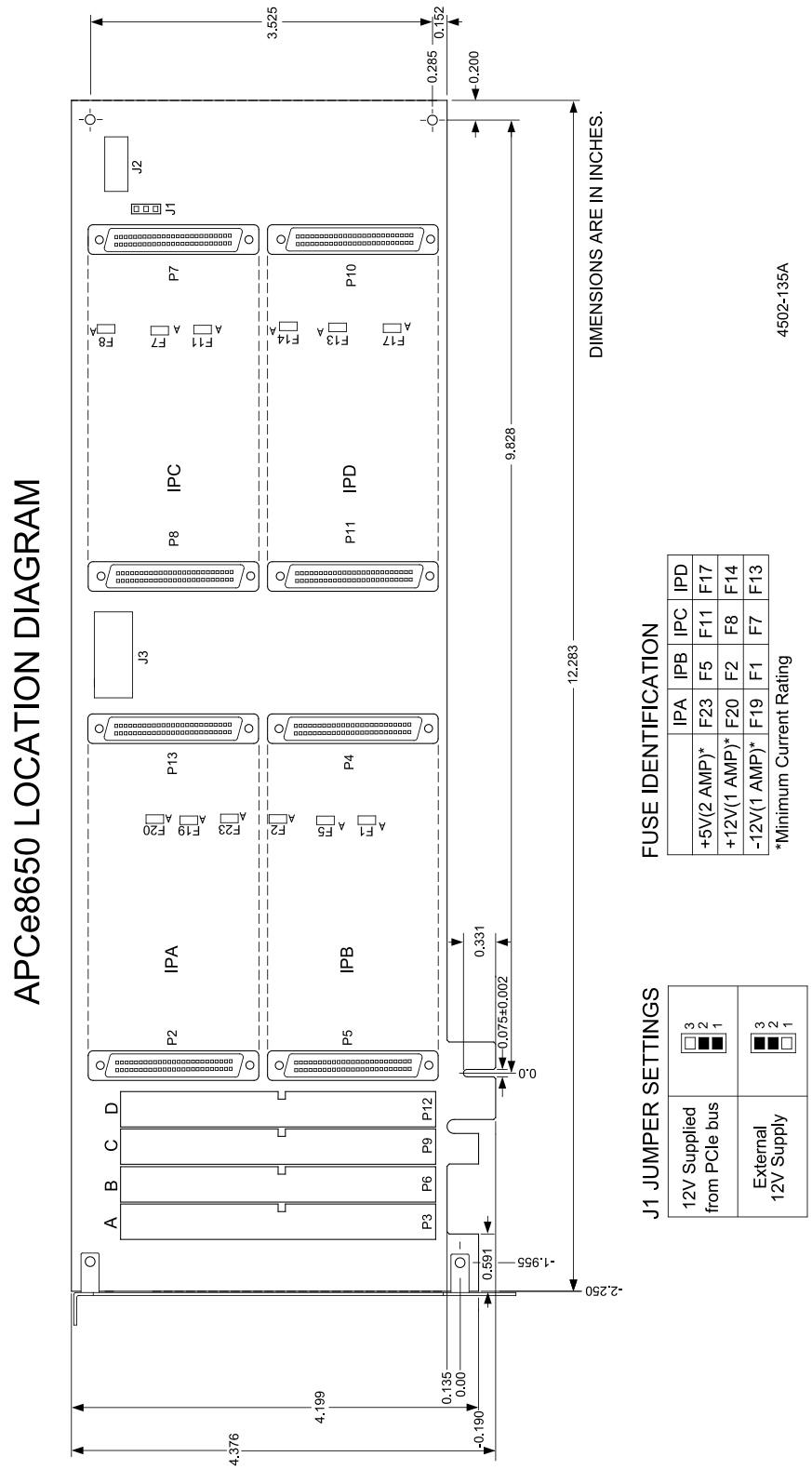


Figure 1 APCe8650 Block Diagram

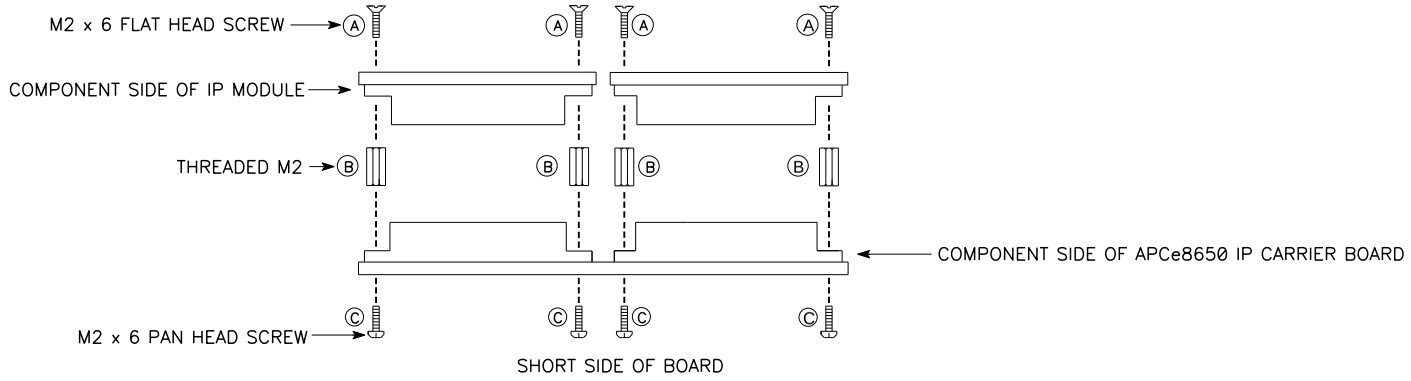
DRAWINGS


APCe8650 LOCATION DIAGRAM
DIMENSIONS ARE IN INCHES.
4502-135A
3.525
0.152
0.285
0.200
9.828
12.283
J1
J2
J3
P7
P10
P8
P11
IPC
IPD
F8
F7
F11
F14
F13
F17
P13
P4
P2
P5
IPA
IPB
F20
F19
F23
F2
F5
F1
P12
P9
P6
P3
D
C
B
A
0.331
0.075±0.002
0.0
1.955
0.591
2.250
0.135
0.00
4.199
0.190
4.376
FUSE IDENTIFICATION
IPA IPB IPC IPD
+5V(2 AMP)* F23 F5 F11 F17
+12V(1 AMP)* F20 F2 F8 F14
-12V(1 AMP)* F19 F1 F7 F13
*Minimum Current Rating
J1 JUMPER SETTINGS
12V Supplied from PCIe bus
External 12V Supply
3 2 1
3 2 1

IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY

ASSEMBLY PROCEDURE:

1. THREADED SPACERS ARE PROVIDED IN TWO DIFFERENT LENGTHS. THE SHORTER LENGTH IS FOR USE WITH APCe8650 CARRIER BOARD (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (16 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (16 PLACES).



4502-148A

7. Revision History

The following table shows the revision history for this document:

Release Date	Version	EGR/DOC	Description of Revision
31-MAY-11	A	JCL	Initial Acromag release.
18-OCT-13	B	JCL	Added Certificate of Volatility
29-OCT-13	C	JCL	Added detail to Certificate of Volatility
03-MAY-16	D	CAB/MJO	Updated 3M P/N's to TE Connectivity P/N's for A-D Connectors. Updated Acromag Contact Information.