APCe7040E-LF PCI Express AcroPack Carrier Board

USER'S MANUAL

ACROMAG INCORPORATED
30765 South Wixom Road
Wixom, MI 48393-2417 U.S.A.
Tel: (248) 295-0310

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1. GENERAL INFORMATION

Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the AcroPack module.

Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag.

Trademark, Trade Name and Copyright Information

Radio Frequency Interference Statement

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

APCe7040E-LF Overview

The APCe7040E-LF is a Peripheral Component Interconnect Express (PCIe) card and is a carrier for mini-PCIe or AcroPack mezzanine modules. This carrier board provides a modular approach to system assembly, since each carrier can be populated with any combination of analog input/output, digital input/output, communication, etc. AcroPack modules. Thus, the user can create a board which is customized to the application. This saves money and space – a single carrier board populated with AcroPack modules may replace

several dedicated function PCI or PCIe bus boards. The APCe7040E-LF non-intelligent carrier board provides impressive functionality at low cost.

Model	Board Size (Length)	AcroPack Slots	Operating Temperature Range
APCe7040E-LF	12.283 inches	4 (A, B, C, D)	-40 to +85°C (with 200 LFM airflow)

KEY APCe7040E-LF FEATURES

Interface for AcroPack modules – The APCe7040E-LF provides an electrical and mechanical interface for up to four industry standard mini-PCIe or AcroPack modules. AcroPack modules are available from Acromag. Mini-PCIe cards are available from other vendors in a wide variety of input/output configurations to meet the needs of varied applications.

PCI Express Version 2.1 Compliant Carrier: - Includes a PCIe switch to allow four PCIe devices (AcroPack or mini-PCIe) to share a single slot on the PC motherboard.

Board Identification – A unique carrier and site number can be set for each AcroPack site by a DIP switch. This feature provides the capability to distinguish a particular AcroPack module from others when multiple instances of the same module are used in a system.

JTAG Programming Header – A standard 14-pin Xilinx JTAG programming header is provided for programming and debugging the FPGA on some AcroPack modules. The JTAG ports of the two AcroPack modules are daisy-chained.

Individually Fused Power – Fused +1.5V, +3.3V, +5V, +12V, and -12V DC power is provided. A fuse is present on each supply line serving each AcroPack module. Fuses F1 – F3, F7 – F9, F13 – F15, and F19 – F21 corresponding to +5, +12, and -12V supplies are user replaceable. F4, F6, F10, F12, F16, F18, and F2, F24 corresponding to +1.5 and +3.3V are not user replaceable, you must return the board to Acromag to replace these fuses.

SIGNAL INTERFACE PRODUCTS

This AcroPack carrier board will mate directly to most industry standard mini-PCIe and AcroPack modules. Acromag provides the following interface products (all connections to field signals are made through the carrier board which passes them to the individual AcroPack modules):

Cable

Model 5028-420 Round cable, shielded, 34 twisted pairs, male SCSI-3 connector to 68 pin CHAMP 0.8mm, 2 meters long.

Termination Panel

Model 5025-288 DIN-rail mountable panel provides 68 screw terminals for universal field I/O termination, SCSI-3 connector.

Software Support

The AcroPack series products require support drivers specific to your operating system. Supported operating systems include: Linux®, Windows®, and VxWorks®.

Windows®

Acromag provides software products (sold separately) to facilitate the development of Windows® applications interfacing with AcroPack modules. This software (model APSW-API-WIN) consists of low-level drivers and Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

VxWorks®

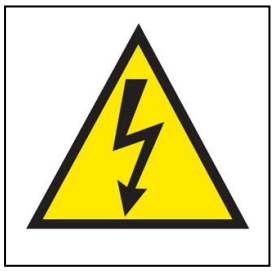
Acromag provides a software product (sold separately) consisting of VxWorks® software. This software (Model APSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of “C” functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

Linux®

Acromag provides a software product consisting of Linux® software. This software (Model APSW-API-LNX) is composed of Linux® libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of “C” functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

2. PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.

WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

BOARD CONFIGURATION

Power should be removed from the board when changing jumper configurations, changing/removing fuses, or when installing AcroPack modules, cables and field wiring.

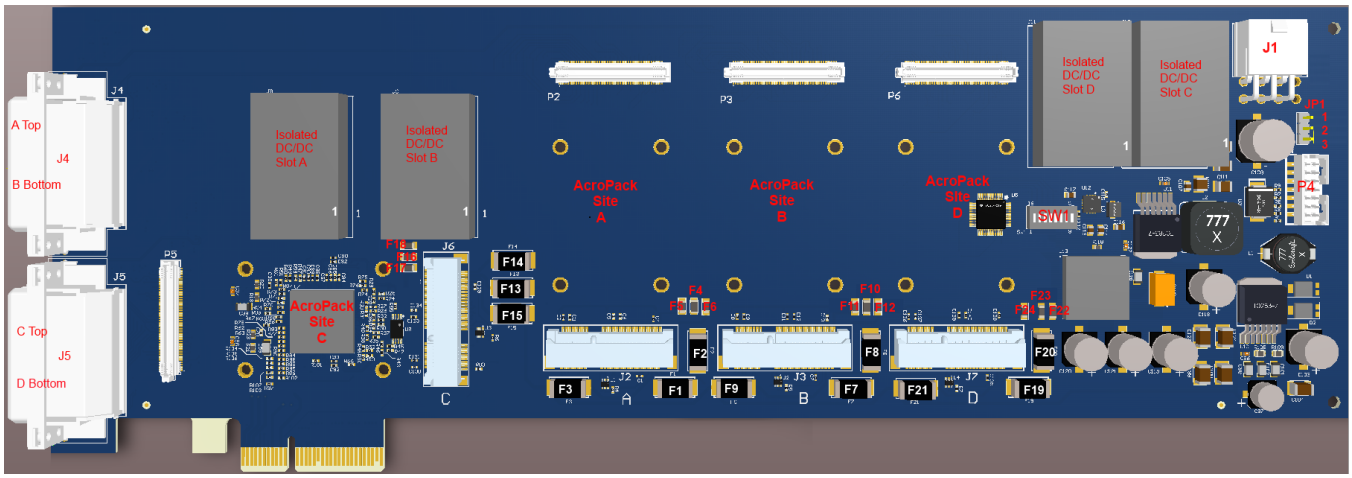


Figure 1 Connector, Switch, Jumper, and Fuse Locations

Power and Cooling Considerations

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed AcroPack modules within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The lack of air circulation within the computer chassis could be a cause for some concern. Most, if not all computer chassis do not provide a fan for cooling of add-in boards. The dense packing of the AcroPack modules to the carrier board alone results in elevated module and carrier board temperatures, and the restricted air flow within the chassis aggravates this problem. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

Jumpers

Refer to Figure 1 Jumper JP1 select the source of the +12 Volt power. The jumper must be present in one of the two configuration for proper board operation.

Table 1 JP1 +12V Power Source Select Jumper

Power Source	Jumper Position
PCIe Card Edge	1-2
PCIe Graphics Power	2-3

The carrier confirms to the 25 Watt slot power supply rail requirements with +12V supply current 2.1 Amp (max) available from the PCIe Card Edge. The board PCIe Graphics Power connector ATX12V 2.x specification allows for a delivery capability of 75 W (six-pin connector) or 150 W (eight-pin connector). The recommended jumper configuration is with Jumper installed in position 2-3.

Carrier Fuses

CAUTION: Acromag has used pins labeled as reserved in the Mini-PCIe specification for additional power connections. If you are installing a Mini-PCIe card from another manufacturer in slot A remove fuses F1(+12V), F2(+5V) and F3 (-12V). When installing a Mini-PCIe card in from another manufacturer in slot B remove fuses F7(+12V), F8(+5V) and F9 (-12V). When installing a Mini-PCIe card in from another manufacturer in slot C remove fuses F13(+12V), F14(+5V) and F15 (-12V). When installing a Mini-PCIe card in from another manufacturer in slot D remove fuses F19(+12V), F20(+5V) and F21 (-12V). Fuse locations are shown in Figure 1.

Other fuses present on the board include +1.5V Fuses F6 (slot A), F12 (slot B), F18 (slot C), F24 (slot D). Also present on the board our +3.3V Fuses F4 (slot A), F10 (slot B), F16 (slot C), F22 (slot D). These fuses are not user replaceable. Return the carrier board to Acromag to replace these fuses. Both Mini-PCIe cards from other manufacturers and the AcroPack modules can use +1.5V and +3.3V power.

Fuses not present on the board include+3.3V Aux Fuses F5 (slot A), F11 (slot B), F17 (slot C), F23 (slot D). Some standard Mini PCIe cards may require +3.3V Aux to power the module. For a site using such a module the +3.3V fuse will need to be remove and the +3.3 Aux fuse will need to be installed. Return the carrier board to Acromag to remove and install these fuses.

Isolation Considerations

WARNING: This AcroPack carrier is designed to provide isolation between the AcroPack Field I/O signals and the host. The AcroPack module must also be an isolated AcroPack module to maintain the isolation between the logic and field I/O signals. Unless isolation is provided on the AcroPack module itself, the field I/O connections are not isolated from the PCIe bus.

When this carrier is used with isolated AcroPack modules, both AcroPacks in slots A and B or C and D should be isolated AcroPacks. Non-isolated AcroPacks sharing the same Connector will compromise the isolation integrity of the other AcroPack.

Isolated Power

The use of an optional isolated DC/DC Converter is required for use with a few of Acromag's isolated AcroPack modules. See Figure 1 for carrier board location allocated for the isolated DC/DC converter corresponding to each slot.

The power supplies of one AcroPack site must be isolated from the power supplies of other AcroPack sites. The four separate isolated DC/DC converters make this possible. The DC/DC converted should only be populated on the carrier for AcroPacks needing the isolated power. Each isolated AcroPack module will list the requirement of the external DC/DC converter if needed.

The isolated DC/DC converter provide dual +12V and -12V power to the AcroPack module on field I/O pins 49 and 50 as listed in the Table below.

Table 2 Carrier Isolated Power

Supply Voltage	Current (Min)	Field I/O Pin
+12V +/- 8% (max)	0.16 A	50[1]
-12V +/- 8% (max)	0.16 A	49[1]
Return (GND)	1 A	48[1]

Note 1: AcroPack carriers without provisions for the isolated power supplies can provide external power from the field power to the AcroPack module on pins 48, 49 and 50.

CARRIER ADDRESS ASSIGNMENT

Following are the instructions for setting the slot address of the carrier. By assigning a unique address to each carrier, system software can distinguish this carrier from other similarly configured carriers installed in a system. Figure 1 shows the location of switch SW1. Set the switch state as shown in Table 3 below to assign a unique slot address to this carrier. Note: switch positions are indicated on the switch. Factory default address is zero.

Table 3 Switch SW1 assignments

SW1 Position	Function	Factory Default
1	A0	On
2	A1	On
3	A2	On
4	A3	On
5	A4	On
6	Not used	N/A
7	Not used	N/A
8	Not used	N/A

ACROPACK MODULE INSTALLATION

Power should be removed from the carrier board when installing AcroPack modules, cables, termination panels, and field wiring. Refer to Figure 2 while reading this section. To install, first insert the edge of the AcroPack module into the carrier connector at an angle similar to that shown in the figure. Next, using a rocking motion while gently applying force to keep the edge of the board against the back of the carrier connector, position the module such that the field I/O connector is just above the mating connector. Verify that the two connectors are properly aligned. Once alignment is achieved, you can fully seat the connector. It will snap into place. Install two M2.5 screws as shown.

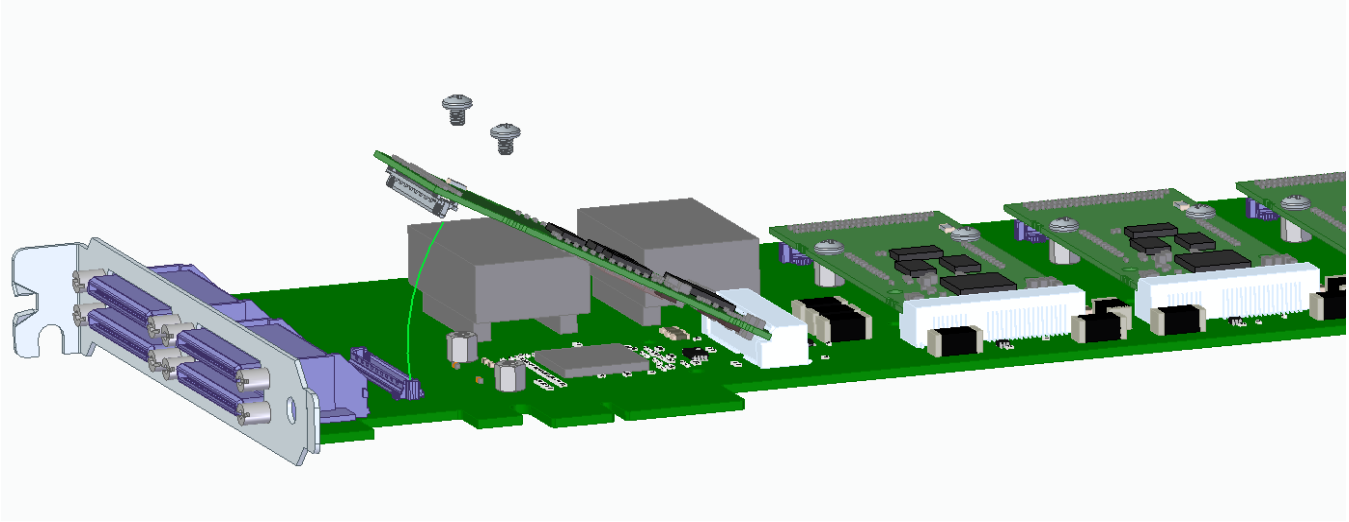


Figure 2 AcroPack Module Installation

FIELD GROUNDING CONSIDERATIONS

The Field I/O signals are isolated from chassis and system ground on the carrier. However, some non-isolated AcroPack modules connect Field I/O ground to system ground. Care should be taken in designing installations without isolation to avoid ground loops and noise pickup. This is particularly important for analog I/O applications when a high level of accuracy/resolution is needed (12-bits or more). Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the AcroPack input/output modules.

CONNECTORS

The APCe7040E-LF carrier uses four AcroPack module field I/O connectors, four mini-PCIe connectors, four field I/O connectors and one PCI Express bus interface connector. These are discussed in the following sections.

Front Panel Field I/O Connectors

Field I/O connections are made via two 68 pin, Stacked, 0.8 mm Champ cable connectors mounted on the front panel. The AcroPack module identifier (A to D) is marked on Figure 3 for easy identification. Cables and termination panels (or user defined terminations) can be quickly mated to the field I/O connectors. Pin assignments are defined by the installed AcroPack module.

Figure 3 Slots A to D Field I/O Connector Location

AcroPack Field I/O Connectors

The field side connector of AcroPack modules mate to Samtec SS5-50-3.00-L-D-K-TR socket connectors on the carrier board.

This provides excellent connection integrity due to the gold plating in the mating area. M2.5 screws and spacers provide additional stability for harsh environments.

The functions of each of the Field I/O signals are defined by the installed AcroPack model.

Table 4 Field I/O Pin Assignments

Carrier J4, J5 and Termination Panel	Carrier P2, P3, P5, and P6 Samtec SS5-50-3.00-L-D-K-TR	Module Pin Number	Field I/O Signal
1	2	2	Field I/O 1
35	1	1	Field I/O 2
	4	4	Reserved/isolation
	3	3	Reserved/isolation
2	6	6	Field I/O 3
36	5	5	Field I/O 4
	8	8	Reserved/isolation
	7	7	Reserved/isolation
3	10	10	Field I/O 5
37	9	9	Field I/O 6
	12	12	Reserved/isolation
	11	11	Reserved/isolation
4	14	14	Field I/O 7
38	13	13	Field I/O 8
	16	16	Reserved/isolation
	15	15	Reserved/isolation
5	18	18	Field I/O 9
39	17	17	Field I/O 10
	20	20	Reserved/isolation
	19	19	Reserved/isolation
6	22	22	Field I/O 11
40	21	21	Field I/O 12
	24	24	Reserved/isolation
	23	23	Reserved/isolation
7	26	26	Field I/O 13
41	25	25	Field I/O 14
	28	28	Reserved/isolation

Carrier J4, J5 and Termination Panel	Carrier P2, P3, P5, and P6 Samtec SS5-50-3.00-L-D-K-TR	Module Pin Number	Field I/O Signal
	27	27	Reserved/isolation
8	30	30	Field I/O 15
42	29	29	Field I/O 16
	32	32	Reserved/isolation
	31	31	Reserved/isolation
9	34	34	Field I/O 17
43	33	33	Field I/O 18
	36	36	Reserved/isolation
	35	35	Reserved/isolation
10	38	38	Field I/O 19
44	37	37	Field I/O 20
	40	40	Reserved/isolation
	39	39	Reserved/isolation
11	42	42	Field I/O 21
45	41	41	Field I/O 22
	44	44	Reserved/isolation
	43	43	Reserved/isolation
12	46	46	Field I/O 23
46	45	45	Field I/O 24
	48	48	Reserved/isolation
	47	47	Reserved/isolation
13	50	50	Field I/O 25
47	49	49	Field I/O 26
	52	52	Reserved/isolation
	51	51	Reserved/isolation
14	54	54	Field I/O 27
48	53	53	Field I/O 28
	56	56	Reserved/isolation
	55	55	Reserved/isolation
15	58	58	Field I/O 29
49	57	57	Field I/O 30
	60	60	Reserved/isolation
	59	59	Reserved/isolation
16	62	62	Field I/O 31
50	61	61	Field I/O 32

Carrier J4, J5 and Termination Panel	Carrier P2, P3, P5, and P6 Samtec SS5-50-3.00-L-D-K-TR	Module Pin Number	Field I/O Signal
	64	64	Reserved/isolation
	63	63	Reserved/isolation
17	66	66	Field I/O 33
51	65	65	Field I/O 34
	68	68	Reserved/isolation
	67	67	Reserved/isolation
18	70	70	Field I/O 35
52	69	69	Field I/O 36
	72	72	Reserved/isolation
	71	71	Reserved/isolation
19	74	74	Field I/O 37
53	73	73	Field I/O 38
	76	76	Reserved/isolation
	75	75	Reserved/isolation
20	78	78	Field I/O 39
54	77	77	Field I/O 40
	80	80	Reserved/isolation
	79	79	Reserved/isolation
21	82	82	Field I/O 41
55	81	81	Field I/O 42
	84	84	Reserved/isolation
	83	83	Reserved/isolation
22	86	86	Field I/O 43
56	85	85	Field I/O 44
	88	88	Reserved/isolation
	87	87	Reserved/isolation
23	90	90	Field I/O 45
57	89	89	Field I/O 46
	92	92	Reserved/isolation
	91	91	Reserved/isolation
24	94	94	Field I/O 47
58	93	93	Field I/O 48
	96	96	Reserved/isolation
	95	95	Reserved/isolation
25	98	98	Field I/O 49

Carrier J4, J5 and Termination Panel	Carrier P2, P3, P5, and P6 Samtec SS5-50-3.00-L-D-K-TR	Module Pin Number	Field I/O Signal
59	97	97	Field I/O 50
	100	100	Reserved/isolation
	99	99	Reserved/isolation

Mini-PCIe Connectors

The AcroPack Mini-PCIe connectors mate to TE Connectivity 1759457-1 connectors on the carrier board. AcroPack locations A to D are labeled on the board for easy identification.

Pin assignments for these connectors are based on the Mini-PCIe specification with the exceptions noted in Table 5.

Table 5 Mini-PCIe Connectors J1 and J2 Pin Assignments

Pin #	Name	Pin #	Name
51	**+5V**[3]	52	+3.3V[4]
49	**+12V**[3]	50	GND
47	**-12V**[3]	48	+1.5V
45	**Present**	46	N.C. (LED_WPAN#)[1]
43	GND	44	N.C. (LED_WLAN#)[1]
41	+3.3V[4]	42	N.C. (LED_WWAN#)[1]
39	+3.3V[4]	40	GND
37	GND	38	N.C. (USB_D+)[1]
35	GND	36	N.C. (USB_D-)[1]
33	PETp0	34	GND
31	PETn0	32	SMB_DATA[5]
29	GND	30	SMB_CLK[5]
27	GND	28	+1.5V
25	PERp0	26	GND
23	PERn0	24	+3.3V[4]
21	GND	22	PERST#
19	**TDI** (UIM_C4)[1,2]	20	N.C. (W_DISABLE#)[1]
17	**TDO** (UIM_C8)[1,2]	18	GND
15	GND	16	N.C. (UIM_VPP)[1]
13	RECLK+	14	N.C. (UIM_RESET)[1]
11	REFCLK-	12	N.C. (UIM_CLK)[1]
9	GND	10	N.C. (UIM_DATA)[1]
7	CLKREQ#	8	N.C. (UIM_PWR)[1]
5	**TCK** (COEX2)[1]	6	+1.5V
3	**TMS** (COEX1)[1]	4	GND
1	N.C. (WAKE#)[1]	2	+3.3V[4]

Notes:

1. The following mini-PCIe signals are not supported: USB_D+, USB_D-, WAKE#, LED_WPAN#, LED_WLAN#, LED_WWAN#, W_DISABLE#, COEX1, COEX2, UIM_C4, UIM_C8, UIM_VPP, UIM_RESET, UIM_CLK, UIM_DATA, UIM_PWR. The following signals UIM_C4, UIM_C8, COEX2 and COEX1 are repurposed for JTAG.
2. TDI is tied to TDO on modules that do not use JTAG.
3. +5, +12, and -12 Volt power supplies have been assigned to pins that are reserved in the mini-PCIe specification. Remove the fuses on these power supplies for mini-PCIe cards from other vendors that cannot tolerate power applied to these reserved pins (see Power and Cooling Considerations section for details).
4. All +3.3Vaux power pins are changed to system +3.3V power.
5. The SM bus signals SMB_CLK and SMB_DATA are used to communicate with a CPLD on the carrier that reports slot ID. These signals will be under the control of the AcroPack module.

PCI Express Bus Connections

Table 6 indicates the pin assignments for the PCIe bus signals at the card edge connector P1. Connector pins are designated by a letter and a number. The letter indicates which side of a particular connector the pin contact is on. “B” is on the top (component) side of the carrier board while “A” is on the bottom (solder side). Connector “gold finger” numbers increase with distance from the bracket end of the printed circuit board.

Refer to the PCI Express bus specification for additional information on the PCI Express bus signals.

Table 6 PCIe Bus P1 CONNECTIONS

Signal	Pin	Pin	Signal
+12V	B01	A01	PRSNT1*
+12V	B02	A02	+12V
+12V	B03	A03	+12V
GND	B04	A04	GND
SMCLK	B05	A05	TCK
SMDAT	B06	A06	TDI
GND	B07	A07	TDO
+3.3V	B08	A08	TMS
TRST*	B09	A09	+3.3V
+3.3Vaux[3]	B10	A10	+3.3V
WAKE*	B11	A11	PERST*
RSVD	B12	A12	GND
GND	B13	A13	REFCLKp
Tx0p	B14	A14	REFCLKn
Tx0n	B15	A15	GND
GND	B16	A16	Rx0p
N.C.	B17	A17	Rx0n
GND	B18	A18	GND

Signal	Pin	Pin	Signal
Tx1p	B19	A19	***RSVD***
Tx1n	B20	A20	GND
GND	B21	A21	Rx1p
GND	B22	A22	Rx1n
Tx2p	B23	A23	GND
Tx2n	B24	A24	GND
GND	B25	A25	Rx2p
GND	B26	A26	Rx2n
Tx3p	B27	A27	GND
Tx3n	B28	A28	GND
GND	B29	A29	Rx3p
RSVD	B30	A30	Rx3n
PRSNT2*	B31	A31	GND
GND	B32	A32	***RSVD***

Notes:

1. Asterisk (*) is used to indicate an active-low signal.
2. BOLD ITALIC Logic Lines are NOT USED by the carrier board.
3. +3.3Vaux power to AcroPacks is not used by the carrier. Contact Acromag to enable +3.3Vaux power to AcroPack modules. The carrier provides +3.3V power to the modules.

JTAG Programming/Debug Connector

A JTAG programming/debug connector is provided for developing applications that use Acromag's FPGA AcroPack modules. See reference designator P4 in Figure 1. This is a standard 14-pin Xilinx programming header for connecting a Xilinx Platform USB II programming device (or equivalent). The pin assignment for P4 is shown below. A bypass circuit is included that will detect a vacant AcroPack site and close a switch to bypass the TDI and TDO signals. A CPLD on the carrier is included in the JTAG chain. The Xilinx Vivado tools can detect the presence of the CPLD in the JTAG chain, and skip it when accessing the FPGAs on the AcroPack modules.

Table 7 JTAG Programming/Debug Connector Pin Assignment

Signal	Pin	Pin	Signal
N.C.[1]	1	2	_+3.3V
GND	3	4	TMS
GND	5	6	TCK
GND	7	8	TDO
GND	9	10	TDI
GND	11	12	N.C. [1]
N.C. [1]	13	14	N.C. [1]

Notes:

1. N.C. – not connected

TMS – **JTAG Test Mode Select**. This pin is the JTAG mode signal establishing appropriate TAP state transitions for target ISP devices sharing the same data stream.

TCK – **JTAG Test Clock**. This pin is the clock signal for JTAG operations and should be connected to the TCK pin on all target ISP devices sharing the same data stream.

TDO – **JTAG Test Data Out**. This pin is the serial data stream received from the TDO pin on the last device in a JTAG chain.

TDI – **JTAG Test Data In**. This pin outputs the serial data stream transmitted to the TDI pin on the first device in a JTAG chain.

+3.3V – The target reference voltage V_{REF} is 3.3 Volts

GND – Signal Return

3. PROGRAMMING INFORMATION

This APCe7040E-LF carrier board has no end user programmable components. The PCIe switch on the carrier is transparent to the end user.

4. THEORY OF OPERATION

This section describes the functionality of the circuitry used on the carrier board. Refer to Figure 4 as you read this section.

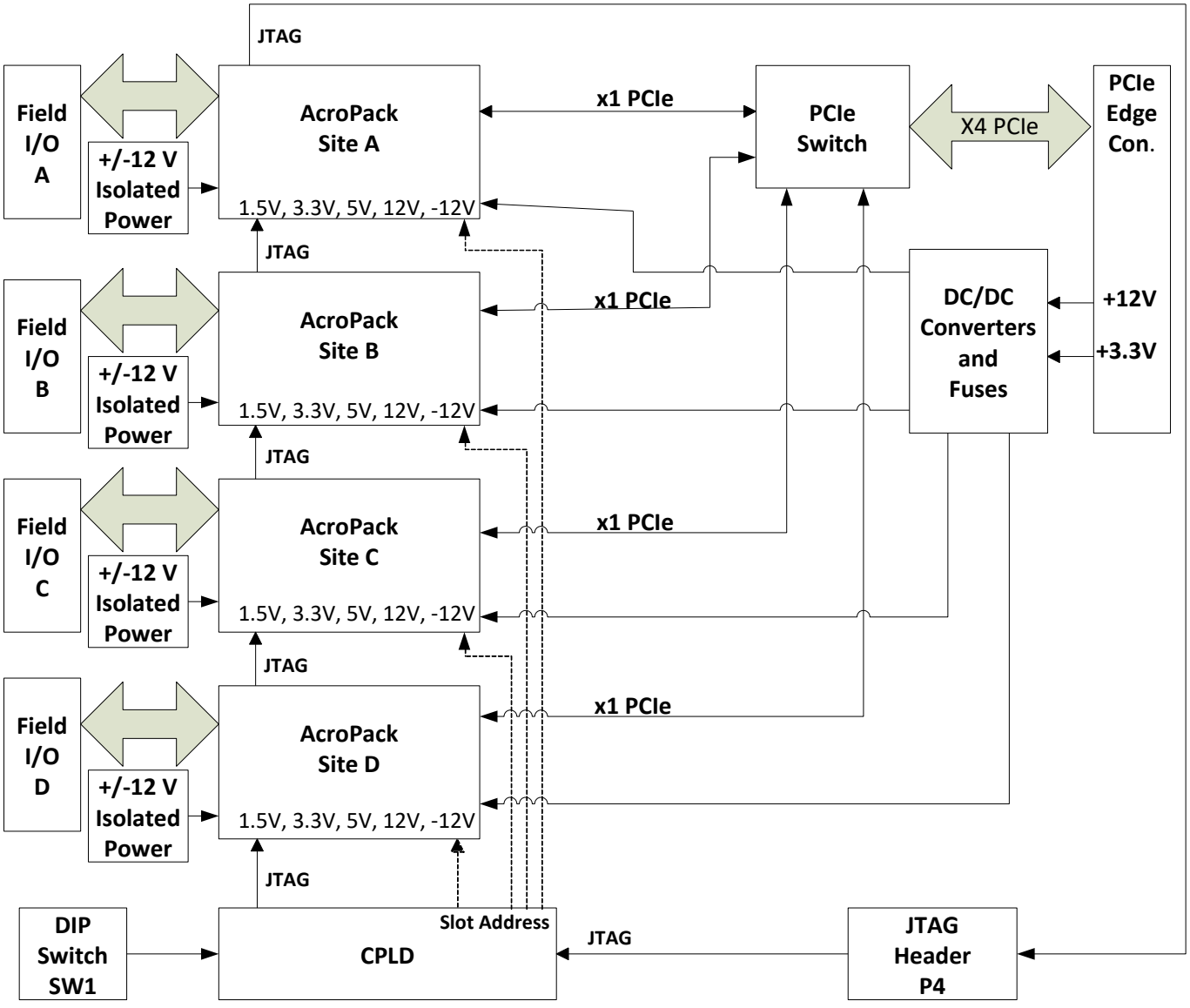


Figure 4 APCe7040E-LF AcroPack Carrier Block Diagram

PCIe Switch

The PCIe switch is a 6 port 8 lane PCIe Gen 2 switch. It expands the single host PCIe port to four ports, one for each AcroPack site. The host port consists of four PCIe lanes, each of the AcroPack sites have one lane each.

Important Note: The APCe7040E-LF board is not hot-swappable.

DC/DC Converter

The APCe7040E-LF has four DC/DC converters to provide the power supply voltages to the AcroPack modules that are not present at the host interface. The +1.5 Volt supply is sourced from the +3.3 Volt host power. The +3.3V Local, +5 Volt, and -12 Volt supplies are sourced from +12 Volt host power.

Slot Addressing

The APCe7040E-LF carrier can be assigned a slot address by selecting the appropriate combination of switch settings. The slot address is 8 bits long and consists of 3 bits to identify the site on the carrier where the AcroPack module is installed and 5 bits that are determined by the switch settings on the carrier. The CPLD will serialize the slot address and transmit the address to the AcroPack module as requested by the AcroPack module. The processes of reading the slot address is typically initiated by host software. See CARRIER ADDRESS ASSIGNMENT in section 2 for details regarding slot address selection.

JTAG

A JTAG interface is provided for programming and debugging FPGAs on AcroPack modules. It is intended to be used with a Xilinx Platform USB II programming device. A bypass circuit is included that will detect a vacant AcroPack site and close a switch to complete the JTAG chain. When four AcroPack modules with Xilinx FPGAs are installed on the carrier the module in slotD appears first in the chain followed by the module in slot C, B, and A. The slot address CPLD is also included in the JTAG chain for factory programming.

Power Supply Fuses

The power supplies to each AcroPack module are individually fused. A blown fuse can be identified by visible inspection or by use of an ohm meter. The location of the fuses are shown in Figure 1 Fuses corresponding to each voltage and AcroPack module are listed in section 2. The current rating for each of the fuses is listed in the Fuses paragraph in section 6.

5. SERVICE AND REPAIR

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. .

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Before beginning repair, be sure that all of the procedures in Section 2, PREPARATION FOR USE, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Verify that there are no blown fuses. Replacement of the carrier and/or AcroPack with one that is known to work correctly is a good technique to isolate a faulty board.

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at acromag.com. Our web site contains the most up-to-date product and software information.

Go to the "Support" tab to access:

- Application Notes/White Papers
- I/O Questions Answered

Acromag's application engineers can also be contacted directly for technical assistance via email or telephone through the contact information listed below. Note that an email question can also be submitted from within the "I/O Questions Answered" or directly from the "Contact Us" tab. When needed, complete repair services are also available.

- Email: solutions@acromag.com
- Phone: 248-295-0310

6. SPECIFICATIONS

PHYSICAL

Physical Configuration

Length (APCe7040E-LF).....12.283 inches (312.0 mm)
Height.....4.375 inches (111.12 mm)
Board thickness.....0.062" +/-0.006" (1.575 mm)
Max component height .....0.402 inches (10.21 mm)
Max component height under AcroPack modules
0. 0789 inches (2.00 mm)
Weight.....6.698 oz. (189.9 g)

Connectors

P1 (PCIe Bus).....PCI Express V2.1 x4 lane (PCIe Gen 2 Switch)
J4, 5 (Carrier Field I/O).....68-pin, Stacked, Champ (TE Connectivity 5787962)
P2, 3, 5, 6 (AcroPack Field I/O) .....100-pin socket (Samtec SS5-50-3.00-L-D-K-TR)
J2, 3, 6, 7 (Mini-PCIe) .....52-pin socket (TE Connectivity 1759547-1)
P4 (JTAG).....14-pin header (Molex 87832-1420)

Isolation

This AcroPack carrier is designed to provide isolation between the AcroPack Field I/O signals and the host. The AcroPack module must also be an isolated AcroPack module to maintain the isolation between the logic and field I/O signals. Unless isolation is provided on the AcroPack module itself, the field I/O connections are not isolated from the PCIe bus.

Host logic and field I/O are isolated from each other for voltages up to 250VAC or DC on a continuous basis (unit will withstand a 1500V AC dielectric strength test for one minute without breakdown). The carrier is designed to be used with isolated AcroPack modules.

The carrier also provides 100VAC or DC on a continuous basis between the signals of different AcroPack modules.

Due to the spacing between the pads of the 68-pin Champ connector and cable, the isolation between adjacent pins/signals on the front I/O is 30 V.

When this carrier is used with isolated AcroPack modules, both AcroPacks in slots A and B or C and D should be isolated AcroPacks. Non-isolated AcroPacks sharing the same Connector will compromise the isolation integrity of the other AcroPack.

Isolated Power

The use of an optional isolated DC/DC Converter is required for use with isolated Acromag AcroPack modules. See section 2 and Figure 1 for carrier board locations of the isolated DC/DC converters corresponding to each AcroPack module.

Compatible DC/DC isolated converter modules are listed below:
DELTA DH06S/D Series, 6 Watt (+/- 12 VDC +/- 250mA), DH06D1212A

XP Power JCE Series, 6 Watt (+/- 12 VDC +/- 250mA), JCE0612D12
TRACO POWER, TEN 6N Series, 6 Watt (+/-12 VDC +/-250mA), TEN 6-1222N

Power

Board power requirements are a function of the installed AcroPack modules. This specification below lists Current specified is for the APCe7040E-LF carrier board only.

+3.3 Volts (±5 %) 0.383 A Typical
+12 Volts (±8 %) 0.175 A Typical

Add the current for each of the AcroPack modules to calculate the total current required from each supply. The carrier is designed to provide the following voltage and currents to each AcroPack module.

Supply Voltage	Current (Max)
+12V +/- 8% (max)	0.5 A
-12V +/- 8% (max)	0.5 A
+5V +/- 5% (max)	0.5 A
+3.3V +/- 5% (max)	1.1 A^2
+1.5V +/- 5% (max)	0.5 A
+3.3Vaux +/- 9% (max)	100mA

The carrier board provides +1.5V, +3.3V, +5V, +12V and -12V power to each AcroPack module. The APCe7040E-LF utilizes DC/DC converters to generate the +3.3V, +5V and -12V supplies from the +12V. +12V power can be supplied either from the PCIe bus +12V supply or from the PCIe graphics power connector J1 (see top right corner of Figure 1). The +12V power source for the carrier is selected by jumper JP1.

The APCe7040E-LF also uses a DC/DC converter to generate the +1.5V supply from the +3.3V PCIe bus edge connector.

Jumpers

JP1.....Power source selection, PCIe card edge or PCIe graphics power connector.
.....The carrier confirms to the 25 Watt slot power supply rail requirements with +12V supply current 2.1 Amp (max) available from the PCIe Card Edge. The board PCIe Graphics Power connector ATX12V 2.x specification allows for a delivery capability of 75 W (six-pin connector) or 150 W (eight-pin connector). The recommended jumper configuration is with Jumper installed in position 2-3 (selecting external PCIe Graphics Power).

Fuses

Each AcroPack module supply line is individually fused. Note that the maximum amount of current provided to the carrier card via the PCIe bus varies with each system. Refer to your system documentation for more information on PCIe power specifications.

+1.5 .....1.1 Amps F6 (slot A), F12 (slot B), F18 (slot C), F24 (slot D)) Raychem NANOSMDC110F-2

+3.3V ..... 3 Amps F4 (slot A), F10 (slot B), F16 (slot C), F22 (slot D) Littelfuse 0466003.NR

+5V, +12V, -12V ..... 2 Amps F1(+12V), F2(+5V) and F3 (-12V) for slot A, F7(+12V), F8(+5V) and F9 (-12V) for slot B, F13(+12V), F14(+5V) and F15 (-12V) for slot C and F19(+12V), F20(+5V) and F21 (-12V) for slot D Littelfuse 0453002.MR

PCIe BUS COMPLIANCE

Specification.....This device meets or exceeds all written PCI Express specifications per revision 2.1. PCIe bus switch supports PCIe Gen 2 signals but rates exceed the rated bandwidth of the AcroPack connect.

ENVIRONMENTAL

Operating Temperature.....-40 to +85°C (with 200 LFM airflow)
Relative Humidity.....5-95% non-condensing
Storage Temperature.....-55 to +125°C.

EMC Compliance

The APCe7040E-LF is designed to comply with EMC Directive 2004/108/EC.

Immunity.....per EN 61000-6-2
Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2
Radiated Field Immunity (RFI), per IEC 61000-4-3
Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4
Surge Immunity, per IEC 61000-4-5
Conducted RF Immunity (CRFI), per IEC 61000-4-6

Emissions .....per EN61000-6-4
Enclosure Port, per CISPR 16
Low Voltage AC Mains Port, per CISPR 16
Note: This is a Class A product

Vibration and Shock Standard

The APCe7040E-LF is designed to pass the following Vibration and Shock standards.

Vibration, Sinusoidal Operating ...Designed to comply with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis

Vibration, Random Operating .....Designed to comply with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis

Shock, Operating.....Designed to comply with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3mS half sine, 18 shocks at 6 orientations for both test levels

Reliability Prediction

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled, G_BG_C*

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	1,546,707	176.6	646.5
40°C	1,000,619	114.3	999.4

[1] FIT is Failures in 10^9 hours.

MTBF based on APCe7043E-LF report

7. CERTIFICATE OF VOLATILITY

Certificate of Volatility					
Acromag Model APCe7040E-LF	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393				
Volatile Memory					
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) □ Yes ■ No					
Non-Volatile Memory					
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No					
Type (EEPROM, FLASH etc.) FLASH	Size: 1 Mbit	User Modifiable Yes	Function: PCIe switch configuration	Process to Sanitize: Overwrite FLASH contents.	
Acromag Representative					
Name: Russ Nieves	Title: Director of Sales and Marketing	Email: rnieves@acromag.com	Office Phone: 248-295-0838	Office Fax: 248-624-9234	

8. REVISION HISTORY

Release Date	Version	EGR/DOC	Description of Revision
27 FEB 2017	A	LMP/MJO	Initial Acromag release.
8-SEPT-2017	B	LMP/MJO	Figure 3 silk location updated
6-JAN-2022	C	LMP/AMM	Add MTBF Values