Series APC330, 16-Bit Analog Input Board PCI Bus

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The APC330 board is a precision 16-bit, high density, short size PCI board, with the capability to monitor 16 differential or 32 single-ended analog input channels. The APC330 utilizes state of the art Surface Mounted Technology (SMT) to achieve its high channel density. The APC330 offers a variety of features, which make it an ideal choice for many industrial and scientific applications as described below.

The APC330 boards are available in standard or extended temperature range as follows:

Model	Board Size (Length)	Operating Temperature Range
APC330	Short (6.600")	0 to 70°C
APC330E	Short (6.600")	-40 to 85°C

KEY APC330 FEATURES

- **A/D 16-Bit Resolution** - 16-bit capacitor-based successive approximation Analog to Digital Converter (ADC) with integral sample and hold and reference.
- **8µsec Conversion Time** - A maximum conversion rate of 125KHz is supported. Maximum recommended conversion rate for specified accuracy is 67KHz.
- **High Density** - Monitors up to 16 differential or 32 single-ended analog inputs (acquisition mode and channels are selected via programmable control registers).
- **Individual Channel Mail Box -** Two storage buffer registers are available for each of the 16 differential channels. If configured for 32 single-ended channels, one storage buffer register is available for each of the 32 channels.
- **Interrupt Upon Conversion Complete Mode** - May be programmed to interrupt upon completion of conversion for each individual channel or upon completion of conversion of the group of all scanned channels.
- **Programmable Control of Channel Scanning** - Scan all channels or a subset of the channels to allow an overall higher sample rate. The channels digitized include all

sequential channels beginning with a specified start-channel value and ending with a specified end-channel value.

- **User Programmable Interval Timer** - Controls the delay between each channel converted when Uniform-Continuous or Single Scan modes are selected. If Burst-Continuous is selected, the Interval Timer controls the delay after a group of channels are converted before conversion is initiated on the group again. Supports a minimum interval of 8μsec and a maximum interval of 2.09 seconds.
- **Uniform Continuous Scanning Mode** - All channels selected for scanning are continually digitized in a round robin fashion with the interval between conversions controlled by the programmed interval timer. The results of each conversion are stored in the channel's corresponding mail box buffer. Scanning is initiated by a software or external trigger. Scanning is stopped by software control.
- **Burst Continuous Scanning Mode** - All selected input scan channels are sequentially digitized at a 67KHz conversion rate (15μ second conversion time). At the end of a programmed interval time a new conversion of all channels is re-initiated. The conversion results are stored in each channel's mail box buffer. This mode can be used as a pseudo-simultaneous sampling mode for low to medium speed applications requiring simultaneous channel acquisition. For example, if four channels are selected then they could be pseudo-simultaneously converted every 60μ seconds (each of the channels actually takes 15μ seconds). This is repeated in bursts determined by the programmed interval time. The scan is initiated by a software or external trigger. Scanning is stopped by software control.
- **Uniform Single Cycle Scan Mode** - All channels selected for scanning are digitized once with the idle time between each channel conversion controlled by the programmed interval timer. The scan is initiated by a software or external trigger.
- **Burst Single Cycle Scan Mode** - All channels selected for scanning are digitized once at a 66.7KHz conversion rate (15μsec/Channel). The scan is initiated by a software or external trigger.
- **External Trigger Scan Mode** - A single channel is digitized with each external trigger. Successive channels are digitized in sequential order with each new external trigger. This mode allows synchronization of conversions with external events that are often asynchronous.
- **External Trigger Output** - The external trigger is assigned to a field I/O line. This external trigger may be configured as an output signal to provide a means to synchronize other APC330's or devices to a single APC330's on board timer reference.
- **User Programmable Gain Amplifier** - Provides independent software controlled gains (1, 2, 4, and 8V/V) for each of the 16 differential or 32 single-ended channels.
- **Precision On Board Calibration Voltages** - Calibration autozero and autospan precision voltages are available to permit host computer correction of conversion errors. Trimmed calibration voltages include: 0V (local analog ground), 4.9V, 2.45V, 1.225V, and 0.6125V.
- **Hardware DIP Switch For Selection of A/D Ranges** - Both bipolar (±5V, ±10V) and unipolar (0 to 5V and 0 to 10V) ranges are available. Selected range applies to all channels and can-not be individually selected on a per channel basis.
- **New Data Register** - This register can be polled, to indicate when new digitized data is available in the mail box. A set bit indicates a new digitized data value is available in the bit's corresponding mail box register. Register bits are cleared upon read of their corresponding mail box register or start of a new scan cycle.
- **Missed Data Register** - A set bit in the Missed Data register indicates that the last digitized value was not read by the host computer and has been overwritten by a new conversion. The Missed Data register has a bit corresponding to each of the 16 differential or 32 single-ended channels. Each Missed Data register bit is cleared by a read of its corresponding mail box data value or start of a new scan cycle.
- **User Programmable Data Output Format** - Software control provides selection of straight binary or binary two's complement data output format.
- **Fault Protected Input Channels** - Analog input overvoltage protection from -35 V to +55 V is provided in the event of power loss or power off.

PCI BUS INTERFACE FEATURES

- **Slave Module**- All read and write accesses are implemented as either a 32-bit, 16-bit or 8-bit single data transfer.
- **Immediate Disconnect on Read** - The PCI bus will immediately disconnect after a read. The read data is then stored in a read FIFO. Data in the read FIFO is then accessed by the PCI bus when the read cycle is retried. This allows the PCI bus to be free for other system operations while the read data is moved to the read FIFO.
- **Interrupt Support** - PCI bus INTA# interrupt request is supported. All board interrupts are mapped to INTA#. The APC330 board software programmable registers are utilized as interrupt request control and status monitors.

SIGNAL INTERFACE PRODUCTS
(See Appendix for more information on compatible products)

The APC330 field I/O is accessed from a SCSI-2 (50-pin) front panel connector. This board only supports front I/O access.

The cables and termination panels, described in the following paragraphs, are also available. For optimum performance with the 16-bit APC330 analog input module, use of the shortest possible length of shielded input cable is recommended.

Cables:

Model 5025-187 (SCSI-2 to Flat Ribbon Cable, Shielded): A round 50 conductor shielded cable with a male SCSI-2 connector at one end and a flat female ribbon connector at the other end. The cable is used for connecting the APC330 module to Model 5025-552 termination panels.

Termination Panel:

Model 5025-552: DIN-rail mountable panel provides 50 screw terminals for universal field I/O termination. Connects to Acromag APC330, via SCSI-2 to Flat Ribbon Cable, Shielded (Model 5028-187).

APC330 ActiveX CONTROL SOFTWARE

Acromag provides a software product (sold separately) consisting of APC330 ActiveX (Object Linking and Embedding) drivers for Windows 95® and newer compatible application programs (Model PMCSW-ATX). This software provides individual drivers that allow Acromag APC330 boards to be easily integrated into Windows® application programs, such as Visual

C++™, Visual Basic®, Microsoft® Office® applications and others. The ActiveX controls provide a high-level interface to APC330 boards, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the ActiveX controls. These functions consist of an ActiveX control for each Acromag PMC board (APC products use the corresponding PMC Module software).

APC330 VxWORKS SOFTWARE

Acromag provides a software product (sold separately) consisting of APC330 VxWorks® library. This software (Model PMCSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all Acromag PMC boards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag PMC boards (APC products use the corresponding PMC Module software).

APC330 QNX SOFTWARE

Acromag provides a software product (sold separately) consisting of APC330 QNX® library. This software (Model PCISW-API-QNX) is composed of QNX® (real time operating system) libraries for all Acromag PMC boards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag PMC boards (APC products use the corresponding PMC Module software).

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, Inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the APC330 board to within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

The board may be configured differently, depending on the application. All possible DIP switch positions will be discussed in the following sections. The DIP switch locations are shown in Drawing 4501-924.

Remove power from the APC330 board when configuring DIP switch postions, installing cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-924 and the following paragraphs for configuration and assembly instructions.

Default Hardware Jumper Configuration

When the board is shipped from the factory, it is configured as follows:

- Analog input range is configured for a bipolar input with a 10 volt span (i.e. an ADC input range of -5 to +5 Volts).
- The default programmable software control register bits at power-up are described in section 3. The control registers must be programmed to the desired gain, mode, and channel configuration before starting ADC analog input acquisition.

Analog Input Range Hardware Jumper Configuration

The ADC input range is programmed via hardware DIP switches. The DIP switches control the input voltage span and the selection of unipolar or bipolar input ranges. The configuration of the DIP switch for the different ranges is shown in Table 2.1. A switch selected as "ON" would be positioned to the side of the DIP labeled "ON". The DIP switch location is shown in Drawing 4501-924.

Table 2.1: Analog Input Range Selections/DIP Switch Settings

Desired ADC Input Range* (VDC)	Required Input Span (Volts)	Required Input Type	Switch Settings ON	Switch Settings OFF
-5 to +5	10	Bipolar	1,3,4,9	2,5,6,7,8
-10 to +10	20	Bipolar	2,5,6,9	1,3,4,7,8

0 to +5	5	Unipolar	1,3,5,8	2,4,6,7,9
0 to +10	10	Unipolar	1,3,4,7	2,5,6,8,9

* Assuming a gain of 1.

Software Configuration

Software configurable control registers are provided for control of external trigger mode, data output format, acquisition mode, timer control, interrupt mode, convert channel(s) selection, and channel gain selection. No hardware jumpers are required for control of these functions. These control registers must also be configured as needed for the application before starting ADC analog input acquisition. Refer to section 3 for programming details.

CONNECTORS

Front Panel Field I/O Connector P2

The front panel connector P2 provides the field I/O interface connections. P2 is a SCSI-2 50-pin female connector (AMP 787082-5 or equivalent) employing latch blocks and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the front panel via round shielded cable (Model 5028-187).

Front panel connector P2 pin assignments are shown in Table 2.2. When reading Table 2.2 note that channel designations are abbreviated to save space. For example, single ended channel 0 is abbreviated as “S00”; the +input for differential channel 0 is abbreviated as “D00+”. Both of these labels are attached to pin 1, but only one is active for a particular installation (i.e. if your inputs are applied differentially, which is recommended for the lowest noise and best accuracy, follow the differential channel labeling for each channel’s + and - input leads).

Table 2.2: APC330 Field I/O Pin Connections for P2

IMPORTANT: All unused analog input pins should be tied to analog ground. Floating unused inputs can drift outside the input range causing temporary saturation of the input analog circuits. Recovery from saturation is slow and affects the reading of the desired channels.

Pin Description	Number	Pin Description	Number
S00,D00+	1	S24,D08-	26
S16,D00-	2	COMMON	27
COMMON	3	S09,D09+	28
S01,D01+	4	S25,D09-	29
S17,D01-	5	COMMON	30
COMMON	6	S10,D10+	31
S02,D02+	7	S26,D10-	32
S18,D02-	8	COMMON	33
COMMON	9	S11,D11+	34
S03,D03+	10	S27,D11-	35
Pin Description	Number	Pin Description	Number
S19,D03-	11	COMMON	36
COMMON	12	S12,D12+	37
S04,D04+	13	S28,D12-	38
S20,D04-	14	COMMON	39
COMMON	15	S13,D13+	40
S05,D05+	16	S29,D13-	41
S21,D05-	17	SENSE	42
COMMON	18	S14,D14+	43
S06,D06+	19	S30,D14-	44
S22,D06-	20	N.C.*	45
COMMON	21	S15,D15+	46
S07,D07+	22	S31,D15-	47
S23,D07-	23	N.C.*	48
COMMON	24	EXT TRIGGER**	49
S08,D08+	25	SHIELD	50

***** Indicates no connection.
****** Indicates that the signal is active low.

Analog Inputs: Noise and Grounding Considerations

Differential inputs require two leads (+ and -) per channel, and provide rejection of common mode voltages. This allows the desired signal to be accurately measured. However, the signal being measured cannot be floating--it must be referenced to analog common on the APC330 board and be within the normal input voltage range.

Differential inputs are the best choice when the input channels are sourced from different locations having slightly different ground references and when minimizing noise and maximizing accuracy are key concerns. See Drawing 4501-921 for analog input connections for differential and single-ended inputs. Shielded cable of the shortest length possible is also strongly recommended.

Single-ended inputs only require a single lead (+) per channel, with a shared "sense" (reference) lead for all channels, and can be used when a large number of input channels come from the same location (e.g. printed circuit board). The channel density doubles when using single-ended inputs, and is a powerful incentive for their use. However, caution must be exercised since the single "sense" lead references all channels to the same common which will induce noise and offset to the degree they are different.

The APC330 is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the APC330 board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections. This is particularly important for analog inputs when a high level of accuracy/resolution is needed. Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the APC330 board.

External Trigger Input/Output

The external trigger signal on pin 49 of the front panel connector can be programmed as disabled, or to input a TTL compatible external trigger signal, or output APC330 hardware generated triggers to allow synchronization of multiple APC330s.

As an input, the external trigger must be a 5 Volt logic, TTL-compatible, debounced signal referenced to analog common. The external trigger signal is an active low edge sensitive signal. That is, the external trigger signal will trigger the APC330 hardware on the falling edge. Once the external trigger signal has been driven low, it should remain low for a minimum of 500n seconds.

As an output an active-low TTL signal can be driven to additional APC330s, thus providing a means to synchronize the

conversions of multiple APC330s. The additional APC330s must program their external trigger for signal input and convert on external trigger only mode. See section 3.0 for programming details to make use of this signal.

PCI Bus Connector P1

Table 2.3 indicates the pin assignments for the PCI bus signals at the card edge connector. Connector pins are designated by a letter and a number. The letter indicates which side of a particular connector the pin contact is on. "B" is on the component side of the carrier board while "A" is on the solder side. Connector "gold finger" numbers increase with distance from the bracket end of the printed circuit board.

Refer to the PCI bus specification for additional information on the PCI bus signals.

TABLE 2.3: PCI Bus P1 CONNECTIONS

Bracket End ↑

Signal	Pin	Pin	Signal
-12V	B01	A01	***TRST#***
TCK	B02	A02	***+12V***
Ground	B03	A03	***TMS***
TDO	B04	A04	TDI
+5V	B05	A05	+5V
+5V	B06	A06	INTA#
INTB#	B07	A07	***INTC#***
INTD#	B08	A08	+5V
PRSNT1#	B09	A09	***Reserved***
Reserved	B10	A10	+5V
PRSNT2#	B11	A11	***Reserved***
Ground	B12	A12	Ground
Ground	B13	A13	Ground
Reserved	B14	A14	***Reserved***
Ground	B15	A15	RST#
CLK	B16	A16	+5V
Ground	B17	A17	***GNT#***
REQ#	B18	A18	Ground
+5V	B19	A19	***Reserved***
AD[31]	B20	A20	AD[30]
AD[29]	B21	A21	***+3.3V***
Ground	B22	A22	AD[28]
AD[27]	B23	A23	AD[26]
AD[25]	B24	A24	Ground
+3.3V	B25	A25	AD[24]
C/BE[3]#	B26	A26	IDSEL
AD[23]	B27	A27	***+3.3V***
Ground	B28	A28	AD[22]
AD[21]	B29	A29	AD[20]
AD[19]	B30	A30	Ground
+3.3V	B31	A31	AD[18]
AD[17]	B32	A32	AD[16]
C/BE[2]#	B33	A33	***+3.3V***
Ground	B34	A34	FRAME#
IRDY#	B35	A35	Ground
+3.3V	B36	A36	TRDY#
DEVSEL#	B37	A37	Ground
Ground	B38	A38	STOP#
LOCK#	B39	A39	***+3.3V***
PERR#	B40	A40	***SDONE***
+3.3V	B41	A41	***SBO#***
SERR#	B42	A42	Ground
+3.3V	B43	A43	PAR
C/BE[1]#	B44	A44	AD[15]
AD[14]	B45	A45	***+3.3V***
Ground	B46	A46	AD[13]
AD[12]	B47	A47	AD[11]
AD[10]	B48	A48	Ground
Ground	B49	A49	AD[09]
KEYWAY			KEYWAY
KEYWAY			KEYWAY
AD[08]	B52	A52	C/BE[0]#
AD[07]	B53	A53	***+3.3V***
+3.3V	B54	A54	AD[06]
AD[05]	B55	A55	AD[04]
AD[03]	B56	A56	Ground
Ground	B57	A57	AD[02]
AD[01]	B58	A58	AD[00]
+5V	B59	A59	+5V
ACK64#	B60	A60	***REQ64#***
+5V	B61	A61	+5V
+5V	B62	A62	+5V

(#) s used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by this board.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the APC330 board.

This Acromag APC330 board complies with PCI Specification Version 2.2. It is a PCI bus slave board.

The PCI bus is defined to address three distinct address spaces: I/O, memory, and configuration space. The APC330 board can be accessed via the PCI bus memory space and configuration spaces only.

The PCI card's configuration registers are initialized by system software at power-up to configure the card. The PCI board is a Plug-and-Play card. As a Plug-and-Play card the board's base address and system interrupt request line are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCI bus configuration access is used to access a PCI card's configuration registers.

PCI Configuration Address Space

When the computer is first powered-up, the computer's system configuration software scans the PCI bus to determine what PCI devices are present. The software also determines the configuration requirements of the PCI card.

The system software accesses the configuration registers to determine how many blocks of memory space the board requires. It then programs the boards configuration registers with the unique memory address range assigned.

The configuration registers are also used to indicate that the PCI board requires an interrupt request line. The system software then programs the configuration registers with the interrupt request line assigned to the PCI board.

Since this PCI board is re-locatable and not hardwired in address space, this board's mapping and IRQ information is stored in the board's Configuration Space registers.

Configuration Registers

The PCI specification requires software driven initialization and configuration via the Configuration Address space. This board provides 256 bytes of configuration registers for this

purpose. The APC330 contains the configuration registers, shown in Table 3.1, to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers and the Interrupt Line Register which must be read to determine the base address assigned to the APC330 and the interrupt request line that goes active on an APC330 interrupt request.

Table 3.1 Configuration Registers

Reg. Num.	D31 D24	D23 D16	D15 D8	D7 D0
0	Device ID=4B47		Vendor ID= 16D5	
1	Status		Command	
2	Class Code=118000			Rev ID=00
3	BIST	Header	Latency	Cache
4	32-bit Memory Base Address for APC330 4K-Byte Block			
5 : 10	Not Used			
11	Subsystem ID=0000		Subsystem Vendor ID=0000	
12	Not Used			
13,14	Reserved			
15	Max_Lat	Min_Gnt	Inter. Pin	Inter. Line

MEMORY MAP

This board is allocated a 4K byte block of memory that is addressable in the PCI bus memory space to control the acquisition of analog inputs from the field. As such, three types of information are stored in the memory space: control, status, and data.

The memory space address map for the APC330 is shown in Table 3.2. Note that the base address for the APC330 in memory space must be added to the addresses shown to properly access the APC330 registers. Register accesses as 32, 16, and 8-bit data in memory space are permitted. All the registers of the APC330 are accessed via data lines D0 to D15. The most significant word of a 32-bit access is not used by the APC330. A 32-bit read will return logic “0” for the most significant word.

Table 3.2: APC330 Memory Map[2]

Base Addr+	MSB D15 D08	LSB D07 D00	Base Addr+
01	Interrupt Register		00
05	Control Register		04
09	Timer Prescaler		08
0D	Conversion Timer		0C
11	End Channel Value	Start Channel Value	10
15	New Data Register Channels 0 to 15		14
19	New Data Register Channels 16 to 31		18
1D	Missed Data Register Channels 0 to 15		1C
21	Missed Data Register Channels 16 to 31		20
25	Not Used Bits15 to Bit 01	Start Convert Bit-0	24
29	Not Used[1]		28
	↓		
3D	Not Used[1]		3C
41	Gain Select Register Channels 0 to 7		40
45	Gain Select Register Channels 8 to 15		44
49	Gain Select Register Channels 16 to 23		48
4D	Gain Select Register Channels 24 to 31		4C
51	Not Used[1]		50
	↓		
7D	Not Used[1]		7C
81	Mail Box Ch 00 (SE or Diff. Mode)[3]		80
85	Mail Box Ch 01 (SE or Diff. Mode)		84
89	Mail Box Ch 02 (SE or Diff. Mode)		88
8D	Mail Box Ch 03 (SE or Diff. Mode)		8C
91	Mail Box Ch 04 (SE or Diff. Mode)		90
95	Mail Box Ch 05 (SE or Diff. Mode)		94
99	Mail Box Ch 06 (SE or Diff. Mode)		98
9D	Mail Box Ch 07 (SE or Diff. Mode)		9C
A1	Mail Box Ch 08 (SE or Diff. Mode)		A0
A5	Mail Box Ch 09 (SE or Diff. Mode)		A4
A9	Mail Box Ch 10 (SE or Diff. Mode)		A8
AD	Mail Box Ch 11 (SE or Diff. Mode)		AC
B1	Mail Box Ch 12 (SE or Diff. Mode)		B0
B5	Mail Box Ch 13 (SE or Diff. Mode)		B4
B9	Mail Box Ch 14 (SE or Diff. Mode)		B8
BD	Mail Box Ch 15 (SE or Diff. Mode)		BC
C1	Mail Box Ch 16 SE (Ch 00 Diff. Mode)[3]		C0
C5	Mail Box Ch 17 SE (Ch 01 Diff. Mode)		C4
C9	Mail Box Ch 18 SE (Ch 02 Diff. Mode)		C8
CD	Mail Box Ch 19 SE (Ch 03 Diff. Mode)		CC
D1	Mail Box Ch 20 SE (Ch 04 Diff. Mode)		D0
D5	Mail Box Ch 21 SE (Ch 05 Diff. Mode)		D4
D9	Mail Box Ch 22 SE (Ch 06 Diff. Mode)		D8
DD	Mail Box Ch 23 SE (Ch 07 Diff. Mode)		DC
E1	Mail Box Ch 24 SE (Ch 08 Diff. Mode)		E0
E5	Mail Box Ch 25 SE (Ch 09 Diff. Mode)		E4
E9	Mail Box Ch 26 SE (Ch 10 Diff. Mode)		E8
ED	Mail Box Ch 27 SE (Ch 11 Diff. Mode)		EC
F1	Mail Box Ch 28 SE (Ch 12 Diff. Mode)		F0
F5	Mail Box Ch 29 SE (Ch 13 Diff. Mode)		F4
F9	Mail Box Ch 30 SE (Ch 14 Diff. Mode)		F8
FD	Mail Box Ch 31 SE (Ch 15 Diff. Mode)		FC
101	Not Used[1]		100
	↓		
FFD	Not Used[1]		FFC

Notes (Table 3.2):

1. The APC330 will return 0 for all addresses that are "Not Used".
2. All Reads and writes are 8 clock cycles (except a Mail Box read issued simultaneously with an ongoing hardware write of a new convert value. In this case a read cycle will disconnect without data and will return data on a retry).
3. The Mail Box is one level deep when using single ended channels; it is two levels deep with differential mode.

This memory map reflects byte accesses using the “Little Endian” byte ordering format. Little Endian uses even-byte addresses to store the low-order byte. The Intel x86 family of

microprocessors uses “Little Endian” byte ordering. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses.

Interrupt Register, (Read/Write) - (Base + 00H)

This read/write register is used to enable board interrupt, determine the pending status of interrupts, and release an interrupt.

The function of each of the interrupt register bits are described in Table 3.3. This register can be read or written with either 8-bit or 16-bit data transfers. A power-up or system reset sets all interrupt register bits to 0.

Table 3.3: Interupt Register

BIT	FUNCTION
0	Board Interrupt Enable Bit. This bit must be set to logic “1” to enable generation of interrupts from the APC330. Setting this bit to logic “0” will disable board interrupts. (Read/Write Bit)
1	Interrupt Pending Status Bit. This bit can be read to determine the interrupt pending status of the APC330. When this bit is logic “1” an interrupt is pending and will cause an interrupt request if bit-0 of the register is set. When this bit is a logic “0” an interrupt is not being requested.
14 to 2	Not Used[1]
15	Interrupt Release Bit. This bit must be set to a logic “1” to release an interrupt request. This bit is typically set in the interrupt service routine to remove the interrupt request. Once an interrupt request is generated on the APC330, it will continue to assert the interrupt request until this Interrupt Release bit is set to logic “1” or interrupts are disabled via bit 0 of this register.

Notes (Table 3.3):

1. All bits labeled “Not Used” will return logic “0” when read.

Control Register, (Read/Write) - (Base + 04H)

This read/write register is used to select the output data format, select the external trigger signal as an input or output, select acquisition input mode, select scan mode, enable/disable the timer, and select the interrupt mode.

The function of each of the control register bits are described in Table 3.4. This register can be read or written with either 8-bit or 16-bit data transfers. A power-up or system reset sets all control register bits to 0.

Table 3.4: Control Register

BIT	FUNCTION
0	Output Data Format 0 = Binary Two’s Complement 1 = Straight Binary See Tables 3.5 and 3.6 for a description of these two data formats.
2,1	External Trigger 00, 11 = Disabled 01 = Input 10 = Output It is possible to synchronize the data acquisition of multiple APC330 modules. A single master APC330 module must be selected to output the external trigger signal while all other APC330 modules are selected to input the external trigger signal. The external trigger signals (pin 49 of the front panel field I/O connector) must also be wired together for all synchronized modules. The External Trigger input could be sensitive to external EMI noise, which can cause erroneous external triggers. If External Trigger input or output is not required, the External Trigger should be configured as Disabled.
5,4,3	Acquisition Input Mode 000 = All Channels Differential Input 001 = All Channels Single Ended Input 010 = Not Used 011 = 4.9000v Calibration Voltage Input 100 = 2.4500v Calibration Voltage Input 101 = 1.2250v Calibration Voltage Input 110 = 0.6125v Calibration Voltage Input 111 = Auto Zero Calibration Voltage Input
7,6	Not Used[1]
10,9,8	Scan Mode 000 = Disable 001 = Uniform Continuous 010 = Uniform Single 011 = Burst Continuous 100 = Burst Single 101 = Convert on External Trigger Only 110 = Not Used 111 = Not Used See the Modes of Operation section for a description of each of these scan modes.
11	Timer Enable 0 = Disable 1 = Enable
13,12	Interrupt Control 00 = Disable Interrupts 01 = Interrupt After Convert of Each Channel 10 = Interrupt After Conversion of all selected channels is completed. A group of channels includes all channels from the Start Channel up to and including the End Channel value. 11 = Disable Interrupts
14,15	Not Used[1]

Notes (Table 3.4):

1. All bits labeled “Not Used” will return logic “0” when read.

Analog Input Ranges and Corresponding Digital Output Codes

Selection of an analog input range is implemented via the DIP switch settings given in Table 2.1. The ideal input voltage corresponding to each of the supported input ranges is given in

Table 3.5. In Table 3.6 the digital output code corresponding to each of the given ideal analog input values is given in both binary two's complement and straight binary formats.

Table 3.5: Supported Full-Scale Ranges and Ideal Analog Input

DESCRIPTION	ANALOG INPUT			
Input Range	±10V	0 to 10V	±5V	0 to 5V
LSB (Least Significant Bit) Weight	305μV	153μV	153μV	76μV
+ Full Scale Minus One LSB	9.999695 Volts	9.999847 Volts	4.999847 Volts	4.999924 Volts
Midscale	0V	5V	0V	2.5V
One LSB Below Midscale	-305μV	4.999847 Volts	-153μV	2.499924 Volts
- Full Scale	-10V	0V	-5V	0V

The digital output format is controlled by bit-0 of the Control register. The two formats supported are Binary Two's Complement and Straight Binary. The hex codes corresponding to these two data formats are depicted in Table 3.6.

Table 3.6: Digital Output Codes and Input Voltages

DESCRIPTION	DIGITAL OUTPUT	
	Binary 2's Comp (Hex Code)	**Straight Binary** (Hex Code)
+ Full Scale - 1 LSB	7FFF	FFFF
Midscale	0000	8000
1 LSB Below Midscale	FFFF	7FFF
- Full Scale	8000	0000

Timer Prescaler Register (Read/Write, 09H)

The Timer Prescaler register can be written with an 8-bit value to control the interval time between conversions.

Timer Prescaler Register							
MSB							LSB
15	14	13	12	11	10	09	08

This 8-bit number divides an 8 MHz clock signal. The clock signal is further divided by the number held in the Conversion Timer Register. The resulting frequency can be used to generate periodic triggers for precisely timed intervals between conversions.

The Timer Prescaler has a minimum allowed value restriction of 40 hex or 64 decimal. A Timer Prescaler value of less then 64 (decimal) will result in an empty Mail Box Register buffer. This minimum value corresponds to a conversion interval of 8μ seconds which translates to the maximum conversion rate of 125KHz. Although the board will operate at the 125KHz conversion rate, conversion accuracy will be sacrificed.

The formula used to calculate and determine the desired Timer Prescaler value is given in the Conversion Timer section which immediately follows.

Read or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers. The Timer Prescaler register contents are cleared upon reset.

Conversion Timer Register (Read/Write, 0CH)

The Conversion Timer Register can be written to control the interval time between conversions. Read or writing to this register is possible with either 32-bit, 16-bit or 8-bit data transfers. This register's contents are cleared upon reset.

Conversion Timer Register	
MSB	LSB
15 14 13 12 11 10 09 08	07 06 05 04 03 02 01 00

This 16-bit number is the second divisor of an 8MHz. clock signal and is used together with the Timer Prescaler Register to derive the frequency of periodic triggers for precisely timed intervals between conversions.

The interval time between conversion triggers is generated by cascading two counters. The first counter, the Timer Prescaler, is clocked by an 8MHz. clock signal. The output of this clock is input to the second counter, the Conversion Timer, and the output is used to generate periodic trigger pulses. The time period between trigger pulses is described by the following equation:

$$\frac{\text{Timer Prescaler} * \text{Conversion Timer}}{8} = \text{T in } \mu\text{seconds}$$

Where: **T** = time period between trigger pulses in microseconds.
Timer Prescaler can be any value between 64 and 255 decimal.
Conversion Timer can be any value between 1 and 65,535 decimal.

The maximum period of time which can be programmed to occur between conversions is (255 * 65,535) ÷ 8 = 2.0889 seconds. The minimum time interval which can be programmed to occur is (64 * 1) ÷ 8 = 8μ seconds. This minimum of 8μ seconds is defined by the minimum conversion time of the hardware but does sacrifice conversion accuracy. To achieve specified conversion accuracy a minimum conversion time of 15μ seconds is recommended (see the specification chapter for details regarding accuracy).

Start Channel Value Register (Read/Write, 10H)

The Start Channel Value register must be written to set the first channel that is to be converted once conversions have been triggered. All channels between the start and end channel values are converted. A single channel can be selected by writing the desired channel value in both the Start and End Channel Value registers.

The Start Channel Value register can be read or written with 8-bit data transfers. In addition, the Start Channel Value register can be simultaneously accessed with the End Channel Value via a 32-bit or 16-bit data transfer. The unused bits are zero when read. The register contents are cleared upon reset.

Start Channel Value Register	
Unused	Start Channel Value

07	06	05	04	03	02	01	00

After data conversions are halted, the internal hardware pointers are reinitialized to the start channel value. Thus, when conversions are started again, the first channel converted is defined by the Start Channel Value register.

End Channel Value Register (Read/Write, 11H)

The End Channel Value register must be written to indicate the last channel in a sequence to be converted. When scanning, all channels between and including the start and end channels are converted. A single channel can be selected by writing the desired channel value in both the Start and End Channel Value registers.

The End Channel Value register can be read or written with 8-bit data transfers. In addition, the End Channel Value register can be simultaneously accessed with the Start Channel Value with a 32-bit or 16-bit data transfer. The unused data bits are zero when read. The register contents are cleared upon reset.

End Channel Value Register							
Unused			End Channel Value				
15	14	13	12	11	10	09	08

New Data Registers (Read Only, 14H to 19H)

The New Data registers can be read to determine which channels of the Mail Box buffer contain new converted data. A set bit in the New Data register indicates that the Mail Box buffer, corresponding to the channel of the set bit, contains new converted data. A set New Data register bit is cleared upon a read of its corresponding Mail Box buffer.

The New Data bits are also cleared at the start of all new data acquisition cycles initiated with either the Software Start Convert command or an external trigger. This is done to avoid mistaking data from an old scan cycle with that of a new scan cycle.

The New Data registers can be read via 32-bit, 16-bit or 8-bit data transfers. In addition, the register contents are cleared upon reset.

New Data Register (Read Only, 14H)								
Data Bit	07	06	05	04	03	02	01	00
SE or Diff. Ch. I	07	06	05	04	03	02	01	00
New Data Register (Read Only 15H)								
Data Bit	15	14	13	12	11	10	09	08
SE or Diff. Ch.	15	14	13	12	11	10	09	08
New Data Register (Read Only 18H)								
Data Bit	07	06	05	04	03	02	01	00
SE Channel	23	22	21	20	19	18	17	16
Diff. Channel	07	06	05	04	03	02	01	00
New Data Register (Read Only 19H)								
Data Bit	15	14	13	12	11	10	09	08
SE Channel	31	30	29	28	27	26	25	24
Diff. Channel	15	14	13	12	11	10	09	08

Missed Data Registers (Read Only, 1CH to 21H)

The Missed Data registers can be read to determine if a channel's Mail Box buffer has been overwritten with new converted data before the last converted value was read. A set bit in the Missed Data register indicates a converted value corresponding to the channel of the set bit was overwritten before being read. A set Missed Data register bit is cleared upon a read of its corresponding Mail Box buffer.

The Missed Data bits are also cleared at the start of all new data acquisition cycles initiated with either the Software Start Convert command or an external trigger. This is done to avoid mistaking missed data from an old scan cycle with that of a new scan cycle.

The Missed Data registers can be read via 32-bit, 16-bit or 8-bit data transfers. In addition, the register contents are cleared upon reset.

Missed Data Register (Read Only, 1CH)								
Data Bit	07	06	05	04	03	02	01	00
SE or Diff. Ch.	07	06	05	04	03	02	01	00
Missed Data Register (Read Only 1DH)								
Data Bit	15	14	13	12	11	10	09	08
SE or Diff. Ch.	15	14	13	12	11	10	09	08
Missed Data Register (Read Only 20H)								
Data Bit	07	06	05	04	03	02	01	00
SE Channel	23	22	21	20	19	18	17	16
Diff. Channel	07	06	05	04	03	02	01	00
Missed Data Register (Read Only 21H)								
Data Bit	15	14	13	12	11	10	09	08
SE Channel	31	30	29	28	27	26	25	24
Diff. Channel	15	14	13	12	11	10	09	08

Start Convert Register (Write Only, 24H)

The Start Convert register is a write-only register and is used to trigger conversions by setting data bit-0 of this register to a logic one. The desired mode of data acquisition must first be configured by setting the following registers to the desired values and modes: Control, Interrupt Vector, Timer Prescaler, Conversion Timer, Start Channel Value, End Channel Value, and Gain Select.

This register can be written with either a 32-bit, 16-bit or 8-bit data value. Data bit-0 must be a logic one to start data conversions.

For the External Trigger Only mode the Software Start Convert bit is not used to start data acquisition. However, the

Start Convert bit should be set prior to the first external trigger. In this mode the Start Convert bit serves as a means for the hardware to identify the occurrence of the first External Trigger. On the first external trigger (given the Software Start Convert bit is set) converted data from the A/D Converter is not written to the Mail Box buffer since it is old convert data. See the Convert On External Trigger Only-Mode (in the Modes of Operation section) for additional details.

Start Convert Register	
Not Used	Start Convert
Bits 15 to 01	Bit 00

At least 5μ seconds of data acquire time should be provided after programming of the Control register, Start Value register, and Gain Selects before a Software Start Convert command is issued. These configuration registers control the APC330 on board multiplexers and programmable gain amplifier which, respectively, control the channel and gain selected for the input provided to the converter.

Gain Select Registers (Read/Write, 40H – 4DH)

The Gain Select registers are read/writeable and are used to individually select the gain corresponding to each of the 32 channels. See Table 3.2 which lists the Gain Select register addresses corresponding to each of the 32 channels. In differential mode, only Gain Select registers corresponding to channels 0 to 15 are utilized.

The four gain settings supported (1, 2, 4, and 8) are listed in Table 3.7 with their corresponding binary select code. A gain can be selected by writing the desired binary code to the required two bits corresponding to each channel as shown in Table 3.8

Table 3.7: Gain Select Binary Codes

Gain	Binary Code
1	00
2	01
4	10
8	11

Table 3.8 Gain Select Registers

Reg Adr	D15	D12	D11	D8	D7	D4	D3	D0
40	Ch 07	Ch 06	Ch 05	Ch 04	Ch 03	Ch 02	Ch 01	Ch 00
44	Ch 15	Ch 14	Ch 13	Ch 12	Ch 11	Ch 10	Ch 09	Ch 08
48	Ch 23	Ch 22	Ch 21	Ch 20	Ch 19	Ch 18	Ch 17	Ch 16
4C	Ch 31	Ch 30	Ch 29	Ch 28	Ch 27	Ch 26	Ch 25	Ch 24

The Gain Select registers corresponding to all channels selected for conversion must be written with the desired gain select binary codes prior to initializing data conversions.

The Gain Select registers can be read or written via 32-bit, 16-bit or 8-bit data transfers. The contents of these registers are cleared upon reset.

Mail Box Buffer (Read Only, 80H - FDH)

The Mail Box Buffer is read-only, and contains 16-bit digitized input channel values. The Mail Box Buffer has 32 storage locations-one for each of the 32 channels supported by the APC330 in the single ended mode of operation. If the APC330 is used in the differential mode of operation each of the 16 channels supported are allocated two Mail Box Buffer locations.

See Table 3.2 which gives the Mail Box Buffer address locations corresponding to each of the 32 channels (or 16 channels in differential mode). In differential mode the first digitized data values will be stored in buffer locations 80H to BDH while the second digitized values are stored in buffer locations C0H to FDH. The storage of data in the Mail Box, in differential mode will, continue to alternate between these two Mail Box sections.

The New Data register can be read to determine which Mail Box Buffers contain updated digitized data. A set bit in the New Data register indicates an updated digitized data value resides in its corresponding Mail Box Buffer. In addition, the Missed Data register can be read to determine if a Mail Box Buffer has been overwritten with a new digitized value before the previous one had been read. A set bit in the Missed Data register indicates that a digitized data value has been overwritten.

All register accesses to the APC330 require 8 PCI clock cycles with the exception of a read access to the Mail Box Buffer. A read access to the Mail Box Buffer will typically be executed in 8 PCI clock cycles. However, on occasion the access will encounter a retry termination if a read is issued while a hardware write to the same Mail Box is currently underway. A retry termination forces the PCI master that initiated the read to retry the same read again.

MODES OF OPERATION

The APC330 provides five different modes of analog input acquisition to give the user maximum flexibility for each application. These modes of operation include: uniform continuous, uniform single, burst continuous, burst single, and convert on external trigger only. In all modes, a single channel or a sequence of channels may be converted. The following sections describe the features of each and how to best use them.

Uniform Continuous-Mode

In uniform continuous mode of operation, conversions are performed continuously (in sequential order) for all channels between and including the Start and End Channel Values. The interval between conversions is controlled by the interval timer (Timer Prescaler and Conversion Timer as described in the Conversion Timer Register section). The interval timer must be used in this mode of operation.

After software selection of the uniform continuous mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit. If the external trigger is to be used bits 2 and 1 of the Control register must be set “01” to accept the external trigger as an input signal.

Stopping the execution of uniform continuous conversions is possible by writing 000 to the Scan Mode bits (10-8) of the Control register. See the Control register section for additional information on the Scan Mode control bits and the Control register board address location.

When configured for differential input, the Mail Box functions as a dual level data buffer. The first half of the Mail Box is used to store all selected channel data for the initial pass through the channels defined by the Start and End Value registers. The second half of the Mail Box is then used to store the channel data corresponding to the second pass though all selected channels. Storage of channel data continues to alternate between the first and second halves of the Mail Box Buffer. As seen in Table 3.2, the first half of the Mail Box is defined by word addresses 80H to BDH while the second half is defined by word addresses C0H to FDH.

Interrupts can be enabled to activate after conversion of each channel or the group of channels defined by the Start and End Channel Values. If interrupts are configured to go active after the conversion of each channel, the actual interrupt will be issued 8μ seconds after the programmed interval has lapsed. If interrupt upon completion of a group of channels is selected, the interrupt will be issued 8μ seconds after the interval time of the last selected channel has expired.

If interrupts are selected to go active after conversion of each channel be sure to program a large enough interval between conversions to allow adequate time for execution of an interrupt service routine. It may also be necessary to allow time for your computer to perform other housekeeping operations between servicing interrupts.

Uniform Single-Mode

In uniform single mode of operation, conversions are performed once (in sequential order) for all channels between and including the Start and End Channel Values. The interval between conversions is controlled by the interval timer (Timer Prescaler and Conversion Timer as described in the Conversion Timer Register section). The interval timer must be used in this mode of operation.

After software selection of the uniform single mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit. If the external trigger is to be used bits 2 and 1 of the Control register must be set ”01” to accept the external trigger as an input signal.

When configured for differential input, the Mail Box functions as a dual level data buffer. However, for Uniform Single Mode, only one pass from the start channel to the end channel is implemented. Thus, only the first half of the Mail Box buffer is utilized. As seen in Table 3.2, the first half of the Mail Box is defined by word addresses 80H to BDH

Interrupts can be enabled to activate after conversion of each channel or the group of channels as defined by the Start and End Channel Values. If interrupts are configured to go active after the conversion of each channel, the actual interrupt will be issued 8μ seconds after the programmed interval has lapsed. If interrupt upon completion of a group of channels is selected, the interrupt will be issued 8μ seconds after the interval time of the last selected channel has expired.

Burst Continuous-Mode

In burst continuous mode of operation, conversions are continuously performed in sequential order from the channel defined by the Start Channel Value to the channel defined by the End Channel Value. Within a group of channels, the interval between conversions is fixed at 15μ seconds. However, the interval after conversion of a group of channels can be controlled by the interval timer (Timer Prescaler and Conversion Timer).

Burst modes can be used to provide pseudo-simultaneous sampling for many low to medium speed applications requiring simultaneous channel acquisition. The 15μ seconds between conversions of each channel can essentially be considered simultaneous sampling for low to medium frequency applications.

After software selection of the burst continuous mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit. If the external trigger is to be used bits 2 and 1 of the Control register must be set to “01” to accept the external trigger as an input signal.

Stopping the execution of burst continuous conversions is accomplished by writing 000 to the Scan Mode bits (10-8) of the Control register. See the Control register section for additional information on the Scan Mode control bits and the Control register board address location.

When configured for differential input, the Mail Box functions as a dual level data buffer. The first half of the Mail Box is used to store all selected channel data for the initial pass through the channels defined by the Start and End Value registers. The second half of the Mail Box is then used to store the channel data corresponding to the second pass though all selected channels. Storage of channel data continues to alternate between the first and second halves of the Mail Box Buffer. As seen in Table 3.2, the first half of the Mail Box is defined by word addresses 80H to BDH while the second half is defined by word addresses C0H to FDH.

Interrupts can be enabled to activate after conversion of each channel or the group of channels as defined by the Start and End Channel Values. If interrupts are configured to go active after the conversion of each channel, the actual interrupt will be issued every 15μ seconds. If interrupt upon completion of a group of channels is selected, the interrupt will be issued 23μ seconds after conversion of the last channel in the group has started.

At the time of this writing, 15μ seconds between interrupts is not sufficient time to perform back to back interrupt acknowledge cycles on the PCI platforms. Thus, interrupting after each channel is converted is not recommended.

Burst Single-Mode

In burst single mode of operation conversions are performed once for all channels (in sequential order) starting with the Start Channel and ending with the End Channel. The interval between conversions of each channel is fixed at 15μ seconds. The interval timer has no functionality in this mode of operation.

After software selection of the burst single mode of operation, conversions are started either by an external trigger, or by setting the software start convert bit. If the external trigger is to be used bits 2 and 1 of the Control register must be set to “01” to accept the external trigger as an input signal.

When configured for differential input, the Mail Box functions as a dual level data buffer. However, for Burst Single Mode, only one pass from the start channel to the end channel is implemented. Thus, only the first half of the Mail Box buffer is

utilized. As seen in Table 3.2, the first half of the Mail Box is defined by word addresses 80H to BDH.

Interrupts can be enabled to activate after conversion of each channel or the group of channels as defined by the Start and End Channel Values. If interrupts are configured to go active after the conversion of each channel, an interrupt will be issued every 15μ seconds (not recommended). If interrupt upon completion of a group of channels is selected, the interrupt will be issued 23μ seconds after conversion of the last channel has started.

When burst single operations are run back to back with less then 7μ seconds between the previous burst and the start of a new burst signal operation, software must issue a scan disable command before issuing burst single mode and a start convert. This will prevent erroneous operation of the next burst signal operation.

Convert On External Trigger Only-Mode

In convert on External Trigger Only Mode of operation each conversion is initiated by an external trigger (falling edge of a logic low pulse) input to the APC330 on the EXT TRIGGER* signal of the front panel field I/O connector. Conversions are performed for each channel between and including the Start and End Channel Values in sequential order. The interval between conversions is controlled by the period between external triggers. The interval timer has no functionality in this mode of operation.

The external trigger signal must be configured as an input for this mode of operation. The external trigger can be configured as an input by setting bits 2 and 1 of the Control register to “01”.

At least 5μ seconds of data acquire time should be provided after programming the Control register, Start Value register, and Gain Selects before the first external trigger is issued. These configuration registers control the APC330 on board multiplexers and programmable gain amplifier which, respectively, control the channel and gain selected for the input provided to the converter.

In the external trigger, only mode, it is important to understand the sequence in which converted data is transferred from the ADC to the Mail Box Buffer. Upon an external trigger the selected analog signal is converted but remains at the ADC while the previous digitized value is output from the ADC to the Mail Box Buffer. Thus, with this sequence the Mail Box is consistently updated with the previous cycle’s converted data. In other words, new data in the Mail Box is one cycle behind the ADC. With this sequence, at the end of data conversions, one additional external trigger is required to move the data from the ADC to the Mail Box buffer. At the start of data conversion, with the first external trigger signal (given the Start Convert Bit is set), data is not input to the Mail Box buffer since the data in the ADC buffer is old convert data.

The APC330 requires the setting of the Start Convert bit to logic one prior to receiving the first active external trigger pulse. This will prevent erroneous data from being written into the Mail Box Buffer corresponding to the first channel converted. This is the only mode of operation in which the Start Convert bit does not cause data conversions.

When configured for differential input, the Mail Box functions as a dual level data buffer. The first half of the Mail Box is used to store all selected channel data for the initial pass through the channels defined by the Start and End Value registers. The second half of the Mail Box is used to store the channel data corresponding to the second pass though all selected channels. Storage of channel data continues to alternate between the first and second halves of the Mail Box Buffer. As seen in Table 3.2, the first half of the Mail Box is defined by word addresses 80H to BDH while the second half is defined by word addresses C0H to FDH.

Interrupts can be enabled to activate after conversion of each channel or the group of channels as defined by the Start and End Channel Values. If interrupts are configured to go active after the conversion of each channel, an interrupt will be issued 8μ seconds after a valid external trigger pulse is detected. The only exception to this is upon the very first external trigger pulse, no interrupt will be issued since data is not written to the Mail Box buffer. If interrupt upon completion of a group of channels is selected, an interrupt will be issued 8μ seconds after detection of the first external trigger following conversion of all channels in the selected group. Again, one extra external trigger is needed to complete update of the Mail Box buffer for the selected group of channels.

External Trigger Only mode of operation can be used to synchronize multiple APC330 modules to a single APC330 running in uniform continuous, uniform single, burst continuous, or burst single mode. The external trigger, of the APC330 running uniform or burst mode, must be programmed as an output. The external trigger signal of that APC330 must be connected to the external trigger signals of all other APC330s (programmed for external trigger input) that are to be synchronized. These other APC330s must be programmed for External Trigger Only Mode. Data conversion can then be started by writing high to the Start Convert bit of the APC330 configured for Uniform or Burst mode.

PROGRAMMING CONSIDERATIONS FOR ACQUIRING ANALOG INPUTS

The APC330 provides different methods of analog input acquisition to give the user maximum flexibility for each application. Examples are presented in the following sections to illustrate programming the different modes of operation.

USE OF CALIBRATION SIGNALS

Reference signals for analog input calibration have been provided for use to improve the accuracy over the uncalibrated state. The use of software calibration allows the elimination of hardware calibration potentiometers traditionally used in precision analog front ends.

Software calibration uses some fairly complex equations. **Acromag recommends purchase of our ActiveX, QNX, or VxWorks software to make communication with the board and calibration easy. It relieves you from having to turn the equations in the following sections into debugged software calibration code.**

Uncalibrated Performance

The uncalibrated performance is affected by two primary error sources. These are the Programmable Gain Amplifier (PGA) and the Analog to Digital Converter (ADC). The untrimmed PGA and ADC have significant offset and gain errors

(see specifications in chapter 6) which reveal the need for software calibration.

Calibrated Performance

Very accurate calibration of the APC330 can be accomplished by using calibration voltages present on the board. The four voltages and the analog ground reference are used to determine two points of a straight line which defines the analog input characteristic. The calibration voltages are precisely adjusted at the factory to provide optimum performance, as detailed in section 6.

The calibration voltages are used with the auto zero signal to find two points that determine the straight-line characteristic of the analog front end for a particular range. The recommended calibration voltage selection for each range is summarized in Table 3.9.

Equation (1) following is used to correct the actual ADC data (i.e. the uncorrected bit count read from the ADC) making use of the calibration voltages and range constants.

$$\text{Corrected\_Count} = \left[\frac{65536 * m}{\text{Ideal\_Volt\_Span}}\right] * \left[\text{Count\_Actual} + \frac{(\text{Volt}_{\text{CALLO}} * \text{Gain}) - \text{Ideal\_Zero}}{m} - \text{Count}_{\text{CALLO}}\right] \quad (1)$$

where, "**m**" represents the actual slope of the transfer characteristic as defined in equation 2:

$$m = \text{Gain} * \left[\frac{\text{Volt}_{\text{CALHI}} - \text{Volt}_{\text{CALLO}}}{\text{Count}_{\text{CALHI}} - \text{Count}_{\text{CALLO}}}\right] \quad (2)$$

Gain = The Programmable Gain Amplifier Setting Used (See Table 3.9)

$\text{Volt}_{\text{CALHI}}$ = High Calibration Voltage (See Table 3.9)

$\text{Volt}_{\text{CALLO}}$ = Low Calibration Voltage (See Table 3.9)

$\text{Count}_{\text{CALHI}}$ = Actual ADC Data Read With High Calibration Voltage Applied

$\text{Count}_{\text{CALLO}}$ = Actual ADC Data Read With Low Calibration Voltage Applied

Ideal_Volt_Span = Ideal ADC Voltage Span (See Table 3.10)

Count_Actual = Actual Uncorrected ADC Data For Input Being Measured

Ideal_Zero = Ideal ADC Input For "Zero" (See Table 3.10)

Table 3.9: Recommended Calib. Voltages For Input Ranges

Input Range (Volts)	PGA Gain	ADC Range (Volts)	Rec. Low Calib. Voltage "$\text{Volt}_{\text{CALLO}}$" (Volts)	Rec. High Calib. Voltage "$\text{Volt}_{\text{CALHI}}$" (Volts)
-5 to +5	1	-5 to +5	0.0000 (Auto Zero)	4.9000 (CAL0)
-2.5 to +2.5	2	-5 to +5	0.0000 (Auto Zero)	2.4500 (CAL1)
-1.25 to +1.25	4	-5 to +5	0.0000 (Auto Zero)	1.2250 (CAL2)
-0.625 to +0.625	8	-5 to +5	0.0000 (Auto Zero)	0.6125 (CAL3)
-10 to +10	1	-10 to +10	0.0000 (Auto Zero)	4.9000 (CAL0)
-5 to +5	2	-10 to +10	0.0000 (Auto Zero)	4.9000 (CAL0)
-2.5 to +2.5	4	-10 to +10	0.0000 (Auto Zero)	2.4500 (CAL1)
-1.25 to +1.25	8	-10 to +10	0.0000 (Auto Zero)	1.2250 (CAL2)
0 to +5	1	0 to +5	0.6125 (CAL3)	4.9000 (CAL0)
0 to +2.5	2	0 to +5	0.6125 (CAL3)	2.4500 (CAL1)
0 to +1.25	4	0 to +5	0.6125 (CAL3)	1.2250 (CAL2)
0 to +0.625*	8	0 to +5	0.0000 (Auto Zero)*	0.6125 (CAL3)
0 to +10	1	0 to +10	0.6125 (CAL3)	4.9000 (CAL0)
0 to +5	2	0 to +10	0.6125 (CAL3)	4.9000 (CAL0)
0 to +2.5	4	0 to +10	0.6125 (CAL3)	2.4500 (CAL1)
0 to +1.25	8	0 to +10	0.6125 (CAL3)	1.2250 (CAL2)

* The hardware offset may prevent you from calibrating this range.

Table 3.10: Ideal Voltage Span and Zero For Input Ranges

Input Range (Volts)	PGA Gain	ADC Range (Volts)	"Ideal_Volt_Span" (Volts)	"Ideal_Zero" (Volts)
-5 to +5	1	-5 to +5	10.0000	-5.0000
-2.5 to +2.5	2	"	"	"
-1.25 to +1.25	4	"	"	"
-0.625 to +0.625	8	"	"	"
-10 to +10	1	-10 to +10	20.0000	-10.0000
-5 to +5	2	"	"	"
-2.5 to +2.5	4	"	"	"
-1.25 to +1.25	8	"	"	"
0 to +5	1	0 to +5	5.0000	0.0000
0 to +2.5	2	"	"	"
0 to +1.25	4	"	"	"
0 to +0.625	8	"	"	"
0 to +10	1	0 to +10	10.0000	0.0000
0 to +5	2	"	"	"
0 to +2.5	4	"	"	"
0 to +1.25	8	"	"	"

The calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) for each active input range should not be determined immediately after startup but after the module has reached a stable temperature and updated periodically (e.g. once an hour, or more often if ambient temperatures change) to obtain the best accuracy. Note that several readings (e.g. 64) of the calibration parameters should be taken via the ADC and averaged to reduce the measurement uncertainty, since these points are critical to the overall system accuracy.

Calibration Programming Example 1

Assume that the desired input range is -10 to +10 volts (select desired input range via hardware DIP switch). Channels 0 to 3 are connected differentially, and corrected input channel data is desired. From Tables 3.9 & 3.10, several calibration parameters can be determined:

Gain = 1 (From Table 3.9)
$Volt_{CALHI}$ = 4.9000 volts (CAL0; From Table 3.9)
$Volt_{CALLO}$= 0.0000 volts (Auto Zero; From Table 3.9)
Ideal_Volt_Span = 20.0000 volts (From Table 3.10)
Ideal_Zero = -10.0000 volts (From Table 3.10)

The calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) remain to be determined before uncorrected input channel data can be taken and corrected.

Determination of the $Count_{CALLO}$ Value

1. Execute Write of 0439H to Control Register at Base Address + 04H.
   a) Select Straight Binary
   b) External Trigger Disabled
   c) Auto Zero Calibration Voltage
   d) Burst Single Scan Mode
   e) Timer Disabled
   f) Interrupts Disabled

2. Execute Write of 1F00H to End/Start Channel Value Register at Base Address + 10H. This will permit 32 conversions of the Auto Zero value to be stored in the 32 Mail Box Buffers.

3. Execute write of 00H to Gain Select Channel Registers at Base Address + 40H to 4CH. This selects a gain of one for all 32 channels.

4. Wait at least 5μ seconds before the Start Convert bit is set to allow the input signal to settle.

5. Execute Write of 0001H to the Start Convert Bit at Base Address + 24H. This starts the burst single mode of conversions. Thirty-two conversions of the Auto Zero are implemented and stored in the 32 Mail Box Buffers.

6. Execute Read of the 32 Mail Box Buffers at Base Address + 80H to FCH.

7. Take the average of the 32 ADC values and save this number as $Count_{CALLO}$.

Determination of the $Count_{CALHI}$ Value

8. Execute Write of 0419H to Control Register at Base Address + 04H.
   a) Select Straight Binary
   b) External Trigger Disabled
   c) Select 4.9000v Calibration Voltage
   d) Burst Single Scan Mode
   e) Timer Disabled
   f) Interrupts Disabled

9. Writing the Start Channel Value, End Channel Value, and the Gain Selects is not necessary if they have not been changed from that programmed in steps 2 and 3 above.

10. Wait at least 5μ seconds before the Start Convert bit is set to allow the input signal to settle.

11. Execute Write of 0001H to the Start Convert Bit at Base Address + 24H. This starts the burst single mode of conversions. Thirty-two conversions of the 4.9-volt calibration voltage are implemented and stored in the 32 Mail Box Buffers.

12. Execute Read of the 32 Mail Box Buffers at Base Address + 80H to FCH.

13. Take the average of the 32 ADC values and save this number as $Count_{CALHI}$.

Calculate Equation 2

Calculate m = actual slope from equation 2, since all parameters are known. It is now possible to correct input channel data from any input channel using the same input range (i.e. -10 to +10 volts with a PGA gain = 1). Repeat the above steps periodically to re-measure the calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) as required.

Measure Channels 0 to 3 Differentially and Correct

14. Execute Write of 0401H to Control Register at Base Address + 04H.
   a) Select Straight Binary
   b) External Trigger Disabled
   c) All Channels Differential Input
   d) Burst Single Scan Mode
   e) Timer Disabled
   f) Interrupts Disabled

15. Execute Write of 0300H to End/Start Channel Value Register at Base Address + 10H. This will permit conversions of channels 0 to 3. Writing the Gain Selects is not necessary since they do not need to change from that programmed in step 3 above.

16. Wait at least 5μ seconds before the Start Convert bit is set to allow the input signal to settle.

17. Execute Write of 0001H to the Start Convert Bit at Base Address + 24H. This starts the burst single mode of conversions. Conversions of channels 0 to 3 are implemented and corresponding results are stored in the first four Mail Box Buffer locations at Base Address + 80H to 8CH.

18. Execute Read of the 4 Mail Box Buffers at Base Address + 80H to 8CH. The data represents the uncorrected "Count_Actual" term in equation 1. Since all parameters on the right hand side of equation 1 are known, calculate the calibrated value "Corrected_Count". This is the desired, corrected value. Repeat this procedure for each of the channels.

19. If channel response time requirements are not high speed it is recommended that a running average (i.e. of the last 8, 16, 32, etc.) of readings be maintained for each channel. This will minimize noise effects and provide the best accuracy.

Calibration Programming Example 2

Assume that the desired input range is 0 to +1.25 volts (selection of the desired input range is implemented via hardware DIP switch). Channels 3 to 13 are connected single ended, and corrected input channel data is desired. The calibration voltages are converted using burst single mode (for quick conversion of the calibration voltages) while the actual data will be converted using uniform single mode. From Tables 3.9 and 3.10, several calibration parameters can be determined:

Preselect 0 to 10v ADC Range via hardware DIP switch.
Gain = 8 (From Table 3.9)
$Volt_{CALHI}$ = 1.2250 volts (CAL2; From Table 3.9)
$Volt_{CALLO}$ = 0.6125 volts (CAL3; From Table 3.9)
Ideal_Volt_Span = 10.0000 volts (From Table 3.10)
Ideal_Zero = 0.0000 volts (From Table 3.10)

The 0 to +5v ADC range could alternatively be used with a gain of 4. This approach may reduce the effect of noise over the ADC range and gain selected in this example.

The calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) remain to be determined before uncorrected input channel data can be taken and corrected.

Determination of the $Count_{CALLO}$ Value

1. Execute Write of 0431H to Control Register at Base Address + 04H.
   a) Select Straight Binary
   b) External Trigger Disabled
   c) Select 0.6125v Calibration Voltage
   d) Burst Single Scan Mode
   e) Timer Disabled
   f) Interrupts Disabled

2. Execute Write of 1F00H to End/Start Channel Value Register at Base Address + 10H. This will permit 32 conversions of the calibration voltage to be stored in the 32 Mail Box Buffers.

3. Set each channel's Gain Select bits to FFH in the Gain Select Channel Registers at Base Address + 40H to 4CH. This selects a gain of eight for all 32 channels.

4. Wait at least 5μ seconds before the Start Convert bit is set to allow the input signal to settle.

5. Execute Write of 0001H to the Start Convert Bit at Base Address + 24H to start burst single mode conversions. Thirty-two conversions of the calibration voltage are implemented and stored in the 32 Mail Box Buffers.

6. Execute Read of the 32 Mail Box Buffers at Base Address + 80H to FCH.

7. Take the average of the 32 ADC values and save this number as $Count_{CALLO}$.

Determination of the $Count_{CALHI}$ Value

8. Execute Write of 0429H to Control Register at Base Address + 04H.
   a) Select Straight Binary
   b) External Trigger Disabled
   c) Select 1.2250v Calibration Voltage
   d) Burst Single Scan Mode
   e) Timer Disabled
   f) Interrupts Disabled

9. Writing the Start Channel Value, End Channel Value, and the Gain Selects is not necessary if they have not been changed from that programmed in steps 2 and 3 above.

10. Wait at least 5μ seconds before the Start Convert bit is set to allow the input signal to settle.

11. Execute Write of 0001H to the Start Convert Bit at Base Address + 24H. This starts a burst single mode of conversions. Thirty-two conversions of the 1.2250 calibration voltage are implemented and stored in the 32 Mail Box Buffers.

12. Execute Read of the 32 Mail Box Buffers at Base Address + 80H to FCH.

13. Take the average of the 32 ADC values and save this number as $Count_{CALHI}$.

Calculate Equation 2

Calculate m = actual slope from equation 2, since all parameters are known. It is now possible to correct input channel data from any input channel using the same input range (i.e. 0 to +1.25 volts with a PGA gain = 8). Repeat the above steps periodically to re-measure the calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) as required.

Measure Channels 3 to 13 Single Ended and Correct Using Uniform Single Mode

14. Execute Write of 0A09H to Control Register at Base Address + 04H.
   a) Select Straight Binary
   b) External Trigger Disabled
   c) Select Single Ended Input
   d) Uniform Single Scan Mode
   e) Timer Enabled
   f) Interrupts Disabled

15. Execute Write of 0D03H to End/Start Channel Value Register at Base Address + 10H. This will permit conversions of channels 3 to 13. Writing the Gain Selects is not necessary since they do not need to change from that programmed in step 3 above.

16. Execute Write of 50H, as a byte data transfer, to the Timer Prescaler at Base Address + 09H. This sets the Timer Prescaler to 80 decimal.

17. Execute Write 0008H to the Conversion Timer at Base Address + 0CH. This Conversion Timer value in conjunction with the Timer Prescaler sets the interval time between conversions to (80 * 8) ÷ 8 = 80μ seconds.

18. Wait at least 5μ seconds before the Start Convert bit is set to allow the input signal to settle.

19. Execute Write of 0001H to the Start Convert Bit at Base Address + 24H. This starts the uniform single mode of conversions. Conversions of channels 3 to 13 are implemented and stored in their corresponding Mail Box Buffers.

20. Execute Read of the Mail Box Buffers at Base Address + 8CH to B4H. The data represents the uncorrected "Count_Actual" term in equation 1. Since all parameters on the right hand side of equation 1 are known. The calibrated value "Corrected_Count" can be calculated for each of the channels.

21. If channel response time requirements are not high speed it is recommended that a running average (i.e. of the last 8, 16, 32, etc.) of readings be maintained for each channel. This will minimize noise effects and provide the best accuracy.

Error checking should be performed on the "Corrected_Count" value to make sure that calculated values below 0 or above 65,535 are restricted to those end points. Note that the software calibration cannot recover signals near the end points of each range which are clipped off due to the uncalibrated hardware (e.g. PGA and ADC) or power supply limitations.

See the specifications in section 6 for details regarding the maximum corrected (i.e. calibrated) error.

Programming Interrupts

Interrupts can be enabled for generation after conversion of individual channels or after a group of channels have been converted. Interrupts generated by the APC330 use interrupt request line INTA# . The interrupt release mechanism is release on register access. That is, the APC330 will release the INTA# signal when bit-15 of the Interrupt Register at Base Address + 00H is set to logic "1".

Interrupt Programming Example

1. Enable APC330 board interrupt by writing a "1" to bit 0 of the Interrupt register at Base Address + 00H.
2. Enable the APC330 for interrupt after each channel or after conversion of a group of channels by setting bits 12 and 13 of the Control register (at Base Address + 04H) as required.
3. Interrupts can now be generated after start of a scan mode of operation (burst, continuous, or external trigger only).

General Sequence of Events for Processing an Interrupt

1. The APC330 asserts the Interrupt Request Line (INTA#) in response to an interrupt condition.
2. Determine the IRQ line assigned to the APC330 during system configuration (read configuration register number 15).
3. Set up the system interrupt vector for the appropriate interrupt.
4. Unmask the IRQ in the system interrupt controller.
5. The interrupt service routine pointed to by the vector set up in step 3 starts.
6. Interrupt service routine determines if the APC330 has a pending interrupt request by reading the Interrupt pending bit-1 of the Interrupt register.
7. Example of Generic Interrupt Handler Actions:
   a) Disable the interrupting APC330 by writing "0" to bit-0 of the Interrupt Register to disable interrupts on the APC330.
   b) Service the interrupt by reading converted data resident in the Mail Box buffer of the APC330. Use the New Data Available register to identify valid Mail Box Buffer data.
   c) Clear the interrupt request by writing a "1" to bit-15 of the Interrupt register.
   d) Enable the APC330 for interrupts by writing "1" to bit-0 of the Interrupt register.
8. Write "End-Of-Interrupt" command to the system's interrupt controller.
9. If the APC330's interrupt stimulus has been removed, the interrupt cycle is completed and the board holds the INTA# inactive.

4.0 THEORY OF OPERATION

This section contains information regarding the hardware of the APC330. A description of the basic functionality of the circuitry used on the board is also provided. Refer to the Block Diagram shown in Drawing 4501-922 as you review this material.

FIELD ANALOG INPUTS

The field I/O interface to the APC330 is provided through the front panel connector (refer to Table 2.3). **Field I/O signals are NON-ISOLATED.** This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring this effect may cause operational errors, and with extreme abuse, possible circuit damage. Refer to Drawing 4501-921 for example wiring and grounding connections.

Analog inputs and calibration voltages are selected via analog multiplexers. APC330 control logic automatically programs the multiplexers for selection of the required analog input channel. The required control is based upon selection of single ended or differential analog input and the Start and End channel register values.

Single ended and differential channels cannot be mixed (i.e. they must all be single ended or differentially wired). Up to 32 single ended inputs can be monitored, where each channel's + input is individually selected along with a single sense lead for all channels. Up to 16 differential inputs can be monitored, where each channel's + and - inputs are individually selected.

A Programmable Gain (Instrumentation) Amplifier (PGA) takes as input the selected channel's + and - inputs (or + and sense) and outputs a single ended voltage proportional to it. The

gain can be 1, 2, 4, or 8 and is selected through the Gain Control registers.

The output of the PGA feeds the ADC (Analog to Digital Converter). The ADC is a state of the art, 16-bit, successive approximation converter with a built-in sample and hold circuit. The sample and hold circuit goes into the hold mode when a conversion is initiated. This maintains the selected channel's voltage constant until the ADC has accurately digitized the input. Then it returns to sample mode to acquire the next channel. Once a conversion has been started, control logic on the APC330 automatically updates the multiplexer and PGA for the next channel to be converted as required. This allows the input to settle for the next channel while the previous channel is converting. This pipelined mode of operation facilitates maximum system throughput.

A miniature DIP switch on the board controls the range selection for the ADC (-5 to +5, -10 to +10, 0 to 5, and 0 to 10 Volts) as detailed in section 2. DIP switch selection should be made prior to powering the unit. Thus, all channels will use the same ADC range. However, the analog input range can vary on an individual channel basis depending on the programmable gain selection.

The board contains four precision voltage references and a ground (autozero) reference for use in calibration. These provide considerable flexibility in obtaining accurate calibration for the desired ADC range and gain combination, when compared to fixed hardware potentiometers for offset and gain calibration of the ADC and PGA.

LOGIC/POWER INTERFACE

The logic interface to the board is made through the P1 of the PCI connector (refer to Table 2.2). This connector also provides +5V and ±12V power to the board. Note that the signals in bold italic are not used.

A Field Programmable Gate-Array (FPGA) installed on the APC330 board provides an interface to the PCI Bus to the CPU board. The interface to the CPU board allows complete control of all APC330 functions.

PCI INTERFACE LOGIC

The PCI bus interface logic is imbedded within the FPGA. This logic includes support for PCI commands, including: configuration read/write, and memory read/write. In addition, the PCI target interface performs parity error detection, uses a single 4K base address register, and implements target abort, retry, and disconnect. The APC330 logic also implements interrupt requests via interrupt line INTA#.

All register accesses to the APC330 require 8 PCI clock cycles with the exception of a read access to the Mail Box Buffer. A read access to the Mail Box Buffer will typically be executed in 8 PCI clock cycles. On a rare occasion read and write operations to the Mail Box buffer may contend. Since the Mail Box buffer is not implemented as a dual port memory, simultaneous read and write access to RAM is not possible. If a read access to the RAM is initiated simultaneously with an internal RAM write (for update of the Mail Box buffer with ADC data), the read access will complete as a retry termination. On a retry termination the bus master is forced to initiate another read to the same Mail Box Buffer at a later time.

APC330 CONTROL LOGIC

All logic to control data acquisition is imbedded in the FPGA. The control logic of the APC330 is responsible for controlling the operation of a user specified sequence of data acquisitions. Once the APC330 has been configured, the control logic performs the following:

- Controls the channel multiplexers based upon start and end channel values, and single ended or differential analog input mode.
- Selects channel gain at the programmable gain amplifier corresponding to the current channel.
- Controls data conversion at the ADC based on one of five different scan modes of operation.
- Controls data transfer from the ADC to the FPGA's 16-bit serial shift register.
- Controls and updates the Mail Box buffer, New Data register, and Missed Data register.
- Stops data acquisition for Single Cycle Scan modes.
- Provides external or internal trigger control.
- Controls the interval between data conversions.
- Issues interrupt requests to the carrier.

INTERNAL CHANNEL POINTERS

Internal counters in the FPGA are used as pointers to: control the multiplexers for selection of the current channel's analog signal; select and set the current channel's Gain; and control update of the Mail Box RAM buffer. The start channel register controls the value at which these counters start and the end value register controls the maximum channel number for which data is converted.

In the continuous modes of operation these counters continuously cycle, in sequential order, from the defined start value to the defined end value. When the continuous mode of operation is halted by disabling the scan mode via the control register, the internal hardware counter remains at the count value reached when halted. Upon start of a new scan mode, via the software start convert bit or external trigger, the internal pointers are reinitialized. Thus, the first channel converted, upon restart of data conversions, will correspond to that set in the start value register.

A 16-bit serial shift register is implemented in the FPGA. This serial shift register interfaces to the ADC. A clock signal provided by the converter is used to serially shift the new data from the converter to the FPGA's 16-bit serial shift register. Use of the converter's clock signal (instead of an external clock) minimizes the danger of digital noise feeding through and corrupting the results of a conversion in process.

The converted data serially shifted from the ADC to the FPGA, represents the analog signal digitized in the previous convert cycle. That is, the ADC transfers digitized analog input data to the FPGA one convert cycle after it has been digitized. Serially shifting the 16-bits of digitized data to the FPGA and then writing to the Mail Box buffer is completed 8μ seconds after start of the convert cycle.

Upon initiation of an ADC convert cycle, the analog input data is digitized and stored into an internal ADC buffer. Also during

this cycle, the last converted data value is moved from the ADC buffer to the FPGA's Mail Box Buffer. At this time, the New Data Available bit corresponding the previous converted channel is set in the FPGA register.

Understanding this sequence of events is important when using the External Trigger Only scan mode. The first digitized value received from the ADC in External Trigger Only mode will not be written to the Mail Box buffer if the Start Convert bit is set prior to issuance of the first external trigger signal. This first value received from the ADC is digitized data that has remained in the ADC's buffer from a previous data acquisition session. Likewise, to update the Mail Box with the last desired digitized data value one additional convert cycle is required.

For all other scan modes, the FPGA control logic will automatically discard the first digitized data value received from the ADC. It is not written to the Mail Box buffer. In addition, the FPGA logic also automatically generates the required "flush" convert signals to obtain the last converted data value from ADC.

EXTERNAL TRIGGER

The external trigger connection is made via pin 49 of the Field I/O Front Panel Connector. For the Burst and Continuous scan modes the falling edge of the external trigger will start data acquisition which will then be controlled by the FPGA. For External Trigger, Only mode, each falling edge of the external trigger causes a conversion at the ADC. Once the external trigger signal has been driven low, it should remain low for a minimum of 500n seconds.

TIMED PERIODIC TRIGGER CIRCUIT

Timed Periodic Triggering is provided by two programmable counters (an 8-bit Timer Prescaler and a 16-bit Conversion Timer). The Timer Prescaler is clocked by the 8MHz. board clock. The output of the Timer Prescaler counter is then used to clock the second counter (Conversion Timer). In this way, the two counters are cascaded to provide variable time periods anywhere from 8μ seconds to 2.0889 seconds. The output of the second counter is used to trigger the start of new ADC conversions for the Uniform Scan modes of operation. For the Burst Continuous mode, the interval between conversions of each channel is fixed at 15μ seconds. However, the interval between the group (burst) of channels can be controlled by the Interval Timer.

INTERRUPT CONTROL LOGIC

The APC330 can be configured to generate an interrupt after completion of conversion of a single channel or after conversion of a group of channels is completed. APC330 interrupt signal INTA# is driven active to the carrier/CPU to request an interrupt. Bit-1 of the Interrupt register (at Base Address + 0H) can be read to identify a pending interrupt. The interrupt release mechanism employed is release on register access. The APC330 will release the interrupt request when bit-15 of the Interrupt register (at Base Address + 0H) is set to a logic "1".

APC Software

Acromag also provides a software product (sold separately) consisting of APC330 ActiveX (Object Linking and Embedding) drivers for Windows 95® and newer compatible application programs (Model PMCSW-ATX). This software provides individual drivers that allow Acromag APC330 boards to be easily integrated into Windows® application programs, such as Visual C++™, Visual Basic®, Microsoft® Office® applications and others. The ActiveX controls provide a high-level interface to APC330 boards, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the ActiveX controls. These functions consist of an ActiveX control for each Acromag PMC board (APC products use the corresponding PMC Module software).

In addition, Acromag provides a software product (sold separately) consisting of APC330 VxWorks® library or QNX® library. This software (Model PMCSW-API-VXW or Model PCISW-API-QNX) is composed of VxWorks® or QNX® (real time operating system) libraries for all Acromag PMC boards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag PMC boards (APC products use the corresponding PMC Module software).

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

The APC330 is shipped pre-calibrated by Acromag and may be returned at the discretion of the customer to measure the accuracy of the calibration at some defined period. Recalibration, if required, can be performed by the customer if the proper equipment is available to them and is otherwise offered through the Service Department at Acromag for a fee.

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

PHYSICAL

Physical Configuration…… Short PCI 5 Volt Board.
Height..... 4.200 inches (106.68 mm).
Depth…….. 6.600 inches (167.64 mm).
Board Thickness..... 0.062 inches (1.59 mm).
Max Component Height….. 0.570 inches (14.48 mm).
Recommended Card Spacing…….. 0.800 inches (20.32 mm).
Connectors:
P1 (PCI Bus)…….. PCI Specification Version 2.2. 5 V card "finger" edge spacing.
P2 (Field I/O)…….. 50-pin, SCSI-2, female receptacle header (AMP 787082-5 or equivalent).

Power Requirements		Board APC330
5V[2] (±5%)	Typical	230 mA
	Max.	275 mA
+12V[3] (±5%)	Typical	0 mA
	Max.	0 mA
-12V[3] (±5%)	Typical	0 mA
	Max.	0 mA

Note:
1. Circuit board is selectively coated with a fungus resistant acrylic conformal coating.
2. Maximum rise time of 100m seconds.
3. The +/-12 volt power supplies on the PCI bus connector (P1) are not used. This board uses a DC-DC converter, which uses the 5V supply from the PCI bus connector (P1) and generates +/-15 volt supplies for the board.

ENVIRONMENTAL

Operating Temperature..... 0 to +70°C.
-40 to +85°C (E Versions)
Relative Humidity…..... 5-95% Non-Condensing.
Storage Temperature…..... -55°C to 100°C.
Non-Isolated..... Logic and field commons have a direct electrical connection.
Radiated Field Immunity[4](RFI).. Designed to comply with IEC1000-4-3 Level 3 (10V/m, 80 to 1000MHz AM & 900MHz. keyed) and European Norm EN50082-1 with error less than ±0.50% of FSR.
Electromagnetic Interference Immunity[4] (EMI)…..…… Error is less than ±0.25% of FSR under the influence of EMI from switching solenoids, commutator motors, and drill motors.
Surge Immunity…… Not required for signal I/O per European Norm EN50082-1.
Electric Fast Transient Immunity[4](EFT)…… Complies with IEC1000-4-4 Level 2 (0.5KV at field input and output terminals) and European Norm EN50082-1.
Radiated Emissions[4]…… Meets or exceeds European Norm EN50081-1 for class A equipment.
FCC…….. Only the APC Models are compliant to standard FCC PART 15, Subpart.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this installation does cause harmful interference to the radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or experienced radio/TV technician for help.*

Warning: This is a class A product. In a domestic environment this product may cause radio interference in which the user may be required to take adequate measures to suppress.

Note:
4. Reference Test Conditions: Differential inputs, all channels, PGA Gain = 1, Temperature 25°C, using a 2 meter shielded cable length connection to the field analog input signals.

Reliability Prediction

Mean Time Between Failure….. MTBF = TBD hours (not available at time of printing) @ 25°C, Using MIL-HDBK-217F, Notice 2.

ANALOG INPUTS

Input Channels (Field Access).. 32 Single-ended or 16 Differential Via 50-pin front panel connector.
Analog Input Data Buffer…… 32 16-bit Registers
Input Signal Type..... Voltage (Non-isolated).
Input Ranges (DIP switch selectable)…… Bipolar -5 to +5 Volts[5]
Bipolar -10 to +10 Volts[5]
Unipolar 0 to +5 Volts[5]
Unipolar 0 to +10 Volts[5]

Notes:
5. Range assumes the programmable gain is equal to one. Additional ranges are created with other gains. Divide the listed range by the programmable gain to determine the actual input range.

Programmable Gains..... x1, x2, x4, x8.
Input Overvoltage Protection..... VSS - 20 V to VDD + 40 V with Power ON.
-35 V to +55 Volts Power OFF
Input Resistance..... 1 MΩ, Typical.
Input Bias Current..... 1nA., Typical.
Common Mode Voltage Range. ± (I V_s I – 2.5) Volts, Typical.
Common Mode Rejection Ratio

(60Hz)[10]……96 dB., Typical.
Channel to Channel Rejection 96 dB., Typical.
Ratio (60Hz)[10]……..

(ADC) ADS7809U OR AD977AR @25°C:

A/D Resolution.....16-bits.
Data Format……. Binary 2's Complement and Straight Binary
No Missing Codes[10]..... No Missing Codes 15-bits ADC
A/D Integral Linearity Error[10].....±1 LSB Typical, ±3 LSB Maximum ADC
Unipolar Zero Error[7]..... ±10mV Maximum, for 0-10V Range, ±10mV Maximum for 0-5V Range.
Bipolar Offset Error[7].....±10mV Maximum, for ±10V Range, ±10mV Maximum for ±5V Range.
Full Scale Error[7].....±0.5% Maximum.

(PGA) PGA206UA @25°C:

PGA.....Burr-Brown PGA206UA
PGA Linearity Error.....±0.005% Maximum (3.27 LSB)
Offset Error RTI[7].....±1.0mV Typical, ±2.5mV Max.
Gain Error (all gains)[7].....0. 01% Typical, 0.1% Maximum.

Note:
7. Software calibration eliminates these error components.

Programmable Calibration Voltages

Calibration Signal	Ideal Value (Volts)	Maximum Tolerance @25°C (Volts)	Maximum Temperature Drift[8] (ppm/°C)
Auto Zero	0.0000	±0.000150	0
CAL0	4.9000	±0.000228	±6
CAL1	2.4500	±0.000228	±11
CAL2	1.2250	±0.000228	±11
CAL3	0.6125	±0.000228	±11

Note:
8. Worst case temperature drift is the sum of the ±6 ppm/°C * drift of the calibration voltage reference plus the ±5 ppm/°C drift of the resistors in the voltage divider.

Maximum Overall Calibrated Error @ 25°C

The maximum corrected (i.e. calibrated) error is the worst-case accuracy possible. It is the sum of error components due to ADC quantization of the low and high calibration signals, PGA and ADC linearity error, and the absolute errors of the recommended calibration voltages at 25°C.

Input Range (Volts)	PGA Gain	ADC Range (Volts)	Max Err[9,10,12] ±LSB (% Span)	Typ. Err[9,10,12] ±LSB (% Span)
-5 to +5	1	-5 to +5	±8.6 LSB (0.013%)	±4 LSB (0.006%)
-10 to+10	1	±10	±9.4 LSB (0.014%)	±3 LSB (0.005%)

Note:
9. A total of 64 input samples, autozero values, and calibration voltages were averaged with a throughput Rate of 67khz conversions/second. Follow the input connection recommendations of Section 2, because input noise and non-ideal grounds can degrade overall system accuracy. For critical applications, multiple input samples should be averaged to improve performance. Accuracy versus temperature depends on the temperature coefficient of the calibration voltage.

Settling Time (20V step)[10]..... 3.5uS to 0.01%, Typical (PGA).
A/D Conversion Time.....8uS Maximum
Conversion Rate..... 125KHz Maximum
Recommended Conversion Rate…… 67KHz
A/D Triggers..... External and Software.
Input Noise[10,11]..... 1.8 LSB rms, Typical. ±5V input range
Temperature Coefficient..... See spec. of calibration voltages.

Note:
10. Reference Test Conditions: Differential inputs, all channels, PGA Gain = 1, Temperature 25°C, 67K conversions/second, with a 2 meter shielded cable length connection to the field analog input signals.
11. A total of 2048 input samples were taken statistically, assuming a normal distribution, to determine the RMS value.
12. Accuracy may be further improved by increasing the time between conversions (e.g. from 15μ seconds to 30μ seconds).

External Trigger Input/Output

As An Input:..... Must be an active low 5 volt logic TTL compatible, debounced signal referenced to analog common. Conversions are triggered on the falling edge of this trigger signal. Minimum pulse width 500n seconds.
As An Output:.....Active low 5 volt logic TTL compatible output is generated. The trigger pulse is low for a maximum of 500n seconds.

PCI BUS COMPLIANCE

Specification…… This device meets or exceeds all written PCI Local Bus specifications per revision 2.2
Electrical/Mechanical Interface. Short 5V Board
PCI Target …….....Implemented by Altera FPGA
4K Memory Space Required…. One Base Address Register
PCI Commands Supported…… Configuration Read/Write, Memory Read/Write, 32,16, and 8-bit data transfer types supported.
Signaling…… 5V Compliant, 3.3V Tolerant.
INTA#…… Interrupt A is used to request an interrupt: 1) After each channel is converted or 2) After a group of channels are converted.
Access Times…… 8 PCI Clock Cycles for all registers except the Mail Box . A read access to the Mail Box Buffer will typically be executed

in 8 PCI clock cycles. On rare occasions the Mail Box read will complete as a **retry termination.** The retry termination is necessary to avoid Mail Box Buffer contention when a RAM read is initiated simultaneously with an internal RAM write. On a retry termination the bus master is forced to initiate another read to the same Mail Box Buffer at a later time.

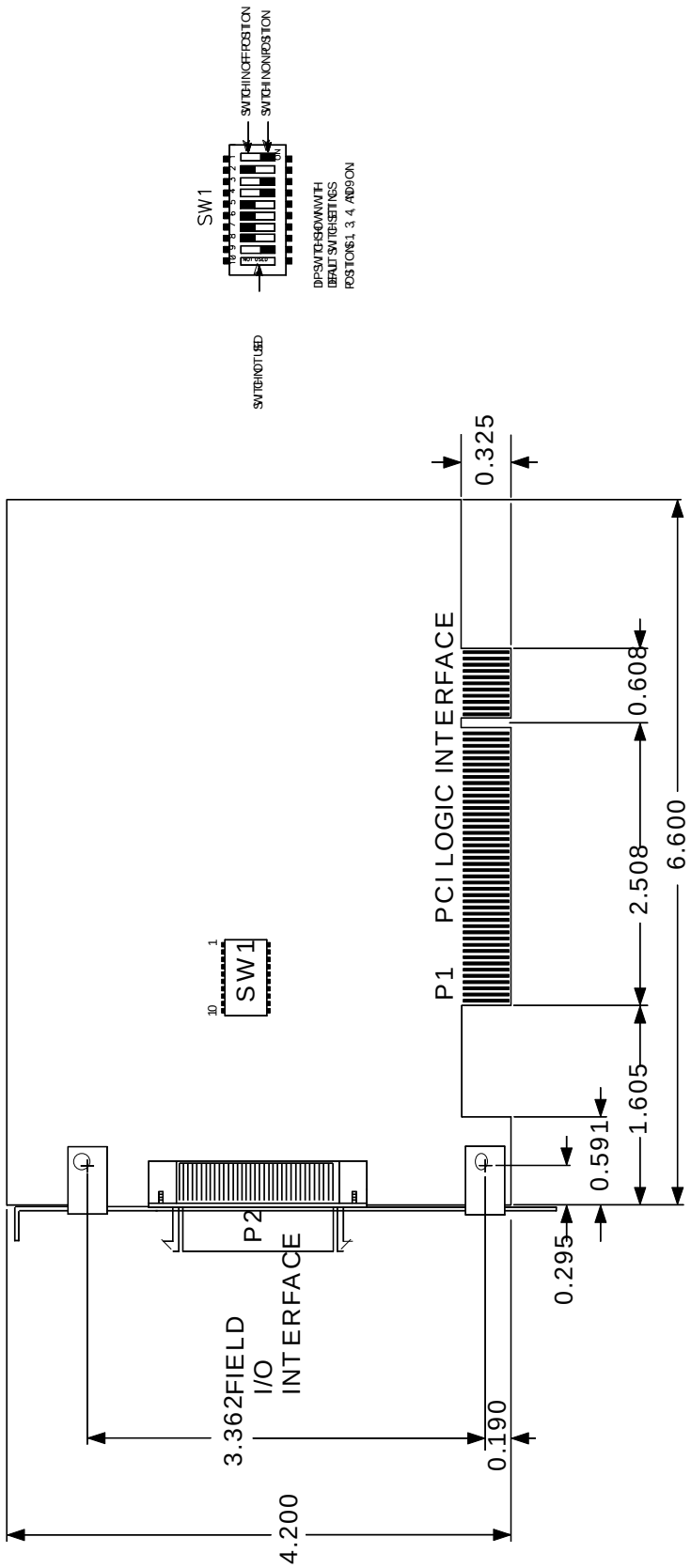
APPENDIX

CABLE: MODEL 5028-187 (SCSI-2 to Flat Ribbon, Shielded)

Type: Round shielded cable, 50-wires (SCSI-2 male connector at one end and a flat female ribbon connector at the other end). The cable length is 2 meters (6.56 feet). This shielded cable is recommended for all I/O applications (both digital I/O and precision analog I/O).
Application: Used to connect Model 5025-552 termination panel to the APC330 board.
Length: Standard length is 2 meters (6.56 feet). Consult factory for other lengths. It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50 conductors, 28 AWG on 0.050 inch centers (permits mass termination for IDC connectors), foil/braided shield inside a PVC jacket.
Connectors: (One End): SCSI-2, 50-pin male connector with backshell and spring latch hardware.
(Other End): IDC, 50-pin female connector with strain relief.
Keying: The SCSI-2 connector has a “D Shell” and the IDC connector has a polarizing key to prevent improper installation.
Schematic and Physical Attributes: See Drawing 4501-758.
Electrical Specifications: 30 VAC per UL and CSA (SCSI-2 connector spec.’s). 1 Amp maximum at 50% energized (SCSI-2 connector spec.’s).
Operating Temperature: -20°C to +80°C.
Storage Temperature: -40°C to +85°C.
Shipping Weight: 1.0 pound (0.5Kg), packed.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For APC Boards.
Application: To connect field I/O signals to the APC boards.
Termination Panel: Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the APC board via a flat ribbon cable (Model 5025-551-x). Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to field I/O (pins 1-50) on the APC board. Each APC board has its own unique pin assignments. Refer to the APC board manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight: 1.25 pounds (0.6kg) packaged.



4501-924A

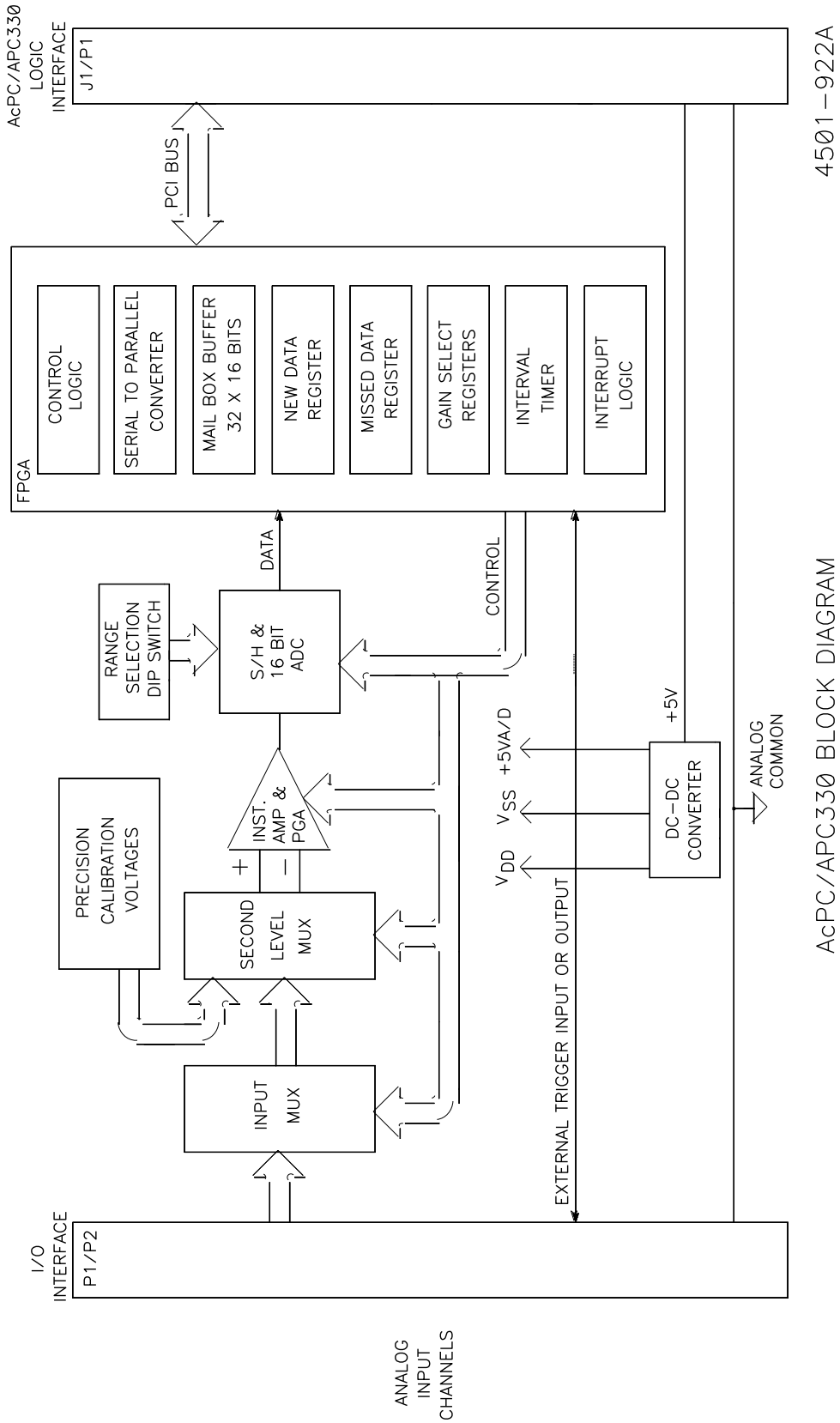
APC330 MECHANICAL ASSEMBLY

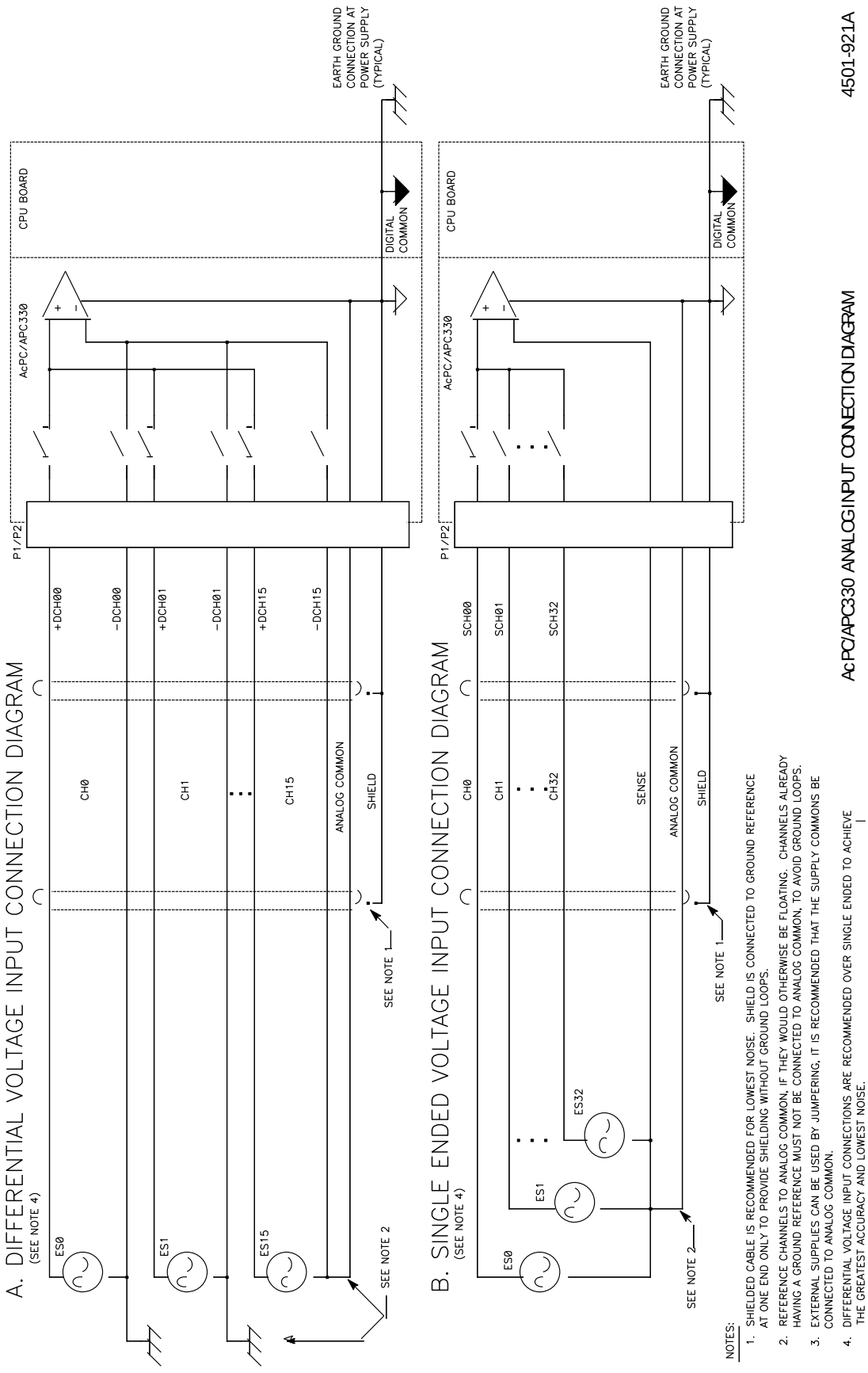
ANALOG INPUT RANGE SELECTION (SW1 DIP SWITCH SETTINGS)

DESIRED ADC INPUT RANGE * (VDC)	REQUIRED INPUT SPAN (VOLTS)	REQUIRED INPUT TYPE	SWITCH SETTINGS ON	SWITCH SETTINGS OFF
−5 TO +5**	10	BIPOLAR	1,3,4,9	2,5,6,7,8
−10 TO +10	20	BIPOLAR	2,5,6,9	1,3,4,7,8
0 TO +5	5	UNIPOLAR	1,3,5,8	2,4,6,7,9
0 TO +10	10	UNIPOLAR	1,3,4,7	2,5,6,8,9

* ASSUMING A GAIN OF 1

** THE BOARD IS SHIPPED WITH THE DEFAULT DIP SWITCH SETTING FOR THE −5 TO +5 VOLT ADC INPUT RANGE AS SHOWN IN THE ABOVE DIAGRAM.

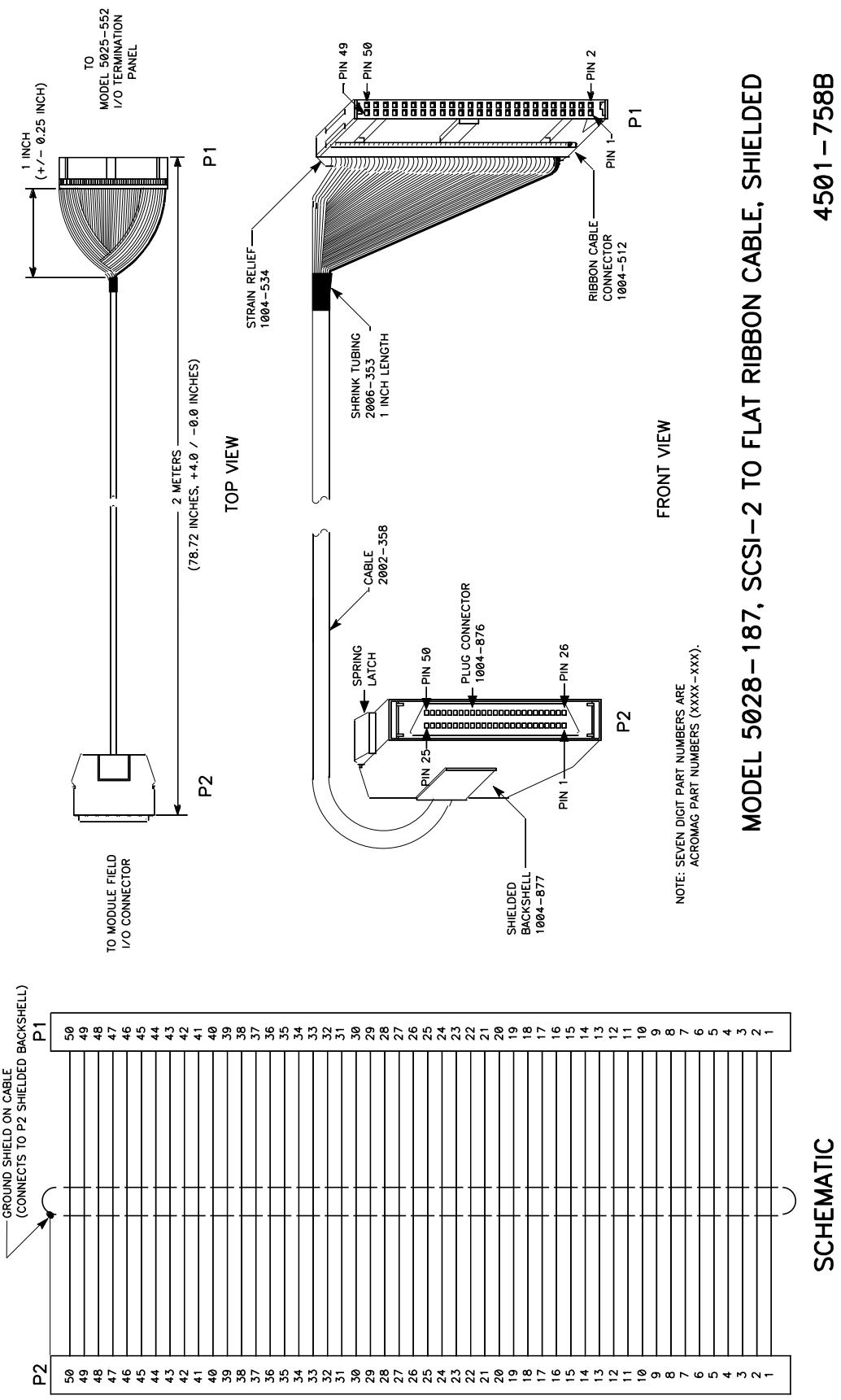

AcPC/APC330 LOGIC INTERFACE
J1/P1
PCI BUS
FPGA
CONTROL LOGIC
SERIAL TO PARALLEL CONVERTER
MAIL BOX BUFFER 32 X 16 BITS
NEW DATA REGISTER
MISSED DATA REGISTER
GAIN SELECT REGISTERS
INTERVAL TIMER
INTERRUPT LOGIC
DATA
CONTROL
RANGE SELECTION DIP SWITCH
S/H & 16 BIT ADC
INST. AMP & PGA
PRECISION CALIBRATION VOLTAGES
SECOND LEVEL MUX
INPUT MUX
+5V
+5VA/D
VSS
VDD
DC-DC CONVERTER
ANALOG COMMON
EXTERNAL TRIGGER INPUT OR OUTPUT
I/O INTERFACE
P1/P2
ANALOG INPUT CHANNELS
4501-922A
AcPC/APC330 BLOCK DIAGRAM

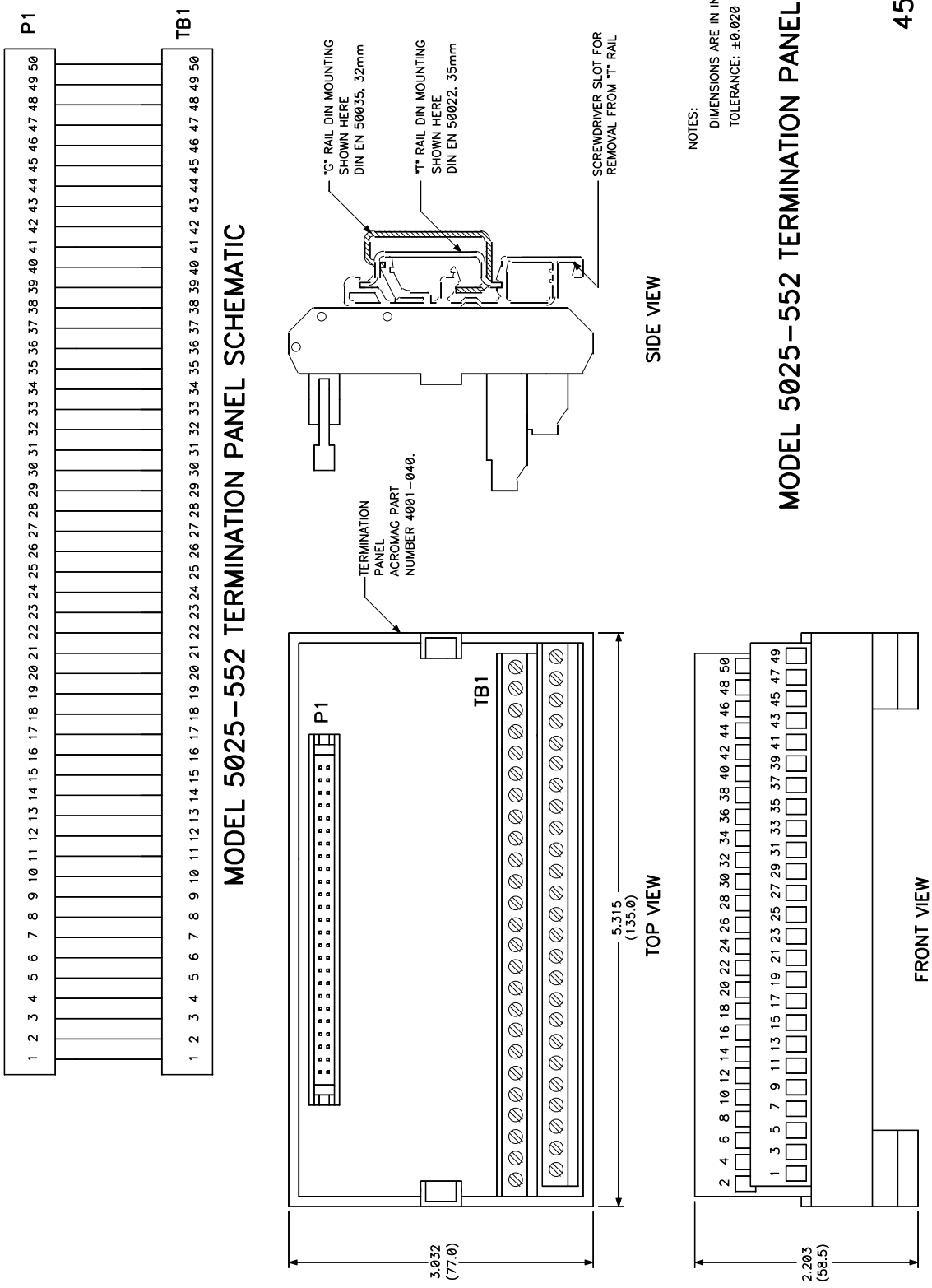


NOTES:

1. SHIELDED CABLE IS RECOMMENDED FOR LOWEST NOISE. SHIELD IS CONNECTED TO GROUND REFERENCE AT ONE END ONLY TO PROVIDE SHIELDING WITHOUT GROUND LOOPS.
2. REFERENCE CHANNELS TO ANALOG COMMON, IF THEY WOULD OTHERWISE BE FLOATING. CHANNELS ALREADY HAVING A GROUND REFERENCE MUST NOT BE CONNECTED TO ANALOG COMMON, TO AVOID GROUND LOOPS.
3. EXTERNAL SUPPLIES CAN BE USED BY JUMPERING, IT IS RECOMMENDED THAT THE SUPPLY COMMONS BE CONNECTED TO ANALOG COMMON.
4. DIFFERENTIAL VOLTAGE INPUT CONNECTIONS ARE RECOMMENDED OVER SINGLE ENDED TO ACHIEVE THE GREATEST ACCURACY AND LOWEST NOISE.

AcPC/APC330 ANALOG INPUT CONNECTION DIAGRAM 4501-921A


TO
MODEL 5025-552
I/O TERMINATION
PANEL
1 INCH
(+/- 0.25 INCH)
P1
2 METERS
(78.72 INCHES, +4.0 / -0.0 INCHES)
P2
TOP VIEW
TO MODULE FIELD
I/O CONNECTOR
PIN 49
PIN 50
PIN 2
PIN 1
P1
STRAIN RELIEF
1004-534
SHRINK TUBING
2006-353
1 INCH LENGTH
RIBBON CABLE
CONNECTOR
1004-512
FRONT VIEW
CABLE
2002-358
SPRING
LATCH
PIN 50
PLUG CONNECTOR
1004-876
PIN 26
PIN 25
PIN 1
P2
SHIELDED
BACKSHELL
1004-877
NOTE: SEVEN DIGIT PART NUMBERS ARE
ACROMAG PART NUMBERS (XXXX-XXX).
MODEL 5028-187, SCSI-2 TO FLAT RIBBON CABLE, SHIELDED
4501-758B
GROUND SHIELD ON CABLE
(CONNECTS TO P2 SHIELDED BACKSHELL)
P1
P2
SCHEMATIC


P1
TB1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
MODEL 5025-552 TERMINATION PANEL SCHEMATIC
"G" RAIL DIN MOUNTING SHOWN HERE DIN EN 50035, 32mm
"T" RAIL DIN MOUNTING SHOWN HERE DIN EN 50022, 35mm
SCREWDRIVER SLOT FOR REMOVAL FROM "T" RAIL
SIDE VIEW
NOTES:
DIMENSIONS ARE IN INCHES (MILLIMETERS).
TOLERANCE: ±0.020 (±0.5).
MODEL 5025-552 TERMINATION PANEL
4501-464A
TERMINATION PANEL ACROMAG PART NUMBER 4001-040.
P1
TB1
5.315 (135.0)
TOP VIEW
3.032 (77.0)
2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48 50
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 41 43 45 47 49
FRONT VIEW
2.203 (58.5)

REVISION HISTORY

The following table details the revision history of this document:

Release Date	Version	EGR/DOC	Description of Revision
4-AUG-2017	D	CAP/JAA	Remove CE Mark due to non-RoHS compliant part. Refer to ECN # 17G016.

Notes: