Series AP48x AcroPack
Counter Timer Module

USER'S MANUAL

ACROMAG INCORPORATED
30765 South Wixom Road
Wixom, MI 48393-2417 U.S.A.
Tel: (248) 295-0310
Email: Solutions@acromag.com

8501060G

Table of Contents

1.0 GENERAL INFORMATION

1.1 Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the AcroPack module. It is not intended for a general, non-technical audience that is unfamiliar with AcroPack devices and their application.

1.2 Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag,

1.2.1 Trademark, Trade Name and Copyright Information

1.2.2 Class A Product Warning

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

1.2.3 Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

1.3 AcroPack Information – All Models

The AcroPack IO module are based on the PCI Express Mini Card Electromechanical specification and are 70mm in length with an add 100 pin field I/O connector.

The AcroPack is 19.05mm longer than the full length mini PCIe card at 50.95mm. It has the same mPCIe board width of 30mm and uses the same mPCIe standard board hold down standoff and screw keep out areas.

The AP482 board has ten 32-bit multifunction counter/timers. In addition, two digital input channels and six digital output channels are provided.

The AP483 board has five TTL and three RS422/RS485 32-bit multifunction counter/timers. In addition, one digital input channel and three digital output channels are provided.

The AP484 board has six RS422/RS485 32-bit multifunction counter/timers.

The AP48X modules utilizes state of the art Surface-Mounted Technology (SMT) to achieve its wide functionality and is an ideal choice for a wide range of industrial I/O applications that require a high-density, highly reliable, high-performance interface at a low cost.

The counters can be configured for quadrature position measurement, pulse width modulated output, watchdog timer, event counter, frequency measurement, pulse width measurement, period measurement, or one shot pulse output.

1.3.1 Ordering Information

The AcroPack ordering options are given in the following table.

Model Number	Temperature	I/O Type	Counters
AP482E-LF[1,2]	-40°C to 85°C	TTL	10
AP483E-LF[1,2]	-40°C to 85°C	TTL RS422/RS485	5 3
AP484E-LF[1,2]	-40°C to 85°C	RS422/RS485	6

Note 1: Operating temperature range for models:*-40°C to 85°C*. Applications requiring operating temperatures of *70°C to 85°C* will require purchase of *AcroPack Heatsink Accessory* ***AP-CC-01.***

AP-CC-01

AcroPack Heatsink Conduction Cool Kit

See Appendix A for installation instructions.

1.3.2 Key Features

- **TTL I/O** – 482 Counter/Timer I/O is available as TTL only. Mixed TTL and RS422/RS485 I/O options are available on the 483 models. Only RS422/RS485 I/O is available on the 484 models.

- **Quadrature Position Measurement –** Three input signals can be used to determine bi-direction motion. The sequence of logic high pulses for two input signals, A and B, indicate direction and a third signal (index) is used to initialize the counter. X1, X2, and X4 decoding is also implemented. X1 decoding executes one count per duty cycle of the A and B signals, while X2, and X4 execute two and four counts per duty cycle respectively.
- **Pulse Width Modulation** – Each counter can be programmed for pulse width modulation. The duration of the logic high and low levels of the output signal can be independently controlled. An external gate signal can also be used to start/stop generation of the output signal.
- **Watchdog Timer** – Each counter can be configured as a countdown timer for implementation as a watchdog timer. A gate-off signal is available for use to stop the count down operation. Interrupt generation upon a countdown to zero condition is available.
- **Event Counter** – Each counter can be configured to count input pulses or events. A gate-off signal is provided to control count-up or count down with each event. Interrupt generation upon programmed count condition is available.
- **Frequency Measurement** – Each counter can be configured to count how many active edges are received during a period defined by an external count enable signal. An interrupt can be generated upon measurement complete.
- **Pulse-Width or Period Measurement –** Each counter can be configured to measure pulse-width or waveform period. In addition, an interrupt can be generated upon measurement complete.
- **One-Shot and Repetitive One-Shot** – A one-shot pulse waveform may also be generated by each counter. The duration of the pulse and the delay until the pulse goes active is user programmable. A repetitive one-shot can be initiated with repetitive trigger pulses.
- **Programmable Interface Polarity –** The polarities of the counter's external trigger, input, and output pins are programmable for active high or low operation. These counter control signals are available through the board's field connector.
- **Internal or External Triggering –** A software or hardware trigger is selectable to initiate quadrature position measurement, pulse width modulation, watchdog countdown, event counting, frequency measurement, pulse-width measurement, period measurement, or one shot.

- **TTL Compatible Thresholds –** Input and output signal thresholds are at TTL levels.

1.3.3 Key Features PCIe Interface

- **PCIe Bus** – The AP module includes a PCI Express Generation 1 interface operating at a bus speed of 2.5 Gbps with one lane in each direction.
- **Compatibility** – PCI Express Base Specification v2.1 compliant PCI Express Endpoint.

1.4 Signal Interface Products

This AcroPack Module will mate directly to all Acromag AP carriers. Once connected, the module is accessed via a front panel connector.

The cables and termination panels are also available. For optimum performance with the AP440 digital I/O module, use of the shortest possible length of shielded I/O cable is recommended.

1.5 Software Support

The AcroPack series products require support drivers specific to your operating system. Supported operating systems include: Linux, Windows, and VxWorks

Windows®

Acromag provides software products (sold separately) to facilitate the development of Windows® applications interfacing with AcroPack modules, VPX I/O board products, and PCIe I/O Cards. This software (model APSW-API-WIN) consists of low-level drivers and Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

VxWorks®

Acromag provides a software product (sold separately) consisting of VxWorks® software. This software (Model APSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

Linux®

Acromag provides a software product consisting of Linux® software. This software (Model APSW-API-LNX) is composed of Linux® libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

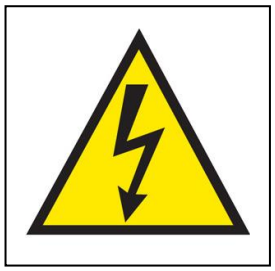
1.6 References

The following resources regarding AcroPack modules are available for download on Acromag's website or by contacting your sales representative.

- PCI Express MINI Card Electromechanical Specification, REV 1.2 https://www.pcisig.com

2.0 PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.

WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

2.1 Unpacking and Inspecting

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static-sensitive components and should only be handled at a static-safe workstation.

2.2 Installation Considerations

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

Refer to the specifications section for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

In an air cooled assembly, adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

In a conduction cooled assembly, adequate thermal conduction must be provided to prevent a temperature rise above the maximum operating temperature.

2.3 Board Configuration

Power should be removed from the board when installing AP modules, cables, termination panels, and field wiring. Model AP482/3/4 counter timer boards have no hardware jumpers or switches to configure.

2.4 Field I/O Connector

A field I/O interface connector provides a mating interface between the AP modules and the carrier board. The 100 pin ST5-50-1.50-L-D-P-TR Samtec connector is used on the AcroPack card as board to board interconnect. This connector will mate with the 100 pin SS5-50-3.00-L-D-K-TR Samtec connector on the carrier. The stack height is 4.5mm.

Threaded metric M2.5 screws and spacers are supplied with the carrier to provide additional stability for harsh environments.

Pin assignments are unique to each AP model. Tables 2.1 to 2.3 lists signal pin assignments for the module field I/O connector. Every other pin of the 100 pin connector is left unconnected in order to meet the minimum creepage distance required for 60 Volt isolation.

Table 2.1 AP482 Field I/O Connector Pin Assignments

68 Pin Champ Carrier Connector	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
1	1	1	2	In0_A
35	26	2	1	In1_A
			4	Reserved/isolation
			3	Reserved/isolation
2	2	3	6	In2_A
36	27	4	5	In3_A
			8	Reserved/isolation
			7	Reserved/isolation
3	3	5	10	In4_A
37	28	6	9	In5_A
			12	Reserved/isolation
			11	Reserved/isolation
4	4	7	14	In6_A
38	29	8	13	In7_A
			16	Reserved/isolation
			15	Reserved/isolation
5	5	9	18	In8_A
39	30	10	17	In9_A
			20	Reserved/isolation
			19	Reserved/isolation
6	6	11	22	In0_B
40	31	12	21	In1_B
			24	Reserved/isolation
			23	Reserved/isolation
7	7	13	26	In2_B
41	32	14	25	In3_B
			28	Reserved/isolation
			27	Reserved/isolation
8	8	15	30	In4_B
42	33	16	29	In5_B
			32	Reserved/isolation
			31	Reserved/isolation
9	9	17	34	In6_B
43	34	18	33	In7_B
			36	Reserved/isolation
			35	Reserved/isolation
10	10	19	38	In8_B
44	35	20	37	In9_B
			40	Reserved/isolation

			39	Reserved/isolation
11	11	21	42	In0_C
45	36	22	41	In1_C
			44	Reserved/isolation
			43	Reserved/isolation
12	12	23	46	In2_C
46	37	24	45	In3_C
			48	Reserved/isolation
			47	Reserved/isolation
13	13	25	50	In4_C
47	38	26	49	In5_C
			52	Reserved/isolation
			51	Reserved/isolation
14	14	27	54	In6_C
48	39	28	53	In7_C
			56	Reserved/isolation
			55	Reserved/isolation
15	15	29	58	In8_C
49	40	30	57	In9_C
			60	Reserved/isolation
			59	Reserved/isolation
16	16	31	62	Din0
50	41	32	61	Din1
			64	Reserved/isolation
			63	Reserved/isolation
17	17	33	66	Out0
51	42	34	65	Out1
			68	Reserved/isolation
			67	Reserved/isolation
18	18	35	70	Out2
52	43	36	69	Out3
			72	Reserved/isolation
			71	Reserved/isolation
19	19	37	74	Out4
53	44	38	73	Out5
			76	Reserved/isolation
			75	Reserved/isolation
20	20	39	78	Out6
54	45	40	77	Out7
			80	Reserved/isolation
			79	Reserved/isolation
21	21	41	82	Out8
55	46	42	81	Out9
			84	Reserved/isolation

			83	Reserved/isolation
22	22	43	86	DOut0
56	47	44	85	DOut1
			88	Reserved/isolation
			87	Reserved/isolation
23	23	45	90	DOut2
57	48	46	89	DOut3
			92	Reserved/isolation
			91	Reserved/isolation
24	24	47	94	DOut4
58	49	48	93	DOut5
			96	Reserved/isolation
			95	Reserved/isolation
25	25	49	98	External Clock
59	50	50	97	GND
			100	Reserved/isolation
			99	Reserved/isolation

Table 2.2 AP483 Field I/O Connector Pin Assignments

68 Pin Champ Carrier Connector	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
1	1	1	2	In0_A
35	26	2	1	In1_A
			4	Reserved/isolation
			3	Reserved/isolation
2	2	3	6	In2_A
36	27	4	5	In3_A
			8	Reserved/isolation
			7	Reserved/isolation
3	3	5	10	In4_A
37	28	6	9	In0_B
			12	Reserved/isolation
			11	Reserved/isolation
4	4	7	14	In1_B
38	29	8	13	In2_B
			16	Reserved/isolation
			15	Reserved/isolation
5	5	9	18	In3_B
39	30	10	17	In4_B
			20	Reserved/isolation
			19	Reserved/isolation

6	6	11	22	In0_C
40	31	12	21	In1_C
			24	Reserved/isolation
			23	Reserved/isolation
7	7	13	26	In2_C
41	32	14	25	In3_C
			28	Reserved/isolation
			27	Reserved/isolation
8	8	15	30	In4_C
42	33	16	29	Din 0
			32	Reserved/isolation
			31	Reserved/isolation
9	9	17	34	Out0
43	34	18	33	Out1
			36	Reserved/isolation
			35	Reserved/isolation
10	10	19	38	Out2
44	35	20	37	Out3
			40	Reserved/isolation
			39	Reserved/isolation
11	11	21	42	Out4
45	36	22	41	DOut0
			44	Reserved/isolation
			43	Reserved/isolation
12	12	23	46	DOut1
46	37	24	45	DOut2
			48	Reserved/isolation
			47	Reserved/isolation
13	13	25	50	In5_A+
47	38	26	49	In5_A-
			52	Reserved/isolation
			51	Reserved/isolation
14	14	27	54	In5_B+
48	39	28	53	In5_B-
			56	Reserved/isolation
			55	Reserved/isolation
15	15	29	58	In5_C+
49	40	30	57	In5_C-
			60	Reserved/isolation
			59	Reserved/isolation
16	16	31	62	Out5+
50	41	32	61	Out5-
			64	Reserved/isolation
			63	Reserved/isolation

17	17	33	66	In6_A+
51	42	34	65	In6_A-
			68	Reserved/isolation
			67	Reserved/isolation
18	18	35	70	In6_B+
52	43	36	69	In6_B-
			72	Reserved/isolation
			71	Reserved/isolation
19	19	37	74	In6_C+
53	44	38	73	In6_C-
			76	Reserved/isolation
			75	Reserved/isolation
20	20	39	78	Out6+
54	45	40	77	Out6-
			80	Reserved/isolation
			79	Reserved/isolation
21	21	41	82	In7_A+
55	46	42	81	In7_A-
			84	Reserved/isolation
			83	Reserved/isolation
22	22	43	86	In7_B+
56	47	44	85	In7_B-
			88	Reserved/isolation
			87	Reserved/isolation
23	23	45	90	In7_C+
57	48	46	89	In7_C-
			92	Reserved/isolation
			91	Reserved/isolation
24	24	47	94	Out7+
58	49	48	93	Out7-
			96	Reserved/isolation
			95	Reserved/isolation
25	25	49	98	External Clock
59	50	50	97	GND
			100	Reserved/isolation
			99	Reserved/isolation

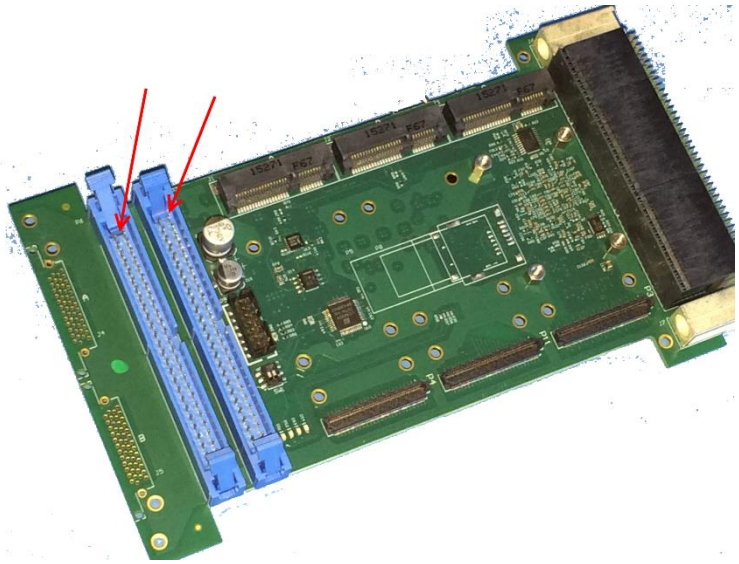
Table 2.3 AP484 Field I/O Connector Pin Assignments

68 Pin Champ Carrier Connector	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
1	1	1	2	In0_A+
35	26	2	1	In0_A-
			4	Reserved/isolation
			3	Reserved/isolation
2	2	3	6	In0_B+
36	27	4	5	In0_B-
			8	Reserved/isolation
			7	Reserved/isolation
3	3	5	10	In0_C+
37	28	6	9	In0_C-
			12	Reserved/isolation
			11	Reserved/isolation
4	4	7	14	Out0+
38	29	8	13	Out0-
			16	Reserved/isolation
			15	Reserved/isolation
5	5	9	18	In1_A+
39	30	10	17	In1_A-
			20	Reserved/isolation
			19	Reserved/isolation
6	6	11	22	In1_B+
40	31	12	21	In1_B-
			24	Reserved/isolation
			23	Reserved/isolation
7	7	13	26	In1_C+
41	32	14	25	In1_C-
			28	Reserved/isolation
			27	Reserved/isolation
8	8	15	30	Out1+
42	33	16	29	Out1-
			32	Reserved/isolation
			31	Reserved/isolation
9	9	17	34	In2_A+
43	34	18	33	In2_A-
			36	Reserved/isolation
			35	Reserved/isolation
10	10	19	38	In2_B+
44	35	20	37	In2_B-
			40	Reserved/isolation

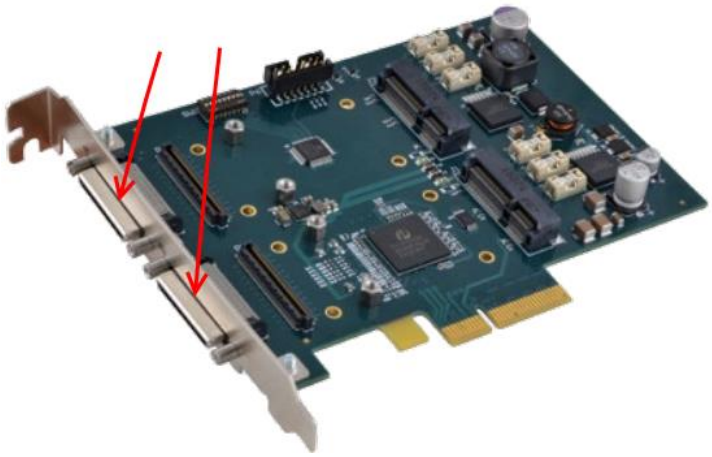
			39	Reserved/isolation
11	11	21	42	In2_C+
45	36	22	41	In2_C-
			44	Reserved/isolation
			43	Reserved/isolation
12	12	23	46	Out2+
46	37	24	45	Out2-
			48	Reserved/isolation
			47	Reserved/isolation
13	13	25	50	In3_A+
47	38	26	49	In3_A-
			52	Reserved/isolation
			51	Reserved/isolation
14	14	27	54	In3_B+
48	39	28	53	In3_B-
			56	Reserved/isolation
			55	Reserved/isolation
15	15	29	58	In3_C+
49	40	30	57	In3_C-
			60	Reserved/isolation
			59	Reserved/isolation
16	16	31	62	Out3+
50	41	32	61	Out3-
			64	Reserved/isolation
			63	Reserved/isolation
17	17	33	66	In4_A+
51	42	34	65	In4_A-
			68	Reserved/isolation
			67	Reserved/isolation
18	18	35	70	In4_B+
52	43	36	69	In4_B-
			72	Reserved/isolation
			71	Reserved/isolation
19	19	37	74	In4_C+
53	44	38	73	In4_C-
			76	Reserved/isolation
			75	Reserved/isolation
20	20	39	78	Out4+
54	45	40	77	Out4-
			80	Reserved/isolation
			79	Reserved/isolation
21	21	41	82	In5_A+
55	46	42	81	In5_A-

			84	Reserved/isolation
			83	Reserved/isolation
22	22	43	86	In5_B+
56	47	44	85	In5_B-
			88	Reserved/isolation
			87	Reserved/isolation
23	23	45	90	In5_C+
57	48	46	89	In5_C-
			92	Reserved/isolation
			91	Reserved/isolation
24	24	47	94	Out5+
58	49	48	93	Out5-
			96	Reserved/isolation
			95	Reserved/isolation
25	25	49	98	External Clock
59	50	50	97	GND
			100	Reserved/isolation
			99	Reserved/isolation

Note 1: **VPX4500-CC-LF is an example of a carrier that uses the ribbon cable connector see image of carrier.**



Note 2: **APCe7020E-LF is an example of a carrier that uses the Champ connector see image of carrier.**



Each 32-bit counter has three input and one output signal. For example counter 1 has the input signals labeled IN1_A, IN1_B, IN1_C and the output signal labeled OUT1.

2.5 Noise and Grounding Considerations

The board is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

2.6 Logic Interface Connector

The AP module logic edge connector interfaces to the mating connector on the carrier board. The pin assignments of this connector are standard for all AP modules according to the PCI Express MINI Card Electromechanical Specification, REV 1.2 (with exceptions shown in Table 2.2 and noted below).

Threaded metric M2.5 screws and spacers are supplied with the AP module to provide additional stability for harsh environments.

Power supplies +5, +12, and -12 Volt have been assigned to pins that are reserved in the mini-PCIe specification. The Present signal is grounded on the AP module. In addition, COEX1, COEX2 – wireless transmitter control are reassigned to JTAG signals TMS and TCK. Lastly, UIM_C4, UIM_C8 – reserved User Identity Module signals are reassigned to JTAG signals TDI and TDO.

Table 2.4: Logic Interface Connections

Pin #	Name	Pin #	Name
51	**+5V**[2]	52	+3.3V[3]
49	**+12V**[2]	50	GND
47	**-12V**[2]	48	+1.5V
45	**Present**[2]	46	N.C. (LED_WPAN#)[1]
43	GND	44	N.C. (LED_WLAN#)[1]
41	+3.3V[3]	42	N.C. (LED_WWAN#)[1]
39	+3.3V[3]	40	GND
37	GND	38	N.C. (USB_D+)[1]
35	GND	36	N.C. (USB_D-)[1]
33	PETp0	34	GND
31	PETn0	32	SMB_DATA[4]
29	GND	30	SMB_CLK[4]
27	GND	28	+1.5V
25	PERp0	26	GND
23	PERn0	24	+3.3V[4]
21	GND	22	PERST#
19	**TDI** (UIM_C4)[1]	20	N.C. (W_DISABLE#)[1]
17	**TDO** (UIM_C8)[1]	18	GND
15	GND	16	UIM_VPP
13	RECLK+	14	UIM_RESET
11	REFCLK-	12	UIM_CLK
9	GND	10	UIM_DATA
7	CLKREQ#	8	UIM_PWR
5	**TCK** (COEX2)[1]	6	+1.5V
3	**TMS** (COEX1)[1]	4	GND
1	N.C. (WAKE#)[1]	2	+3.3V[3]

Note 1: The following mini-PCIe signals are not used by the AP440: USB_D+, USB_D-, WAKE#, LED_WPAN#, LED_WLAN#, LED_WWAN#, W_DISABLE#, COEX1, COEX2, UIM_C4, UIM_C8.

Note 2: +5, +12, and -12 Volt power supplies have been assigned to pins that are reserved in the mini-PCIe specification. The Present signal is tied to circuit common on the AP module.

Note 3: All +3.3Vaux power pins are changed to system +3.3V power.

Note 4: The SM bus signals SMB_CLK and SMB_DATA will be used to clock a carrier location serial stream from the carrier. These signals are under the control of the AcroPack module.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the AP48X module.

The PCIe bus is defined to address three distinct address spaces: I/O, memory, and configuration space. The AcroPack module can be accessed via the PCIe bus memory space and configuration spaces, only.

The AcroPack configuration registers are initialized by system software at power-up to configure the card. The AcroPack module is a Plug-and-Play PCIe card. As a Plug-and-Play card the board's base address and system interrupt request are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCIe bus configuration access is used to access the AcroPack's configuration registers.

When the computer is first powered-up, the computer's system configuration software scans the PCIe bus to determine what PCIe devices are present. The software also determines the configuration requirements of the PCIe card.

The system software accesses the configuration registers to determine how many blocks of memory space the module requires. It then programs the board's configuration registers with the unique memory base address.

Since this board is not fixed in address space, its device driver must use the mapping information stored in the board's Configuration Space registers to determine where the board is mapped in memory space.

The configuration registers are also used to indicate that the board requires an interrupt request. The system software then programs the configuration registers with the interrupt request for the board.

CONFIGURATION REGISTERS

The PCIe specification requires software driven initialization and configuration via the Configuration Address space. This board provides 512 bytes of configuration registers for this purpose. It contains the configuration registers shown in the following table to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers and the Interrupt Register which must be read to determine the base address assigned to the board and the interrupt request that goes active on a board interrupt request.

Table 3.1 Configuration Registers

Reg. Num.	D31 D24	D23 D16	D15 D8	D7 D0
0	**Device ID** 0x7042 AP482 0x7043 AP483 0x7044 AP484		**Vendor ID** 16D5	
1	Status		Command	
2	Class Code=118000			Rev ID=00
3	BIST	Header	Latency	Cache
4	64-bit Memory Base Address for Memory Accesses to PCIe interrupt and I/O registers 4K Space **(BAR0)**			
5:10	Not Used			
11	**Subsystem ID** 0x7042 AP482 0x7043 AP483 0x7044 AP484		**Subsystem Vendor ID** 16D5	
12	Not Used			
13,14	Reserved			
15	Max_Lat	Min_Gnt	Inter. Pin	Inter. Line

This board is allocated a 4K byte block of memory (BAR0), to access the PCIe interrupt and I/O registers. The PCIe bus decodes 4K bytes for BAR0 for this memory space.

The memory space address map for the AP48X is shown in Table 3.2. Note that the base address for the board (BAR0) in memory space must be added to the addresses shown to properly access these AP48X registers. Register accesses as 32, 16, and 8-bit data in memory space are permitted. All the registers of the AP48X are accessed via data lines D0 to D31.

Table 3.2: AP482 Memory Map

BAR0 Base Address	Bit(s)	Description
0x0000 0000	7:0	Global Interrupt Enable and Pending Status
0x0000 0004	15:0	Location in System Register
0x0000 0008	15:0	Counters Interrupt Status/Clear Register
0x0000 000C	7:0	Counter Interrupt Enable/Disable Register

Notes:

1. The AP will respond to addresses that are "Not Used". The board will return "0" for all address reads that are not used or reserved.

Model AP483

Counters 0 to 4 TTL

Counter 5 to 7 RS485

Counters 8-9 Not Used

Model AP484

Counters 0 to 5 RS485

Counters 6 to 9 Not Used

0x0000 0010	15:0	Counter Trigger Register
0x0000 0014	15:0	Counter Stop Register
0x0000 0018	15:0	Load Read Back Register
0x0000 001C	15:0	Toggle Constant Register
0x0000 0020	15:0	Counter 0 Control Register
0x0000 0024	15:0	Counter 0 Interrupt Information Register
0x0000 0028	31:0	Counter 0 Read Back Register
0x0000 002C	31:0	Counter 0 Constant A Register
0x0000 0030	31:0	Counter 0 Constant A Register2
0x0000 0034	31:0	Counter 0 Constant B Register
0x0000 0038	31:0	Counter 0 Constant B Register2
0x0000 003C	31:0	NOT USED
0x0000 0040	15:0	Counter 1 Control Register
0x0000 0044	15:0	Counter 1 Interrupt Information Register
0x0000 0048	31:0	Counter 1 Read Back Register
0x0000 004C	31:0	Counter 1 Constant A Register
0x0000 0050	31:0	Counter 1 Constant A Register2
0x0000 0054	31:0	Counter 1 Constant B Register
0x0000 0058	31:0	Counter 1 Constant B Register2
0x0000 005C	31:0	NOT USED
0x0000 0060	15:0	Counter 2 Control Register
0x0000 0064	15:0	Counter 2 Interrupt Information Register
0x0000 0068	31:0	Counter 2 Read Back Register
0x0000 006C	31:0	Counter 2 Constant A Register
0x0000 0070	31:0	Counter 2 Constant A Register2
0x0000 0074	31:0	Counter 2 Constant B Register
0x0000 0078	31:0	Counter 2 Constant B Register2

0x0000 007C	31:0	NOT USED
0x0000 0080	15:0	Counter 3 Control Register
0x0000 0084	15:0	Counter 3 Interrupt Information Register
0x0000 0088	31:0	Counter 3 Read Back Register
0x0000 008C	31:0	Counter 3 Constant A Register
0x0000 0090	31:0	Counter 3 Constant A Register2
0x0000 0094	31:0	Counter 3 Constant B Register
0x0000 0098	31:0	Counter 3 Constant B Register2
0x0000 009C	31:0	NOT USED
0x0000 00A0	15:0	Counter 4 Control Register
0x0000 00A4	15:0	Counter 4 Interrupt Information Register
0x0000 00A8	31:0	Counter 4 Read Back Register
0x0000 00AC	31:0	Counter 4 Constant A Register
0x0000 00B0	31:0	Counter 4 Constant A Register2
0x0000 00B4	31:0	Counter 4 Constant B Register
0x0000 00B8	31:0	Counter 4 Constant B Register2
0x0000 00BC	31:0	NOT USED
0x0000 00C0	15:0	Counter 5 Control Register
0x0000 00C4	15:0	Counter 5 Interrupt Information Register
0x0000 00C8	31:0	Counter 5 Read Back Register
0x0000 00CC	31:0	Counter 5 Constant A Register
0x0000 00D0	31:0	Counter 5 Constant A Register2
0x0000 00D4	31:0	Counter 5 Constant B Register
0x0000 00D8	31:0	Counter 5 Constant B Register2
0x0000 00DC	31:0	NOT USED
0x0000 00E0	15:0	Counter 6 Control Register
0x0000 00E4	15:0	Counter 6 Interrupt Information Register

0x0000 00E8	31:0	Counter 6 Read Back Register
0x0000 00EC	31:0	Counter 6 Constant A Register
0x0000 00F0	31:0	Counter 6 Constant A Register2
0x0000 00F4	31:0	Counter 6 Constant B Register
0x0000 00F8	31:0	Counter 6 Constant B Register2
0x0000 00FC	31:0	NOT USED
0x0000 0100	15:0	Counter 7 Control Register
0x0000 0104	15:0	Counter 7 Interrupt Information Register
0x0000 0108	31:0	Counter 7 Read Back Register
0x0000 010C	31:0	Counter 7 Constant A Register
0x0000 0110	31:0	Counter 7 Constant A Register2
0x0000 0114	31:0	Counter 7 Constant B Register
0x0000 0118	31:0	Counter 7 Constant B Register2
0x0000 011C	31:0	NOT USED
0x0000 0120	15:0	Counter 8 Control Register
0x0000 0124	15:0	Counter 8 Interrupt Information Register
0x0000 0128	31:0	Counter 8 Read Back Register
0x0000 012C	31:0	Counter 8 Constant A Register
0x0000 0130	31:0	Counter 8 Constant A Register2
0x0000 0134	31:0	Counter 8 Constant B Register
0x0000 0138	31:0	Counter 8 Constant B Register2
0x0000 013C	31:0	NOT USED
0x0000 0140	15:0	Counter 9 Control Register
0x0000 0144	15:0	Counter 9 Interrupt Information Register
0x0000 0148	31:0	Counter 9 Read Back Register
0x0000 014C	31:0	Counter 9 Constant A Register
0x0000 0150	31:0	Counter 9 Constant A Register2

0x0000 0154	31:0	Counter 9 Constant B Register
0x0000 0158	31:0	Counter 9 Constant B Register2
0x0000 015C	31:0	NOT USED
0x0000 0160	31:0	Digital Input Register
0x0000 0164	31:0	Digital Output Register
0x0000 0168	15:0	XADC Status/Control Register
0x0000 016C	15:0	XADC Address Register
0x0000 0170→ 0x000001FC	31:0	NOT USED[2]
0x0000 0200	31:0	Firmware Revision
0x0000 0204	7:0	Flash Data
0x0000 0208	Bit-0	Flash Chip Select
0x0000 020C→ 0x000007FF	31:0	NOT USED[2]

Global Interrupt Enable Status Register (Read/Write) - (BAR0 + 0x0000 0000)

This read/write register is used to: enable board interrupt, determine the pending status of interrupts.

The function of each of the interrupt register bits are described in Table 3.3. This register can be read or written with either 8-bit, 16-bit, or 32-bit data transfers. A power-up or system reset sets all interrupt register bits to 0.

Table 3.3 Global Interrupt Register

Note that any registers/bits not mentioned will remain at the default value logic low.

Bit(s)	FUNCTION	
0	Board Interrupt Enable Bit. This bit must be set to logic "1" to enable generation of interrupts from the AP module. Setting this bit to logic "0" will disable board interrupts. (Read/Write Bit)	
	0	Disabled
	1	Enabled
1	Interrupt Pending Status Bit. This bit can be read to determine the interrupt pending status of the AP module. When this bit is logic "1" an interrupt is pending and will cause an interrupt request if bit-0 of the register is set. When this bit is logic "0" an interrupt is not being requested.	
	0	No Interrupt
	1	Interrupt Pending
14 to 2	Not Used	
15	Software Reset	

	0	No Reset
	1	Reset
32 - 17	Not Used	

Module Location In System Register (Read Only) - (BAR0 + 0x0000 0004)

This read only register is used identify the module's plugin location in a system.

Table 3.4 Location Register

Note that any registers/bits not mentioned will remain at the default value logic low.

Bit(s)	FUNCTION	
2 to 0	Module Site Location Bits. These bits identify the location on the carrier of the AP module.	
	000	Carrier Site A
	001	Carrier Site B
	010	Carrier Site C
	011	Carrier Site D
7 to 3	Module Slot Location Bits. These bits identify the slot location in a system of the AP module. The Carrier may use backplane signals as in a VPX system or an on carrier DIP switch to uniquely identify the system location of the carrier.	
	XXXXX	System Slot identification bits are described by the AcroPack carrier card.
31 to 8	Not Used	

Counters Interrupt Status/Clear Register (Read/Write) - (BAR0 + 0x0000 0008)

This read/write register is used to: determine the pending status of the Counter/Timer interrupts, and release pending interrupts.

The Counter/Timer interrupt status/clear bits 0 to 9 reflect the status of each of the Counter/Timers. A "1" bit indicates that an interrupt is pending for the corresponding counter/timer.

Read of this bit reflects the interrupt pending status of the counter timer logic.

0 = Interrupt Not Pending

1 = Interrupt Pending

Write a logic "1" to this bit to release a counter timer pending interrupt.

A Counter/Timer interrupt can be cleared by writing a "1" to its bit position in the Interrupt Status/Clear Register (writing a "1" acts as a reset signal to clear the set state). The interrupt will be generated again, if the

condition which caused the interrupt to occur remains. Writing "0" to a bit location has no effect. That is, a pending interrupt will remain pending.

The function of each of the interrupt register bits are described in Table 3.5. This register can be read or written with either 8-bit, 16-bit, or 32-bit data transfers. A power-up or system reset sets all interrupt register bits to 0.

Table 3.5 Counter Interrupt Status Clear Register

Note that any registers/bits not mentioned will remain at the default value logic low.

BIT	FUNCTION
0	Counter/Timer 0 Interrupt Pending/Clear
1	Counter/Timer 1 Interrupt Pending/Clear
2	Counter/Timer 2 Interrupt Pending/Clear
3	Counter/Timer 3 Interrupt Pending/Clear
4	Counter/Timer 4 Interrupt Pending/Clear
5	Counter/Timer 5 Interrupt Pending/Clear
6	Counter/Timer 6 Interrupt Pending/Clear
7	Counter/Timer 7 Interrupt Pending/Clear
8	Counter/Timer 8 Interrupt Pending/Clear
9	Counter/Timer 9 Interrupt Pending/Clear
10-31	Not Used

Counter Interrupt Enable/Disable Register (Read/Write) - (BAR0 + 0x0000 000C)

This read/write register is used to enable or disable interrupts.

The counter interrupts enable/disable bits 0 to 9 reflect whether interrupts are enabled or disabled for the particular counter. Counter interrupts are enabled by writing a "1" to its bit position in the Counter Interrupt Enable/Disable Register, and disabled by writing a "0". A Counter/Timer that is not interrupt enabled will never set its interrupt status flag. The Counter/Timer and its corresponding interrupt enable/disable bits are shown in Table 3.6.

A power-up or system reset sets all bit in the Counter Interrupt Enable/Disable Register to logic "0", disabling all counter interrupts.

Table 3.6 Counter Interrupt Enable Register

Note that any registers/bits not mentioned will remain at the default value logic low.

BIT	FUNCTION
0	Counter/Timer 0 Enable/Disable Interrupts
1	Counter/Timer 1 Enable/Disable Interrupts

2	Counter/Timer 2 Enable/Disable Interrupts
3	Counter/Timer 3 Enable/Disable Interrupts
4	Counter/Timer 4 Enable/Disable Interrupts
5	Counter/Timer 5 Enable/Disable Interrupts
6	Counter/Timer 6 Enable/Disable Interrupts
7	Counter/Timer 7 Enable/Disable Interrupts
8	Counter/Timer 8 Enable/Disable Interrupts
9	Counter/Timer 9 Enable/Disable Interrupts
10-31	Not Used

Counter Trigger Register (Write) - (BAR0 + 0x0000 0010)

This register is used to implement software triggering for all counter timers. Writing a 1 to the counter's corresponding trigger bit of this register will cause the counter function to be triggered. Table 3.7 identifies the trigger bit location corresponding to each of the counters. The contents of this register are not stored and merely act to trigger the corresponding counters.

Triggering may be used to initiate quadrature position measurement, pulse width modulation, watchdog timer (initiates countdown), event counting, frequency measurement, pulse-width measurement, period measurement, or one-shot.

Table 3.7 Counter Trigger Register

Note that any registers/bits not mentioned will remain at the default value logic low.

BIT	FUNCTION
0	Counter 0 Trigger
1	Counter 1 Trigger
2	Counter 2 Trigger
3	Counter 3 Trigger
4	Counter 4 Trigger
5	Counter 5 Trigger
6	Counter 6 Trigger
7	Counter 7 Trigger
8	Counter 8 Trigger
9	Counter 9 Trigger

10-31	Not Used

Counter Stop Register (Write) - (BAR0 + 0x0000 0014)

This register is used to stop the counters of one or a group of Counter/Timers. Writing a "1" to the counter's corresponding stop bit of this register will cause the counter to be disabled. That is, bits 2, 1, and 0 of the counter control register are cleared to "000" thus disabling the counter. Table 3.8 identifies the stop bit location corresponding to each of the counters. The bits of this register are not stored and merely act to stop the corresponding counter when set logic high.

Table 3.8 Counter Stop Register

Note that any registers/bits not mentioned will remain at the default value logic low.

BIT	FUNCTION
0	Counter 0 Stop
1	Counter 1 Stop
2	Counter 2 Stop
3	Counter 3 Stop
4	Counter 4 Stop
5	Counter 5 Stop
6	Counter 6 Stop
7	Counter 7 Stop
8	Counter 8 Stop
9	Counter 9 Stop
10-31	Not Used

Load Read Back Register (Write) - (BAR0 + 0x0000 0018)

This register is used to implement software load of the read back register for all counter/timers. Writing a "1" to the counter's corresponding load read back register bit will cause the current count to be loaded into the read back register. Table 3.9 identifies the load read back register bit corresponding to each of the counters. The contents of this register are not stored and merely act to load the read back registers of the corresponding counters.

Other methods are available to load the read back register. At the end of pulse, period or frequency measurement the read back register is automatically loaded. With Event Counting a pulse on InA when Control register bits 5 and 4 are set "11" will load the read back register. With Quadrature mode a pulse on InC when the Control register bits 9, 8 and 7 are set to "111" will load the read back register.

Table 3.9 Load Read Back Register

Note that any registers/bits not mentioned will remain at the default value logic low.

BIT	FUNCTION
0	Counter 0 Load Read Back Register
1	Counter 1 Load Read Back Register
2	Counter 2 Load Read Back Register
3	Counter 3 Load Read Back Register
4	Counter 4 Load Read Back Register
5	Counter 5 Load Read Back Register
6	Counter 6 Load Read Back Register
7	Counter 7 Load Read Back Register
8	Counter 8 Load Read Back Register
9	Counter 9 Load Read Back Register
10-31	Not Used

Toggle Counter Constants Register (Read/Write) - (BAR0 + 0x0000 001C)

This read/write register is used to toggle Counter Constant A and Counter Constant B for all counter/timers. Writing a "1" to the counter's corresponding toggle counter constants bit will cause the counter to use the values in Counter Constant A Register 2 and Counter Constant B Register 2. Writing a "0" will cause the counter to use the values in Counter Constant A Register and Counter Constant B Register. By default, a counter will always use the values in Counter Constant A Register and Counter Constant B Register. Table 3.10 identifies the toggle counter constants register bit corresponding to each of the counters.

A power-up or system reset clears the Toggle Counter Constants Register, setting all bits to "0".

Table 3.10 Toggle Counter Constant Register

Note that any registers/bits not mentioned will remain at the default value logic low.

BIT	FUNCTION
0	Counter 0 Toggle Counter Constants Register
1	Counter 1 Toggle Counter Constants Register
2	Counter 2 Toggle Counter Constants Register
3	Counter 3 Toggle Counter Constants Register
4	Counter 4 Toggle Counter Constants Register

5	Counter 5 Toggle Counter Constants Register
6	Counter 6 Toggle Counter Constants Register
7	Counter 7 Toggle Counter Constants Register
8	Counter 8 Toggle Counter Constants Register
9	Counter 9 Toggle Counter Constants Register
10-31	Not Used

Counter Control Register (Read/Write)

This register is used to configure counter/timer functionality. It defines the counter mode, output polarity, input polarity, clock source, and debounce enable.

The Counter Timer Module has ten 32-bit Counter/Timers. The Counter Control Register is cleared (set to 0) following a reset, thus disabling the counter/timer. Reading or writing to this register is possible via32-bit, 16-bit or 8-bit data transfers.

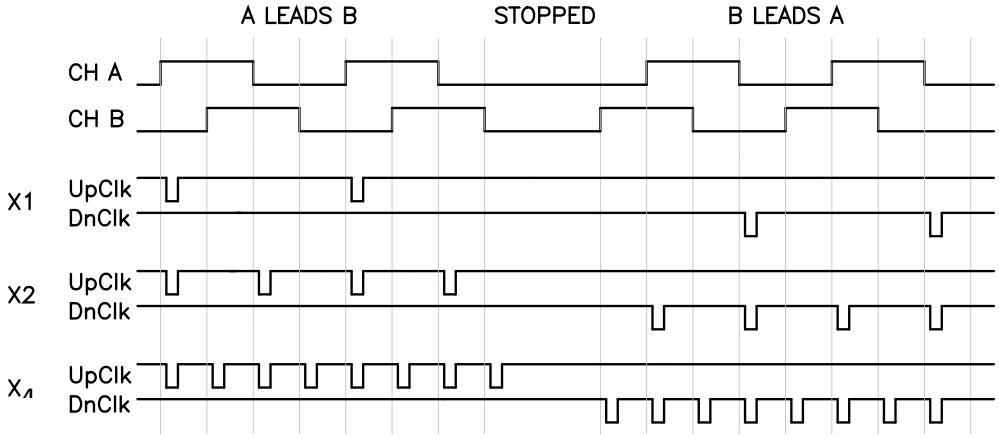
Eight modes of operation are provided: quadrature position measurement, pulse width modulation, watchdog timer, event counting, frequency measurement, pulse width measurement, period measurement, and one-shot pulse mode. The following sections describe the features of each method of operation and how to best use them.

Quadrature Position Measurement

The counter/timers may be used to perform position measurements from quadrature motion encoders. Bits 2 to 0 of the Counter Control Register set to logic "001" configure the counter for quadrature measurement.

A quadrature encoder can have up to three channels: A, B, and Index. When channel A leads channel B by 90° in a quadrature cycle, the counter increments. When channel B leads channel A by 90° in a quadrature cycle, the counter decrements. The number of increments or decrements per cycle depends on the type of encoding: X1, X2, or X4.

Figure 3.1 Quadrature Cycles with X4 Encoding



An X1 encoding Increment occurs on the rising edge of channel A when channel A leads channel B. An X1 encoding decrement occurs on the falling edge of channel A when channel B leads channel A.

For X2 encoding, two increments or decrements (on each edge of channel A) result from each cycle. The counter increments when A leads B and decrements when B leads A.

For X4 encoding, four increments or decrements (on each edge of channel A and B) result from each cycle. The counter increments when A leads B and decrements when B leads A.

Quadrature measurement must be triggered internally via the Counter Trigger Register. An initial software trigger starts quadrature position measurement operation.

InA and InB input signals are used to input the channel A and channel B input signals, respectively. The counter will increment when channel A leads channel B and will decrement when channel B leads channel A. Three rates of increments and decrements are available X1, X2, and X4 which are programmed via counter timer control register bits 5 and 4. Channel B is enabled for input by setting bit-6 to a logic "1".

InC can be used for the Index signal. Encoders that have an index channel can cause the counter to reload with the Counter Constant B value in a specified phase of the quadrature cycle. Reload can be programmed to occur in any one of the four phases in a quadrature cycle. You must ensure that the Index channel is high during at least a portion of the phase you specify for reload. The phase can be selected via the counter timer control register bits 9, 8, and 7 as seen in the following Table.

InC can alternately be used as an external load of the Read Back Register. The signal will be active high and will cause immediate load of the current count value into the Read Back Register. An interrupt will be generated upon hardware load of the Read Back Register (if interrupts are enabled). Load of the Read Back Register can also be implemented by software via the Load Read Back Register. The quadrature measurement value can be read from the Counter Read Back Register.

Table 3.11 Counter Control Register (Quadrature Position Measurement)

Bit(s)	FUNCTION	
2,1,0	Specifies the Counter Mode:	
	001	Quadrature Position Measurement
3	Output Polarity (Output Pin ACTIVE Level):	
	0	Active LOW (Default)[1]
	1	Active HIGH[1]
5, 4	InA / Channel A	
	00	Disabled (Default)
	01	X1 Encoding
	10	X2 Encoding
	11	X4 Encoding
6	InB / Channel B	
	0	Disabled (Default)
	1	Enabled
9,8,7	InC / Index: Channel Interrupt/Reload occurs when Index signal=1 and the A & B input signals are as selected below. See Control bits 14 & 13 for additional interrupt/load control.	
	000	Disabled (Default) 101 and 110 also Disable
	001	A = 0 , B = 1
	010	A = 1 , B = 0
	011	A = 1 , B = 1
	100	A = 0 , B = 0
	InC / Hardware Load Read Back Register	
	111	InC = 0: Inactive State InC = 1: Load Read Back Register on logic high pulse
12,11,10	Counter Operational Frequency Select	
	000	1.953125MHz
	001	3.90625MHz
	010	7.8125MHz
	011	15.625MHz

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

	100		62.5MHz
	101	Undefined	N/A
	110	External InB	CNTInB
	111	External Clock Enable (pin 49)	Up to 15MHz
14,13	Output and Interrupt Condition Select		
	00	No Output or Interrupt Selected	
	01	Output and Interrupt on counter equal Constant A Register	
	10	Output and Interrupt on Index and reload on Index	
	11	Output and Interrupt on Index but do not reload counter on Index.	
15	Input Debounce Enable		
	0	Disabled (Default) – No Debounce Applied to any Input.	
	1	Enabled – Reject A, B, or Index Pulses less than or equal to 2.4μs.	

An interrupt can be generated upon index reload, or when the counter value equals the constant value stored in the Counter Constant A Register. Interrupts must be enabled via the Enable/Disable Counter Interrupts Register. The interrupt type must also be selected via bits 13 and 14 of the Counter Control Register. The interrupt will remain pending until released by setting the required bit of the Counter/Timer Interrupt Status/Clear register. Note that interrupts in Quadrature Position Measurement are generated whenever the interrupt conditions exist. If a pending interrupt is cleared, but the interrupt conditions still exists, another interrupt will be generated.

The Counter Control register bits 14 and 13 are used to control the operation of the counter output signal. With bits 14 and 13 set to "01", the output signal will be driven active while the counter equals the counter Constant A value. With bit 14 set to logic "1" the output signal will be driven active while the index condition remains true.

Encoder output signals can be noisy. It is recommended that the InA, InB, and InC input signals be debounced by setting bit-15 of the Counter Control register to logic "1". Noise transitions less than 2.4μs will be removed with debounce enabled.

Pulse Width Modulation

Pulse width modulated waveforms may be generated at the counter timer output. The pulse width modulated waveform is generated continuously. Pulse Width Modulation generation is selected by setting Counter Control Register bits 2 to 0 to logic "010".

Counter Constant A value controls the time until the pulse goes active. The duration of the pulse is set via the Counter Constant B register. Note that a high pulse will be generated if active high output is selected while a low pulse will be generated if active low output is selected.

The counter goes through a countdown sequence for each Counter Constant value. When the 0 count is detected, the output toggles to the opposite state. Then the second Counter Constant value is loaded into the counter, and countdown resumes, decrementing by one for each rising edge of the clock selected via Control Register bits 12, 11, and 10. For example, a counter constant value of 3 will provide a pulse duration of 3 clock cycles of the selected clock. Note, when the maximum internal clock frequency is selected 62.5MHz, a delay of one extra clock cycle will be added to the counter constant value.

InA can be used as a Gate-Off signal to stop and start the counter and thus the pulse-width modulated output. When InA is enabled via bits 5 and 4 of the control register for active low Gate-Off input, a logic low input will enable pulse-width modulation counting while a logic high will stop PWM counting. When InA is enabled for active high Gate-Off operation, a logic high will enable PWM counting while a logic low will stop PWM counting.

InB can be used to input an external clock for use in PWM. Bits 7 and 6 must be set to either logic "01" or "10". Additionally, the clock source bits 12, 11, and 10 must be set to logic "110" to enable external clock input. PWM can also be internally clocked enabled using control register bits 12, 11, and 10.

InC can be used to externally trigger Pulse Width Modulation generation. Additionally, PWM can be triggered internally via the Counter Trigger Register. An initial trigger, software or external, causes the pulse width modulated signal to be generated. After an initial trigger do not issue additional triggers. Triggers issued while running will cause the Constant A and B values to load at the wrong time. In addition, changing the Control register setting while running can also cause the Constant A and B values to load at the wrong time.

By enabling interrupts via the Enable/Disable Interrupts Register, an interrupt can be generated when the output pulse transitions from low to high and also for transitions from high to low. Thus, an interrupt is generated at each pulse transition.

Table 3.12 Counter Control Register (Pulse Width Modulation)

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

Bit(s)	FUNCTION		
2,1,0	Specifies the Counter Mode:		
	010	Pulse Width Modulation	
3	Output Polarity (Output Pin ACTIVE Level):		
	0	Active LOW (Default)[1]	
	1	Active HIGH	
5, 4	InA Polarity / Gate-Off Polarity		
	00	Disabled (Default)	
	01	Active LOW In A=0 Counter is Enabled In A=1 Counter is Disabled	
	10	Active HIGH In A=0 Counter is Disabled In A=1 Counter is Enabled	
	11	Disabled	
7, 6	InB Polarity / External Clock Input		
	00	Disabled (Default)	
	01	External Clock Enabled	
	10	External Clock Enabled	
	11	Disabled	
9,8	InC Polarity / External Trigger		
	00	Disabled (Default)	
	01	Active LOW External Trigger	
	10	Active HIGH External Trigger	
	11	Disabled	
12,11,10	Clock Enable Frequency		
	000	Internal (Default)	1.953125MHz
	001	Internal	3.90625MHz
	010	Internal	7.8125MHz
	011	Internal	15.625MHz
	100	Internal	62.5MHz
	101	Undefined	N/A
	110	External InB	CNTInB
	111	External Clock (pin 49)	Up to 15MHz
14 ,13	Not Used (bits read back as 0)		
15	Input Debounce Enable		
	0	Disabled (Default) – No Debounce Applied to any Input.	
	1	Enabled – Reject Gate-Off or Trigger Pulses (noise) less than or equal to 2.4µs.	

Watchdog Timer Operation

The watchdog operation counts down from a programmed (Counter Constant A) value until it reaches 0. While counting, the counter output will be in its active state (the output polarity is programmable). Upon time-out, the counter output will return to its inactive state, and an optional interrupt may be generated. Watchdog operation is selected by setting Counter Control Register bits 2 to 0 to logic "011".

A timed-out watchdog timer will not re-cycle until it is reloaded and then followed with a new trigger. Failure to cause a reload would generate an automatic time-out upon re-triggering, since the counter register will contain the 0 it previously counted down to.

InA input can be used to reload the counter with the Constant A register value. InA reload input is enabled via Control register bits 5 and 4. The counter can also be reloaded via a software write to the Counter Constant A register. Writing to the Counter Constant A register will load the value directly into the counter even if watchdog counting is actively counting down.

InB can be used to input an external clock for watchdog timing. Bits 7 and 6 must be set to either logic "01" or "10". Additionally, the clock source bits 12, 11, and 10 must be set to logic "110" to enable external InB clock input. The timer can alternatively be clock enabled via an internal frequencies as selected via control register bits 12, 11, and 10.

InC can be used to either continue/stop watchdog counting or as an external trigger input. When control register bits 9 and 8 are set to logic "11", InC functions as a Continue/Stop signal. When the Continue/Stop signal is high the counter continues counting (when low the counter stops counting). Alternately, when control register bits 9 and 8 are set to logic "01" or "10", the InC input functions as an external trigger input. The watchdog timer may also be internally triggered via the Trigger Control Register.

When triggered, the counter/timer contents are decremented by one for each clock cycle, until it reaches 0, upon which a watchdog timer time-out occurs. For example, a counter constant value of 30 will provide a time-out delay of 30 clock cycles of the selected clock. However, due to the asynchronous relationship between the trigger and the selected clock, one clock cycle of error can be expected. The counter can be read from the Counter Readback register at any time during watchdog operation.

Upon time-out, the counter output pin returns to its inactive state. The Counter/Timer Module will also issue an interrupt upon detection of a count value equal to 0, if enabled via the Interrupt Enable/Disable Register. This could be useful for alerting the host that a watchdog timer time-out has occurred and may need to be reinitialized. The interrupt will remain

pending until the watchdog timer is reinitialized and the interrupt is released by setting the required bit of the Counter/Timer Interrupt Status/Clear register.

Table 3.13 Counter Control Register (Watchdog Timer)

Bit(s)	FUNCTION		
2,1,0	Specifies the Counter Mode:		
	011	Watchdog Function	
3	Output Polarity (Output Pin ACTIVE Level):		
	0	Active LOW (Default)[1]	
	1	Active HIGH	
5, 4	InA Polarity / Counter Reload		
	00	Disabled (Default)	
	01	Active LOW In A=0 Counter Reinitialized In A=1 Inactive State	
	10	Active HIGH In A=0 Inactive State In A=1 Counter Reinitialized	
	11	Disabled	
7, 6	InB Polarity / External Clock Input		
	00	Disabled (Default)	
	01	External Clock Enabled	
	10	External Clock Enabled	
	11	Disabled	
9,8	InC Polarity / External Trigger		
	00	Disabled (Default)	
	01	Active LOW Trigger	
	10	Active HIGH Trigger	
	11	Gate-Off (Continue when high/Stop when low)	
12,11,10	Clock Enable Frequency		
	000	Internal (Default)	1.953125MHz
	001	Internal	3.90625MHz
	010	Internal	7.8125MHz
	011	Internal	15.625MHz
	100	Internal	62.5MHz
	101	Undefined	N/A
	110	External InB	CNTInB
	111	External Clock (pin 49)	Up to 15MHz
14 ,13	Not Used (bits read back as 0)		
15	Input Debounce Enable		
	0	Disabled (Default) – No Debounce Applied to any Input.	

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

	1	Enabled – Reject Gate-Off or Trigger Pulses (noise) less than or equal to 2.4µs.

Event Counting Operation

Positive or negative polarity events can be counted. Event Counting is selected by setting Counter Control Register bits 2 to 0 to logic "100" and setting bits 12 to 10 to logic "000".

Input pulses or events occurring at the input InB of the counter will increment the counter until it reaches the Counter Constant A value. Upon reaching the count limit, an output pulse of 1.728µs will be generated at the counter output pin, and an optional interrupt may be generated. Additionally, the internal event counter is cleared. The counter will continue counting, again from 0, until it reaches the Counter Constant A value. Once triggered, event counting will continue until disabled via Control register bits 2 to 0.

InA can be used as a Gate-Off signal to stop and start event counting, or as an active high hardware load of Read Back Register signal. When InA is enabled via bits 5 and 4 of the control register for active low Gate-Off input, a logic low input will enable event counting while a logic high will stop event counting. When InA is enabled for active high Gate-Off operation, a logic high will enable event counting while a logic low will stop event counting. When InA is enabled for hardware load of Read Back Register, an active high signal will cause load of the Read Back Register and an interrupt will be generated (if interrupts are enabled). The Read Back Register can also be loaded by software via the Load Read Back Register.

InB is used as the event input signal. Active high or low input events can be selected via Control register bits 7 and 6. A minimum event pulse width (InB) of 30ns is required for correct pulse detection with input debounce disabled. Programmable clock selection is not required in event counter mode.

InC can be used to either control up/down counting or as an external trigger input. When control register bits 9 and 8 are set to logic "11", InC functions as an Up/Down signal. When the Up/Down signal is high the counter is in the count down mode (when low the counter counts up). The counter will not count down below a count of zero. Alternately, when control register bits 9 and 8 are set to logic "01" or "10", the InC input functions as an external trigger input. Event counting may also be internally triggered via the Trigger Control Register.

The Counter Constant A Register holds the count-to value (constant). Reading the Counter Read Back Register will return the current count (variable). **The Counter Constant A value must not be left as 0**. The counter upon trigger

starts counting from 0 and since the counter would match the count-to value the counter resets and starts counting from zero again.

If interrupts are enabled via the Enable/Disable Interrupts Register, an interrupt is generated when the number of input pulse events is equal to the Counter Constant A register value. The internal counter is then cleared and will continue counting events until the counter constant A value is again reached and a new interrupt generated. An interrupt will remain pending until released by setting the required bit of the Counters Interrupt Status/Clear register.

Table 3.14 Counter Control Register (Event Counting)

Bit(s)	FUNCTION	
2,1,0	Specifies the Counter Mode:	
	100	Event Counting
3	Output Polarity (Output Pin ACTIVE Level):	
	0	Active LOW (Default)[1]
	1	Active HIGH
5, 4	InA Polarity / Gate-Off	
	00	Disabled (Default)
	01	Active LOW In A=0: Continue Counting In A=1: Stop Counting
	10	Active HIGH In A=0: Stop Counting In A=1: Continue Counting
	InA Hardware Capture Count Mode	
	11	InA = logic high pulse: Causes load of the Read Back register
7, 6	InB Polarity / Event Input	
	00	Disabled (Default)
	01	Active LOW Events
	10	Active HIGH Events
	11	Disabled
9,8	InC Polarity / External Trigger	
	00	Disabled (Default)
	01	Active LOW Trigger
	10	Active HIGH Trigger
	11	Count Up when logic low /Down when logic high
12,11,10	Specifies the Counter Mode:	
	000	Event Counting
14 ,13	Not Used (bits read back as 0)	
15	Input Debounce Enable	
	0	Disabled (Default) – No Debounce Applied to any Input.

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

	1	Enabled – Reject Gate-Off or Trigger Pulses (noise) less than or equal to 2.4µs.

Frequency Measurement Operation

Frequency Measurement is selected by setting Counter Control Register bits 2 to 0 to logic "100" and setting bits 12 to 10 to logic "111". The counter counts how many InB edges (low to high or high to low) are received during the InA enable interval. The frequency is the number of counts divided by the duration of the InA enable signal.

InA is used as an enable signal to start frequency measurement. The InA signal must be a pulse of known width. When InA is configured (via bits 5 and 4 of the control register) as an active low enable input, a logic low input will enable frequency measurement while a logic high will stop frequency measurement. When InA is configured as an active high enable signal, a logic high will enable frequency measurement while a logic low will stop frequency measurement.

InB is used to input the signal whose frequency is to be measured. Input pulses occurring at input InB of the counter are counted while the enable signal present on InA is active. When the InA signal goes inactive, the counter output will generate a 1.73µs output pulse and an optional interrupt.

InC can be used as an external trigger input. When control register bits 9 and 8 are set to logic "01" or "10", the InC input functions as an external trigger input. Frequency measurement may also be internally triggered via the Trigger Control Register. An initial trigger, software or external, starts frequency measurement upon the active edge of the InA enable signal.

The Counter Constant A Register is not used for frequency measurement. Do not write to this register while the counter is actively counting since this will cause the counter to be loaded with the Constant A value.

Reading the Counter Read Back Register will return the current count (variable). A minimum event pulse width (30ns InB) is required for correct pulse detection with input debounce disabled. With debounce enabled, a minimum event pulse width of 2.4µs is required for correct pulse detection. Programmable clock selection is not available for frequency measurement.

If interrupts are enabled via the Enable/Disable Interrupts Register, an interrupt is generated when the input InA enable pulse goes inactive. An

interrupt will remain pending until released by setting the required bit of the Interrupt Status/Clear register.

Table 3.15 Counter Control Register (Frequency Measurement)

Bit(s)	FUNCTION	
2,1,0	Specifies the Counter Mode:	
	100	Frequency Measurement
3	Output Polarity (Output Pin ACTIVE Level):	
	0	Active LOW (Default)[1]
	1	Active HIGH
5, 4	InA Polarity / Enable Pulse of Known Width	
	00	Disabled (Default)
	01	Active LOW Pulse
	10	Active HIGH Pulse
	11	Disabled
7, 6	InB Polarity / Signal Measured/Counted	
	00	Disabled (Default)
	01	Active LOW Pulse Counted
	10	Active HIGH Pulse Counted
	11	Disabled
9,8	InC Polarity / External Trigger	
	00	Disabled (Default)
	01	Active LOW Trigger
	10	Active HIGH Trigger
	11	Disabled
12,11,10	Specifies the Counter Mode:	
	111	Frequency Measurement
14 ,13	Not Used (bits read back as 0)	
15	Input Debounce Enable	
	0	Disabled (Default) – No Debounce Applied to any Input.
	1	Enabled – Reject Gate-Off or Trigger Pulses (noise) less than or equal to 2.4µs.

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

Input Pulse Width Measurement

Setting bits 2 to 0 of the Counter Control Register to logic "101" configures the counter for pulse-width measurement. After pulse-width measurement is triggered, the first input pulse is measured.

InA is used to input the pulse to be measured. An active low or high pulse can be measured.

InB can be used to input an external clock for use in PWM. Bits 7 and 6 must be set to either logic "01" or "10". Additionally, the clock source bits 12, 11, and 10 must be set to logic "110" to enable external clock input. PWM can also be internally clock enabled using control register bits 12, 11, and 10.

InC can be used to externally trigger Pulse Width Measurement. Additionally, Pulse Width Measurement can be triggered internally via the Counter Trigger Register. An initial trigger, software or external, starts pulse width measurement at the beginning of the next active pulse.

For pulse-width measurement, the pulse-width being measured serves as an enable control for an up-counter whose value can be read from the Counter Read Back Register. When triggered, the counter is reset and then increments by one for each clock pulse while the input signal level remains in the active state (high or low according to the programmed polarity of input InA). The resultant pulse-width is equivalent to the count value read from the Counter Read Back Register, multiplied by the clock period. An output pulse will be generated at the counter output pin to signal the completion of a given measurement. Note that the measured pulse may be in error by $\pm$ 1 clock cycle.

Reading a counter value of 0xFFFFFFFF hex indicates that the pulse duration is longer than the current counter size and clock frequency can measure. Upon reading of this overflow value you must select a slower frequency and re-measure.

An interrupt can be generated upon completion of a given pulse width measurement (the pulse has returned to the opposite polarity), if enabled via the interrupt Enable/Disable Register. The interrupt will remain pending until released by setting the required bit of the Interrupt Status/Clear register.

Table 3.16 Counter Control Register (Pulse Width Measurement)

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

Bit(s)	FUNCTION		
2,1,0	Specifies the Counter Mode:		
	101	Pulse-Width Measurement	
3	Output Polarity (Output Pin Active Level):		
	0	Active LOW (Default)[1]	
	1	Active HIGH	
5, 4	InA Polarity / Pulse Polarity to be Measured		
	00	Disabled (Default)	
	01	Active LOW Pulse is Measured	
	10	Active HIGH Pulse is Measured	
	11	Disabled	
7, 6	InB Polarity / External Clock Input		
	00	Disabled (Default)	
	01	External Clock Enabled InB or Pin 49	
	10	External Clock Enabled InB or Pin 49	
	11	Disabled	
9,8	InC Polarity / External Trigger		
	00	Disabled (Default)	
	01	Active LOW Trigger	
	10	Active HIGH Trigger	
	11	Disabled	
12,11,10	Clock Enable Frequency		
	000	Internal (Default)	1.953125MHz
	001	Internal	3.90625MHz
	010	Internal	7.8125MHz
	011	Internal	15.625MHz
	100	Internal	62.5MHz
	101	Undefined	N/A
	110	External InB	CNTInB
	111	External Clock (pin 49)	Up to 15MHz
14 ,13	Not Used (bits read back as 0)		
15	Input Debounce Enable		
	0	Disabled (Default) – No Debounce Applied to any Input.	
	1	Enabled – Reject Gate-Off or Trigger Pulses (noise) less than or equal to 2.4μs.	

Input Period Measurement

The counter/timer may be used to measure the period of an input signal at the counter input InA. Setting bits 2 to 0 of the Counter Control Register to logic "110" configures the counter for period measurement. The first input cycle after period measurement is triggered will be measured.

InA is used to input the signal to be measured. Period measurement can be initiated on the active low or high portion of the waveform. The period of signal is the time the signal is low added to the time the signal is high, before it repeats.

InB can be used to input an external clock for use in period measurement. Bits 7 and 6 must be set to either logic "01" or "10". Additionally, the clock source bits 12, 11, and 10 must be set to logic "110" to enable external clock input. Period measurement can also use an internally clock enabled frequency using control register bits 12, 11, and 10.

InC can be used to externally trigger period measurement. Additionally, Period Measurement can be triggered internally via the Counter Trigger Register. An initial trigger, software or external, starts period measurement at the beginning of the next active period.

The period being measured serves as an enable control for an up-counter whose value can be read from the Counter Read Back Register. When triggered the counter is reset. Then, the active polarity of InA starts period measurement. The counter increments by one for each clock pulse during the input signal period (InA). The resultant period is equivalent to the count value read from the Counter Read Back Register, multiplied by the clock period. A 1.728μs output pulse will be generated at the counter output pin to signal the completion of a given measurement. Note that the measured period may be in error by $\pm$ 1 clock cycle.

Reading a counter value of 0xFFFFFFFF hex indicates that the pulse duration is longer than the current counter size and clock frequency can measure. Upon reading of this overflow value you must select a slower frequency and re-measure.

An interrupt can be generated upon completion of a given period measurement, if enabled via the Interrupt Enable/Disable Register. The interrupt will be generated upon completion of the first complete waveform cycle after the counter is triggered. The interrupt will occur even if an external clock is selected but no clock signal is provided on InB. The count value will be zero in this case. The interrupt, once driven active, will remain pending until released by setting the required bit of the Interrupt Status/Clear register.

Table 3.17 Counter Control Register (Period Measurement)

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

Bit(s)	FUNCTION		
2,1,0	Specifies the Counter Mode:		
	110	Period Measurement	
3	Output Polarity (Output Pin ACTIVE Level):		
	0	Active LOW (Default)[1]	
	1	Active HIGH	
5, 4	InA Polarity / Signal Measured		
	00	Disabled (Default)	
	01	Active LOW starts period measurement.	
	10	Active HIGH starts period measurement.	
	11	Disabled	
7, 6	InB Polarity / External Clock Input		
	00	Disabled (Default)	
	01	External Clock Enabled	
	10	External Clock Enabled	
	11	Disabled	
9,8	InC Polarity / External Trigger		
	00	Disabled (Default)	
	01	Active LOW Trigger	
	10	Active HIGH Trigger	
	11	Disabled	
12,11,10	Clock Enable Frequency		
	000	Internal (Default)	1.953125MHz
	001	Internal	3.90625MHz
	010	Internal	7.8125MHz
	011	Internal	15.625MHz
	100	Internal	62.5MHz
	101	Undefined	N/A
	110	External InB	CNTInB
	111	External Clock (pin 49)	Up to 15MHz
14 ,13	Not Used (bits read back as 0)		
15	Input Debounce Enable		
	0	Disabled (Default) – No Debounce Applied to any Input.	
	1	Enabled – Reject Gate-Off or Trigger Pulses (noise) less than or equal to 2.4μs.	

One-Shot Pulse Mode

One-Shot pulse mode provides an output pulse that is asserted one time or repeated each time it is re-triggered. One-Shot generation is selected by setting Counter Control Register bits 2 to 0 to logic "111".

The Counter Constant A value controls the time until the pulse goes active. The duration of the pulse high or low is set via the Counter Constant B value. Note that the Constant B value defines the logic high pulse width, if active high output is selected, and a low pulse if active low output is selected.

The counter goes through a full countdown sequence for each Counter Constant value. When the 0 count is detected, on the next rising-edge of the clock, the output toggles to the opposite state, and the Counter Constant B value is loaded into the counter and countdown resumes, decrementing by one each clock cycle. For example, a counter constant value of 7 will provide a pulse duration of 7 clock cycles of the selected clock, then 16ns will be added for the count detection of 0.

InA can be used as a Gate-Off signal to stop and start the counter and, thus output. When InA is enabled via bits 5 and 4 of the control register for active low Gate-Off input, a logic low input will enable the one-shot counter while a logic high will stop the one-shot counter. When InA is enabled for active high Gate-Off operation, a logic high will enable the one-shot counter while a logic low will stop the one-shot counter.

InB can be used to input an external clock for use in One-Shot Pulse mode. Bits 7 and 6 must be set to either logic "01" or "10". Additionally, the clock source bits 12, 11, and 10 must be set to logic "110" to enable external clock input. One-Shot Pulse mode can also select an internal clock enabled frequency using control register bits 12, 11, and 10.

InC can be used to externally trigger One-Shot pulse mode. Additionally, a one-shot pulse can be triggered internally via the Counter Trigger Register. An initial trigger, software or external, causes the one-shot signal to be generated with no additional triggers required. Additional triggers must not be input until the one shot pulse has completed count down of the Constant B value.

If interrupts are enabled via the Enable/Disable Interrupts Register, an interrupt is generated when the pulse transitions from low to high and also when the pulse transitions from high to low. The interrupt will remain pending until released by setting the required bit of the Interrupt Status/Clear register.

Table 3.18 Counter Control Register (One-Shot Mode)

1. The default state of the output pin is high (output has pullup resistor installed). Bit 3 specifies the active output polarity when the output is driven.

Bit(s)	FUNCTION		
2,1,0	Specifies the Counter Mode:		
	111	One-Shot Generation	
3	Output Polarity (Output Pin ACTIVE Level):		
	0	Active LOW (Default)[1]	
	1	Active HIGH	
5, 4	InA Polarity / Gate-Off Polarity		
	00	Disabled (Default)	
	01	Active LOW In A=0 Output Enabled In A=1 Output Disabled	
	10	Active HIGH In A=0 Output Disabled In A=1 Output Enabled	
	11	Disabled	
7, 6	InB Polarity / External Clock Input		
	00	Disabled (Default)	
	01	External Clock Enabled	
	10	External Clock Enabled	
	11	Disabled	
9,8	InC Polarity / External Trigger		
	00	Disabled (Default)	
	01	Active LOW Trigger	
	10	Active HIGH Trigger	
	11	Disabled	
12,11,10	Clock Enable Frequency		
	000	Internal (Default)	1.953125MHz
	001	Internal	3.90625MHz
	010	Internal	7.8125MHz
	011	Internal	15.625MHz
	100	Internal	62.5MHz
	101	Undefined	N/A
	110	External InB	CNTInB
	111	External Clock (pin 49)	Up to 15MHz
14 ,13	Not Used (bits read back as 0)		
15	Input Debounce Enable		
	0	Disabled (Default) – No Debounce Applied to any Input.	
	1	Enabled – Reject Gate-Off or Trigger Pulses (noise) less than or equal to 2.4μs.	

Counter Interrupt Information Register (Read Only)

This read only register provides information on what type of interrupt has been generated. This is useful for Quadrature Position Measurement and Event Counting, as it is possible to have more than one interrupt condition in these modes. Each bit position is representative of an interrupt condition. The interrupt conditions for each of the bits can be seen in Table 3.19 below. A "1" indicates that the interrupt condition represented by that bit has occurred. The bit will remain a "1" until the pending interrupt is cleared by writing a "1" to the corresponding bit in the Interrupt Pending/Clear Register.

A power-up or system reset clears the Counter Interrupt Information Register, setting all bits to "0".

Table 3.19 Counter Interrupt Information Register

Note that any registers/bits not mentioned will remain at the default value logic low.

BIT	FUNCTION
0	Counter equal to value in Counter Constant A Register (available in Event Counting and Quadrature Position Measurement)
1	Read Back Register has been loaded by hardware (available in Event Counting and Quadrature Position Measurement)
2	Index Pulse (available in Quadrature Position Measurement)
3	High to Low or Low to High Transitions (available in Pulse Width Modulation or One-Shot Pulse Mode)
4	End of Measurement (available in Frequency Measurement, Input Period Measurement, or Input Pulse Width Measurement)
5	Time Out (available in Watchdog Timer)
6-31	Not Used

Counter Read Back Register (Read Only)

This read-only register is a dynamic function register that returns the current value held in the counter. It is updated with the value stored in the internal counter each time a hardware or software load of the Read Back Register is implemented.

The internal counter is generally initialized with the value in the Counter Constant Register, and its value is incremented or decremented according to the application.

This register must be read using 32-bit accesses.

Counter Constant A Register (Read/Write)

Note that the Counter Constant Registers are cleared (set to 0) following a system or software reset.

This read/write register is used to store the counter/timer constant A value (initial value) for the various counting modes. It is necessary to load the constant value into the counter in one clock cycle. Thus, access to this register is allowed on a 32-bit basis, only.

The contents of the Counter Constant A and Counter Constant A Register 2 can be toggled for the counter/timers. Writing a "1" to the counter's corresponding toggle counter constants bit will cause the counter to use the values in Counter Constant A Register 2. Writing a "0" will cause the counter to use the values in Counter Constant A. By default, a counter will always use the values in Counter Constant A Register.

Counter Constant A Register 2 (Read/Write)

Note that the Counter Constant Registers are cleared (set to 0) following a system or software reset.

This read/write register is used to store the counter/timer constant A register 2 value (initial value) for the various counting modes. It is necessary to load the constant value into the counter in one clock cycle. Thus, access to this register is allowed on a 32-bit basis, only.

The contents of the Counter Constant A and Counter Constant A Register 2 can be toggled for the counter/timers. Writing a "1" to the counter's corresponding toggle counter constants bit will cause the counter to use the values in Counter Constant A Register 2. Writing a "0" will cause the counter to use the values in Counter Constant A. By default, a counter will always use the values in Counter Constant A Register.

Counter Constant B Register (Read/Write)

Note that the Counter Constant Registers are cleared (set to 0) following a system or software reset.

This read/write register is used to store the counter/timer constant B value (initial value) for the various counting modes. It is necessary to load the constant value into the counter in one clock cycle. Thus, access to this register is allowed on a 32-bit basis, only.

The contents of the Counter Constant B and Counter Constant B Register 2 can be toggled for the counter/timers. Writing a "1" to the counter's corresponding toggle counter constants bit will cause the counter to use the values in Counter Constant B Register 2. Writing a "0" will cause the counter to use the values in Counter Constant B. By default, a counter will always use the values in Counter Constant B Register.

Counter Constant B Register 2 (Read/Write)

Note that the Counter Constant Registers are cleared (set to 0) following a system or software reset.

This read/write register is used to store the counter/timer constant B register 2 value (initial value) for the various counting modes. It is necessary to load the constant value into the counter in one clock cycle. Thus, access to this register is allowed on a 32-bit basis, only.

The contents of the Counter Constant B and Counter Constant B Register 2 can be toggled for the counter/timers. Writing a "1" to the counter's

corresponding toggle counter constants bit will cause the counter to use the values in Counter Constant B Register 2. Writing a "0" will cause the counter to use the values in Counter Constant B. By default, a counter will always use the values in Counter Constant B Register.

Digital Input Register (Read Only) - (BAR0 + 0x0000 0160)

AP483 Din 1 not supported

AP484 Din 0 and Din 1 not supported

This 8-bit read only register contains the value of the Digital TTL inputs. A read value of one symbolizes a logic "high" while a value of zero represents a logic "low". Table 3.20 identifies the position of the available input bits.

Table 3.20 Digital Input Register

Note that any registers/bits not mentioned will remain at the default value logic low.

BIT	FUNCTION
0	Din 0
1	Din 1
2-31	Not Used

Digital Output Register (Read/Write) - (BAR0 + 0x0000 0164)

AP483 Dout 3 to Dout 5 not supported

AP484 Dout 0 to Dout 5 not supported

This 8-bit read/write register contains the value of the Digital outputs. To set a digital output "high" write a one to the proper bit position. To set the value logic "low" write a zero to the proper bit. On power-up output bits are initialized to logic "1". Table 3.21 identifies the position of the available output bits.

Table 3.21 Digital Output Register

Note that any registers/bits not mentioned will remain at the default value logic low.

BIT	FUNCTION
0	Dout 0
1	Dout 1
2	Dout 2
3	Dout 3
4	Dout 4
5	Dout 5
6-31	Not Used

XADC Status/Control Register (Read/Write) - (BAR0 + 168H)

This read/write register will access the XADC register at the address set in the XADC Address Register.

For example, the address of the XADC Status register that is to be accessed is first set via the XADC Address register at BAR0 plus 0x16CH. Next, this register at BAR0 plus 0x168H is read. Bits 22 to 16 of this register hold the address of the XADC register that is accessed. Data bits 15 to 6 of this register hold the "ADCcode" temperature, Vccint, or Vccaux value. Data bits 5 to 0 are not used. Valid addresses are given in column one of the table below.

Reading or writing this register is possible via 32-bit data transfers.

The 10-bits digitized and output from the ADC can be converted to temperature by using the following equation.

$$Temperature(°C) = \frac{ADCcode \times 503.975}{1024} - 273.15$$

The 10-bits digitized and output from the ADC can be converted to voltage by using the following equation.

$$SupplyVoltage(volts) = \frac{ADCcode}{1024} \times 3V$$

XADC Address Register (Write Only) - (BAR0 + 16CH)

This write only register is used to set the XADC address register with a valid address for the XADC internal status or control registers. Valid addresses are given in the following table. Additional addresses can be found in the Xilinx XADC document UG480 (available from Xilinx). Writing this register is possible via 32-bit data transfers.

The address value written to this register can be read on bits 22 to 16 of the XADC Status/Control register at BAR0 plus 0x168H.

Table 3.22: System Monitor Register Map

Address	Status Register
0x00	Temperature
0x01	Vccint
0x02	Vccaux
0x20	Maximum Temperature
0x21	Maximum Vccint
0x22	Maximum Vccaux
0x24	Minimum Temperature
0x25	Minimum Vccint
0x26	Minimum Vccaux

Table 3.23 FPGA Voltage and Temperature Range

Symbol	Minimum	Typical	Maximum
Vccint	0.95	1.0	1.05
Vccaux	1.71	1.8	1.89
Temperature operating range	-40C	50-60C	100C

Firmware Revision Register (Read Only) - (BAR0 + 0x0000 0200)

This is a read only register. The ASCII code representing the current revision of the MCS firmware file is readable from this location. For example if the firmware is at revision A then this register will read 0x41 in the least significant byte or B= 0x42, C=0x43, etc.

4.0 THEORY OF OPERATION

This section contains information regarding the hardware of the AP48X. A description of the basic functionality of the circuitry used on the board is also provided. Refer to the Figures 1 to 3 Block Diagrams for the AP48X shown at the end of the manual as you review this material.

4.1 Counter Timer

Counter timer input control signals are TTL or RS422/RS485 logic level and InA, InB, and InC are available via the field connector. See Table 2.1 to 2.3 for the list of these signals and their corresponding pin assignments. Counter timer out signals OUT1 to 10 are TTL or RS422/RS485 logic level and are available via the field I/O connector. See Table 2.1 to 2.3 for the output signals and their corresponding pin assignments.

4.2 Digital Input/Output

Digital input/output signals to the FPGA are buffered using TTL drivers. Field inputs to these buffers include a 4.7K pullup resistor to +3.3V. Output operation is considered 'Fail-safe'. That is, the Digital Input/Output signals are always configured as input upon FPGA configuration during power-up. This is done for safety reasons to ensure reliable control under all conditions. Once configured the Digital Output channels will be set as output signals.

4.3 Mini PCIe Interface

The Mini PCIe interface to the carrier board is made through 52-pin connector (refer to Table 2.4). These connectors also provide +3.3V power and JTAG signals to the module.

4.4 PCIe Interface Logic

The PCIe bus interface logic is embedded within the FPGA. This logic includes support for PCIe commands, including: configuration read/write, and memory read/write. In addition, the PCIe target interface uses a single 4K base address register, and implements target abort, retry, and disconnect. The AP48X logic also implements interrupt requests via the PCIe bus.

A FPGA device provides the control signals required to operate the board. It decodes the selected addresses, control signals, and interrupt handling. It also returns the acknowledgement messages required by the carrier/CPU board per the PCIe specification. The program for the FGPA is stored in separate Flash memory and loaded upon power-up.

5.0 SERVICE AND REPAIR

5.1 Service and Repair Assistance

Surface-Mounted Technology (SMT) boards like the AcroPack family of carrier boards are generally difficult to repair. The board can be easily damaged unless special SMT repair and service tools are used. For these and other reasons, it is strongly recommended that a non-functioning board be returned to Acromag for repair. Acromag has automated diagnostic and test equipment that thoroughly checks the performance of suspect boards. Furthermore, when any repair is made, the board is retested before return shipment to the customer.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts, or return parts for repair.

5.2 Preliminary Service Procedure

CAUTION: POWER MUST BE TURNED OFF BEFORE SERVICING BOARDS

Before beginning repair, be sure that all of the procedures in the "Preparation for Use" section have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique for isolating a faulty part.

5.3 Where to Get Help

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at https://www.acromag.com. Our web site contains the most up-to-date product and software information.

Go to the "Support" tab or your specific AcroPack model ordering page.

Acromag's application engineers can also be contacted directly for technical assistance via email, telephone, or FAX through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab. When needed, complete repair services are also available.

- Email: solutions@acromag.com
- Phone: 248-295-0310

6.0 SPECIFICATIONS

6.1 Physical

Height: 12.5 mm (0.4921 in)

Height defines Carrier to Module Maximum component height

Board Thickness 1.0 mm (0.03937 in)

- AcroPack L x W: 70 mm x 30.00 mm (2.76 in x 1.18 in)

Unit Weight (does not include shipping material):

- AcroPack 0.2432ounces (6.9 grams)

6.2 Power Requirements

Summarized below are the expected current draws for each of the specified power supply voltages.

Power Supply Voltage	Current Draw
• 3.3 VDC +/- 5%	0.43 A Typical, 0.57 A maximum (AP482E-LF)
• 3.3 VDC +/- 5%	0.43 A Typical, 0.57 A maximum (AP483E-LF)
• 3.3 VDC +/- 5%	0.43 A Typical, 0.57 A maximum (AP484E-LF)
• 1.5 VDC +/- 5%[1]	Not Used
• 5.0 VDC +/- 5%[1]	Not Used
• +12 VDC +/- 5%[1]	Not Used
• -12 VDC +/- 5%[1]	Not Used

6.3 Environmental Considerations

Summarized below are the operating temperature range, airflow and other environmental requirements and applicable standards for the AcroPack module.

6.3.1 Operating Temperature

Model Number	*Temp Range*	I/O Type	32-bit Counters
AP482E-LF[1,2]	-40°C to 85°C	TTL	10
AP483E-LF[1,2]	-40°C to 85°C	TTL RS422/RS485	5 3
AP484E-LF[1,2]	-40°C to 85°C	RS422/RS485	6

Note 1: An air cooled application with an AcroPack module will require a minimum airflow of 200LFM.

Note 2: Applications requiring operating temperatures of *70*°C *to 85*°C will require purchase of *AcroPack Heatsink Accessory* ***AP-CC-01.***

6.3.2 Other Environmental Requirements

6.3.2.1 Relative Humidity

The range of acceptable relative humidity is 5% to 95% non-condensing.

6.3.2.2 Isolation

The PCIe bus and field commons are non-isolated and have a direct electrical connection.

6.3.3 Vibration and Shock Standards

The AcroPack is designed to pass the following Vibration and Shock standards.

Vibration, Sinusoidal Operating: Designed to comply with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis
Vibration, Random Operating: Designed to comply with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis
Shock, Operating: Designed to comply with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3mS half sine, 18 shocks at 6 orientations for both test levels

6.3.4 EMC Directives

The AcroPack complies with EMC Directive 2004/108/EC.

- **Immunity per EN 61000-6-2:**
  Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2.
  Radiated Field Immunity (RFI), per IEC 61000-4-3.
  Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4.
  Surge Immunity, per IEC 61000-4-5.
  Conducted RF Immunity (CRFI), per IEC 61000-4-6.
- **Emissions per EN 61000-6-4:**
  Enclosure Port, per CISPR 16.
  Low Voltage AC Mains Port, per CISPR 16.
  Note: This is a Class A product

6.4 Reliability Prediction

AP482E-LF

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled,* G_BG_C

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	2,538,632	289.8	393.9
40°C	1,674,587	191.2	597.2

[1] FIT is Failures in 10^9 hours.

AP483E-LF

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled,* G_BG_C

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	1,888,624	215.6	529.5
40°C	1,124,919	128.4	889.0

[1] FIT is Failures in 10^9 hours.

AP484E-LF

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled,* G_BG_C

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	1,775,256	202.7	563.3
40°C	1,013,331	115.7	986.8

[1] FIT is Failures in 10^9 hours.

6.5 Counter/Timers

Counter Functions: Quadrature Position Measurement, Pulse Width Modulation, Watchdog Timer, Event Counting, Frequency Measurement, Period Measurement, Pulse-Width Measurement, and One Shot/Repetitive

Counter Input — **Each Counter has an InA, InB, and InC input port.** These TTL or RS485 input ports are used to control Start/Stop, Reload, Event Input, External Clock, Trigger, and Up/Down operations.

Counter Output — **Each Counter has an Output port.** These TTL or RS485 output ports are used for waveform output, watchdog active indicator, or1.73µs pulse upon counter function completion. Counter output is programmable as active high or low.

Debounce Interval — Input signal with duration less then 2.4µs are filtered with debounce enabled via counter control register.

Counter Clock Enable Frequencies — 62.5MHz, 15.625MHz, 7.8125MHz, 3.90625MHz, 1.953125MHz or External up to 15MHz

Minimum Input Event:	32nS
Minimum Pulse Measurement:	32nS
Minimum Period Measurement:	64nS
Minimum Gate/Trigger Pulse:	32nS
TTL Input and Output Electrical Characteristics	• VIH: 2.0V minimum • VIL: 0.8V maximum • IOH: –32.0mA • IOL: 64mA • VOH: 2.0V minimum • VOL: 0.55V maximum at 64mA
Digital Propagation Delay	• Driver/Receiver Input to Output Delay = 3.5ns Maximum
TTL Channel Pull-up Resistors	• 4.7KΩ pull-up resistor is installed for each TTL Output/Input.
RS485/RS422 Electrical Characteristics	• 3 V Max.: Driver Common Mode Output Voltage • –7V to 12V Common Mode Input/Output Voltage Range • Driver Differential Vout = 1.5V Minimum, RL = 54Ω, • 100mV Typical: Input Hysteresis • 96KΩ Minimum Input Resistance • Data Rates up to 20Mbps
Differential Propagation Delay	• Driver Input to Output Delay = 27ns Typical, 40ns Maximum • Receiver Input to Output Delay = 33ns Typical, 60ns Maximum
RS485/RS422 Termination Resistors	120Ω termination resistor are not installed but can be added with installation in the requested open resistor locations.

6.6 PCIe Bus Specifications

Compatibility	Conforms to PCI Express Base Specification, Revision 2.1
Line Speed	Gen1 (2.5Gbps) Available through front connector
Lane Operation	1-Lane
4K Memory Space Required	One Base Address Register

Table 6.6 PCIe Bus Data Rates

PCIe Gen 1 (1 lane)	Giga bit / second	Bytes / second
Signaling Rate	2.5 Gb/s	312 Mbyte/s
Ideal Rate[1]	2 Gb/s	250 Mbyte/s
Header Burden plus 4byte Sample Rate[2]	0.332 Gb/s	41.6 Mbyte/s
Actual Measured 4 Byte Read Rate[3]	0.019 Gb/s	2.35 Mbytes/s
Actual Measured DMA 4 Byte Read Rate[4]	0.327 Gb/s	40.9 Mbyte/s
Actual Measured 4 Byte Write Rate[5]	0.320 Gb/s	40 Mbyte/s

Note 1: PCIe x1 Gen 1 = 2.5GT/s (with 10-bit encoding we have a 20% loss in possible throughput due to encoding) giving 2.0 G bits/sec or 250M Bytes/sec.

Note 2: With PCIe we have a header for address and read/write command that is sent with every packet. This header is 20 Bytes with data payload of 4 Bytes (for our typical AcroPack). For each 4 Byte data sample, 24 Bytes are sent.

$\frac{250 MByte/s}{24\ Bytes}$ = 10.4 M samples/sec or 41.6 M Bytes/sec or 0.332 G bit/sec

Note 3: For our typical AcroPack have measured back to back 4 Byte read operations completing every 1.7usec. A read operation starts with a host read request. The AcroPack must process the read and fetch the data and then generated the completion back to the host. The host then sends a message back that says I got it. This back and forth hand shaking slows down individual reads.

Note 4: DMA Read of 1024 sample takes 100us. Each sample is 4 Bytes. 100us/1024=0.0977us per sample or 4/0.0977us = 40.94Mbyte/s. We use DMA transfers to improve data transfers on the AP341/2 and AP225/235.

Note 5: Simple write operations are just as fast as DMA read operations. Write data is presented to the AcroPack in one transaction. Measured 4-byte back to back write accesses taking place every 100ns.

Figure 1 AP482 Block Diagram

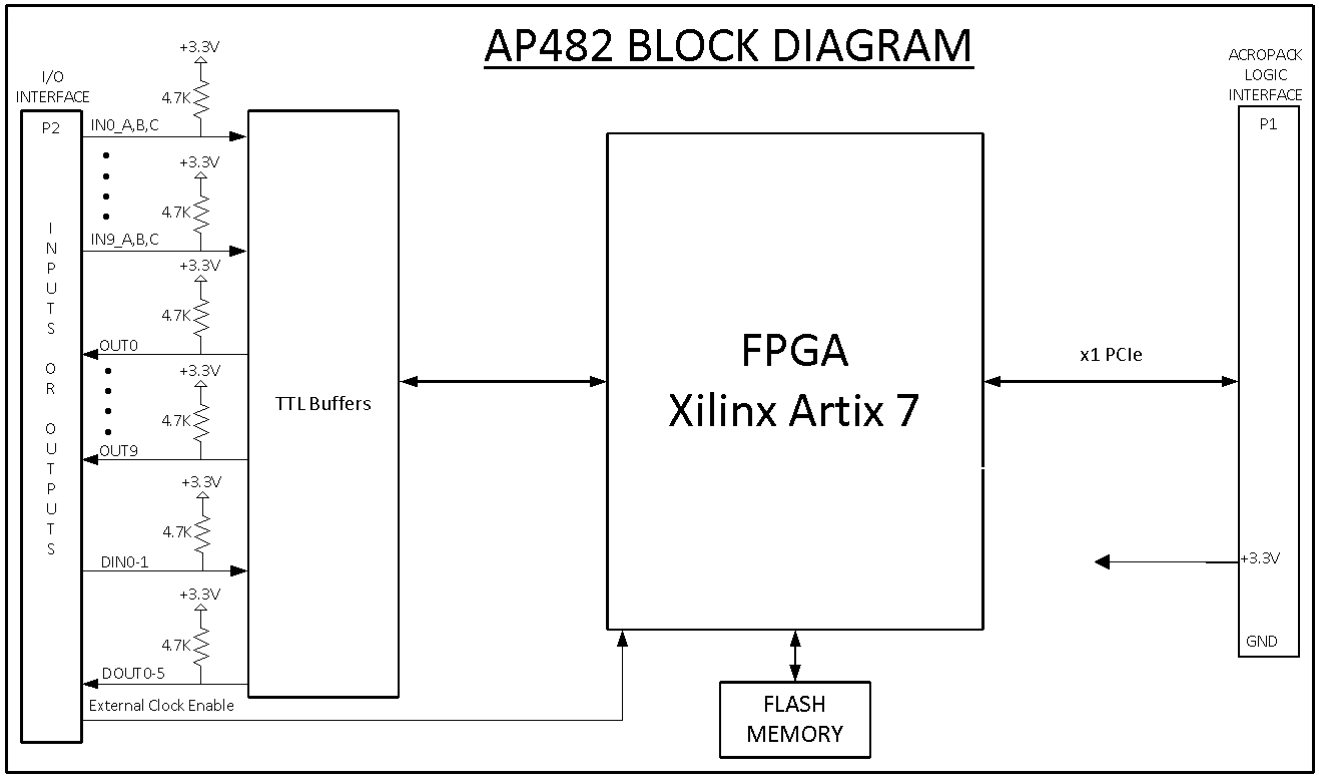


Figure 2 AP483 Block Diagram

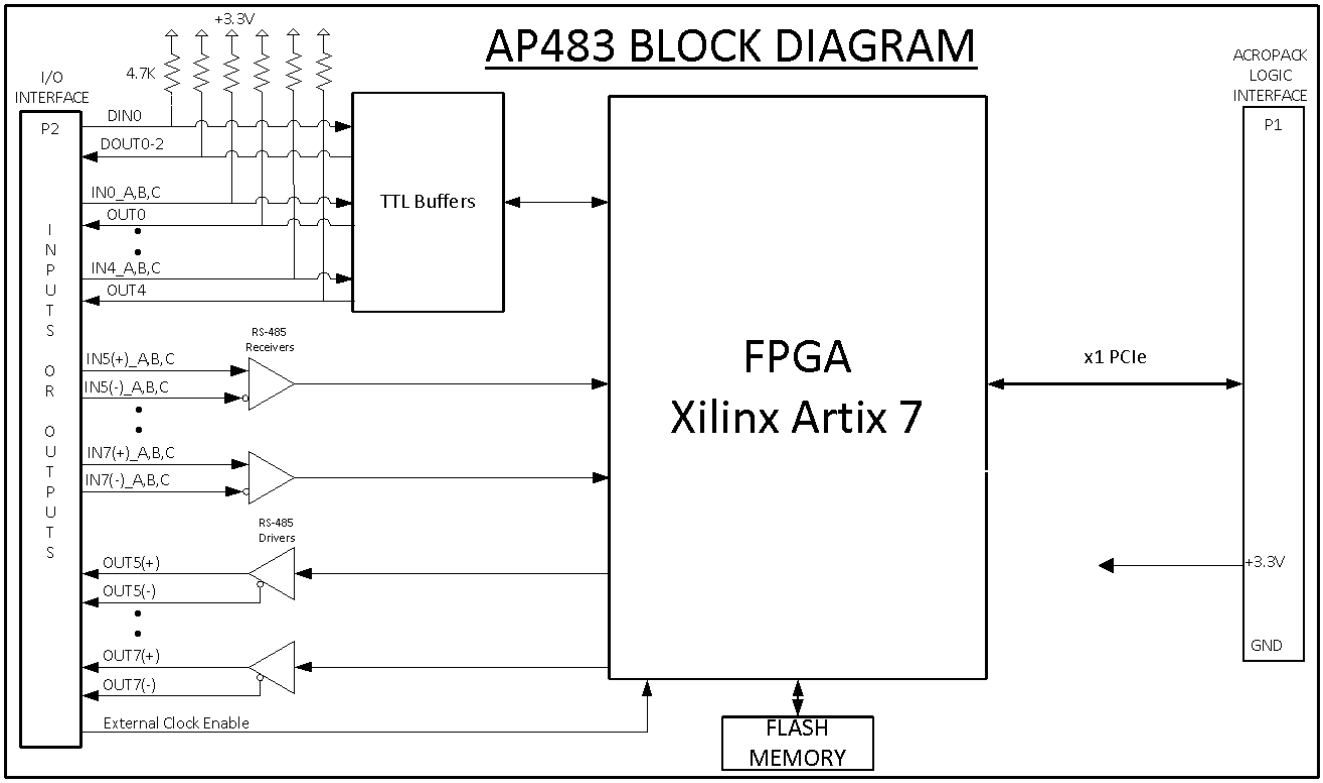
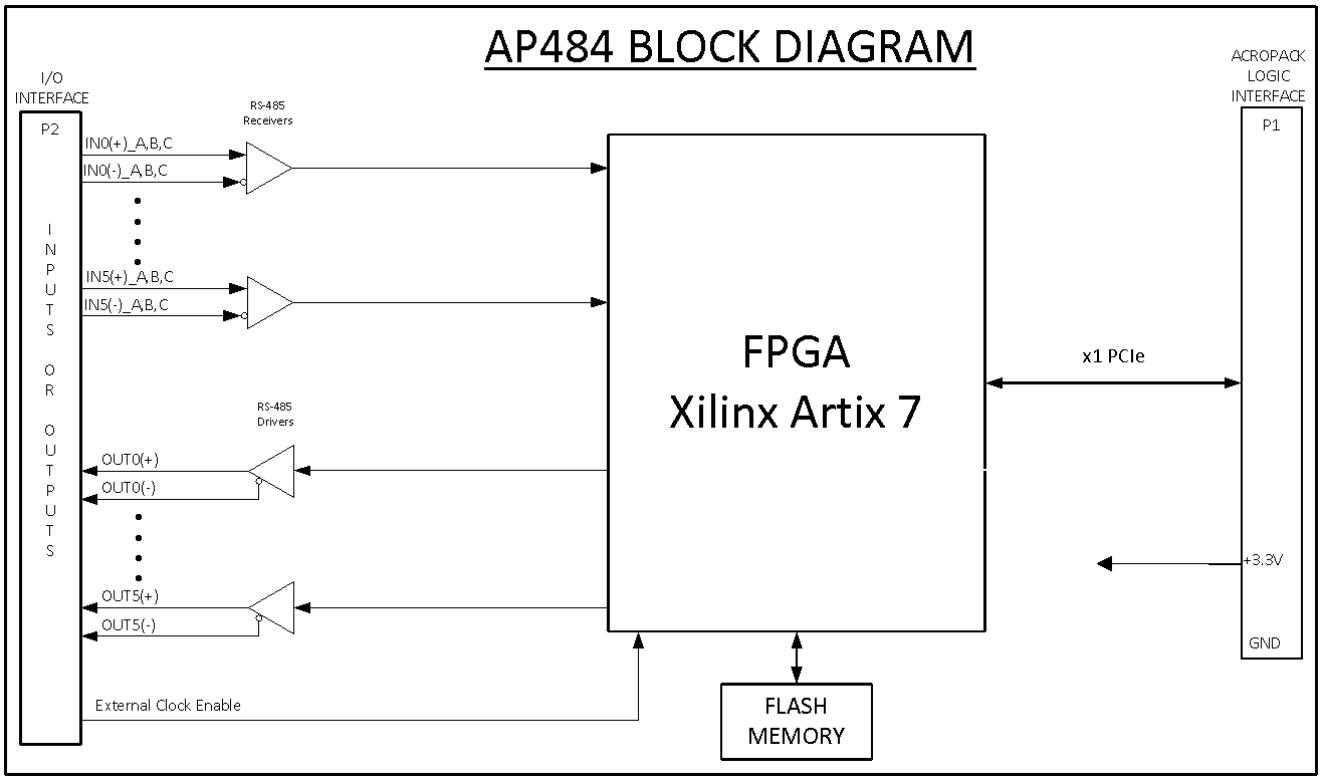
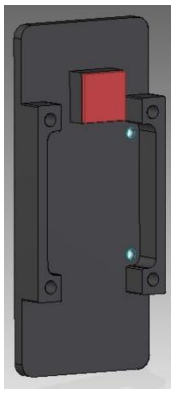


Figure 3 AP484 Block Diagram



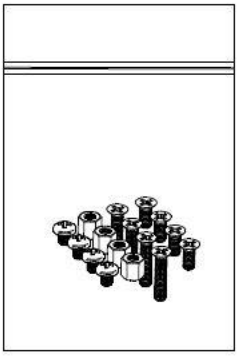
Appendix A

AP-CC-01 Heatsink Kit Installation



Bottom view

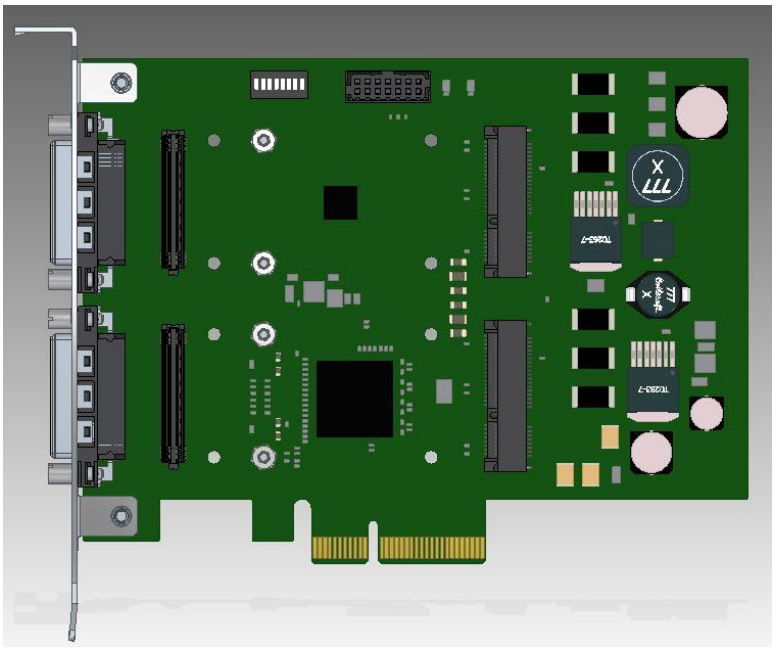
Top view



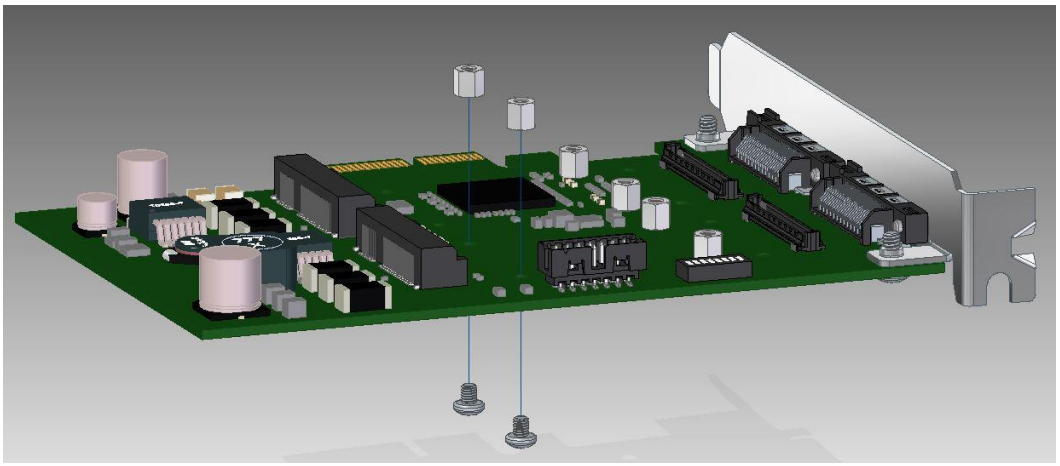
Hardware

AP-CC-01 Heat Sink Kit

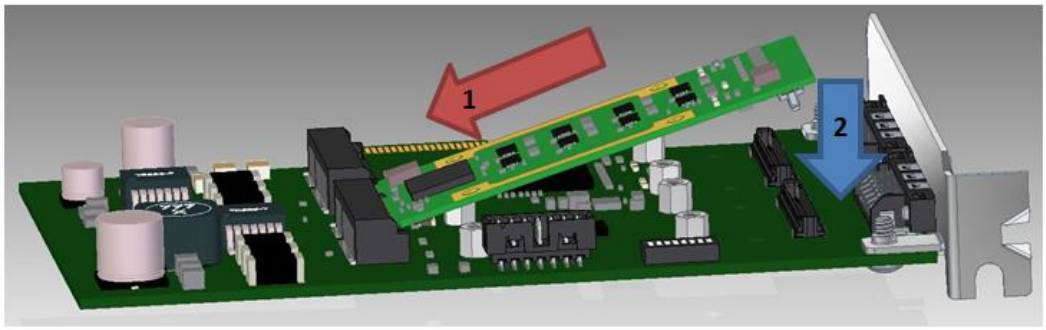
This example will show how to install the AP-CC-01 Heatsink kit with an APCe7020 carrier.



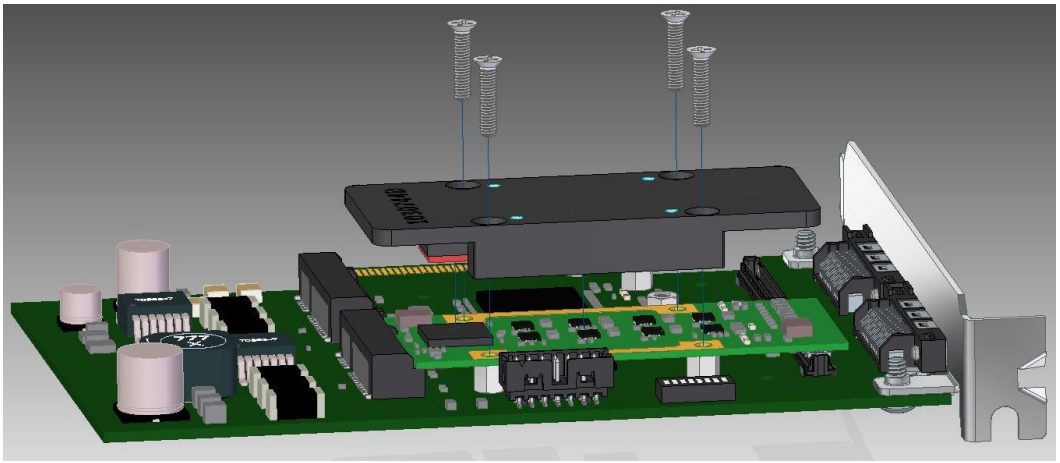
1. Install two standoffs and secure with two screws.



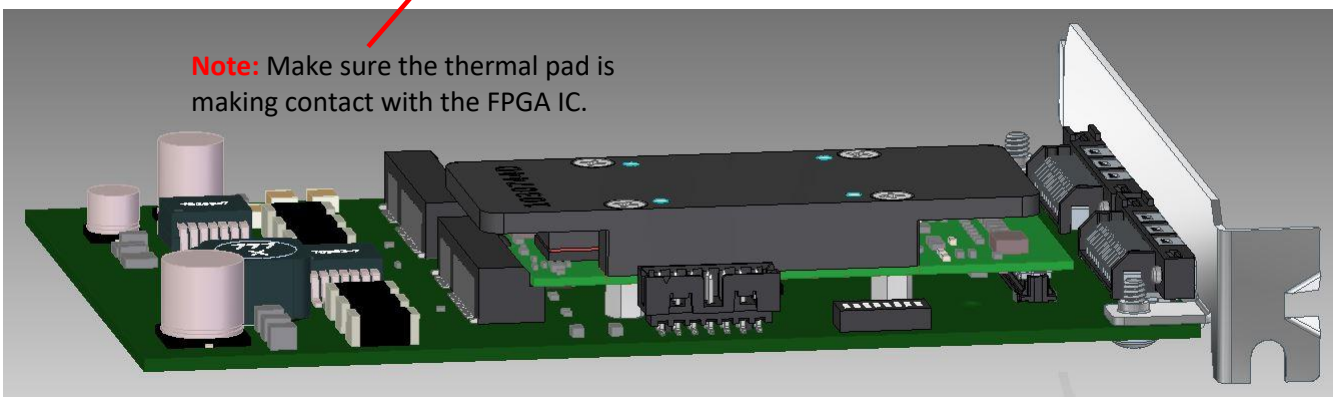
2. Install the AcroPack module.



3. Install the Heatsink and secure with 4 screws.



4. AP-CC-01 Installation is complete.



Certificate of Volatility

Acromag Model AP440-xE-LF	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) ■ Yes □ No				
Type (SRAM, SDRAM, etc.) Configurable Logic Blocks and Block RAM Blocks	Size: 16,640 Logic Cells and 900 Kb Block RAM	User Modifiable ■ Yes □ No	Function: FPGA logic blocks and RAM blocks	Process to Sanitize: Power Down
Type (SRAM, SDRAM, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No				
Type(EEPROM, Flash, etc.) Flash	Size: 32 Meg x 1bit	User Modifiable ■ Yes □ No	Function: Data storage for FPGA	Process to Sanitize: Erase using JTAG
Type(EEPROM, Flash, etc.) One Time Programmable area in flash device	Size:3 x 256-byte	User Modifiable □ Yes ■ No	Function: The OTP area has been disabled by writing the lock bits with logic 1.	Process to Sanitize: Not applicable

Acromag Representative				
Name: Russ Nieves	Title: Sales and Marketing	Email: solutions@acromag.com	Office Phone: 248-295-0310	Office Fax: 248-624-9234

Revision History

The revision history for this document is summarized in the table below.

Release Date (mm/dd/yyyy)	Version	EGR/DOC	Description of Revision
1/27/2016	Preliminary	LMP/LMP	Preliminary Document Publication
7/7/2016	A	LMP/LMP	Revision A Document Publication
10/07/2016	B	LMP/ARP	Certificate of Volatility flash and OTP update, Table 2.1 added 68 Pin Champ Carrier Connector, and changed "design to comply with" to "complies with" for the EMC directives.
13 APR 2017	C	LMP/MJO	Updated section 1.3 descriptions and section 5.3 Where to Get Help.
22 NOV 2017	D	LMP/MJO	Updated section 6.5 TTL and RS485 specifications
16 JAN 2018	E	LMP/ARP	Add Table 6.6 PCIe Bus Data Rates.
07 DEC 2020	F	ENZ/AMM	Updated MTBF Numbers for AP482E-LF and added MTBF Tables for AP483E-LF and AP484E-LF.
10 MAR 2021	G	LMP/AMM	Removed "50-Pin" in reference to the Front Panel Connector.