Series AP441 AcroPack
32-Channel Isolated Digital Input Module
With Interrupts
USER'S MANUAL

ACROMAG INCORPORATED
30765 South Wixom Road
Wixom, MI 48393-2417 U.S.A.
Tel: (248) 295-0310
Email: solutions@acromag.com

8501119B

Table of Contents

1.0 GENERAL INFORMATION

1.1 Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the AcroPack modules. It is not intended for a general, non-technical audience that is unfamiliar with I/O devices and their application.

1.2 Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag.

1.2.1 Trademark, Trade Name and Copyright Information

1.2.2 Class A Product Warning

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

1.2.3 Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

1.3 AcroPack Information – All Models

AcroPack IO modules are based on the PCI Express Mini Card Electromechanical specification and are 70mm in length with an additional 100 pin field I/O connector.

The AcroPack is 19.05mm longer than the full length mini PCIe card at 50.95mm. It has the same mPCIe board width of 30mm and uses the same mPCIe standard board hold down standoff and screw keep out areas.

1.3.1 Ordering Information

The AcroPack ordering options are given in the following table.

Model Number	*Description*	*Threshold*
AP441-1E-LF [1]	±4V to ±18V DC or AC peak	±4V Max
AP441-2E-LF [1]	±16V to ±40V DC or AC peak	±16V Max
AP441-3E-LF [1]	±38V to ±60V DC or AC peak	±38V Max

Note 1: *Operating temperature range for models: -40°C to 85°C. Applications requiring operating temperatures of 70°C to 85°C will require purchase of AcroPack Heatsink Accessory* ***AP-CC-01****.*

AP-CC-01 AcroPack Conduction Cool Kit (See Appendix B for installation instructions)

1.3.2 Key Features

- **High Channel Count** - Provides programmable monitor and control of 32 optically isolated input points.
- **Wide Range Bipolar Input Voltage** - Three model ranges provide interface capability for bipolar voltages from ±4 to ±60V DC or AC peak (see Specifications section).
- **Optically Isolated** - Individual bipolar opto-couplers provide isolation. There are four groups (ports) of 8 channels, each which include separate port commons to ensure port-to-port isolation. Individual ports are isolated from each other and from the logic.
- **Programmable Polarity Event Interrupts** - Interrupts are software programmable for change-of-state input transitions, positive (low-to-high) or negative (high-to-low) input level transitions on all 32 channels.
- **Input Hysteresis** - Isolated inputs include hysteresis for increased noise immunity.

- **Programmable Debounce** - The event sense input circuitry includes programmable debounce times for all 32 channels. Debounce time is the duration of time that must pass before the input transition is recognized as valid at the FPGA input. This helps prevent false events and increases noise immunity.
- **Reverse Polarity Protection** - Bipolar inputs are not polarized and are inherently reverse polarity protected.
- **No Configuration Jumpers or Switches** - All configuration is performed through software commands with no internal jumpers to configure or switches to set.
- **Loopback Compatible with AP445 Output Module** - The field side of this model are directly compatible with those of the Acromag Model AP445 32-Channel Digital Output Module for direct closed-loop monitoring of the output states. The AP441 also shares the same pinout used on the Acromag non-isolated AP408 32-Channel I/O Module, for channels 0-31.
- **Module Health Monitoring**- On board supply voltages and FPGA junction temperature can be monitored for out of tolerance conditions via XADC registers.

1.3.3 Key Features PCIe Interface

- **PCIe Bus** – The AP module includes a PCI Express Generation 1 interface operating at a bus speed of 2.5 Gbps with one lane in each direction.
- **Compatibility** – PCI Express Base Specification v2.1 compliant PCI Express Endpoint.

1.4 Signal Interface Products

This AcroPack Module will mate directly to all Acromag AP carriers. Once connected, the module is accessed via a front panel connector on most carrier boards.

Accessory cables and termination panels are also available. For optimum performance with the AP441 digital I/O module, use of the shortest possible length of shielded I/O cable is recommended.

1.5 Software Support

The AcroPack series products require support drivers specific to your operating system. Supported operating systems include: Linux, Windows, and VxWorks.

Windows®

Acromag provides software products (sold separately) to facilitate the development of Windows® applications interfacing with AcroPack modules, VPX I/O board products, and PCIe I/O Cards. This software (model APSW-API-WIN) consists of low-level drivers and Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

VxWorks®

Acromag provides a software product (sold separately) consisting of VxWorks® software. This software (Model APSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

Linux®

Acromag provides a software product consisting of Linux® software. This software (Model APSW-API-LNX) is composed of Linux® libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

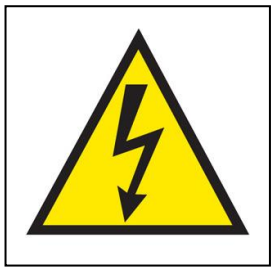
1.6 References

The following resources regarding AcroPack modules are available for download on Acromag's website or by contacting your sales representative.

- PCI Express MINI Card Electromechanical Specification, REV 1.2 http://www.pcisig.com

2.0 PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.

WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

2.1 Unpacking and Inspecting

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

2.2 Installation Considerations

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

Refer to the specifications section for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

In an air-cooled assembly, adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

In a conduction cooled assembly, adequate thermal conduction must be provided to prevent a temperature rise above the maximum operating temperature.

2.3 Non-Isolation Considerations

Power should be removed from the board when installing AP modules, cables, termination panels, and field wiring. Model AP441 digital input boards have no hardware jumpers or switches to configure.

2.4 Field I/O Connector

A field I/O interface connector provides a mating interface between the AP modules and the carrier board. The 100 pin ST5-50-1.50-L-D-P-TR Samtec connector is used on the AcroPack card as board to board interconnect. This connector will mate with the 100 pin SS5-50-3.00-L-D-K-TR Samtec connector on the carrier. The stack height is 4.5mm.

Pin assignments are unique to each AP model. Table 2.1 lists signal pin assignments for the module field I/O connector. Some pins are left unconnected in order to meet the minimum creepage distance required for 60 Volt isolation.

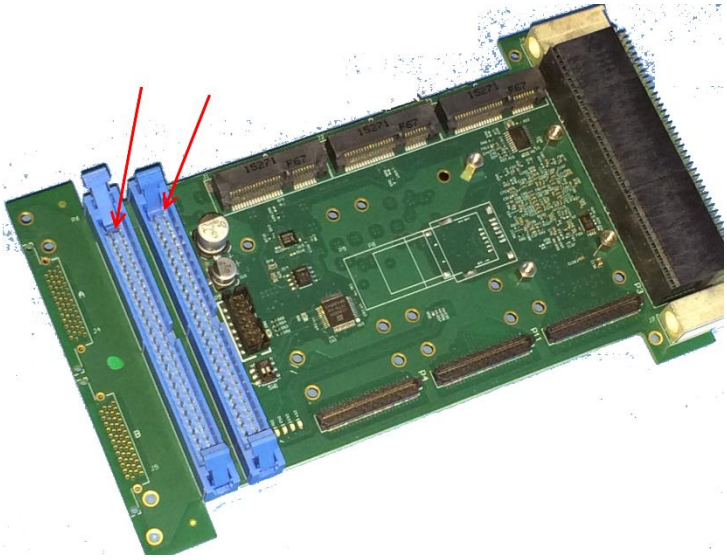
Table 2.1 Field I/O Connector Pin Assignments

68 Pin Champ Carrier Connector[3]	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
1	1	1	2	Field I/O 1
35	26	2	1	Field I/O 2
			4	Reserved/isolation
			3	Reserved/isolation
2	2	3	6	Field I/O 3
36	27	4	5	Field I/O 4
			8	Reserved/isolation
			7	Reserved/isolation
3	3	5	10	NC
37	28	6	9	Field I/O 5
			12	Reserved/isolation
			11	Reserved/isolation
4	4	7	14	Field I/O 6
38	29	8	13	Field I/O 7
			16	Reserved/isolation
			15	Reserved/isolation
5	5	9	18	Field I/O 8
39	30	10	17	ACOM
			20	Reserved/isolation
			19	Reserved/isolation
6	6	11	22	Field I/O 9
40	31	12	21	Field I/O 10
			24	Reserved/isolation
			23	Reserved/isolation
7	7	13	26	Field I/O 11
41	32	14	25	Field I/O 12
			28	Reserved/isolation
			27	Reserved/isolation
8	8	15	30	NC
42	33	16	29	Field I/O 13
			32	Reserved/isolation
			31	Reserved/isolation
9	9	17	34	Field I/O 14
43	34	18	33	Field I/O 15
			36	Reserved/isolation
			35	Reserved/isolation
10	10	19	38	Field I/O 16
44	35	20	37	BCOM
			40	Reserved/isolation

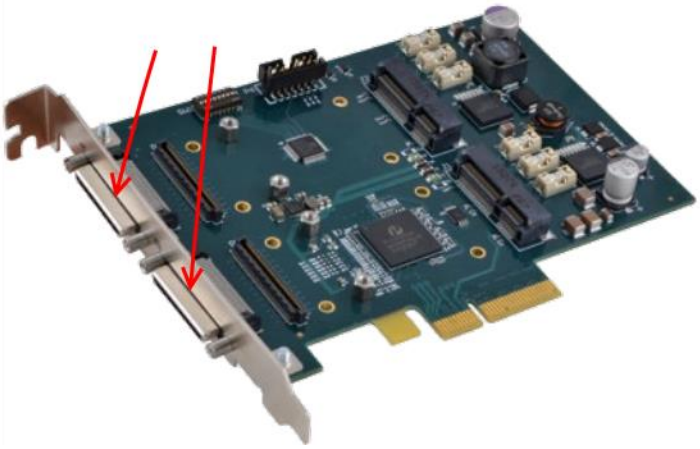
68 Pin Champ Carrier Connector[3]	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
			39	Reserved/isolation
11	11	21	42	Field I/O 17
45	36	22	41	Field I/O 18
			44	Reserved/isolation
			43	Reserved/isolation
12	12	23	46	Field I/O 19
46	37	24	45	Field I/O 20
			48	Reserved/isolation
			47	Reserved/isolation
13	13	25	50	NC
47	38	26	49	Field I/O 21
			52	Reserved/isolation
			51	Reserved/isolation
14	14	27	54	Field I/O 22
48	39	28	53	Field I/O 23
			56	Reserved/isolation
			55	Reserved/isolation
15	15	29	58	Field I/O 24
49	40	30	57	CCOM
			60	Reserved/isolation
			59	Reserved/isolation
16	16	31	62	Field I/O 25
50	41	32	61	Field I/O 26
			64	Reserved/isolation
			63	Reserved/isolation
17	17	33	66	Field I/O 27
51	42	34	65	Field I/O 28
			68	Reserved/isolation
			67	Reserved/isolation
18	18	35	70	NC
52	43	36	69	Field I/O 29
			72	Reserved/isolation
			71	Reserved/isolation
19	19	37	74	Field I/O 30
53	44	38	73	Field I/O 31
			76	Reserved/isolation
			75	Reserved/isolation
20	20	39	78	Field I/O 32
54	45	40	77	DCOM
			80	Reserved/isolation
			79	Reserved/isolation

68 Pin Champ Carrier Connector[3]	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
21	21	41	82	NC
55	46	42	81	NC
			84	Reserved/isolation
			83	Reserved/isolation
22	22	43	86	NC
56	47	44	85	NC
			88	Reserved/isolation
			87	Reserved/isolation
23	23	45	90	NC
57	48	46	89	NC
			92	Reserved/isolation
			91	Reserved/isolation
24	24	47	94	NC
58	49	48	93	NC
			96	Reserved/isolation
			95	Reserved/isolation
25	25	49	98	NC
59	50	50	97	NC
			100	Reserved/isolation
			99	Reserved/isolation

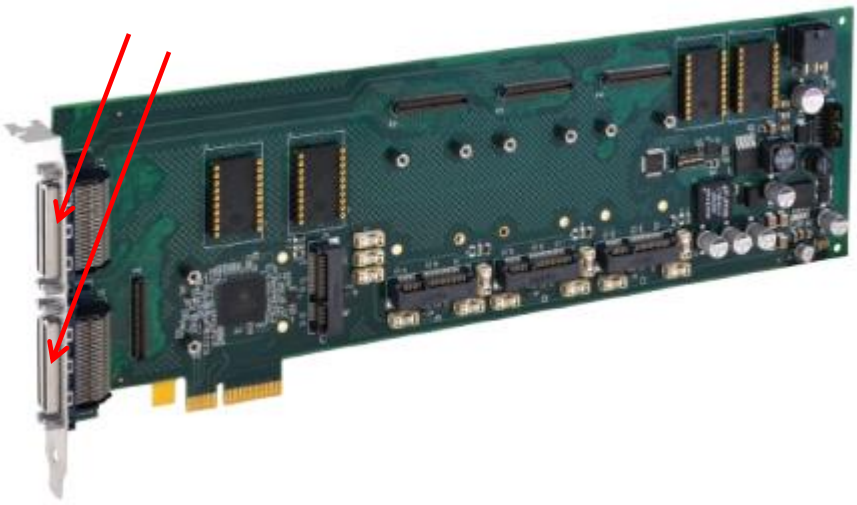
Note 1: VPX4500-CC-LF is an example of a carrier that uses the ribbon cable connector. See image of carrier.



Note 2: APCe7020E-LF is an example of a carrier that uses the 50-pin Champ connector. See image of carrier.



Note 3: APCe7040E-LF is an example of a carrier that uses the 68-pin Champ connector. See image of carrier.



Input channels of this module are divided into four ports of eight channels each. Channels of a port share a common signal connection with each other (ACOM, BCOM, CCOM, and DCOM). Isolation is provided between ports and between each port and the AP logic. With respect to interrupt generation and events, event polarities may be defined as positive (low-to-high), or negative (high-to-low) each channel. Change-of-State detection can also be programmed on an individual basis.

Field I/O pinouts are arranged to be compatible with similar AcroPack models. This model is directly loopback compatible with the Acromag Model AP445 Digital Output Module. Likewise, pin assignments are identical to those of Acromag Model AP408.

Note that the inputs of this device are bipolar, and may be connected in any polarity with respect to the port common. Further, do not confuse port commons with signal common. For the AP441, port common only infers that this lead is connected common to the 8 inputs of the port (a separate port common for each port). Likewise, the port commons of the AP441 input module and

AP445 output module are normally not connected together for loopback interconnection of the AP441 and AP445 (see Figure 2 in Appendix A).

2.5 Noise and Earth Grounding Considerations

Input lines of the AP441 are optically isolated between the logic and field input connections. Likewise, separate port commons facilitate port-to-port isolation. Consequently, the field I/O connections are isolated from the carrier board and backplane, thus minimizing the negative effects of ground bounce, impedance drops, and switching transients. However, care should be taken in designing installations to avoid inadvertent isolation bridges, noise pickup, isolation voltage clearance violations, equipment failure, or ground loops.

2.6 Logic Interface Connector

The AP module logic card edge connector interfaces to the mating connector on the carrier board. The pin assignments of this connector are standard for all AP modules according to the PCI Express MINI Card Electromechanical Specification, REV 1.2 (with exceptions shown in Table 2.2 and noted below).

Power supplies +5, +12, and -12 Volt have been assigned to pins that are reserved in the mini-PCIe specification. The 'Present' signal is grounded on the AP module. In addition, COEX1, COEX2 – wireless transmitter control are reassigned to JTAG signals TMS and TCK. Lastly, UIM_C4, UIM_C8 – reserved User Identity Module signals are reassigned to JTAG signals TDI and TDO.

Table 2.2 Logic Interface Connections

Pin #	Name	Pin #	Name
51	+5V[1,2]	52	+3.3V[3]
49	+12V[1,2]	50	GND
47	-12V[1,2]	48	N.C. (+1.5V)[1]
45	Present[4]	46	N.C. (LED_WPAN#)[1]
43	GND	44	N.C. (LED_WLAN#)[1]
41	+3.3V[3]	42	N.C. (LED_WWAN#)[1]
39	+3.3V[3]	40	GND
37	GND	38	N.C. (USB_D+)[1]
35	GND	36	N.C. (USB_D-)[1]
33	PETp0	34	GND
31	PETn0	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	N.C. (+1.5V)[1]
25	PERp0	26	GND
23	PERn0	24	+3.3V[3]
21	GND	22	PERST#
19	TDI (UIM_C4)[1]	20	N.C. (W_DISABLE#)[1]
17	TDO (UIM_C8)[1]	18	GND
15	GND	16	N.C. (UIM_VPP)[1]
13	RECLK+	14	N.C. (UIM_RESET)[1]
11	REFCLK-	12	N.C (UIM_CLK)[1]
9	GND	10	N.C. (UIM_DATA)[1]
7	CLKREQ#	8	N.C. (UIM_PWR)[1]
5	TCK (COEX2)[1]	6	N.C. (+1.5V)[1]
3	TMS (COEX1)[1]	4	GND
1	N.C. (WAKE#)[1]	2	+3.3V[3]

Note 1: The following mini-PCIe signals are not used by the AP441: USB_D+, USB_D-, WAKE#, LED_WPAN#, LED_WLAN#, LED_WWAN#, W_DISABLE#, COEX1, COEX2, UIM_C4, UIM_C8. The following signals UIM_C4, UIM_C8, COEX2 and COEX1 are repurposed for JTAG.

Note 2: +5, +12, and -12 Volt power supplies have been assigned to pins that are reserved in the mini-PCIe specification. The Present signal is tied to circuit common on the AP module.

Note 3: All +3.3Vaux power pins are changed to system +3.3V power.

Note 4: The SM bus signals SMB_CLK and SMB_DATA will be used to clock a carrier location serial stream from the carrier. These signals are under the control of the AcroPack module.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the AP441 module.

The PCIe bus is defined to address three distinct address spaces: I/O, memory, and configuration space. The AcroPack module can be accessed via the PCIe bus memory space and configuration spaces, only.

The AcroPack configuration registers are initialized by system software at power-up to configure the card. The AcroPack module is a Plug-and-Play PCIe card. As a Plug-and-Play card the board's base address and system interrupt request are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCIe bus configuration access is used to access the AcroPack's configuration registers.

When the computer is first powered-up, the computer's system configuration software scans the PCIe bus to determine what PCIe devices are present. The software also determines the configuration requirements of the PCIe card.

The system software accesses the configuration registers to determine how many blocks of memory space the module requires. It then programs the board's configuration registers with the unique memory base address.

Since this board is not fixed in address space, its device driver must use the mapping information stored in the board's Configuration Space registers to determine where the board is mapped in memory space.

The configuration registers are also used to indicate that the board requires an interrupt request. The system software then programs the configuration registers with the interrupt request for the board.

CONFIGURATION REGISTERS

The PCIe specification requires software driven initialization and configuration via the Configuration Address space. This board provides 512 bytes of configuration registers for this purpose. It contains the configuration registers shown in the following table to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers which must be read to determine the base address assigned to the board and the Interrupt Register which must be read to determine the interrupt request that goes active on a board interrupt request.

Table 3.1 Configuration Registers

Reg. Num.	D31 D24	D23 D16	D15 D8	D7 D0
0	**Device ID** 0x7031 AP441-1E-LF 0x7032 AP441-2E-LF 0x7033 AP441-3E-LF		**Vendor ID** 16D5	
1	Status		Command	
2	Class Code=118000			Rev ID=00
3	BIST	Header	Latency	Cache
4	64-bit Memory Base Address for Memory Accesses to PCIe interrupt and I/O registers 4K Space **(BAR0)**			
5:10	Not Used			
11	**Subsystem ID** 0x7031 AP441-1E-LF 0x7032 AP441-2E-LF 0x7033 AP441-3E-LF		**Subsystem Vendor ID** 16D5	
12	Not Used			
13,14	Reserved			
15	Max_Lat	Min_Gnt	Inter. Pin	Inter. Line

This board is allocated a 4K byte block of memory (BAR0), to access the PCIe interrupt and I/O registers. The PCIe bus decodes 4K bytes for BAR0 for this memory space.

This board is addressable in the PCIe memory space to control the configuration and status monitoring of 32 digital input or event channels.

Memory Map

The memory space address map for the AP441 is shown in Table 3.2. Note that the base address for the board (BAR0) in memory space must be added to the addresses shown to properly access these AP441 registers. Register accesses as 32, 16, and 8-bit data in memory space are permitted.

This board provides access to the control, configuration and monitoring of the 32 digital input lines. The input signal monitoring and controls are addressed in separate registers for each of the four ports (eight input signals per port). These ports share common and are electrically isolated from one another. Data is read or written to the channels as designated by the address and read and write signals. Event Sense inputs allow for event triggered flags to be set and interrupts to be generated. Selectable hardware debounce may also be applied for noise free edge-detection of incoming signals. Registers are also provided to enable interrupt generation and to generate a software reset.

Table 3.2: Memory Map

Notes:

1. The AP441 will respond to addresses that are "Not Used". The board will return "0" for all address reads that are not used or reserved.

Base BAR0 Address	Bit(s)	Name
0x0000	7:0	Interrupt Enable Status Register
0x0004	7:0	Location in System Register
0x0008	7:0	Input Port A Register IN00-IN07
0x000C	7:0	Input Port B Register IN08-IN15
0x0010	7:0	Input Port C Register IN16-IN23
0x0014	7:0	Input Port D Register IN24-IN31
0x0018	7:0	Event Enable Register IN00-IN07
0x001C	7:0	Event Enable Register IN08-IN15
0x0020	7:0	Event Enable Register IN16-IN23
0x0024	7:0	Event Enable Register IN24-IN31
0x0028	7:0	Event Type Register IN00-IN07
0x002C	7:0	Event Type Register IN08-IN15
0x0030	7:0	Event Type Register IN16-IN23
0x0034	7:0	Event Type Register IN24-IN31
0x0038	7:0	Event Polarity Register IN00-IN07
0x003C	7:0	Event Polarity Register IN08-IN15
0x0040	7:0	Event Polarity Register IN16-IN23
0x0044	7:0	Event Polarity Register IN24-IN31
0x0048	7:0	Event Pending/Clear Register IN00-IN07
0x004C	7:0	Event Pending/Clear Register IN08-IN15
0x0050	7:0	Event Pending/Clear Register IN16-IN23

0x0054	7:0	Event Pending/Clear Register IN24-IN31
0x0058	7:0	Debounce Control Register IN00-IN07
0x005C	7:0	Debounce Control Register IN08-IN15
0x0060	7:0	Debounce Control Register IN16-IN23
0x0064	7:0	Debounce Control Register IN24-IN31
0x0068	15:0	Debounce Duration Register IN00-IN07
0x006C	15:0	Debounce Duration Register IN08-IN15
0x0070	15:0	Debounce Duration Register IN16-IN23
0x0074	15:0	Debounce Duration Register IN24-IN31
0x0078	0	Software Reset Register
0x007C	32:0	XADC Status/Control Register
0x0080	32:0	XADC Address Register
0x0084→0x01FC	-	Not Used
0x0200	7:0	Firmware Revision Register

Interrupt Enable Status Register (Read/Write)

(BAR0 + 0x0000 0000)

This read/write register is used to: enable board interrupts and determine the pending status of interrupts.

The function of each of the interrupt register bits are described in Table 3.3. This register can be read or written with either 8-bit, 16-bit, or 32-bit data transfers. A power-up or system reset sets all interrupt register bits to 0.

With both an enabled Event Sense bit and Board Interrupt Enable bit, then interrupts can be generated.

Table 3.3 Interrupt Register

Note that any registers/bits not mentioned will remain at the default value logic low.

Bit(s)	FUNCTION	
0	Board Interrupt Enable Bit. This bit must be set to logic "1" to enable generation of interrupts from the AP module. Setting this bit to logic "0" will disable board interrupts. (Read/Write Bit)	
	0	Disabled
	1	Enabled
1	Board Interrupt Pending Status Bit. This bit can be read to determine the interrupt pending status of the AP module. When this bit is logic "1" an interrupt is pending and will cause an interrupt request if bit-0 of the register is set. When this bit is logic "0" and interrupt is not being requested.	
	0	No Interrupt
	1	Interrupt Pending

2	Interrupt Pending Port A Status Bit. This bit can be read to determine the interrupt pending status of the AP module. When this bit is logic "1" an interrupt is pending and will cause an interrupt request if bit-0 of the register is set. When this bit is logic "0" an interrupt is not being requested.	
	0	No Interrupt from Port A
	1	Interrupt Pending from Port A
3	Interrupt Pending Port B Status Bit. This bit can be read to determine the interrupt pending status of the AP module. When this bit is logic "1" an interrupt is pending and will cause an interrupt request if bit-0 of the register is set. When this bit is logic "0" an interrupt is not being requested.	
	0	No Interrupt from Port B
	1	Interrupt Pending from Port B
4	Interrupt Pending Port C Status Bit. This bit can be read to determine the interrupt pending status of the AP module. When this bit is logic "1" an interrupt is pending and will cause an interrupt request if bit-0 of the register is set. When this bit is logic "0" an interrupt is not being requested.	
	0	No Interrupt from Port C
	1	Interrupt Pending from Port C
5	Interrupt Pending Port D Status Bit. This bit can be read to determine the interrupt pending status of the AP module. When this bit is logic "1" an interrupt is pending and will cause an interrupt request if bit-0 of the register is set. When this bit is logic "0" an interrupt is not being requested.	
	0	No Interrupt from Port D
	1	Interrupt Pending from Port D
31 to 6	Not Used	

Module Location In System Register (Read Only)

(BAR0 + 0x0000 0004)

This read only register is used identify the module's plugin location in a system.

Table 3.4 Location Register

Note that any registers/bits not mentioned will remain at the default value logic low.

Bit(s)	FUNCTION	
2 to 0	Module Site Location Bits. These bits identify the location on the carrier of the AP module.	
	000	Carrier Site A
	001	Carrier Site B
	010	Carrier Site C
	011	Carrier Site D

7 to 3	Module Slot Location Bits. These bits identify the slot location of the AP module in a system. The Carrier may use backplane signals as in a VPX system or an on-carrier DIP switch to uniquely identify the system location of the carrier.	
	XXXXX	System Slot identification bits are described by the AcroPack carrier card.
31 to 8	Not Used	

Input Port X Registers (Read)

(BAR0 + 0x0000 0008 – 0x0000 0014)

Four registers are provided to monitor 32 possible input points. Data is read from one of four groups of eight I/O lines, as designated by the address and read and write signals. A read of this register returns the status (ON/OFF) of the input point. Bit 0 of each register corresponds to the lowest numbered I/O point, while Bit 7 corresponds to the highest numbered I/O point.

Event Enable Registers (Read/Write)

(BAR0 + 0x0000 0018 – 0x0000 0024)

The Event Enable Registers provide a mask bit for each of the 32 possible interrupt channels. A "0" bit will prevent the corresponding input channel from detecting an event. A "1" bit will allow the corresponding input channel to detect events as configured by the Event Type and Event Polarity Control Registers. Bit 0 of each register corresponds to the lowest numbered I/O point, while Bit 7 corresponds to the highest numbered I/O point.

If both an Event Sense and the board Interrupt Enable bit is set, then interrupts can be generated.

Event Type (COS or H/L) Configuration Registers (Read/Write)

(BAR0 + 0x0000 0028 – 0x0000 0034)

The Event Type Configuration Registers determine the type of input channel transition that will generate an event for each of the thirty-two possible event sensing channels. A "0" bit selects event on level transition. An event will be generated when the input channel level specified by the Event Polarity Register occurs (i.e. low or high-level transition event). A "1" bit means the event will occur when a Change-Of-State (COS) occurs at the corresponding input channel (i.e. any state transition, low to high or high to low). Bit 0 of each register corresponds to the lowest numbered I/O point, while Bit 7 corresponds to the highest numbered I/O point.

Note that no events will be detected until enabled via the Event Enable Register. Further, interrupts will not be reported to the system unless the Interrupt enable bit-0 has been configured for enable via the Interrupt Register. All bits are set to "0" following a reset which means that, if enabled, the inputs will cause events and/or interrupts for the levels specified by the Event Polarity Register.

Event Polarity Control Registers (Read/Write)

(BAR0 + 0x0000 0038 – 0x0000 0044)

A write to these registers controls the polarity of the input sense event for each channel. A "1" written to a bit in these registers will cause the corresponding event sense input channel to flag positive events (low-to-high transitions). A "0" will cause negative events to be sensed (high-to-low

transitions). Bit 0 of each register corresponds to the lowest numbered I/O point, while Bit 7 corresponds to the highest numbered I/O point.

Note that no events will be detected until enabled via the Event Enable Register. Further, interrupts will not be reported to the system unless the Interrupt enable bit-0 has been configured for enable via the Interrupt Register. All bits are set to "0" following a reset which means that negative events will be flagged by default.

Event Pending/Clear Registers (Read/Write)

(BAR0 + 0x0000 0048 – 0x0000 0054)

The Event Pending/Clear Registers reflect the status of the 32 possible interrupt channels. A "1" bit indicates that an event flag has been set for the corresponding channel. A channel that does not have events enabled will never set its event pending flag. A channel's event can be cleared by writing a "1" to its bit position in the Event Pending/Clear Register. Bit 0 of each register corresponds to the lowest numbered I/O point, while Bit 7 corresponds to the highest numbered I/O point.

Note that no events will be detected until enabled via the Event Enable Register. Further, interrupts will not be reported to the system unless the Interrupt enable bit-0 has been configured for enable via the Interrupt Register. All bits are set to "0" following a reset.

Debounce Control Registers (Read/Write)

(BAR0 + 0x0000 0058 – 0x0000 0064)

These registers are used to control whether each individual channel is to be passed through the debounce logic before being recognized by the circuitry. A "0" disables the debounce logic for the corresponding channel, and a "1" enables the debounce logic. Debounce applies to both inputs and event sense inputs. Bit 0 of each register corresponds to the lowest numbered I/O point, while Bit 7 corresponds to the highest numbered I/O point.

Furthermore, after enabling the debounce circuitry, wait at least three times the programmed debounce duration prior to reading the input ports or event signals to ensure valid data. All bits are set to "0" following a reset.

Debounce Duration Registers (Read/Write)

(BAR0 + 0x0000 0068 – 0x0000 0074)

These registers control the duration required by each input signal before it is recognized by each individual input. Two bits control the debounce duration for each channel. A 31.25MHz internal system clock is used for debounce. The debounce times are selected as shown below (actual times vary to within minus 25% of nominal).

Table 3.5 Debounce Duration Register Channels 0 to 15 (Channels 16 to 31 and 32 to 47 similar)

Bit(s)	FUNCTION	
1 to 0	Channel 0 Debounce Value	
	00	3-4us
	01	48-64us
	10	0.75-1ms
	11	6-8ms
3 to 2	Channel 1 Debounce Value	
	00	3-4us
	01	48-64us
	10	0.75-1ms
	11	6-8ms
. . .	Channel x Debounce Value	
	00	3-4us
	01	48-64us
	10	0.75-1ms
	11	6-8ms
15 to 14	Channel 7 Debounce Value	
	00	3-4us
	01	48-64us
	10	0.75-1ms
	11	6-8ms

Software Reset Register (Write Only)

(BAR0 + 0x0000 0078)

Writing a 1 to the bit 0 position of this register will cause a software reset to occur. This bit is not stored and merely acts as a trigger for software reset generation (this bit will always read back as 0). The Interrupt Enable Bit of the Interrupt Enable and Status register is not cleared in response to a software reset. Bits 1-7 of this register are not used and will always read as zero.

XADC Status/Control Register (Read/Write)

(BAR0 + 0x0000 007C)

This read/write register will access the XADC register at the address set in the XADC Address Register. This allows the board's temperature and supply voltages to be read.

For example, the address of the XADC Status register that is to be accessed is first set via the XADC Address register at BAR0 plus 0x74H. Next, this register at BAR0 plus 0x70H is read. Bits 22 to 16 of this register hold the address of the XADC register that is accessed. Data bits 15 to 6 of this register hold the "ADCcode" temperature, Vccint, or Vccaux value. Data bits 5 to 0 are not used. Valid addresses are given in column one of the table below.

Reading or writing this register is possible via 32-bit data transfers.

The 10-bits digitized and output from the ADC can be converted to temperature by using the following equation.

$$Temperature(°C) = \frac{ADCcode \times 503.975}{1024} - 273.15$$

The 10-bits digitized and output from the ADC can be converted to voltage by using the following equation.

$$SupplyVoltage(volts) = \frac{ADCcode}{1024} \times 3V$$

XADC Address Register (Write Only)

(Bar0 + 0x0000 0080)

This write only register is used to set the XADC address register with a valid address for the XADC internal status or control registers. Valid addresses are given in the following table. Additional addresses can be found in the Xilinx XADC document UG480 (available from Xilinx). Writing this register is possible via 32-bit data transfers.

The address value written to this register can be read on bits 22 to 16 of the XADC Status/Control register at BAR0 plus 0x70H.

Table 3.6: System Monitor Register Map

Address	Status Register
0x00	Temperature
0x01	Vccint
0x02	Vccaux
0x20	Maximum Temperature
0x21	Maximum Vccint
0x22	Maximum Vccaux
0x24	Minimum Temperature
0x25	Minimum Vccint
0x26	Minimum Vccaux

Table 3.7: FPGA Voltage and Temperature Range

	Minimum	Typical	Maximum
Vccint	0.95	1.0	1.05
Vccaux	1.71	1.8	1.89
Temperature operating range	-40C	50-60C	100C

Firmware Revision Register (Read Only) - (BAR0 + 0x0000 0200)

This is a read only register. The ASCII code representing the current revision of the MCS firmware file is readable from this location. For example, if the firmware is at revision A then this register will read 0x41 in the least significant byte or B= 0x42, C=0x43, etc.

The Effect of Reset

A power-up or bus-initiated software reset will disable event sensing and debounce. Pull-up resistors on the I/O lines ensure a false (high) input signal for inputs left floating (i.e. reads as 0). Further, all event inputs are reset, set to negative events, and are disabled following reset. However, the Interrupt Enable bit is not cleared with a software reset.

Basic Input Operation

Note that the input lines of this module are assembled in groups of eight. Each group of eight lines is referred to as a port. Ports 0-3 control and monitor input lines 0-31.

Each port input line is bipolar and accepts both positive and negative input voltages in two ranges according to the model number. Individual input lines of a port share a common signal connection with each other. Separate commons are provided for each port to facilitate port-to-port isolation. A high signal is derived from the absolute value of the input voltage measured between the input line and the port common for the input ranges of 4-18V (AP441-1 models), 16-40V (AP441-2 models), and 38-60V (AP441-3 models). Inputs are non-inverting and inputs left floating (not recommended) will register a low (false=0) input indication.

Each group of eight parallel input lines (a port) are isolated. A high input will read as "1" and all inputs include hysteresis and programmable debounce.

Event Sensing

The AP441 has edge-programmable event sense logic built-in for all 32 input lines, IN00 through IN31. Event sensing may be configured to generate an interrupt to the carrier, or to merely reflect the interrupt internally. The event sensing is enabled on an individual channel basis. Each input can be set to detect positive, negative or change-of-state events. You can combine event sensing with the built-in debounce control circuitry to obtain "glitch-free" edge detection of incoming signals.

To program events, determine which input lines are to have events enabled, what type of event to detect (transition or change-of-state) and which polarity is to be detected, high-to-low level transitions (negative) or low-to-high level transitions (positive). Set each corresponding bit to the desired type and polarity, and then enable each of the event inputs to be detected. Optionally, if interrupt requests are desired, enable interrupts in the Interrupt Register. Note that all event inputs are reset, set to negative events, and disabled after a power-up or software reset has occurred.

Debounce Control

Debounce control is built into the on-board digital FPGA employed by the AP441. You can combine debounce with event sensing to obtain "glitch-free" edge detection of incoming signals for all 32 channels. That is, the debounce circuitry will automatically filter out "glitches" or transients that can occur on received signals, for error-free edge detection and increased noise immunity.

With debounce, an incoming signal must be stable for the entire debounce time before it is recognized by the I/O or event sense logic. Debounce is applied to both inputs and event sense inputs.

A debounce value of 4us, 64us, 1ms, or 8ms may be selected (see the Debounce Duration Registers). As such, an incoming signal transition must be stable for the debounce time before it is recognized by the I/O pin or event sense logic.

Upon initialization of the debounce circuitry, be sure to delay at least the programmed debounce time before reading any of the input channels or event signals to ensure that the input data is valid prior to being used by the software.

Interrupt Generation

This model provides control for generation of interrupts on change-of-state, or positive or negative events, for all 32 channels. Interrupts are only generated when events are enabled via the Event Enable registers. Writing "1" to the corresponding event sense bit in the Event Pending/Clear register will clear the event. Interrupts may be reflected internally and reported by polling the module. Control of this feature is done via bit 0 of the Interrupt Enable Register.

The event sense status is a flag that is raised when a specific change-of-state, positive, or negative transition has occurred for a given I/O point, while the state refers to its current level. Enabling both an Event Sense bit and the board interrupts will allow interrupts to be generated

Note that the Interrupt Enable Register is cleared following a power-up or bus initiated hardware reset, but not a software reset initiated via writing a one to bit 0 of the Software Reset Register. Keep this in mind when you wish to preserve the information in these two registers following a reset.

Programming Example

The following example outlines the steps necessary to configure the AP441 to setup event-generated interrupts, configure debounce, and read inputs. It is assumed that the module has been reset and no prior (non-default) configuration exists.

For this example, we will configure Port A inputs as an 4-channel change-of-state detector. Any change-of-state detected on these input signal lines will cause an interrupt to be generated.

1. The default debounce duration is 4µs. This time applies to the FPGA input signal and does not include opto-coupler delay. Write 0x0055 to the Debounce Duration Register at BAR0 + 0x0000 0068 to select a 64µs debounce time for channels 0 thru 3. An incoming signal must be stable for the entire debounce time before it will be recognized as a valid input transition.

If the module had been configured earlier, you would first read this register to check the existing settings of debounce duration for the other channels in Port A with the intent of preserving their configuration by adjusting the value written above.

2. Enable the debounce circuitry for channel 0 thru 3 inputs by setting bits 0 thru 7 of the Debounce Control Register at BAR0 + 0x0000 0058. Write 000FH to the Debounce Control Register. If the module had been configured earlier, you would first read this register to check the existing settings of debounce enable for the other channels in Port A with the intent of preserving their configuration by adjusting the value written above.

3. For our example, channels 0 thru 3 will be used to detect change-of-state transitions. Write 000FH to the Event Type Register at BAR0 + 0x0000 0028 to set channels 0 thru 3 to change-of-state detection. Note that the Event Polarity Registers are not used if change-of-state type events are selected. If the module had been configured earlier, you would first read this register to check the existing settings of event type for the other channels in Port A with the intent of preserving their configuration by adjusting the value written above.

4. To enable event sensing for channels 0 thru 3, write 000FH to the Event Enable Register at BAR0 + 0x0000 0018.

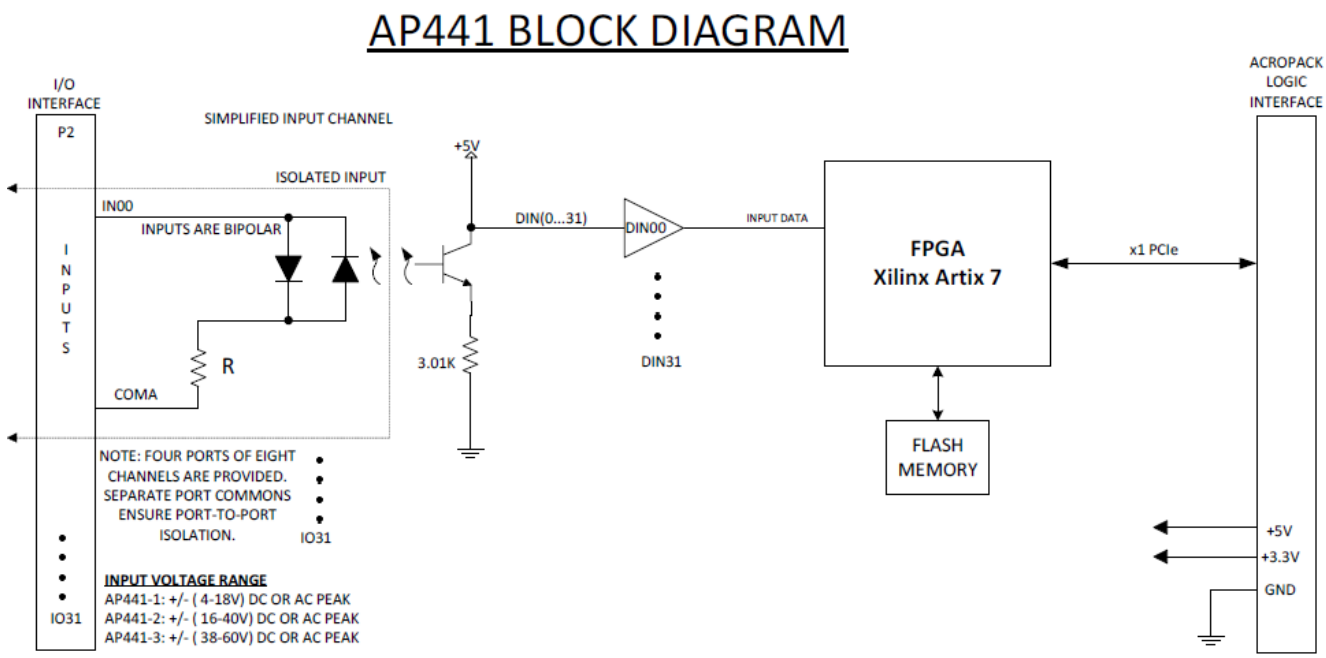
5. (OPTIONAL) Write 01H to the Interrupt Enable Register to enable interrupt request.

   When a change-of-state is detected, an interrupt will be generated (if the event sense detection circuitry has been enabled and Interrupt Enable bit 0=1).

   Note that the state of the inputs (on/off) can be determined by reading the corresponding Input Registers. The event sense status can only be determined by reading the corresponding Event Pending/Clear Register. Remember, the event sense status is a flag that is raised when a specific transition has occurred for a given input point, while the state refers to its current level.

4.0 THEORY OF OPERATION

This section provides a description of the basic functionality of the circuitry used on the board. Refer to the Block Diagram shown below as you review this material.



4.1 AcroPack 441 Operation

The AP441 is built around a digital FPGA chip that provides I/O interface and configuration functions. This chip performs monitor and control functions of up to 32 open-drain inputs. The FPGA also provides debounce control and event sensing functions. The FPGA provides the control interface necessary to operate the module.

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.1). Individual optocouplers for each channel isolate the field from the control logic for the AP441. Channels are isolated from each other in groups of eight. There are eight channels to a group or port. Because the output lines of a single port share a common connection, individual outputs are not isolated from each other within the same port. However, separate port commons are provided to facilitate port-to-port isolation.

Input optocouplers of this device are bipolar and accept voltages in three ranges: ± (4-18V), ± (16-40V), and ± (38-60V), DC or AC peak. The optocouplers connect directly to the FPGA functioning as a controller that provides the I/O read/write functionality, interrupt handling, and debounce control.

4.2 PCIe Interface Logic

The PCIe bus interface logic is imbedded within the FPGA. This logic includes support for PCIe commands, including: configuration read/write, and

memory read/write. In addition, the PCIe target interface uses a single 4K base address register, and implements target abort, retry, and disconnect. The AP441 logic also implements interrupt requests via the PCIe bus.

A FPGA device provides the control signals required to operate the board. It decodes the selected addresses, control signals, and interrupt handling. It also returns the acknowledgement messages required by the carrier/CPU board per the PCIe specification. The program for the FGPA is stored in separate Flash memory and loaded upon power-up.

5.0 SERVICE AND REPAIR

5.1 Service and Repair Assistance

Surface-Mounted Technology (SMT) boards like the AcroPack family of carrier and I/O boards are generally difficult to repair. The board can be easily damaged unless special SMT repair and service tools are used. For these and other reasons, it is strongly recommended that a non-functioning board be returned to Acromag for repair. Acromag has automated diagnostic and test equipment that thoroughly checks the performance of suspect boards. Furthermore, when any repair is made, the board is retested before return shipment to the customer.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts, or return parts for repair.

5.2 Preliminary Service Procedure

CAUTION: POWER MUST BE TURNED OFF BEFORE SERVICING BOARDS

Before beginning repair, be sure that all of the procedures in the "Preparation for Use" section have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique for isolating a faulty part.

5.3 Where to Get Help

If you continue to have problems, your next step should be to visit the Acromag website at https://www.acromag.com. Our website contains the most up-to-date product and software information.

Go to the "Support" tab or your specific AcroPack model ordering page.

Acromag's application engineers can also be contacted directly for technical assistance via email, telephone, or FAX through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab. When needed, complete repair services are also available.

Phone: 248-295-0310
Email: solutions@acromag.com

6.0 SPECIFICATIONS

6.1 Physical

Height: 12.5 mm (0.4921 in)

Height defines Carrier to Module Maximum component height

Board Thickness 1.0 mm (0.03937 in)

- AcroPack L x W: 70 mm x 30.00 mm (2.76 in x 1.18 in)

Unit Weight (does not include shipping material):

- AcroPack 0.314 ounces (8.9 g)

6.2 Power Requirements

Summarized below are the expected current draws for each of the specified power supply voltages.

Power Supply Voltage	Current Draw
3.3 VDC +/- 5%[1]	0.48 A Typical, 0.63 A maximum
1.5 VDC +/- 5%[1]	Not Used
5.0 VDC +/- 5%[1]	0.048 A Typical, 0.052 A maximum
+12 VDC +/- 5%[1]	Not Used
-12 VDC +/- 5%[1]	Not Used

Note 1: *Typical current draw is using an AP441-1E-LF*

6.3 Environmental Considerations

Summarized below are the operating temperature range, airflow and other environmental requirements and applicable standards for the AcroPack module.

6.3.1 Operating Temperature

Model Number	***Description***	***Temp Range***
AP441-1E-LF	± 4V to ±18V DC or AC peak	*-40*°C *to 85*°C[1,2]
AP441-2E-LF	± 16V to ±40V DC or AC peak	*-40*°C *to 85*°C[1,2]
AP441-3E-LF	± 38V to ±60V DC or AC peak	*-40*°C *to 85*°C[1,2]

Note 1: An air cooled application with an AcroPack module will require a minimum airflow of 200LFM.

Note 2: Applications requiring operating temperatures of *70*°C *to 85*°C will require purchase of *AcroPack Heatsink Accessory* ***AP-CC-01.***

6.3.2 Relative Humidity

The range of acceptable relative humidity is 5% to 95%, non-condensing.

6.3.3 Isolation

Logic and field connections are optically isolated (see INPUT specifications). Individual ports are also isolated from each other. However, input lines of individual ports share a common connection and are not isolated from each other. Separate port commons are provided to facilitate port-to-port working voltage isolation of 100V (r.m.s. or DC). Logic and field lines are isolated from each other for working voltages up to 250V (r.m.s. or DC) on a continuous basis (unit will withstand a 1250V AC dielectric strength test for one minute without breakdown).

6.3.4 Vibration and Shock Standards

The AcroPack is designed to meet the following Vibration and Shock standards.

Vibration, Sinusoidal Operating: Designed to comply with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis

Vibration, Random Operating: Designed to comply with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis

Shock, Operating: Designed to comply with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3mS half sine, 18 shocks at 6 orientations for both test levels

6.3.5 EMC Directives

The AcroPack complies with EMC Directive 2014/30/EU.

- **Immunity per EN 61000-6-2:**
  Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2.
  Radiated Field Immunity (RFI), per IEC 61000-4-3.
  Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4.
  Surge Immunity, per IEC 61000-4-5.
  Conducted RF Immunity (CRFI), per IEC 61000-4-6.
- **Emissions per EN 61000-6-4:**
  Enclosure Port, per CISPR 16.
  Low Voltage AC Mains Port, per CISPR 16.
  Note: This is a Class A product

6.4 Reliability Prediction

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled,* $G_B G_C$

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	1,627,792	185.8	614.3
40°C	1,002,977	114.5	997.0

[1] FIT is Failures in 10^9 hours.

6.5 INPUTS

Input channel Configuration	32 Optically isolated bipolar inputs. For DC or AC voltage applications within specified range limits.
Isolation Medium	Photo-transistor optocoupler, Renesas PS2915-1 or equivalent.
Bipolar Input Voltage Range	AC or DC Volts peak, according to model number: ±4V to ±18V (Model AP441-1E-LF); ± 16V to ± 40V (Model AP441-2E-LF); ± 38V to ± 60V (Model AP441-3E-LF).
Input Threshold	Input Low-to-High threshold is: ±4V Maximum, ±2.0V Typical (AP441-1E-LF); ±16V Maximum, ±6.4V Typical (AP441-2E-LF); ±38V Maximum, ± 12.9V Typical (AP441-3E-LF). The AP441-1E-LF model may be used to interface with open-drain TTL outputs when used with an appropriate pullup to +5V.
Input Hysteresis	80mV Typical
Input Capacitance	45pF Typical
Turn-On Time	Measured to the point of positive event interrupt detection - 15us Typical (25°C) for a 0 to threshold value input step. This time increases as the magnitude of the step is increased above the threshold.
Turn-Off Time	Measured to the point of negative event interrupt detection - 35us Typical (25°C) for a threshold to 0V input step. This time increases as the magnitude of the step value is increased from the threshold.
Input Debounce	Each input includes debounce circuitry with variable debounce times. Debounce times are programmable and derived from a 31.25MHz clock, in combination with the debounce duration register value. Debounce times are applied at the FPGA input and do not include optocoupler delay time. Debounce values of 3-4us, 48-64us, 0.75-1ms, and 6-8ms may be configured.
Interrupts	32 channels of interrupts may be configured for high-to-low, low-to- high, and change-of-state event types.
Forward Voltage Drop	1.1V Typical, 1.5V Maximum (Diode) + I*R. Series input current-limiting resistors are 1.62K (AP441-1E-LP), 10K (AP441-2E-LP), or 21.5K (AP441-3E-LP) and installed on board.

Input Current	Varies according to model number and input signal voltage level. For Model AP441-1E-LF, the current is computed by dividing the signal level minus 1.5V, by its current limiting resistor (1620Ω for AP441-1E-LF, 10000Ω for AP441-2E-LF, and 21500Ω for AP441-3E-LF).

6.6 PCIe Bus Specifications

Compatibility	Conforms to PCI Express Base Specification, Revision 2.1
Line Speed	Gen1 (2.5Gbps) Available through system connector
Lane Operation	1-Lane
4K Memory Space Required	One Base Address Register (BAR)

Table 6.6 PCIe Bus Data Rates

PCIe Gen 1 (1 lane)	Giga bit / second	Bytes / second
Signaling Rate	2.5 Gb/s	312 Mbyte/s
Ideal Rate[1]	2 Gb/s	250 Mbyte/s
Header Burden plus 4byte Sample Rate[2]	0.332 Gb/s	41.6 Mbyte/s
Actual Measured 4 Byte Read Rate[3]	0.019 Gb/s	2.35 Mbytes/s
Actual Measured DMA 4 Byte Read Rate[4]	0.327 Gb/s	40.9 Mbyte/s
Actual Measured 4 Byte Write Rate[5]	0.320 Gb/s	40 Mbyte/s

Note 1: PCIe x1 Gen 1 = 2.5GT/s (with 10-bit encoding there is a 20% loss in possible throughput due to encoding) giving 2.0 G bits/sec or 250M Bytes/sec.

Note 2: A header for address and read/write command is sent with every packet. This header is 20 Bytes with data payload of 4 Bytes (for a typical AcroPack). For each 4 Byte data sample, 24 Bytes are sent.

$\frac{250MByte/s}{24\ Bytes}$ = 10.4 M samples/sec or 41.6 M Bytes/sec or 0.332 G bit/sec

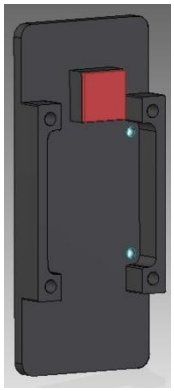
Note 3: For a typical AcroPack measured back to back 4 Byte read operations completing every 1.7usec. A read operation starts with a host read request. The AcroPack must process the read and fetch the data and then generated the completion back to the host. The host then sends a message back that says I got it. This back and forth hand shaking slows down individual reads.

Note 4: DMA Read of 1024 sample takes 100us. Each sample is 4 Bytes. 100us/1024=0.0977us per sample or 4/0.0977us = 40.94Mbyte/s. DMA is used to improve data transfer speed on the AP341/2 and AP225/235.

Note 5: Simple write operations are just as fast as DMA read operations. Write data is presented to the AcroPack in one transaction. Measured 4-byte back to back write accesses taking place every 100ns.

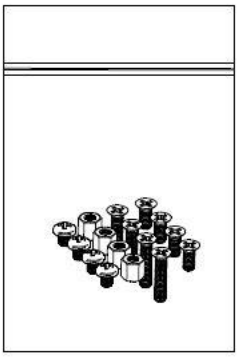
Appendix A

AP-CC-01 Heatsink Kit Installation



Bottom view

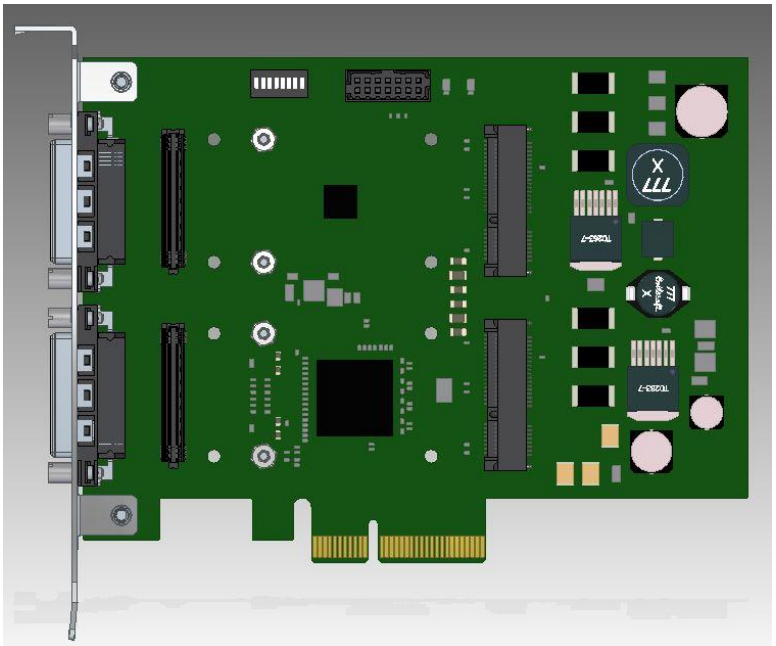
Top view



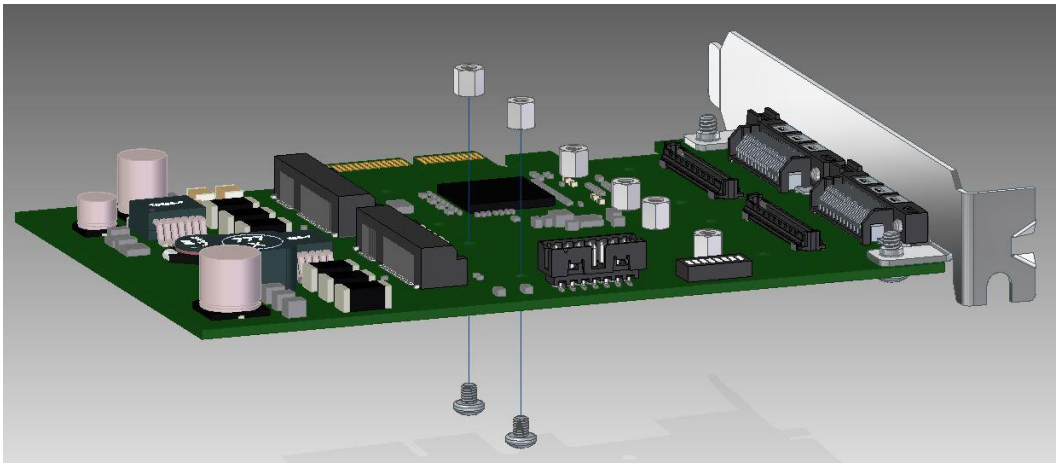
Hardware

AP-CC-01 Heat Sink Kit

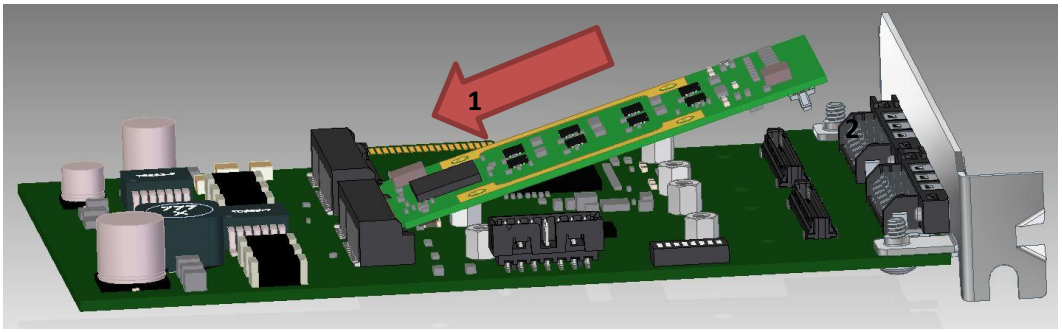
This example will show how to install the AP-CC-01 Heatsink kit with an APCe7020 carrier.



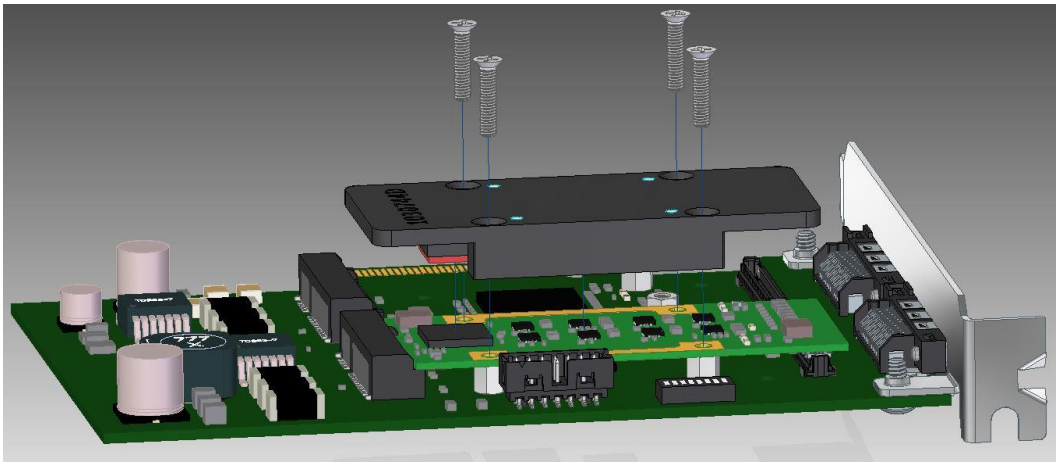
1. Install two standoffs and secure with two screws.



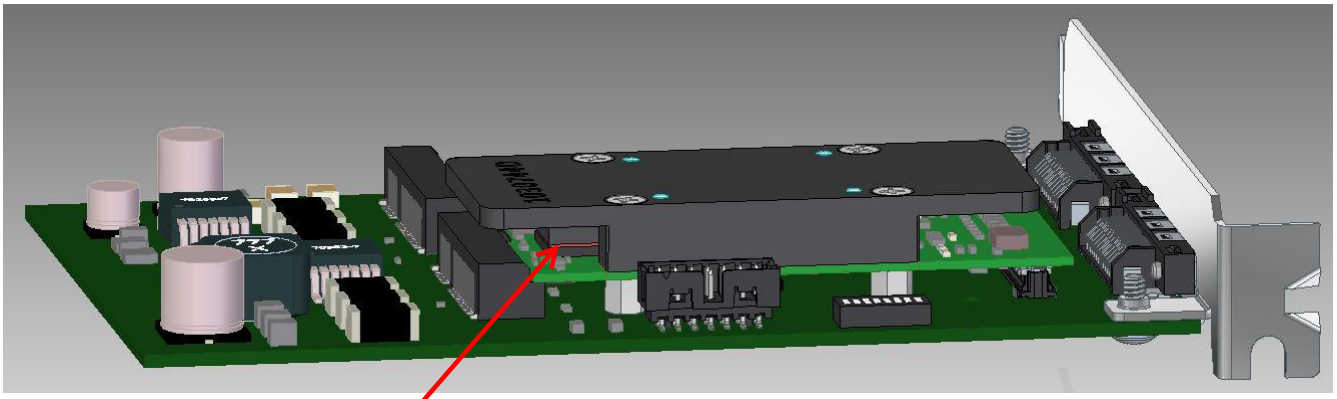
2. Install the AcroPack module.



3. Install the Heatsink and secure with 4 screws.



4. AP-CC-01 Installation is complete.



Note: Make sure the thermal pad is making contact with the FPGA IC.

Appendix B

Figure 1 AP441 Block Diagram

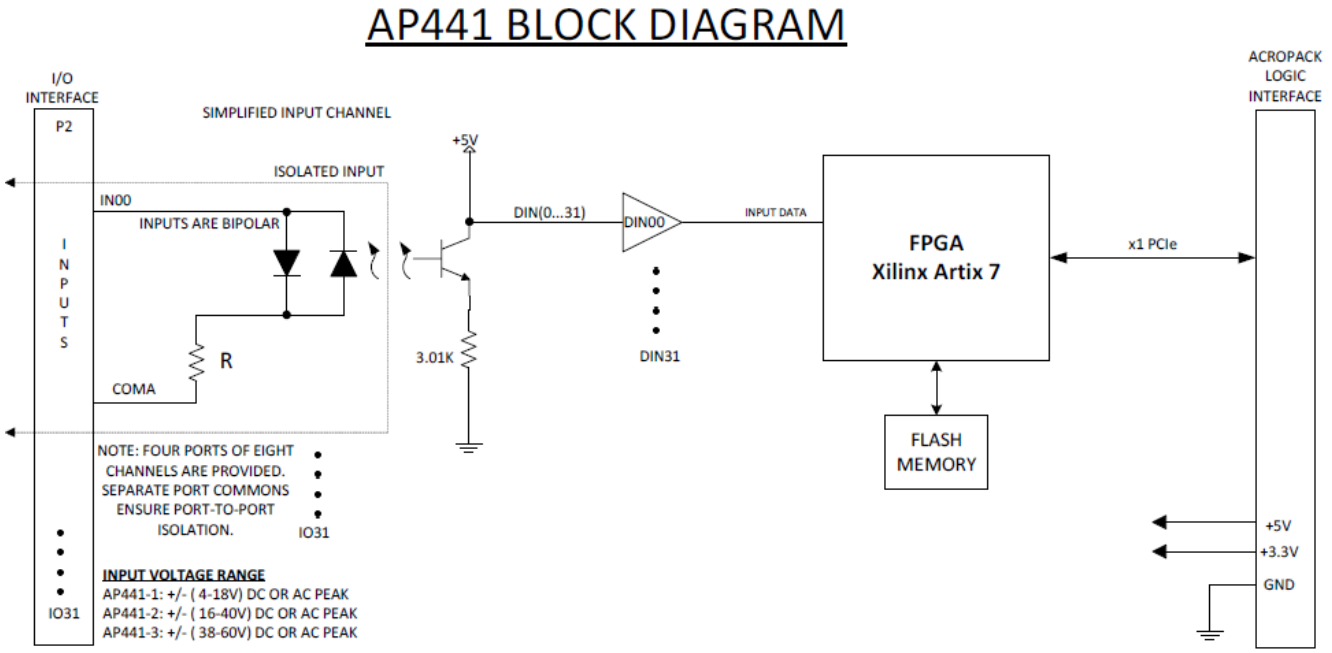
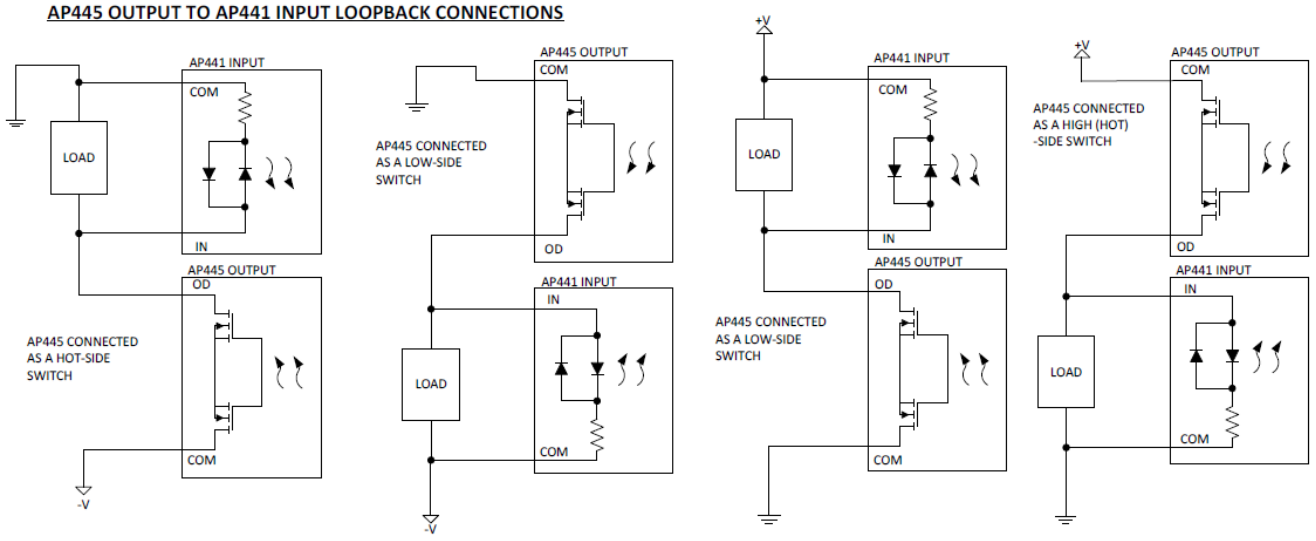
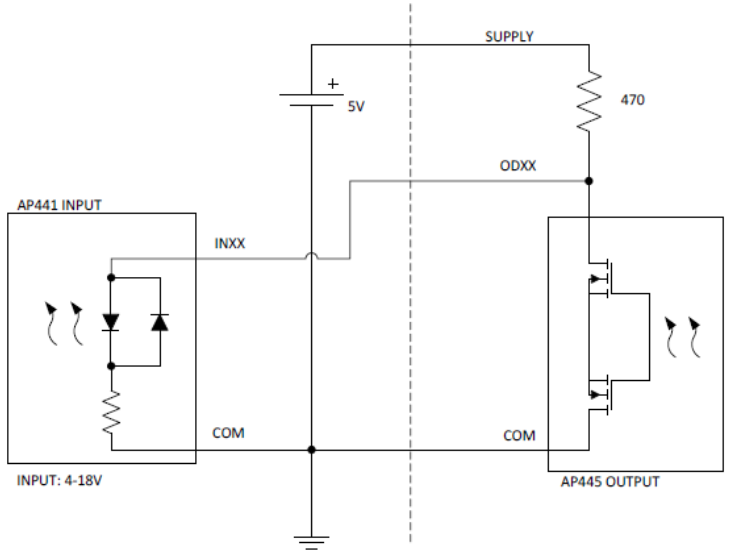


Figure 2 AP441 and AP445 Loopback Interconnect



NOTE THAT FOR LOOPBACK PURPOSES, THE COMMON LINE OF AN AP441 PORT AND THE COMMON LINE OF AN AP445 PORT DO NOT NECESSARILY CONNECT TOGETHER.

THE AP441 & AP445 INCLUDE 4 PORTS OF 8 CHANNELS EACH. EACH PORT SHARES A PORT COMMON. SEPARATE PORT COMMONS FACILITATE PORT TO PORT ISOLATION. THE AP445 ALSO INCLUDES SEPARATE PORT SUPPLY PINS FOR CONNECTING TO THE ON-BOARD PULLUPS.



AP445 DIGITAL OUT TO AP441 DIGITAL INPUT

WHEN INTERFACING DIGITAL OUTPUT LEVELS TO THE AP441, USE THE MODEL AP441-1 (4V THRESHOLD) AND ADJUST THE EXTERNAL PULLUP VALUE ACCORDINGLY.

470 OHM PULLUPS SHOULD BE INSTALLED ON THE AP445.

WHEN INTERFACING THE AP445 TO A TYPICAL TTL INPUT DEVICE LIKE THE 74LS541. THE 4.7K PULLUPS SHOULD BE INSTALLED AND THE CONNECTED TO THE PART SUPPLY PIN.

P2 PINOUTS OF THE AP441 AND AP445 ARE DIRECTLY COMPATABLE. HOWEVER, THE AP445 INCLUDES A PULLUP SUPPLY PIN FOR EACH PORT AT PIN 5 (PORT0), PIN 15 (PORT 1), PIN 25 (PORT 2), AND PIN 35 (PORT 3). THESE PINS ARE NOT CONNECTED ON THE AP441.

AP441 INPUTS AND AP445 OUTPUTS ARE BIPOLAR AND MAY BE CONNECTED IN ANY DIRECTION WITH RESPECT TO PORT COMMON.

Certificate of Volatility

Acromag Model AP441E-LF	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) ■ Yes □ No				
Type (SRAM, SDRAM, etc.) Configurable Logic Blocks and Block RAM Blocks	Size: 16,640 Logic Cells and 900 Kb Block RAM	User Modifiable ■ Yes □ No	Function: FPGA logic blocks and RAM blocks.	Process to Sanitize: Power Down
Type (SRAM, SDRAM, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No				
Type(EEPROM, Flash, etc.) Flash	Size: 32Mb	User Modifiable ■ Yes □ No	Function: Data storage for FPGA	Process to Sanitize: Erase using JTAG
Type(EEPROM, Flash, etc.) One Time Programmable area in flash device	Size: 3 x 256-byte	User Modifiable □ Yes ■ No	Function: The OTP area has been disabled by writing the lock bits with logic 1.	Process to Sanitize: Not applicable

Acromag Representative				
Name: Russ Nieves	Title: Sales and Marketing	Email: solutions@acromag.com	Office Phone: 248-295-0310	Office Fax: 248-624-9234

Revision History

The revision history for this document is summarized in the table below.

Release Date	Version	EGR/DOC	Description of Revision
30 MAR 2018	A	ENZ/MJO	Document Release.
13 NOV 2020	B	ENZ/AMM	Added MTBF Information.