AP341 AcroPack

Simultaneous Sample and Hold Analog to Digital Converter Module

USER'S MANUAL

ACROMAG INCORPORATED
30765 South Wixom Road
Wixom, MI 48393-2417 U.S.A.
Tel: (248) 295-0310

8501058C

Table of Contents

1. GENERAL INFORMATION

Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the AcroPack module.

Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag.

Trademark, Trade Name and Copyright Information

Class A Product Warning

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

AcroPack Information – All Models

The AcroPack IO modules are based on the PCI Express Mini Card Electromechanical specification and are 70mm in length with an added 100 pin field I/O connector.

The AcroPack is 19.05mm longer than the full length mini PCIe card at 50.95mm. It has the same mPCIe board width of 30mm and uses the same mPCIe standard board hold down standoff and screw keep out areas.

Ordering Information

The AcroPack ordering options are given in the following table.

Table 1 AP341 Modules

Model Number	*Description*
AP341E-LF	16 channel, 14-bit, simultaneous sample and hold ADC module

Operating temperature range for all models: -40°C to 80°C. Applications requiring operating temperatures above 70°C will require purchase of AcroPack Heatsink Accessory AP-CC-01. See Appendix A for installation instructions.

Key Features

- **ADC 14-bit Resolution** – Eight individual, 14-bit, successive approximation, Analog to Digital Converters (ADC), with integral sample and hold, are utilized.
- **8us Conversion Time** – A maximum conversion rate of 125KHz is supported.
- **1025 Sample FIFO Buffer** – A single 1025 sample deep FIFO is available for buffering data from the 16 differential channels. This allows the external processor to service more tasks within a given time. Data tagging is implemented for easy channel identification. The FIFO buffer can be read through host generated PCIe read transactions or through DMA transactions.
- **Interrupt Upon FIFO Threshold Reached** – FIFO interrupt generation is also supported. Upon reaching a FIFO programmable threshold condition an interrupt can be generated to minimize CPU interaction.
- **Automatic DMA Transfers Upon FIFO Threshold Reached** – In Auto DMA Mode, DMA transfers will automatically be started when the FIFO threshold has been met to minimize CPU interaction.
- **FIFO Full, Empty and Threshold Reached Flags** – FIFO Full, Empty and Threshold Reached flag bits are available to implement software polling schemes for FIFO buffer data control.
- **Programmable Control of Channels Converted** – Up to 16 differential analog inputs are monitored. Channels 0 to 7 are simultaneously converted followed by the simultaneous conversion of channels 8 to 15. Channels may be individually enabled/disabled for simultaneous conversion.
- **User Programmable Conversion Timer** – A programmable conversion timer is available to control the time between simultaneous conversion of new banks of channel data. For example, channels 0 to 7 are converted immediately upon trigger and then channels 8 to 15 are converted after a

user programmable delay from the start of the first eight channels. An overall count value is also used to control when conversions will start again with the first eight channels. Supports a maximum interval of 274.9 seconds.

- **Continuous Conversion Mode** – All channels selected for conversion are continually digitized with the interval between conversions controlled by the programmed conversion timer registers. Scanning is initiated by a software or external trigger. Scanning is stopped by software control.
- **Single Cycle Conversion Mode** – All channels selected for conversion are digitized once with the time between channels 0 to 7 and group 8 to 15 controlled by a programmable timer. Single cycle conversion mode is initiated by a software or external trigger.
- **External Trigger Input or Output** – The external trigger is assigned to a field I/O line. This external trigger may be configured as an input, output or disabled. As an output, this signal provides a means to synchronize other modules to a single AP341 timer reference.
- **Calibration Constants** – Factory calibration constants used to correct gain and offset errors are stored in on-board flash memory. Gain and offset correction constants are stored for each analog to digital converter.
- **Fault Protected Input Channels** – Analog input overvoltage protection to +/-25V with power on and +/-40V with power off.

Signal Interface Products

This AcroPack Module will mate directly to all Acromag AP carriers. Once connected, the module is accessed via a 50 pin or 68 pin front panel connector.

Compatible cables and termination panels are also available. For optimum performance with the AP341 analog to digital controller module, use of the shortest possible length of shielded I/O cable is recommended.

PCIe Interface Features

- **PCIe Bus** – The example design includes a PCI Express Generation 1 interface operating at a bus speed of 2.5 Gbps per lane per direction.
- **PCIe Bus Master** – The PCIe interface logic becomes the bus master to perform DMA transfers.
- **DMA Operation** – The design includes a DMA controller to move data between the FPGA memory and the PCIe bus interface.
- **Compatibility** – PCI Express Base Specification v2.1 compliant PCI Express Endpoint. Provides one interrupt.

Software Support

The AcroPack series products require support drivers specific to your operating system. Supported operating systems include: Linux®, Windows®, and VxWorks®.

Windows

Acromag provides software products (sold separately) to facilitate the development of Windows applications interfacing with AcroPack modules, VPX I/O board products, and PCIe I/O Cards. This software (model APSW-API-WIN) consists of low-level drivers and Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

VxWorks

Acromag provides a software product (sold separately) consisting of VxWorks software. This software (Model APSW-API-VXW) is composed of VxWorks (real time operating system) libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

Linux

Acromag provides a software product consisting of Linux software. This software (Model APSW-API-LNX) is composed of Linux libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

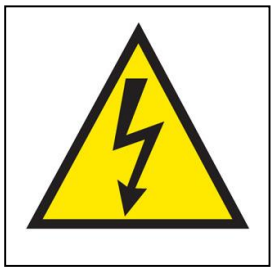
References

The following resources regarding AcroPack modules are available for download on Acromag's website or by contacting your sales representative.

- PCI Express MINI Card Electromechanical Specification, REV 1.2 http://www.pcisig.com

2. PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.

WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

Card Cage Considerations

Refer to the specifications section for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

In an air cooled assembly, adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and

to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

In a conduction cooled assembly, adequate thermal conduction must be provided to prevent a temperature rise above the maximum operating temperature.

Board Installation

Power should be removed from the board when installing AP modules, cables, termination panels, and field wiring. Model AP341 boards have no hardware jumpers or switches to configure.

Non-Isolation Considerations

The board is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

Field I/O Connector

The field I/O interface connector P2 provides a mating interface between the AP341 modules and the carrier board.

Table 2 lists pin assignments for each of the AP341 field I/O signals. Every other pin of the 100 pin P2 connector is left unconnected.

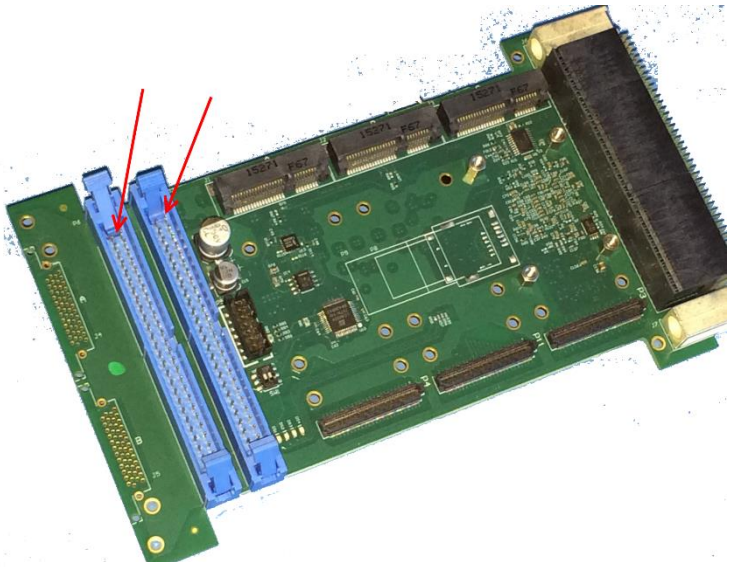
Table 2 Field I/O Connector Pin Assignments

Carrier Connector Ribbon[1]	Carrier Connector 50 Pin Champ[2]	Carrier Connector 68 Pin Champ	Module P2 Pin Number	Field I/O Signal
1	1	1	2	CH0+
2	26	35	1	CH0-
3	2	2	6	CH8+
4	27	36	5	CH8-
5	3	3	10	GND
6	28	37	9	GND
7	4	4	14	CH1+
8	29	38	13	CH1-
9	5	5	18	CH9+
10	30	39	17	CH9-
11	6	6	22	GND
12	31	40	21	GND

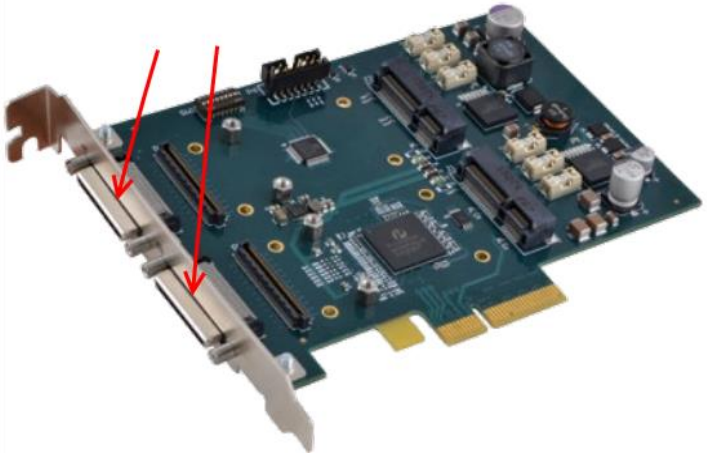
Carrier Connector Ribbon[1]	Carrier Connector 50 Pin Champ[2]	Carrier Connector 68 Pin Champ	Module P2 Pin Number	Field I/O Signal
13	7	7	26	CH2+
14	32	41	25	CH2-
15	8	8	30	CH10+
16	33	42	29	CH10-
17	9	9	34	GND
18	34	43	33	GND
19	10	10	38	CH3+
20	35	44	37	CH3-
21	11	11	42	CH11+
22	36	45	41	CH11-
23	12	12	46	GND
24	37	46	45	GND
25	13	13	50	CH4+
26	38	47	49	CH4-
27	14	14	54	CH12+
28	39	48	53	CH12-
29	15	15	58	GND
30	40	49	57	GND
31	16	16	62	CH5+
32	41	50	61	CH5-
33	17	17	66	CH13+
34	42	51	65	CH13-
35	18	18	70	GND
36	43	52	69	GND
37	19	19	74	CH6+
38	44	53	73	CH6-
39	20	20	78	CH14+
40	45	54	77	CH14-
41	21	21	82	GND
42	46	55	81	GND
43	22	22	86	CH7+
44	47	56	85	CH7-
45	23	23	90	CH15+
46	48	57	89	CH15-
47	24	24	94	GND

Carrier Connector Ribbon[1]	Carrier Connector 50 Pin Champ[2]	Carrier Connector 68 Pin Champ	Module P2 Pin Number	Field I/O Signal
48	49	58	93	GND
49	25	25	98	EXT_TRIGn
50	50	59	97	GND

Note 1: VPX4500-CC-LF is an example of a carrier that uses the ribbon cable connector see image of carrier.



Note 2: APCe7020E-LF is an example of a carrier that uses the Champ connector see image of carrier.



When reading Table 2 note that channel designations are abbreviated to save space. For example, channel 0 is abbreviated as "CH0+" & "CH0-" for the + & - connections, respectively.

The external trigger signal on pin 98 of the Field I/O Connector can be programmed as an input, output or disabled.

The external trigger will accept an external trigger signal when programmed as an input. The external trigger must be a 3.3V logic, TTL-compatible, debounced signal referenced to analog common. The external trigger is an active low edge sensitive signal. That is, the external trigger signal will trigger

the module on the falling edge. Once the external trigger has been driven low, it should remain low for a minimum of 250 nanoseconds.

The external trigger signal will generate triggers to allow synchronization of multiple AP341 modules when programmed as an output. The external trigger output is a 250 nanosecond active low trigger signal driven from the module.

The external trigger can also be disabled. This prevents external noise from falsely triggering the module. See the Analog to Digital Converter Control and Data Registers section for programming details to make use of this signal.

Noise and Grounding Considerations

Differential inputs require two leads (+ and -) per channel, and provide rejection of common mode voltages. This allows the desired signal to be accurately measured. However, the signal being measured cannot be floating – it must be referenced to analog common on the IP module and be within the normal input voltage range.

Differential inputs are the best choice when the input channels are sourced from different locations having slightly different ground references and when minimizing noise and maximizing accuracy are key concerns. See the input connection diagram in Appendix B for analog input connections for differential ended inputs. Shielded cable of the shortest length possible is also strongly recommended.

The AP341 is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the carrier board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections. This is particularly important for analog inputs when a high level of accuracy/resolution is needed. Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the AP341 input modules.

Logic Interface Connector

The AP module logic edge connector interfaces to the mating connector on the carrier board. The pin assignments of this connector are standard for all AP modules according to the PCI Express MINI Card Electromechanical Specification, REV 1.2 (with exceptions shown in Table 3 and noted below).

Power supplies +5, +12, and -12 Volt have been assigned to pins that are reserved in the mini-PCIe specification. The Present signal is grounded on the AP module. In addition, COEX1, COEX2 – wireless transmitter controls, are reassigned to JTAG signals TMS and TCK. Lastly, UIM_C4, UIM_C8 – reserved User Identity Module signals are reassigned to JTAG signals TDI and TDO.

Table 3 Mini-PCIe Connector

Pin #	Name	Pin #	Name
51	**+5V**[2]	52	+3.3V[3]
49	**+12V**[2]	50	GND
47	**-12V**[2]	48	N.C.(+1.5V)[1]
45	**Present**[2]	46	N.C. (LED_WPAN#)[1]
43	GND	44	N.C. (LED_WLAN#)[1]
41	+3.3V[3]	42	N.C. (LED_WWAN#)[1]
39	+3.3V[3]	40	GND
37	GND	38	N.C. (USB_D+)[1]
35	GND	36	N.C. (USB_D-)[1]
33	PETp0	34	GND
31	PETn0	32	SMB_DATA[4]
29	GND	30	SMB_CLK[4]
27	GND	28	N.C.(+1.5V)[1]
25	PERp0	26	GND
23	PERn0	24	+3.3V[3]
21	GND	22	PERST#
19	**TDI** (UIM_C4)[1]	20	N.C. (W_DISABLE#)[1]
17	**TDO** (UIM_C8)[1]	18	GND
15	GND	16	N.C.(UIM_VPP)[1]
13	RECLK+	14	N.C.(UIM_RESET)[1]
11	REFCLK-	12	N.C.(UIM_CLK)[1]
9	GND	10	N.C.(UIM_DATA)[1]
7	CLKREQ#[1]	8	N.C.(UIM_PWR)[1]
5	**TCK** (COEX2)[1]	6	N.C.(+1.5V)[1]
3	**TMS** (COEX1)[1]	4	GND
1	N.C. (WAKE#)[1]	2	+3.3V[3]

1. **Note 1:** Signals are not applicable for the AP341 implementation. Pins are either "no connects" on the module or are repurposed for JTAG (pins 3, 5, 17, 19).
2. **Note 2:** +5, +12, and -12 Volt power supplies have been assigned to pins that are reserved in the mini-PCIe specification. The Present signal is tied to circuit common on the AP module.
3. **Note 3:** All +3.3Vaux power pins are changed to system +3.3V power.
4. **Note 4:** The SM bus signals SMB_CLK and SMB_DATA will be used to clock a carrier location serial stream from the carrier. These signals are under the control of the AcroPack module.

3. PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the board.

PCIe CONFIGURATION ADDRESS SPACE

This AP341 module is PCI Express Base Specification Revision v2.1 compliant.

The PCIe bus is defined to address three distinct address spaces: I/O, memory, and configuration space. This board can be accessed via the PCIe bus memory and configuration spaces.

The card's configuration registers are initialized by system software at power-up to configure the card. The board is a Plug-and-Play PCIe card. As a Plug-and-Play card the board's base address and system interrupt request are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCIe bus configuration access is used to read/write the PCIe card's configuration registers.

When the computer is first powered-up, the computer's system configuration software scans the PCIe bus to determine what PCIe devices are present. The software also determines the configuration requirements of the PCIe card.

The system software accesses the configuration registers to determine how many blocks of memory space the module requires. It then programs the board's configuration registers with the unique memory base address.

Since this board is not fixed in address space, its device driver must use the mapping information stored in the board's Configuration Space registers to determine where the board is mapped in memory space.

The configuration registers are also used to indicate that the board requires an interrupt request. The system software then programs the configuration registers with the interrupt request assigned to the board.

CONFIGURATION REGISTERS

The PCIe specification requires software driven initialization and configuration via the Configuration Address space. This board provides 512 bytes of configuration registers for this purpose. It contains the configuration registers shown in Table 4 to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers and the Interrupt Register which must be read to determine the base address assigned to the board and the interrupt request that goes active on a board interrupt request.

Table 4 Configuration Registers

Reg. Num.	D31 D24	D23 D16	D15 D8	D7 D0
0	**Device ID** 0x7019 AP341E-LF		**Vendor ID** 16D5	
1	Status		Command	
2	Class Code=118000			Rev ID=00
3	BIST	Header	Latency	Cache
4:5	64-bit Memory Base Address for Memory Accesses to PCIe interrupt, I/O registers, System Monitor registers, and Flash memory. 8K Space **(BAR0)**			
6:10	Not Used			
11	**Subsystem ID** 0x7019 AP341E-LF		**Subsystem Vendor ID** 16D5	
12	Not Used			
13,14	Reserved			
15	Max_Lat	Min_Gnt	Inter. Pin	Inter. Line

This board is allocated an 8k byte block of memory (BAR0), to access the CDMA, PCIe interrupt, Analog to Digital Controller Control registers, XADC registers, and Flash memory. The PCIe bus decodes 8k bytes for BAR0 for this memory space.

BAR0 MEMORY MAP

The BAR0 memory address space is used to access the CDMA, PCIe interrupt, ADC (Analog to Digital Converter) Control and Data Registers, System Monitor registers, and Flash memory. Note that the base address for the board (BAR0) in memory space must be added to the addresses shown to properly access these registers.

Table 5 BAR0 Registers

BAR0 Base Address	Size	Description
0x0000_0000→0x0000_0FFF	4K	CDMA
0x0000_1000→0x0000_1FFF	4K	PCIe AXI Bridge Control
0x0000_2000→0x0000_2FFF	4K	Interrupt Controller
0x0000_3000→0x0000_3FFF	4K	XADC System Monitor
0x0000_4000→0x0000_4FFF	4K	Firmware Revision
0x0000_5000→0x0000_5FFF	4K	Flash AXI_QSPI
0x0000_6000→0x0000_6FFF	4K	Location in System
0x0000_7000→0x0000_7FFF	4K	ADC Control and Data

BAR0 Base Address	Size	Description
0x0000_8000→0x0000_FFFF	32K	Reserved
0x0001_0000→0x0001_7FFF	32K	Block RAM

CDMA MEMORY MAP

The Central Direct Memory Access (CDMA) controller can access the following devices: Block RAM, AXI to PCI bridge (BAR0), and the ADC Control and Data registers.

Table 6 CDMA Memory Map

BAR0 Base Address	Size	Description
0x0000_0000→0x0000_6FFF	28K	Reserved
0x0000_7000→0x0000_7FFF	4K	ADC Control and Data
0x0000_8000→0x0000_FFFF	32K	Reserved
0x0001_0000→0x0001_7FFF	32K	Block RAM
0x0001_8000→0x00FF_FFFF	15M	Reserved
0x0100_0000→0x0100_1FFF	8K	AXI to PCIe BAR0

INTERRUPT CONTROLLER

The AXI Interrupt Controller concentrates multiple interrupt inputs from peripheral devices to a single interrupt output to the system processor using the PCIe bus. The interrupt controller contains programmer accessible registers that allow interrupts to be enabled, queried and cleared under software control over the PCIe bus interface.

Table 7 Interrupt Controller Registers

BAR0 Base Addr+	Bit(s)	Description
0x0000_2000	31:0	Interrupt Status Register
0x0000_2004	31:0	Interrupt Pending Register
0x0000_2008	31:0	Interrupt Enable Register
0x0000_200C	31:0	Interrupt Acknowledge Register
0x0000_2010	31:0	Set Interrupt Enable Register
0x0000_2014	31:0	Clear Interrupt Enable Register
0x0000_2018	31:0	Interrupt Vector Register
0x0000_201C	31:0	Master Enable Register

Note that any registers/bits not mentioned will remain at the default value: logic low.

Interrupt Status Register

This Interrupt Status register (ISR) at BAR0 base address + offset 0x2000 is used to monitor board interrupts. When read, the contents of this register indicate the presence or absence of an active interrupt for each of the active interrupting sources. Each bit in this register that is set to a '1' indicates an active interrupt signal on the corresponding interrupt input. Bits that are '0'are not active. The bits in the ISR are independent of the interrupt enable bits in the Interrupt Enable register. Interrupts, even if not enabled, can still show up as active in the ISR.

Table 8 Interrupt Status Register (Read/Write) - (BAR0 + 0x2000)

Bit(s)	FUNCTION	
0	When set indicates an AXI CDMA interrupt. See the CDMA section for more information on the source of this interrupt.	
	0	Interrupt Inactive
	1	Interrupt Active
1	When set indicates that the ADC Data FIFO contains a number of samples equal to or greater than the value stored in the FIFO Full Threshold Register.	
	0	Interrupt Inactive
	1	Interrupt Active
31-2	Reserved	
	0	NA
	1	NA

The ISR register is writable by software only until the Hardware Interrupt Enable bit in the Master Enable Register has been set. Given these restrictions, when this register is written to, any data bits that are set to '1' will activate the corresponding interrupt just as if a hardware input became active. Data bits that are zero have no effect. This allows software to generate interrupts for test purposes.

Interrupt Pending Register

This Interrupt Pending register (IPR) at BAR0 base address + offset 0x2004 is used to monitor board interrupts. Reading the contents of this register indicates the presence or absence of an active interrupt signal that is also

enabled. Each bit in this register is the logical AND of the bits in the Interrupt Status register and the Interrupt Enable register.

Table 9 Interrupt Pending Register (Read) - (BAR0 + 0x2004)

Bit(s)	FUNCTION	
0	When set indicates an AXI CDMA interrupt is pending. See the CDMA section for more information on the source of this interrupt.	
	0	No Interrupt Pending
	1	Interrupt Pending
1	When set indicates that the ADC Data FIFO threshold met or exceeded interrupt is pending.	
	0	No Interrupt Pending
	1	Interrupt Pending
31-2	Reserved	
	0	NA
	1	NA

Interrupt Enable Register

This is a read/write register. Writing a '1' to a bit in this register enables the corresponding Interrupt Status bit to cause assertion of the interrupt output. This Interrupt Enable bit set to '0' does not inhibit an interrupt condition from being captured. It will still show up in the Interrupt Status register even when not enabled here. To show up in the Interrupt Pending register it needs to be enabled here. Writing a '0' to a bit disables, or masks, the generation of interrupt output for the corresponding interrupt input signal. Note however, that disabling an interrupt input is not the same as clearing it. Disabling an active interrupt prevents that interrupt from reaching the IRQ output. When it is re-enabled, the interrupt immediately generates a request on the IRQ output. An interrupt must be cleared by writing to the Interrupt Acknowledge Register, as described below. Reading this Interrupt Enable register indicates

which interrupt inputs are enabled; where a '1' indicates the input is enabled and a '0' indicates the input is disabled.

Table 10 Interrupt Enable Register (Read/Write) - (BAR0 + 0x2008)

Bit(s)	FUNCTION	
0	When set indicates an AXI CDMA interrupt is enabled. See the CDMA section for more information on the source of this interrupt.	
	0	Interrupt Disabled (default)
	1	Interrupt Enabled
1	When set indicates that the ADC Data FIFO threshold met or exceeded interrupt is enabled.	
	0	Interrupt Disabled (default)
	1	Interrupt Enabled
31-2	Reserved	
	0	NA
	1	NA

Interrupt Acknowledge Register

The Interrupt Acknowledge register is a write-only location that clears the interrupt request associated with selected interrupt inputs. Note that writing one to a bit in the Interrupt Acknowledge register clears the corresponding bit in Interrupt Status register, and also clears the same bit in the Interrupt Acknowledge register.

An interrupt input that is active and masked by writing a '0' to the corresponding bit in the Interrupt Enable register will remain active until cleared by acknowledging it. Unmasking an active interrupt causes an interrupt request output to be generated (if the Master Interrupt Enable bit-0 in the Master Enable register is set). Writing 0s has no effect as does writing a '1' to a bit that does not correspond to an active input or for which an interrupt input does not exist. The bit locations in the Interrupt Acknowledge register correspond with the bit locations given in the Interrupt Enable Register Table.

Table 11 Interrupt Acknowledge Register (Write) - (BAR0 + 0x200C)

Bit(s)	FUNCTION
0	Clear AXI CDMA interrupt request.
1	Clear ADC Data FIFO threshold met or exceeded interrupt request.
31-2	Reserved

Set Interrupt Enable Register

Set Interrupt Enable register is a location used to set Interrupt Enable register bits in a single atomic operation, rather than using a read / modify / write

sequence. Writing a '1' to a bit location in the Set Interrupt Enable register will set the corresponding bit in the Interrupt Enable register. Writing 0s does nothing, as does writing a '1' to a bit location that corresponds to a non-existing interrupt input. The bit locations in the Set Interrupt Enable Register correspond with the bit locations given in the Interrupt Enable Register Table.

Table 12 Set Interrupt Enable Register (Write) - (BAR0 + 0x2010)

Bit(s)	FUNCTION
0	Set AXI CDMA interrupt request.
1	Set ADC Data FIFO threshold met or exceeded interrupt request.
31-2	Reserved

Clear Interrupt Enable Register

Clear Interrupt Enable register is a location used to clear Interrupt Enable register bits in a single atomic operation, rather than using a read / modify / write sequence. Writing a '1' to a bit location in Clear Interrupt Enable register will clear the corresponding bit in the Interrupt Enable register. Writing 0s does nothing, as does writing a '1' to a bit location that corresponds to a non-existing interrupt input. The bit locations in the Clear Interrupt Enable Register correspond with the bit locations given in the Interrupt Enable Register Table.

Table 13 Clear Interrupt Enable Register (Write) - (BAR0 + 0x2014)

Bit(s)	FUNCTION
0	Clear AXI CDMA interrupt request.
1	Clear ADC Data FIFO threshold met or exceeded interrupt request.
31-2	Reserved

Interrupt Vector Register

The Interrupt Vector register is a read-only register and contains the ordinal value of the highest priority, enabled, and active interrupt input. INT0 (always the LSB) is the highest priority interrupt input. Each successive input (to the left) has a corresponding lower interrupt priority. If no interrupt inputs are active, the Interrupt Vector register contains all 1s. This Interrupt Vector register acts as an index for giving the correct Interrupt Vector Address.

Table 14 Interrupt Vector Register (Read) - (BAR0 + 0x2018)

Bit(s)	FUNCTION
31-0	Ordinal value of the highest priority enabled active interrupt, 0xFFFFFFFF if no interrupt inputs are active

Master Enable Register

This is a 2-bit, read / write register. The two bits are mapped to the two least significant bits of the location. The least significant bit contains the Master Enable bit and the next bit contains the Hardware Interrupt Enable bit.

Writing a '1' to the Master Enable bit enables the IRQ output signal. Writing a '0' to the Master Enable bit disables the IRQ output, effectively masking all interrupt inputs. The Hardware Interrupt Enable bit is a write-once bit. At reset, this bit is reset to '0', allowing the software to write to the Interrupt Status register to generate interrupts for testing purposes, and disabling any hardware interrupt inputs. Writing a '1' to this bit enables the hardware interrupt inputs and disables software generated inputs. Writing a '1' also disables any further changes to this bit until the device has been reset. Writing 1s or 0s to any other bit location does nothing. When read, this register will reflect the state of the Master Enable and Hardware Interrupt Enable bits. All other bits will read as 0s.

Table 15 Master Enable Register (Read/Write) - (BAR0 + 0x201C)

Bit(s)	FUNCTION	
0	Master IRQ Enable	
	0	All Interrupts Disabled
	1	All Interrupts Enabled
1	Hardware Interrupt Enable	
	0	Software Interrupts Enabled
	1	Hardware Interrupts Only Enabled
31-2	Not Used (bits are read as logic "0")	

AXI-CDMA

The AXI Central Direct Memory Access (CDMA) core is a soft Xilinx Intellectual Property core. The CDMA provides direct memory access between system memory over the PCIe bus and the memory resident on the AP341 module.

The basic mode of operation for the CDMA is Simple DMA. In this mode, the CDMA executes one programmed DMA command and then stops. This requires that the CDMA registers need to be set up by system software over the PCIe bus for each DMA operation required.

Scatter Gather is a mechanism that allows for automated DMA transfer scheduling via a pre-programmed instruction list of transfer descriptors (Scatter Gather Transfer Descriptor Definition). This instruction list is programmed by the user software application into a memory-resident data structure that must be accessible by the AXI CDMA Scatter Gather interface. This list of instructions is organized into what is referred to as a transfer descriptor chain. Each descriptor has an address pointer to the next descriptor to be processed. The last descriptor in the chain generally points back to the first descriptor in the chain but it is not required. The AXI CDMA Tail Descriptor Pointer register needs to be programmed with the address of the first word of the last descriptor of the chain. When the AXI CDMA executes the last descriptor and finds that the Tail Descriptor pointer register contents matches the address of the completed descriptor, the Scatter Gather Engine stops descriptor fetching and waits. See the Xilinx AXI Central Direct

Memory Access product guide PG034 for additional details for Scatter Gather operations.

Table 16 AXI CDMA Registers

BAR0 Base Addr+	Bit(s)	Description
0x0000_0000	31:0	CDMA Control Register
0x0000_0004	31:0	CDMA Status Register
0x0000_0008	31:0	Current Descriptor Pointer Register
0x0000_000C	31:0	Reserved
0x0000_0010	31:0	Tail Descriptor Pointer Register
0x0000_0014	31:0	Reserved
0x0000_0018	31:0	Source Address Register
0x0000_001C	31:0	Reserved
0x0000_0020	31:0	Destination Address Register
0x0000_0024	31:0	Reserved
0x0000_0028	31:0	Bytes to Transfer Register

Note that any registers/bits not mentioned will remain at the default value: logic low.

CDMA Control Register

This register provides software application control of the AXI CDMA.

Table 17 CDMA Control Register (Read/Write) - (BAR0 + 0x0000)

Bit(s)	FUNCTION	
0	This bit is reserved for future definition and will always return zero.	
1	Indicates tail pointer mode is enabled to the Scatter Gather Engine. This bit is fixed to 1 and always read as 1 when Scatter Gather is included. If the CDMA is built with Scatter Gather disabled (Simple Mode Only), the default value of the port is 0.	
	0	Tail Pointer Mode is Disabled
	1	Tail Pointer Mode is Enabled
2	Soft reset control for the AXI CDMA core. Setting this bit to a '1' causes the AXI CDMA to be reset. Reset is accomplished gracefully. Committed AXI4 transfers are then completed. Other queued transfers are flushed. After completion of a soft reset, all registers and bits are in the Reset State.	
	0	Reset Not in Progress

Bit(s)	FUNCTION	
	1	Reset in Progress
3	This bit controls the transfer mode of the CDMA. Setting this bit to a '1' causes the AXI CDMA to operate in a Scatter Gather mode. **Note:** This bit must only be changed when the CDMA engine is IDLE (CDMA Status bit-1 = '1'). Changing the state of this bit at any other time has undefined results. **Note:** This bit must be set to a 0 then back to 1 by the software application to force the CDMA Scatter Gather engine to use a new value written to the CDMA Current Descriptor Pointer register. **Note:** This bit must be set prior to setting Bit-13 of this CDMA Control register.	
	0	Simple DMA Mode
	1	Scatter Gather Mode
4	This bit enables the keyhole read (FIXED address AXI transaction). **Note:** This value should not be changed when a transfer is in progress. This value should remain constant until all the descriptors are processed (for SG = 1). CDMA shows unexpected behavior if the value is changed in the middle of a transfer. **Note:** It is the responsibility of the slave device to enforce the functionality.	
	0	Keyhole Read Disabled
	1	Keyhole Read Enabled
11-5	Reserved	
12	Interrupt on Complete Interrupt Enable. When set to '1', it allows an interrupt after completed DMA transfers.	
	0	Interrupt on Complete Disabled
	1	Interrupt on Complete Enabled
13	Interrupt on Delay Timer Interrupt Enable. When set to '1', it allows a delayed interrupt out. This is only used with Scatter Gather assisted transfers.	
	0	Delayed Interrupt Disabled
	1	Delayed Interrupt Enabled
14	Interrupt on Error Interrupt Enable. When set to '1', it allows an error to generate an interrupt out.	
	0	Error Interrupt Disabled
	1	Error Interrupt Enabled
15	Reserved	

Bit(s)	FUNCTION
23-16	Interrupt Threshold value. This field is used to set the Scatter Gather interrupt coalescing threshold. For Interrupt On Complete interrupt events, an internal counter counts down from the Interrupt Threshold setting. When the count reaches zero, an interrupt output is generated by the CDMA engine. **Note:** The minimum setting for the threshold is 0x01. A write of 0x00 to this register has no effect. If the CDMA is built with Scatter Gather disabled (Simple Mode Only), the default value of the port is zeros.
31-24	Interrupt Delay Time Out. This value is used for setting the interrupt delay time out value. The interrupt time out is a mechanism for causing the CDMA engine to generate an interrupt after the delay time period has expired. This is used for cases when the interrupt threshold is not met after a period of time, and the CPU desires an interrupt to be generated. Timer begins counting when the CDMA is IDLE (CDMA Status bit-1 = '1'). This generally occurs when the CDMA has completed all scheduled work defined by the transfer descriptor chain (reached the tail pointer) and has not satisfied the Interrupt Threshold count. **Note:** Setting this value to zero disables the delay timer interrupt.

CDMA Status Register

This register provides status of the AXI CDMA.

Table 18 CDMA Status Register (Read/Write) - (BAR0 + 0x0004)

Bit(s)	FUNCTION	
0	This bit is reserved for future definition and will always return zero.	
1	CDMA Idle. Indicates the state of AXI CDMA operations. When set and in Simple DMA mode, the bit indicates the programmed transfer has completed and the CDMA is waiting for a new transfer to be programmed. Writing to the "Bytes to Transfer" register in Simple DMA mode causes the CDMA to start (not Idle). When set and in Scatter Gather mode, the bit indicates the Scatter Gather Engine has reached the tail pointer for the associated channel and all queued descriptors have been processed. Writing to the tail pointer register automatically restarts CDMA Scatter Gather operations.	
	0	Not Idle
	1	CDMA is Idle
2	Reserved	

Bit(s)	FUNCTION	
3	Scatter Gather Included. This bit indicates if the AXI CDMA has been implemented with Scatter Gather support included (C_SG_ENABLE = 1). This is used by application software (drivers) to determine if Scatter Gather Mode can be utilized.	
	0	Scatter Gather not included
	1	Scatter Gather is included
4	DMA Internal Error. This bit indicates that an internal error has been encountered by the DataMover on the data transport channel. This error can occur if a 0 value Byte to Transfer register is fed to the AXI DataMover or if the DataMover has an internal processing error. A Bytes to Transfer register value of 0 only happens if the register is written with zeros (in Simple DMA mode) or a Bytes to Transfer register value of zero is specified in the Control word of a fetched descriptor (Scatter Gather Mode). This error condition causes the AXI CDMA to gracefully halt. The CDMA Status register bit-1 is set to '1'when the CDMA has completed shut down. A reset (soft or hard) must be issued to clear the error condition.	
	0	No CDMA Internal Errors
	1	CDMA Internal Error detected. CDMA Engine halts.
5	DMA Slave Error. This bit indicates that an AXI slave error response has been received by the AXI DataMover during an AXI transfer (read or write). This error condition causes the AXI CDMA to gracefully halt. The CDMA Status register bit-1 is set to '1' when the CDMA has completed shut down. A reset (soft or hard) must be issued to clear the error condition.	
	0	No CDMA Slave Errors
	1	CDMA Slave Error detected. CDMA Engine halts.
6	DMA Decode Error. This bit indicates that an AXI decode error has been received by the AXI DataMover. This error occurs if the DataMover issues an address that does not have a mapping assignment to a slave device. This error condition causes the AXI CDMA to halt gracefully. The CDMA Status register bit-1 is set to '1' when the CDMA has completed shut down. A reset (soft or hard) must be issued to clear the error condition.	
	0	No CDMA Decode Errors
	1	CDMA Decode Error detected. CDMA Engine halts.
7	Reserved	
8	Scatter Gather Internal Error. This bit indicates that an internal error has been encountered by the Scatter Gather Engine. This error condition causes the AXI CDMA to gracefully halt. The CDMA Status register bit-1 is set to 1 when the CDMA has completed shut down. A reset (soft or hard) must be issued to clear the error condition.	

Bit(s)	FUNCTION	
	0	No Scatter Gather Internal Errors
	1	Scatter Gather Internal Error. CDMA Engine halts.
9	Scatter Gather Slave Error. This bit indicates that an AXI slave error response has been received by the Scatter Gather Engine during an AXI transfer (transfer descriptor read or write). This error condition causes the AXI CDMA to gracefully halt. The CDMA Status register bit-1 is set to 1 when the CDMA has completed shut down. A reset (soft or hard) must be issued to clear the error condition.	
	0	No Scatter Gather Slave Errors
	1	Scatter Gather Slave Error. CDMA Engine halts.
10	Scatter Gather Decode Error. This bit indicates that an AXI decode error has been received by the Scatter Gather Engine during an AXI transfer (transfer descriptor read or write). This error occurs if the Scatter Gather Engine issues an address that does not have a mapping assignment to a slave device. This error condition causes the AXI CDMA to gracefully halt. The CDMA Status register bit-1 is set to 1 when the CDMA has completed shut down. A reset (soft or hard) must be issued to clear the error condition.	
	0	No Scatter Gather Decode Errors
	1	Scatter Gather Decode Error. CDMA Engine halts.
11	Reserved	
12	Interrupt on Complete. When set to 1, this bit indicates an interrupt event has been generated on completion of a DMA transfer (either a Simple or Scatter Gather). If the Interrupt on Complete (bit-12) of the CDMA Control register = '1', an interrupt is generated from the AXI CDMA. A CPU write of 1 clears this bit to 0. **Note:** When operating in Scatter Gather mode, the criteria specified by the interrupt threshold must also be met.	
	0	No IOC Interrupt
	1	IOC Interrupt active
13	Interrupt on Delay. When set to 1, this bit indicates an interrupt event has been generated on a delay timer time out. If the Interrupt on Delay Timer bit-13 of the CDMA Control register = '1', an interrupt is generated from the AXI CDMA. A CPU write of 1 clears this bit to 0.	
	0	No Delay Interrupt
	1	Delay Interrupt Active
14	Interrupt on Error. When set to 1, this bit indicates an interrupt event has been generated due to an error condition. If the Interrupt on Error bit-14 of the CDMA Control register = '1', an interrupt is generated from the AXI CDMA. A CPU write of 1 clears this bit to 0.	
	0	No Error Interrupt

Bit(s)	FUNCTION	
	1	Error Interrupt Active
15	Reserved	
23-16	Interrupt Threshold Status. This field reflects the current interrupt threshold value in the Scatter Gather Engine.	
31-24	Interrupt Delay Time Status. This field reflects the current interrupt delay timer value in the Scatter Gather Engine.	

CDMA Current Descriptor Pointer Register

Table 19 CDMA Current Descriptor Pointer Register (Read/Write) - (BAR0 + 0x00000008)

Bit(s)	FUNCTION
5-0	Writing to these bits has no effect and they are always read as zeros.
31-6	Current Descriptor Pointer. This register field is written by the software application (in Scatter Gather Mode) to set the starting address of the first transfer descriptor to execute for a Scatter Gather operation. The address written corresponds to a 32-bit system address with the least significant 6 bits truncated. This register field must contain a valid descriptor address prior to the software application writing the CDMA Tail Descriptor Pointer register value. Failure to do so results in an undefined operation by the CDMA. On error detection, the Current Descriptor Pointer register is updated to reflect the descriptor associated with the detected error. **Note:** The register should only be written by the Software application when the AXI CDMA is Idle.

CDMA Tail Descriptor Pointer Register

This register provides Tail Descriptor Pointer for the AXI CDMA Scatter Gather Descriptor Management.

Table 20 CDMA Tail Descriptor Pointer Register (Read/Write) - (BAR0 + 0x00000010)

Bit(s)	FUNCTION
5-0	Writing to these bits has no effect and they are always read as zeros.
31-6	Tail Descriptor Pointer. This register field is written by the software application (in Scatter Gather Mode) to set the current pause pointer for descriptor chain execution. The AXI CDMA Scatter Gather Engine pauses descriptor fetching after completing operations on the descriptor whose current descriptor pointer matches the tail descriptor pointer. When the AXI CDMA is in Scatter Gather Mode, a write by the software application to this register causes the AXI CDMA Scatter Gather Engine to start fetching descriptors starting from the Current Descriptor Pointer register value. If the Scatter Gather engine is paused at a tail pointer pause point, the Scatter Gather engine restarts descriptor execution at the next sequential transfer descriptor. If the AXI CDMA is not idle, writing to this register has no effect except to reposition the Scatter Gather pause point. **Note:** The software application must not move the tail pointer to a location that has not been updated with valid transfer descriptors. The software application must process and reallocate all completed descriptors, clear the completed bits and then move the tail pointer. The software application must move the pointer to the last descriptor address it has updated.

CDMA Source Address Register

This register provides the source address for simple DMA transfers by AXI CDMA.

If a location in system memory is the source address, it must be set with the AXI aperture base address 0x01000000 + the least significant 13-bits of the system memory address.

In addition, the physical address of the location in system memory must be set in the Address Translation Register which is described in the PCIe AXI-Bridge Control section.

Table 21 CDMA Source Address Register (Read/Write) - (BAR0 + 0x0018)

Bit(s)	FUNCTION
31-0	Source Address Register. This register is used by Simple DMA operations as the starting read address for DMA data transfers. The address value written can be at any byte offset. **Note:** The software application should only write to this register when the AXI CDMA is Idle.

CDMA Destination Address Register

This register provides the destination address for simple DMA transfers by AXI CDMA.

If a location in system memory is the destination address, it must be set with the AXI aperture base address 0x01000000 + the least significant 13-bits of the system memory address.

In addition, the physical address of the location in system memory must be set in the Address Translation Register which is described in the PCIe AXI-Bridge Control section.

Table 22 CDMA Destination Address Register (Read/Write) - (BAR0 + 0x0020)

Bit(s)	FUNCTION
31-0	Destination Address Register. This register is used by Simple DMA operations as the starting write address for DMA data transfers. **Note:** The software application should only write to this register when the AXI CDMA is Idle.

CDMA Bytes to Transfer Register

This register provides the value for the bytes to transfer for Simple DMA transfers by the AXI CDMA.

Table 23 CDMA Bytes to Transfer Register (Read/Write) - (BAR0 + 0x0028)

Bit(s)	FUNCTION
22-0	Bytes to Transfer. This register field is used for Simple DMA transfers and indicates the desired number of bytes to DMA from the Source Address to the Destination Address. A maximum of 8,388,606 bytes of data can be specified by this field for the associated transfer. **Writing to this register also initiates the Simple DMA transfer**. Note: A value of zero (0) is not allowed and causes a DMA internal error to be set by AXI CDMA. The software application should only write to this register when the AXI CDMA is Idle.
31-23	Writing to these bits has no effect, and they are always read as zeros.

DMA Key Hole Read Programming Example

It is recommended that the DMA key hole function be used to read the contents of the analog to digital converter data FIFO.

1. Verify the CDMA is idle. Read CDMA Status register bit-1 as logic '1'.

2. Set the CDMA Control register bit 4 to logic '1' for a Key Hole Read and program bit-12 to the desired state for interrupt generation on transfer completion.

3. Write the desired transfer source address to the Source Address register at 0x0018. The transfer data at the source address must be valid and ready for transfer. If we were to select the ADC FIFO Channel and Data Tag Register, we would write 0x0000_7018 to the Source Address register at 0x0018.

4. Write the desired transfer destination address to the Destination Address register at 0x0020. If the destination is the system memory, then the following is required.

    a. Given physical address of buffer of 0x0000333012345678

    b. AXIBAR2PCIEBAR_0U <offset 000F0208> = 0x00003330

    c. AXIBAR2PCIEBAR_0L <offset 000F020C> = 0x12345678

    d. The least significant 13 bits of this address 0x12345678 must be removed and added to the AXI BAR0 Aperture Base address. The new AXI address is 0x01000000 + 0x00001678 = 0x01001678. Write 0x01001678 to 0x0020.

5. Write the number of bytes to transfer to the CDMA Bytes to Transfer register 0x0028. Writing this register also starts the transfer.

6. Either poll the CDMA Status register bit-1 for logic '1' or wait for the CDMA to generate an interrupt if enabled.

7. Clear the interrupt if generated by writing a '1' to bit-12 of the CDMA Status register.

8. Ready for another transfer. Go back to step 1.

AXI-BAR0 Aperture Base Address

The AXI BAR0 aperture base address of 0x01000000 is set as the base address on the AXI bus used to reach system host memory for CDMA transfers.

The address 0x01000000 is the AXI BAR0 Aperture Base address. An 8K address space for the AXI BAR0 Aperture Base Address is reserved.

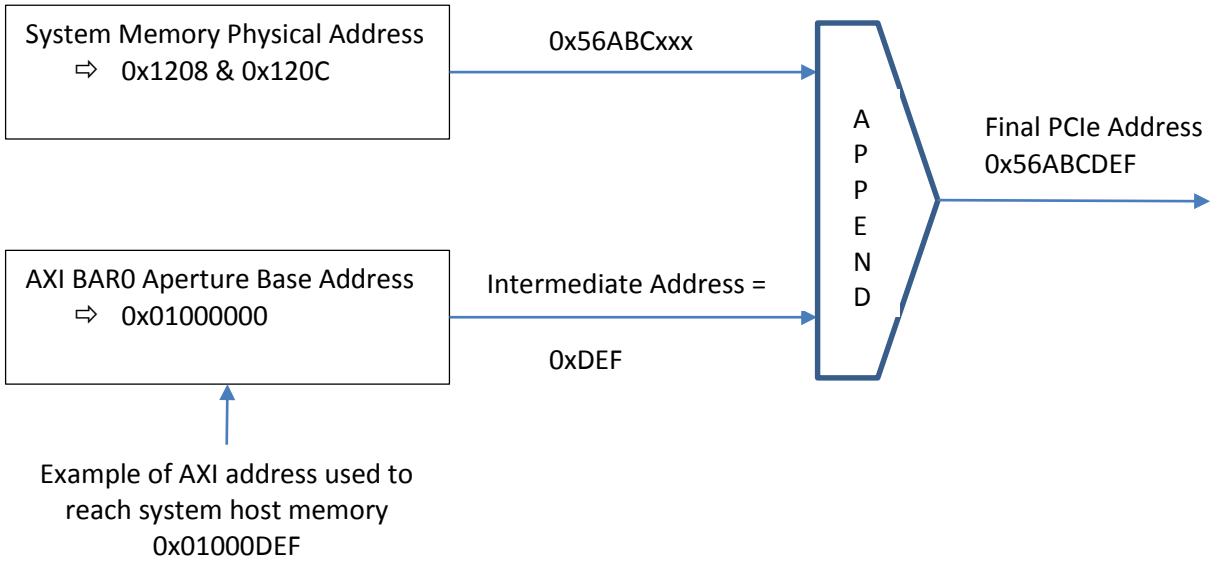
Table 24 AXI BAR0 Aperture Base Address

0x01000000→0x01001FFF	8K	Window into PCIe Interface AXI BAR0 Aperture Base Address

The following is an example of how the AXI BAR0 aperture base address is used.

For example, if the system buffer physical address 0x56ABCDEF were given, then the AXI Base Address Translation Configuration registers at BAR0 + 0x1208 and 0x120C must be set to 0x0 and 0x56ABCDEF respectively.

The least significant 13 bits of this address 0x56ABCDEF must be removed and added to the AXI BAR0 Aperture Base address. The new AXI address is 0x01000000 + 0x00000DEF = 0x01000DEF. These values are then appended by the PCIe AXI bridge to give the final PCIe address of the system memory location.



PCIe AXI-Bridge Control

The PCIe AXI Bridge is an interface between the AXI bus and the PCIe system. This bridge provides the address translation between the AXI4 memory-mapped embedded system and the PCIe system. The AXI Bridge for PCIe translates the AXI memory read or writes to PCIe Transaction Layer Packets (TLP) packets and translates PCIe memory read and write request TLP packets

to AXI interface commands. For more information on the PCIe AXI-Bridge Control registers, refer to the AXI Bridge for PCI Express v2.5 Product Guide.

Table 25 PCIe AXI Bridge Control Registers

BAR0 Base Addr+	Bit(s)	Description
0x0000_1000→ 0x0000_1140	31:0	Not Applicable
0x0000_1144	31:0	PHY Status/Control
0x0000_1148→ 0x0000_1204	31:0	Not Applicable
0x0000_1208	31:0	Address Translation Upper AXIBAR2PCIEBAR_0U
0x0000_120C	31:0	Address Translation Lower AXIBAR2PCIEBAR_0L
0x0000_1210→ 0x0000_1FFF	31:0	Not Applicable

PHY Status/Control Register

This register provides the status of the current PHY state, as well as control of speed and rate switching for Gen2-capable cores.

Table 26 PHY Status/Control Register (Read/Write) - (BAR0 + 0x1144)

Bit(s)	FUNCTION	
0	Reports the current link rate.	
	0	2.5 GT/s
	1	5.0 GT/s
2-1	Reports the current link width.	
	00	x1
	01	x2
	10	x4
	11	x8
8-3	Reports the current Link Training and Status State Machine state. Encoding is specific to the underlying Integrated Block.	
	x	
	x	
10-9	Reports the current lane reversal mode.	
	00	No reversal
	01	Lanes 1:0 reversed
	10	Lanes 3:0 reversed
	11	Lanes 7:0 reversed
11	Reports the current PHY Link-up state.	
	0	Link down

Bit(s)	FUNCTION	
	1	Link up
15-12	Reserved	
31-16	See Xilinx pg055 PHY Status/Control Register	

AXI Base Address Translation Configuration Register

The address space for PCIe is different than the AXI address space. To access one address space from another address space requires an address translation process.

These registers are needed for DMA transfers that move data to the system memory buffer. The location of the system memory buffer is loaded into these registers.

AXI Base Address Translation Configuration register at BAR0 + 0x1208 must be written with the most significant 32 bits of the address in system memory to which the DMA transfer is to read or write. An example of the c code used to set this register with the physical address is shown below.

AXI Base Address Translation Configuration register at BAR0 + 0x120C must be written with the least significant 32 bits of the address in system memory to which the DMA transfer is to read or write. An example of the c code used to set this register with the physical address is shown below.

Example C code:

```
#define AXI2PCIeBAR_0U        (*(DWORD *)(u64BaseAddress + 0x1208))

#define AXI2PCIeBAR_0L        (*(DWORD *)(u64BaseAddress + 0x120C))

iStatus = PCIe7A_DmaGetBuffPhysAddress(iHandle, &u64PhyAddr);

    AXI2PCIeBAR_0U = (DWORD)(u64PhyAddr >> 32);

    AXI2PCIeBAR_0L = (DWORD)(u64PhyAddr & 0xffffffff);
```

This sets the system memory physical address which will be appended with the values written into either the DMA source or destination registers at 0x1018 or 0x1020 respectively. See the example in the CDMA section for additional details.

Flash Memory

The Serial flash memory provides 4M bytes of non-volatile memory for storing the FPGA configuration bitstream. The lower portion of the flash address space is used to store the FPGA configuration bitstream. The upper portion is reserved for the storage of calibration constant and ASCII model identifier string as shown in the tables below. The serial flash is accessible through the AXI Quad SPI interface.

The calibration constants are calculated and stored in flash memory at the factory. All numeric constants are 32 bit values, stored in little endian byte order.

Table 27 Flash Calibration Constant Memory Map (Read/Write)

Addr	D31 D16	D15 D00	Addr
0x3F E003	Channel 0/8 Offset		0x3F E000
0x3F E007	Channel 1/9 Offset		0x3F E004
0x3F E00B	Channel 2/10 Offset		0x3F E008
0x3F E00F	Channel 3/11 Offset		0x3F E00C
0x3F E013	Channel 4/12 Offset		0x3F E010
0x3F E017	Channel 5/13 Offset		0x3F E014
0x3F E01B	Channel 6/14 Offset		0x3F E018
0x3F E01F	Channel 7/15 Offset		0x3F E01C
0x3F E023	Channel 0/8 GainL		0x3F E020
0x3F E027	Channel 1/9 GainL		0x3F E024
0x3F E02B	Channel 2/10 GainL		0x3F E028
0x3F E02F	Channel 3/11 GainL		0x3F E02C
0x3F E033	Channel 4/12 GainL		0x3F E030
0x3F E037	Channel 5/13 GainL		0x3F E034
0x3F E03B	Channel 6/14 GainL		0x3F E038
0x3F E03F	Channel 7/15 GainL		0x3F E03C
0x3F E043	Channel 0/8 GainH		0x3F E040
0x3F E047	Channel 1/9 GainH		0x3F E044
0x3F E04B	Channel 2/10 GainH		0x3F E048
0x3F E04F	Channel 3/11 GainH		0x3F E04C
0x3F E053	Channel 4/12 GainH		0x3F E050
0x3F E057	Channel 5/13 GainH		0x3F E054
0x3F E05B	Channel 6/14 GainH		0x3F E058
0x3F E05F	Channel 7/15 GainH		0x3F E05C

Table 28 Flash ASCII String Identifier Location

Flash Address	Bit(s)	AP341 Model
0x3F EFF0	7:0	A = 0x41
0x3F EFF1	7:0	P = 0x50
0x3F EFF2	7:0	3 = 0x33
0x3F EFF3	7:0	4 = 0x34

Flash Address	Bit(s)	AP341 Model
0x3F EFF4	7:0	1 = 0x31
0x3F EFF5	7:0	0 (null Character)
0x3F EFF6->	7:0	Reserved
0x3F EFFF	7:0	Reserved

AXI XADC Analog to Digital Converter (System Monitor)

The XADC Analog to Digital Converter is used to monitor the die temperature and supply voltages of the FGPA. The XADC channel sequencer is configured to continuously sample the temperature, Vccint and Vccaux channels. The results from the A/D conversions can be read at the addresses given in column one of Table 29.

Data bits 15 to 4 of these registers hold the "ADCcode" representing the temperature, Vccint, or Vccaux value. Data bits 3 to 0 are not used.

The 12-bits output from the ADC can be converted to temperature using the following equation.

$$Temperature(°C) = \frac{ADCcode \times 503.975}{4096} - 273.15$$

The 12-bits output from the ADC can be converted to voltage using the following equation.

$$SupplyVoltage(volts) = \frac{ADCcode}{4096} \times 3V$$

Additional information regarding the XADC can be found in the Xilinx XADC product guide PG099 and the user guide UG480

Table 29 System Monitor Register Map – (BAR0 + 0x32xx)

Address	Status Register
0x0000_3200	Temperature
0x0000_3204	V_{CCINT}
0x0000_3208	V_{CCAUX}
0x0000_3280	Maximum Temperature
0x0000_3284	Maximum V_{CCINT}
0x0000_3288	Maximum V_{CCAUX}
0x0000_3290	Minimum Temperature
0x0000_3294	Minimum V_{CCINT}
0x0000_3298	Minimum V_{CCAUX}

The expected values for V_{CCINT}, $V_{CCINT,}$ and Temperature are shown in Table 30.

Table 30 Expected Operating Parameters

Parameter	Min	Max
V_{CCINT} Volts	0.95	1.05
V_{CCAUX}	1.71	1.89
Temperature (recommended)	-40°C	100°C

Firmware Revision Register

This is a read only register located at BAR0 + 0x4000. The ASCII code representing the current revision of the MCS firmware file is readable from this location. For example, if the firmware is at revision A then this register will read 0x41 in the least significant byte or B= 0x42, C=0x43, etc.

AXI Quad SPI

The serial flash memory is accessed through the AXI Quad SPI interface. For a thorough understanding of the interface refer to the Xilinx product guide pg153 and the commands section of the flash memory data sheet S25FL1-K_00. Following is a description of the AXI Quad SPI registers. The AXI Quad SPI interface has been configured as standard mode (Quad message not supported), master mode enabled, no FIFOs, and the interrupt output is not connected. The clock frequency ratio is set at 2 resulting in a 31.25 MHz SPI clock. With the interrupt output unconnected, the Quad SPI IP Interrupt Status Register is still useful for reporting error conditions.

Table 31 AXI Quad SPI Register Map– (BAR0 + 0x50xx)

Address	Register
0x0000_5040	Quad SPI Software Reset Register
0x0000_5060	Quad SPI Control Register
0x0000_5064	Quad SPI Status Register
0x0000_5068	Quad SPI Data Transmit Register
0x0000_506C	Quad SPI Data Receive Register
0x0000_5070	Quad SPI Slave Select Register
0x0000 5020	Quad SPI IP Interrupt Status Register

Quad SPI Software Reset Register

The Software Reset Register (SRR) permits resetting the core independently of other cores in the system. Writing 0x0000_000a to the SRR resets the core register for four AXI clock cycles. Any other write access generates undefined results and results in an error. The bit assignment in the software reset register is shown in and described in Table 32. Any attempt to read this register returns undefined data.

Table 32 Quad SPI Software Reset Register (BAR0 + 0x5040)

Bit(s)	Software Reset Register
0 - 31	The only allowed operation on this register is a write of 0x0000000a, which resets the AXI Quad SPI core

Quad SPI Control Register

The SPI Control Register (SPICR) allows programmer control over various aspects of the AXI Quad SPI core. The bit assignment in the SPICR is described in Table 33.

Table 33 Quad SPI Control Register (BAR0 + 0x5060)

Bit(s)	Quad SPI Control Register	
0	Local loopback mode:	
	0	Normal Operation
	1	Loopback mode. The transmitter output is internally connected to the receiver input. The receiver and transmitter operate normally, except that received data (from remote slave) is ignored.
1	SPI system enable: Setting this bit to 1 enables the SPI devices as noted here. When set to:	
	0	SPI system disabled. Both master and slave outputs are in 3-state and slave inputs are ignored.
	1	SPI system enabled. Master outputs active (for example, IO0 (MOSI) and SCK in idle state) and slave outputs become active if SS becomes asserted. The master starts transferring when transmit data is available.
2	Master (SPI master mode): Setting this bit configures the SPI device as a master or a slave. When set to:	
	0	Slave configuration
	1	Master configuration
3	Clock Polarity: Setting this bit defines the clock polarity. When set to:	
	0	Active-High clock; SCK idles low.
	1	Active-Low clock; SCK idles high.
4	Clock phase: Setting this bit selects one of two fundamentally different transfer formats.	
	0	Data valid on first SCK edge after SS asserted
	1	Data valid on second SCK edge after SS asserted
5	TX Register reset: When written with '1', this bit forces a reset of the transmit FIFO to the empty condition. This bit will read as '0'.	
	0	Transmit FIFO normal operation
	1	Reset transmit FIFO pointer
6	RX FIFO reset: When written with '1', this bit forces a reset of the receive FIFO to the empty condition. This bit will read as '0'.	

Bit(s)	Quad SPI Control Register	
	0	Receive FIFO normal operation
	1	Reset receive FIFO pointer
7	Manual slave select assertion enable: This bit forces the data in the slave select register to be asserted on the slave select output anytime the device is configured as a master and the device is enabled (SPE asserted). When set to:	
	0	Slave select output asserted by master core logic.
	1	Slave select output follows data in slave select register.
8	Master transaction inhibit: This bit inhibits master transactions. This bit has no effect on slave operation. When set to:	
	0	Master transactions enabled.
	1	1 = Master transactions disabled. Note: This bit immediately inhibits the transaction. Setting this bit while transfer is in progress would result in unpredictable outcome.
9	LSB first: This bit selects LSB first data transfer format. The default transfer format is MSB first. When set to:	
	0	MSB first transfer format.
	1	LSB first transfer format. Note: In Dual/Quad SPI mode, only the MSB first mode of the core is allowed.
10 - 31	Reserved	

Quad SPI Status Register

The Quad SPI Status Register (SPISR) is a read-only register that provides the status of some aspects of the AXI Quad SPI core to the programmer. The bit assignment in the SPISR is described in Table 34. Writing to the SPISR does not modify the register contents.

Table 34 Quad SPI Status Register (BAR0 + 0x5064)

Bit(s)	Quad SPI Status Register	
0	Receive Register Empty: This bit is set High when the receive register is empty.	
	0	Rx register Is not empty
	1	Rx register is empty

Bit(s)	Quad SPI Status Register	
1	Receive Register Full: This bit is set High when the Receive Register is full.	
	0	Rx register not full
	1	Rx register full
2	Transmit Register empty: This bit is set to High when the transmit register is empty. This bit goes High as soon as the TX register becomes empty.	
	0	Tx FIFO not empty
	1	Tx FIFO empty
3	Transmit Register Full: This bit is set High when the transmit register is full.	
	0	Tx register not full
	1	Tx register full
4	Mode-fault error flag: This flag is set if the SS signal goes active while the SPI device is configured as a master. MODF is automatically cleared by reading the SPISR. A Low-to-High MODF transition generates a single-cycle strobe interrupt.	
	0	No error
	1	Error condition detected
5	Slave_Mode_Select flag: This flag is asserted when the core is configured in slave mode. Slave_Mode_Select is activated as soon as the master SPI core asserts the chip select pin for the core.	
	0	Asserted when core configured in slave mode and selected by external SPI master
	1	Default in standard mode
6	CPOL_CPHA_Error flag: When set indicates an invalid combination of CPOL and CPHA has been selected.	
	0	Default.
	1	The CPOL and CPHA are set to 01 or 10.
7	Slave mode error flag.	
	0	Master mode is set in the control register (SPICR).
	1	This bit is set when the core is configured with dual or quad SPI mode and the master is set to 0 in the control register (SPICR).
8	MSB error flag	
	0	Default
	1	LSB first bit set in SPICR (not valid for quad mode)
9	Loopback error flag	
	0	Default. The loopback bit in the control register is at default state.
	1	When the SPI command, address, and data bits are set to be transferred in other than standard SPI protocol mode and this bit is set in control register (SPICR).
10	Command error flag	
	0	Default

Bit(s)	Quad SPI Status Register	
	1	The first entry in SPI DTR FIFO is incompatible with the command list for the attached flash device
11 - 31	Reserved	

Quad SPI Data Transmit Register

The Quad SPI Data Transmit Register (SPI DTR) is written with the data to be transmitted on the SPI bus. After the SPE bit is set to 1 in master mode or spisel is active in the slave mode, the data is transferred from the SPI DTR to the shift register.

If a transfer is in progress, the data in the SPI DTR is loaded into the shift register as soon as the data in the shift register is transferred to the SPI DRR and a new transfer starts. The data is held in the SPI DTR until replaced by a subsequent write. The SPI DTR is described in Table 35.

This register cannot be read and can only be written when it is known that space for the data is available. If an attempt to write is made on a full register, the AXI write transaction completes with an error condition. Reading the SPI DTR is not allowed and the read transaction results in undefined data.

Table 35 Quad SPI Data Transmit Register (BAR0 + 0x5068)

Bit(s)	Quad SPI Data Transfer Register
0 - 7	SPI transmit data
8 - 31	Reserved

Quad SPI Data Receive Register

The Quad SPI Data Receive Register (SPI DRR) is used to read data that is received from the SPI bus. This is a double-buffered register. The received data is placed in this register after each complete transfer.

If the SPI DRR was not read and is full, the most recently transferred data is lost and a receive overrun interrupt occurs.

If an attempt is made to read an empty receive register, it gives out an error in the Status register. Writes to the SPI DRR do not modify the register contents and return with a successful OK response.

The power-on reset values for the SPI DRR are unknown. When known data has been written into the SPI DRR during core transactions, the data in this register can be considered for reading. The SPI DRR is described Table 36.

IMPORTANT: Based on the command that is issued to the SPI device, a certain unwanted number of bytes are written to the Receive register. These bytes have to be discarded.

Table 36 Quad SPI Data Receive Register (BAR0 + 0x506C)

Bit(s)	Quad SPI Data Receive Register
0 - 7	SPI receive data

Bit(s)	Quad SPI Data Receive Register
8 - 31	Reserved

Quad SPI Slave Select Register

The SPI Slave Select Register (SPISSR) contains an active-low, slave select vector SS of length one. The bit assignment in the SPISSR is described in Table 37.

Table 37 Quad SPI Slave Select Register (BAR0 + 0x5070)

Bit(s)	Quad SPI Slave Select Register
0	Set to zero to select flash device
1 - 31	Reserved

Quad SPI IP Interrupt Status Register

The IP Interrupt Status Register (IPISR) collects all of the events. Bit assignments are described in Table 38. The interrupt register is a read/toggle-on-write register. Writing a 1 to a bit position within the register causes the corresponding bit to toggle. All register bits are cleared on reset.

Table 38 IP Interrupt Status Register (BAR0 + 0x5020)

Bit(s)	IP Interrupt Status Register
0	Mode-fault error. This interrupt is generated if the SS signal goes active while the SPI device is configured as a master. This bit is set immediately on SS going active.
1	Slave mode-fault error. This interrupt is generated if the SS signal goes active while the SPI device is configured as a slave, but is not enabled. This bit is set immediately on SS going active and continually set if SS is active and the device is not enabled.
2	Data transmit register empty. It is set when the last byte of data has been transferred out to the external flash memory. In master mode if this bit is set to 1, no more SPI transfers are permitted.
3	Data transmit register underrun. This bit is set at the end of a SPI element transfer by a one-clock period strobe to the interrupt register when data is requested from an empty transmit register by the SPI core logic to perform a SPI transfer. This can occur only when the SPI device is configured as a slave in standard SPI configuration and is enabled by the SPE bit as set. All zeros are loaded in the shift register and transmitted by the slave in an under-run condition.
4	Data receive register full. This bit is set at the end of the SPI element transfer, when the receive register has been filled by a one-clock period strobe to the interrupt register.

Bit(s)	IP Interrupt Status Register
5	Data receive register overrun. This bit is set by a one-clock period strobe to the interrupt register when an attempt to write data to a full receive register is made by the SPI core logic to complete a SPI transfer. This can occur when the SPI device is in either master or slave mode (in standard SPI mode) or if the IP is configured in SPI master mode (dual or quad SPI mode).
6	Reserved
7	Slave select mode. The assertion of this bit is applicable only when the core is configured in slave mode in standard SPI configuration. This bit is set when the other SPI master core selects the core by asserting the slave select line. This bit is set by a one-clock period strobe to the interrupt register. Note: This bit is applicable only in standard SPI slave mode.
8 – 31	Reserved

Serial Flash Write/Read Example

This section describes a suggested sequence for accessing the serial Flash. This example reads the Manufacturer's ID and device ID from the flash.

One time, at startup, write the Quad SPI Software Reset Register and the Quad SPI Control registers.

Write 0x0000000A to address 0x00005040 to reset the interface

Write 0x000000E6 to address 0x00005060 to configure the Quad SPI interface as a master, set the Clock Phase and Polarity, and select manual slave select mode.

At the start of each Flash command
Write 0x00000000 to address 0x00005070 to select the slave device.

Write 0x00000090 to address 0x00005068 to write the Flash command to initiate the read ID register sequence to the transmit data register.

Read from 0x00005064 until bit 1, receive register full is set.

Read from 0x0000506C to empty the receive data register.

Write 0x00000000 to address 0x00005068 to write command byte 2 to the transmit data register.

Read from 0x00005064 until bit 1, receive register full is set.

Read from 0x0000506C to empty the receive data register.

Write 0x00000000 to address 0x00005068 to write command byte 3 to the transmit data register.

Read from 0x00005064 until bit 1, receive register full is set.

Read from 0x0000506C to empty the receive data register.

Write 0x00000000 to address 0x00005068 to write command byte 4 to the transmit data register.

Read from 0x00005064 until bit 1, receive register full is set.

Read from 0x0000506C to empty the receive data register. The value should be 0x00.

Write 0x00000000 to address 0x00005068 to write command byte 5 to the transmit data register.

Read from 0x00005064 until bit 1, receive register full is set.

Read from 0x0000506C to empty the receive data register. The value should be the manufacturer's ID 0x01.

Write 0x00000000 to address 0x00005068 to write command byte 6 to the transmit data register.

Read from 0x00005064 until bit 1, receive register full is set.

Read from 0x0000506C to empty the receive data register. The value should be the device ID 0x15.

At the end of each Flash command
Write 0x00000001 to address 0x00005070 to de-select the slave device.

Location in System Register

The Location Register provides the interface to the carrier's Slot ID CPLD. A read of this register triggers a serial transfer from the carrier's Slot ID CPLD to the Location Register. The unique ID enables system software to distinguish this particular AcroPack module from other similar modules.

Table 39 Slot ID Register (BAR0 +0x6000)

Bit(s)	Location in System Register	
0 - 2	Carrier site	
	"000"	site "A"
	"001"	site "B"
	⋮	⋮
	"111"	site "H"
3 - 7	Carrier identification. These bits are set by the backplane global address (VPX carrier).	
8 – 31	Reserved	

Analog to Digital Converter Control and Data Registers

The Analog to Digital Converter (ADC) Control and Data Registers of the AP341 provide control of the conversion and scanning modes for the 16 differential analog channels.

Table 40 lists the ADC Control and Data registers.

Table 40 ADC Control and Data Register Map - (BAR0 + 0x70xx)

Address	Register Description
0x0000_7000	Control Register
0x0000_7004	Channel Enable Control Register
0x0000_7008	Conversion Timer Register
0x0000_700C	High Bank Timer Register
0x0000_7010	FIFO Full Threshold
0x0000_7014	Start Conversion Register
0x0000_7018	FIFO Channel Data and Tag Register
0x0000_701C	ADC Channel 0/8 Offset
0x0000_7020	ADC Channel 1/9 Offset
0x0000_7024	ADC Channel 2/10 Offset
0x0000_7028	ADC Channel 3/11 Offset
0x0000_702C	ADC Channel 4/12 Offset
0x0000_7030	ADC Channel 5/13 Offset
0x0000_7034	ADC Channel 6/14 Offset
0x0000_7038	ADC Channel 7/15 Offset
0x0000_703C	ADC Channel 0/8 GainL Correction
0x0000_7040	ADC Channel 1/9 GainL Correction
0x0000_7044	ADC Channel 2/10 GainL Correction
0x0000_7048	ADC Channel 3/11 GainL Correction
0x0000_704C	ADC Channel 4/12 GainL Correction
0x0000_7050	ADC Channel 5/13 GainL Correction
0x0000_7054	ADC Channel 6/14 GainL Correction
0x0000_7058	ADC Channel 7/15 GainL Correction
0x0000_705C	ADC Channel 0/8 GainH Correction
0x0000_7060	ADC Channel 1/9 GainH Correction
0x0000_7064	ADC Channel 2/10 GainH Correction
0x0000_7068	ADC Channel 3/11 GainH Correction
0x0000_706C	ADC Channel 4/12 GainH Correction
0x0000_7070	ADC Channel 5/13 GainH Correction
0x0000_7074	ADC Channel 6/14 GainH Correction
0x0000_7078	ADC Channel 7/15 GainH Correction

Control Register

This read/write register is used to: enable single or continuous conversions, select conversion of a reference ground voltage or field analog signals, control external trigger input/output module, monitor FIFO status, and issue a software reset to the module.

The function of each of the control register bits are described in Table 41.

Table 41 Control Register - (BAR0 + 0x7000)

Bit(s)	FUNCTION	
1 to 0	Conversion mode:	
	00	Conversions are disabled.

Bit(s)	FUNCTION	
	01	Enable Single Conversion Mode. A single conversion is initiated per software start convert or external trigger. The internal channel timer controls the start conversion of channels 8-15.
	10	Enable Continuous Conversion Mode. Conversions are initiated by a software start or external trigger and continued by internal hardware triggers generated at the frequency set by the interval timer registers.
	11	Reserved.
3 to 2	Channel Input Mode:	
	00	All Channels Differential Input
	01	Reference Ground Voltage Input
	10	Reserved
	11	Reserved
5 to 4	External Trigger Mode: As an output, internal timer triggers are generated on the External Trigger pin of the field I/O connector. The External Trigger output signal can be used to synchronize the conversion of multiple modules. A single master AP341 must be configured for External Trigger output and Continuous Conversion mode while all other modules are configured for External Trigger input and Single Conversion mode. The external trigger signals (pin 98 of the field I/O) must be wired together for all synchronized modules. Also, the High Bank Timer must be programmed with the same value on all synchronized modules. Note that the External Trigger input can be sensitive to external EMI noise which can cause erroneous external triggers. If External Trigger input or output is not required, the External Trigger should be configured as disabled.	
	00	External Trigger Disable
	01	External Trigger Set as Input
	10	External Trigger Set as Output
	11	Reserved
6	Auto DMA Transfer: With Auto DMA Transfer enabled, a DMA transfer of <threshold> size will be automatically kicked off in hardware. Note that the CDMA control, source and destination registers as well as the FIFO threshold register must be set properly prior to setting this bit.	
	0	Hardware initiated DMA transfers disabled.
	1	DMA transfers are initiated automatically in hardware when the FIFO threshold has been met or exceeded.
7	Not Used	

Bit(s)	FUNCTION	
8 status	FIFO Empty Status:	
	0	FIFO Empty
	1	FIFO Not Empty
9 status	FIFO Threshold Status:	
	0	FIFO has less than the number of samples defined by the Threshold Register.
	1	FIFO Threshold Reached. This bit is set when the FIFO contains the number of data samples set by the Threshold Register.
10 status	FIFO Full Status:	
	0	FIFO Not Full
	1	FIFO Full
14 to 11	Not Used	
15	1 = Software Reset	
31 to 16	Not Used.	

The software reset will clear this Control Register, the Channel Enable Register, counter registers, and FIFO buffer. It will also reset the FIFO Threshold Register to its default value of 1023 decimal, and set the gain and offset registers to one and zero, respectively.

Channel Enable Control Register - (BAR0 + 0x7004)

The Channel Enable Control Register (bits 15 to 0) is used to select the channels desired for conversion. Only those channels enabled are stored into the channel data FIFO. When the channel's corresponding bit is set high, per the table below, the channel's converted data is tagged and stored into the FIFO. For example, to enable channels 15, 11 and 7 through 0 the Channel Enable register must be set as 88FF hex.

This register's contents are cleared upon reset. Any register bits not used will remain at the default value logic low.

Table 42 Channel Enable Control Register – (BAR0 + 0x7004)

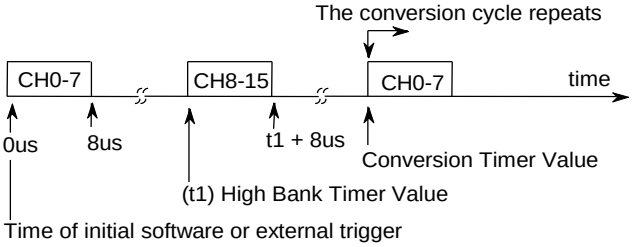
Bit(s)	FUNCTION
15 to 0	Set bit to enable channel. For example, bit 0 corresponds to Channel 0. Bit 13 corresponds to Channel 13.
31 to 16	Not Used

Conversion Timer Register - (BAR0 + 0x7008)

Timed periodic triggering can be used to achieve precise time intervals between conversions. The Conversion Timer register is a 32-bit register value that controls the interval time between conversions of all enabled channels.

The Channel Conversion Timer is used to control the frequency at which the conversion cycle is repeated for all enabled channels. For example, upon

software or external trigger, channels 0 to 7 are simultaneously converted. The time programmed into the High Bank Conversion Time Register then determines when channels 8 to 15 are simultaneously converted. The cycle repeats and the time programmed into Conversion Timer Register determines when channels 0 to 7 will, again, be simultaneously converted. Thus, the Conversion Timer value must always be greater than the High Bank Conversion Timer value by at least 8us. If Continuous Conversions are selected via the Control Register, the conversions will continue until disabled. See Figure 1 for an illustration of the sequence of conversions described in this paragraph.



Where: High Bank Timer Value must be 8µ seconds and Conversion Timer Value must be t1+8µ seconds.

Figure 1: Timeline of channel bank conversions.

The 32-bit Conversion Timer value divides a 15.625MHz clock signal. The output of the Conversion Timer is used to precisely generate periodic trigger pulses to control the frequency at which all enabled channels are converted. The time period between trigger pulses is described by the following equation:

(Conversion Timer Value + 1) ÷ 15,625,000Hz = T (in seconds)

To calculate the conversion timer value, the following equation can be used. Note this gives the values in decimal. It must still be converted to hex before it is written to the Conversion Timer register.

Conversion Timer Value = (T seconds × 15,625,000Hz) – 1

Where:

T = the desired time period between trigger pulses in seconds.

Conversion Timer Value can be a minimum of 124 decimal if only channels 0 to 7 are enabled for conversion. If any channels in the upper bank (channels 8 to 15) are also enabled, then the minimum value is 249 decimal. The maximum value is 4,294,967,295 decimal.

The maximum period of time which can be programmed to occur between simultaneous conversions is (4,294,967,295 + 1) ÷ 15,625,000 = 274.88 seconds. The minimum time interval which can be programmed to occur is (124 + 1) ÷ 15,625,000 = 8µ seconds. This minimum of 8µs is defined by the minimum conversion time of the hardware, given on channels 0 to 7 are enabled for conversions. If any channel from channels 8 to 15 is enabled for conversion, then the minimum time that the Conversion Timer can be

programmed is 249 decimal. This minimum time of 16µ seconds allows 8µ seconds for channels 0 to 7 and 8µ seconds for channels 8 to 15.

The 8µ seconds maximum sample rate corresponds to a maximum sampling frequency of 125KHz. The maximum analog input frequency should be band limited to one half the sample frequency. An anti-aliasing filter should be added to remove unwanted signals above ½ the sample frequency in the input signal for critical applications.

The register's contents are cleared upon reset.

High Bank Timer Register - (BAR0 + 0x700C)

The High Bank Timer register is a 32-bit register that controls when the upper bank of channels 8 to 15 are converted.

The High Bank Timer is used to control the delay after channels 0 to 7 are converted until channels 8 to 15 are simultaneously converted. For example, upon software or external trigger channels 0 to 7 are simultaneously converted. Then, the time programmed into this counter determines when channels 8 to 15 will be simultaneously converted. See Figure 1 for an illustration of this sequence of events.

If a channel within the 8 to 15 bank is enabled in the Channel Enable Control register, then the High Bank Timer register must be programmed with a delay. If this register is left as zero erroneous operation will result.

The 32-bit High Bank Timer value divides a 15.625 MHz clock signal. The output of this timer is used to precisely generate periodic trigger pulses to control the frequency at which the high bank of channels 8 to 15 are simultaneously converted. The time period between trigger pulses is described by the following equation:

Conversion Timer Value = (T seconds × 15,625,000Hz) – 1

Where:

T = the desired time period between trigger pulses in seconds.

High Bank Timer Value can be a minimum of 124 decimal. The maximum value is 4,294,967,295 decimal.

The maximum period of time which can be programmed to occur between conversions is (4,294,967,295 + 1) ÷ 15,625,000 = 274.88 seconds. The minimum time interval which can be programmed to occur is (124 + 1) ÷ 15,625,000 = 8.0µ seconds. This minimum of 8.0µ seconds is defined by the minimum conversion time of the hardware. This gives channels 0 to 7 8µ seconds to complete their simultaneous conversion. Then channels 8 to 15 can be simultaneously converted.

The register's contents are cleared upon reset.

FIFO Full Threshold Register - (BAR0 + 0x7010)

The FIFO Full Threshold register is a 10-bit register that is used to control when an interrupt will be generated and/or DMA transfer will occur. The events, enabled in the ADC Control Register will occur when the FIFO contains the number of samples equal to the FIFO Full Interrupt Threshold value. This register allows selection of any FIFO depth level from 13 up to 1023 samples in the 1025 sample FIFO.

An interrupt request will remain asserted to the system as long as the FIFO threshold is met or exceeded and interrupts are enabled. The interrupt request can be removed by 1) disabling interrupts on the AP module or 2) reading the FIFO until it has fewer samples in it than defined by the threshold register. Note that interrupts must first be enabled in the interrupt enable register of the interrupt register. Please see Interrupt Controller section for more details on interrupts. The default FIFO Full Interrupt Threshold is 1023 samples. A reset will set it to this default value.

Start Conversion Register - (BAR0 + 0x7014)

The Start Convert register is write-only and is used to trigger conversions by setting data bit-0 to a logic one. This method of starting conversions is most useful for its simplicity and for when precise time of conversion is not critical. Typically, software triggering is used for initiating the first conversion. The desired mode of data acquisition must first be configured by setting the following registers to the desired values and modes: Interrupt, Control, Channel Enable, Conversion Timers and CDMA, if necessary.

Data bit-0 must be a logic one to initiate data conversions.

FIFO Channel Data and Tag Register

All channels share a 1025 sample deep FIFO buffer. The FIFO samples are 16-bit data values with a 4-bit channel tag.

The FIFO will be cleared by implementing a software or hardware reset. Any bits not used will remain at the default of logic low.

Table 43 FIFO Channel Data and Tag Register – (BAR0 + 0x7018)

Bit(s)	FUNCTION
15 to 0	FIFO Channel Data
19 to 16	FIFO Channel Tag
31 to 20	Not Used

Gain and offset correction will be applied to each sample prior to writing the result into the FIFO. The addition and multiplication operations are done in FPGA hardware using the FPGA's DSP blocks. The gain and offset registers are set to one and zero respectively upon reset to pass uncorrected ADC values to the FIFOS. Typical start-up operation would include reading factory calibration constants from the flash memory and writing the appropriate correction values for the gain and offset registers for each ADC.

Since all channels share the same FIFO, channel data tagging is implemented. The tag value identifies the channel to which the data corresponds.

Care should be taken when reading data from the FIFO buffer to ensure the FIFO is not empty when a new read is initiated. The FIFO Empty status bit can be read, in the control register, prior to reading the FIFO to avoid reading erroneous data.

If the FIFO exceeds 1025 samples, no more data will be written to the FIFO until data is read and space is freed. It is recommended that interrupts or Auto DMA Transfer be enabled upon meeting the FIFOs set threshold condition.

Analog Input and Corresponding Digital Output Codes

The output data coding is in binary two's compliment. The digital output code corresponding to each of the given ideal analog input values is given in binary two's complement format in Table 44. Note that although the ADC is 14-bit, offset and gain correction leads to a 16-bit digital output from which the most significant 14-bits is the digital output code.

Table 44 Digital Output Codes and Input Voltages

DESCRIPTION	ANALOG INPUT	
Least Significant Bit Weight	0.015259µV	
+ Full Scale Minus One LSB	9.999985 Volts	7FFF hex
Midscale	0V	0000h
One LSB Below Midscale	-0.015259µV	FFFF hex
Minus Full Scale	-10V	8000 hex

ADC Offset Register

The offset register contains a 16-bit two's complement value that is added to the output value from the ADC to correct offset errors. There is a separate offset register for each ADC. Note that channels 0 and 8 share an ADC, similarly 1 and 9 share an ADC, and so on.

Offset correction values must be loaded from the flash to correct new ADC data. The offset registers are set to zero upon reset of the board so that uncorrected ADC values may be stored in the FIFO.

ADC Gain Register (GainL and GainH)

The gain register is a 17-bit fixed point positive fractional number ranging from 0 to 1.999984 weighted as shown in the table below. The 17-bit fixed point number is least significant bit justified in a 32-bit register. This number is multiplied by the offset corrected ADC value to correct for gain errors. There is a separate gain register for each ADC. Note that channels 0 and 8 share an ADC, similarly 1 and 9 share an ADC, and so on. GainL constants are used for negative voltage measurements and GainH constants are used for positive voltage measurements.

Gain correction values must be loaded from the flash to correct new ADC data. The gain registers are set to one upon reset of the board so that uncorrected ADC values may be stored in the FIFO.

Table 45 Gain Constant Number Format

BIT	Binary Fixed Point
31 – 17	(unused, read as 0)
16	1
15	½
14	¼
13	1/8
12	1/16
11	1/32
10	1/64
9	1/128
8	1/256
7	1/512
6	1/1024
5	1/2048
4	1/4096
3	1/8192
2	1/16536
1	1/32768
0	1/65536

Use of Calibration Constants

Factory calibration constants used to correct gain and offset errors are stored in on-board flash memory. Gain and offset correction constants are stored for each ADC. Software calibration uses some fairly complex equations. Acromag provides you with the AcroPack Software Library to make communication with the board and calibration easy. It relieves you from having to turn the equations of the following sections into debugged software calibration code. The functions are written in the "C" programming language and can be linked into your application. Refer to the "README.TXT" file in the root directory and the "INFO341.TXT" file in the "AP341" subdirectory for details.

Uncalibrated Performance

The uncalibrated performance is affected by two primary error sources. These are the Instrumentation Amplifier (IN-AMP) and the Analog to Digital

Converter (ADC). The untrimmed IN-AMP and ADC have significant offset and gain errors (see specifications) which reveal the need for software calibration.

Calibrated Performance

Very accurate calibration of the AP341 can be accomplished by applying external precision calibration voltages. The calibration voltages are used to determine two points of a straight line which defines the analog input characteristic.

The AP341 has eight separate ADC circuits. As such, each of the first eight channels will have their own unique offset and gain errors. Note, channels 8 through 15 share the gain and offset values of channels 0 through 7. The calibration voltages will need to be converted through each of the eight channels to calculate the gain and offset calibration constants as shown in the equations below.

OffsetCorrection = -CountCALZ (Equation 1)

$$IdealSlope = \frac{2^{16}}{FullScaleRange} = \frac{2^{16}}{20}$$

$$ActualSlope_L = \frac{CountCALZ - CountCALLO}{VoltsCALZ - VoltsCALLO}$$

$$ActualSlope_H = \frac{CountCALHI - CountCALZ}{VoltsCALH}$$

$$CorrectionFactor = \frac{IdealSlope}{ActualSlope}$$

*GainCorrection = CorrectionFactor * 2^{16} (Equation 2)*

Note that *GainCorrection* must be calculated for both $ActualSlope_L$ and $ActualSlope_H$, resulting in GainL and GainH correction constants.

Where:

CountCALHI = uncorrected ADC data (16-bit) with high external precision calibration voltage applied (+9.88000V recommended)

CountCALLO = uncorrected ADC data (16-bit) with low external precision calibration voltage applied (-9.88000V recommended)

CountCALZ = uncorrected ADC data (16-bit) with 0V reference voltage applied

VoltsCALHI = actual external precision calibration voltage high

VoltCALLO = actual external precision calibration voltage low

The values calculated for *OffsetCorrection* and *GainCorrection* (GainL and GainH) are stored in flash memory for each ADC channel. The values are then used in the following equation to correct each input sample for offset and gain errors.

$$CorrectedData = \frac{(CountIN + OffsetCorrection) * GainCorrection}{2^{16}} \quad (Equation\ 3)$$

Note: The average of many ADC values (e.g. 2048) should be used when calculating new correction coefficients to reduce the measurement uncertainty.

Calibration Programming Example

Calibration constants are calculated and stored in flash memory in the factory, however, in the case that new constants must be calculated, the calibration parameters *CountCALHI*, *CountCALLO* and *CountCalZ* need to be determined for each of the eight ADCs. These parameters are then used to calculate *OffsetCorrection* and *GainCorrection* (GainL and GainH) constants. Note that channels 0 and 8 share the same INAMP and ADC and thus share the same calibration constants. This is also true for channels 1 and 9, 2 and 10, etc.

Determination of *CountCALLO* Value

1. Execute write of 0002H to the Interrupt Enable Register at Base Address + 2008H. This will enable FIFO Threshold met or exceeded interrupts on the module.
2. Execute write of 0002H to the Control Register at Base Address + 7000H.
    a) Continuous Mode Enabled
    b) Differential Input Selected
    c) External Trigger Disabled
3. Execute write of 00FFH to the Channel Enable Control Register at Base Address + 7004CH. This will permit the values corresponding to channels 0 to 7 to be stored in the data FIFO.
4. Execute write of 176H to the Conversion Timer register at Base Address + 7008H. This sets the interval time between conversions to 24µ seconds.
5. Execute write of 3C0H to the FIFO Full Threshold register at Base Address + 7010H. Since interrupts are enabled in the control register, an interrupt request will be issued when 960 values of the calibration voltage have been stored in the FIFO. This corresponds to 120 values for each of the eight channels enabled.
6. Apply a low (negative) precision calibration voltage, -9.88000V is recommended, to channels 0-7. Execute write of 0001H to the Start Convert Bit at Base Address + 7014H. This starts the continuous mode of conversions.
7. Upon system interrupt execute write of 00H to the Control register at Base Address + 7000H. This disables conversion. Software must calculate a *CountCALLO* value for each channel 0 to 7, by averaging the 120 values for each channel. Note that more samples will reduce measurement uncertainty.

Determination of *CountCALHI* Value

8. Execute write of 0002H to the Control Register at Base Address + 08H.
    a) Continuous Mode Enabled
    b) Differential Input Selected
    c) External Trigger Disabled
9. Writing the Channel Enable register, Conversion Timer Value, and the FIFO Full Threshold is not necessary because they need not change from that programmed in the previous steps.
10. Apply a high (positive) precision calibration voltage, +9.88000V is recommended, to channels 0-7. Execute write of 0001H to the Start Convert Bit at Base Address + 7014H. This starts the continuous mode of conversions.
11. Upon system interrupt execute write of 00H to the Control register at Base Address + 7000H. This disables conversions. Software must calculate a *CountCALHI* value for each channel 0 to 7, by averaging the 120 values for each channel. Note that more samples will reduce measurement uncertainty.

Determination of *CountCALZ* Value

12. Execute write of 0006H to the Control Register at Base Address + 08H.
    d) Continuous Mode Enabled
    e) Reference Ground Voltage Input Selected
    f) External Trigger Disabled
13. Writing the Channel Enable register, Conversion Timer Value, and the FIFO Full Threshold is not necessary because they need not change from that programmed in the previous steps.
14. Execute write of 0001H to the Start Convert Bit at Base Address + 7014H. This starts the continuous mode of conversions.
15. Upon system interrupt execute write of 00H to the Control register at Base Address + 7000H. This disables conversions. Software must calculate a *CountCALHI* value for each channel 0 to 7, by averaging the 120 values for each channel. Note that more samples will reduce measurement uncertainty.

Calculate the Calibration Constants to Store in Flash

16. Use the *CountCALLO, CountCALHI* and *CountCALZ* values in Equation 1 and Equation 2 in the beginning of this section to obtain new *OffsetCorrection* and *GainCorrection* (GainL and GainH) constants for each ADC. These values can then be stored in the flash memory and loaded into the gain and offset registers.

17. Since *OffsetCorrection* and *GainCorrection* constants are known, corrected input data values can now be calculated. Data is corrected in firmware and stored into the FIFO.

Modes of Conversion

The AP341 provides two methods of analog input operation for maximum flexibility with different applications. The following sections describe the features of each method and how to best use them.

Single Conversion Mode

In Single Conversion mode of operation, conversions are initiated by a software or external trigger. Upon the trigger, channels 0 to 7 will be simultaneously converted. Then, after the time programmed into the High Bank Timer has been reached, channels 8 to 15 will be simultaneously converted. All channels enabled in the Channel Enable Control register will be tagged with their channel number and stored to FIFO memory. No additional conversions will be initiated unless a new software or external trigger is generated.

To select this mode of operation bits 1 and 0 of the Channel Control register must be set to digital code "01". Then, issuing a software start convert or external trigger will initiate conversions. The Conversion Timer is not used in this mode of operation. Also, the High Bank Timer is not needed if channels 8 to 15 are disabled.

This mode of operation can be used to initiate conversions based upon external triggers. This can be used to synchronize multiple AP modules to a single module running in a continuous conversion mode. The external trigger of an AP341 "master" must be programmed as an output. The external trigger signal of that module must then be connected to the external trigger signal of all other modules that are to be synchronized. These other modules must be programmed for Single Conversion mode and external trigger input. Also, the High Bank Timer must be programmed with the same value on all synchronized modules. Data conversion can then be initiated via the Start Convert bit of the master IP module configured for continuous conversion mode.

Continuous Conversion Mode

In the Continuous Conversion mode of operation, the hardware controls the continuous conversions of all enabled channels. All channels 0 to 15 are converted at the rate specified by the Conversion Timer. Channels 8 to 15 are converted after channels 0 to 7. The time programmed into the High Bank Timer specifies how long after channels 0 to 7 are converted before channels 8 to 15 are converted.

To initiate this mode of operation bits 1 and 0 of the Channel Control register must be set to digital code "10". Then, issuing a software start convert or

external trigger will initiate the continuous conversions of all enabled channels.

The interrupt capability of the AP module can be employed as a means to indicate to the system that the 1025 sample FIFO is almost full (depending on the threshold selected) and must be read to allow for the writing of new data.

Alternatively, a polling method could be used. The FIFO Empty, Full, and Threshold Reached bits in the Control/Status register can be polled. When the flags indicate that new FIFO data is available the FIFO should be read to avoid writing data to a full FIFO.

Automatic DMA Transfer

In the case where data must be quickly read from the FIFO, Auto DMA Transfer is recommended. Initiate this mode of operation by setting bit 6 of the ADC Control Register to '1'.

Auto-DMA Mode will automatically start a DMA transfer in the amount of the threshold value, once the threshold value is met. The CDMA Control Register, Source and Destination Registers must be properly written before the start of conversions. Keyhole Reading must be enabled in the CDMA control register. It is recommended that DMA completion interrupts be used to signal when new data is available at the specified destination.

When choosing a FIFO threshold value, the conversions time, number of channels enabled and the time for a DMA transfer to complete in the system must be considered.

Programming Considerations

The AP341 provides different methods of analog input acquisition to give the user maximum flexibility for each application. Examples are presented in the following sections to illustrate programming the different modes of operation.

Single Conversion Mode Example

This example will enable channels 0, 3, and 8 through 15 for the single conversion mode of operation. Conversions can be initiated via software or external trigger. Channels 8 to 15 will be simultaneously converted 16µ seconds after channels 0 and 3.

1. Execute write of 0011H to the Control Register at Base Address + 7000H.
    a) Single Conversion is enabled.
    b) Differential inputs selected.
    c) External and Software generated triggers are enabled.
2. Execute write of FF09H to the Channel Enable Control register at Base Address + 7004H. This will enable channels 0, 3, and 8 through 15 for conversion.

3. Execute write of 007CH to the High Bank Timer at Base Address + 700CH.
4. Execute write of 0001H to the Start Convert Bit at Base Address + 7014H. This starts the simultaneous conversion of channels 3 and 0. Then, 8µ seconds later, channels 8 to 15 are simultaneously converted.

Continuous Conversion Mode with Interrupt Example

This example will enable channels 0 through 13 for the continuous conversion mode of operation. Interrupts are enabled and an interrupt threshold of 430 samples is programmed. The Conversion Timer will be set for an 80µ second interval. The High Bank Timer is set to activate the simultaneous conversion of channels 8 through 13 at 24µ seconds after channels 0 to 7. Conversions can be initiated via software or external trigger.

1. Execute write of 0002H to the Interrupt Enable Register at Base Address + 2008H. This will enable FIFO Threshold met or exceeded interrupts on the module.
2. Execute write of 0012H to the Control Register at Base Address + 7000H.
    a) Continuous Conversion mode is selected.
    b) Differential inputs selected.
    c) External and Software generated triggers are enabled.
3. Execute write of 3FFFH to the Channel Enable Control register at Base Address + 7004H. This will enable channels 0 through 13 for conversion.
4. Execute write of 0000004E1H to the Conversion Timer Register at Base Address + 7008H.
    a) This sets the Conversion Timer to 1249 decimal as needed for an 80µ second interval. Note: (1249+1) ÷ 15,625,000 = 80µ seconds.
5. Execute write of 00000176H to the High Bank Timer Register at Base Address + 700CH.
    a) This sets the High Bank Timer to 374 decimal as needed for a 24µ second delay after channels 0 through 7. Note: (374+1) ÷ 15,625,000 = 24µ seconds.
6. Execute write of 1AEH to the FIFO Full Threshold register at Base Address + 7010H.
    a) The AP341 will issue an interrupt to the system when 430 or more samples are present in the FIFO.
7. Execute write of 0001H to the Start Convert Bit at Base Address + 7014H.
    a) This starts the simultaneous conversion of channels 0 to 7. Then, after 24µ seconds, channels 8 through 13 are simultaneously converted. The cycle repeats every 80µ seconds.

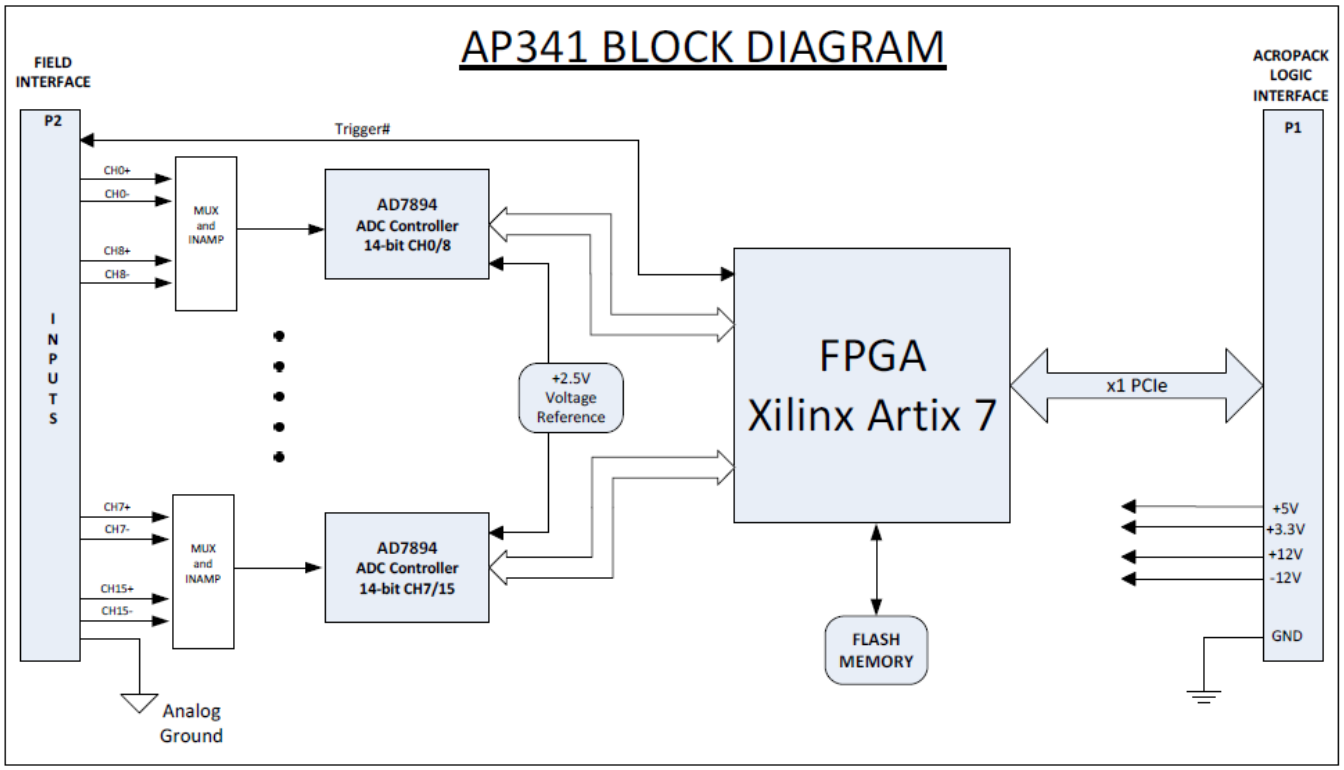
Automatic DMA Mode Example

This example will show how to use the Auto-DMA mode to transfer data quickly from the FIFO to a destination location.

1. Execute write of 0001H to the Interrupt Enable Register at Base Address + 2008H. This will enable AXI CDMA interrupts.
2. Execute write of 5010H to the CDMA Control Register at Base Address + 0000H.
    a) Simple DMA mode.
    b) Keyhole Read enabled.
    c) Interrupt on complete enabled.
3. Execute write of 7018H to the CDMA Source Register at Base Address + 0018h
4. Write CDMA Destination Register. Refer to the AXI-BAR0 Aperture Base Address section for more information on how to obtain a destination address in host memory.
5. Execute write of 0042H to the Control Register at Base Address + 7000H.
    a) Continuous Conversion mode is selected.
    b) Differential inputs selected.
    c) Auto-DMA mode enabled.
6. Execute write of FFFFH to the Channel Enable Register at Base Address + 7004H to enable all channels.
7. Execute write of F9H to the Conversion Timer Register at Base Address + 700CH for a conversion time of 16µs.
8. Execute write of 7CH to the High Bank Timer Register at Base Address + 7008H for conversion of the High Bank 8µ after the start of the Low Bank conversion.
9. Execute write of 200H (512 decimal) to the Threshold Register at Base Address + 7010H.
10. Execute write of 0001H to the Start Convert Bit at Base Address + 7014H. This will start continuous conversion of all 16 channels. When the FIFO threshold is met, a DMA transfer of 512 samples will take place and the completion of the transfer will be signaled in the form of a DMA completion interrupt. Conversions will not stop, the FIFO will continuously be filled and samples will be transferred until conversions are disabled via the ADC Control Register.

4. THEORY OF OPERATION

This section provides a description of the basic functionality of the circuitry used on the board. Refer to the block diagram below as you review this material.



PCIe Interface Logic

The PCIe bus interface logic implemented in the AP341 design provides a one lane PCIe Gen 1 interface to the carrier/CPU. This interface provides access to the AP341 board functions.

The PCIe bus endpoint interface logic is contained within the FPGA. This logic includes support for PCIe commands, including: configuration read/write, and memory read/write. In addition, the PCIe interface supports requester and/or completion accesses. Maximum payload size of up to 1024 bytes is supported.

The logic also implements interrupt requests via message signaled interrupts. Messages are used to assert and de-assert virtual interrupt lines on the link to emulate the Legacy PCI interrupt INTA# signal.

Field Analog Inputs

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2 in the Field IO Connector section). Field I/O signals are NON-ISOLATED. This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Appendix B for connection recommendations). Ignoring

ground loops may cause operation errors, and with extreme abuse, possible circuit damage.

Analog inputs are selected via analog multiplexers. Acropack module control logic drives the select signals of the multiplexer as required per the programming of the control register.

Up to 16 differential inputs can be monitored. The multiplexer stage directs one of two groups of eight channels for simultaneous conversion. Channels 0 to 7 are simultaneously selected and converted as a group by eight individual ADC's, and channels 8 to 15 are also simultaneously converted as a group.

The output of the multiplexer stage feeds an instrumentation amplifier (INAMP) stage. The INAMP has a fixed gain of one. The INAMPs high input impedance allows measurement of analog input signals without loading the source. The INAMP takes in the channel's + and - inputs and outputs a single ended voltage proportional to it.

The output of the INAMP feeds an Analog to Digital Converter (ADC). The ADC is a state of the art, 14-bit successive approximation converter with a built-in sample and hold circuit. The sample and hold circuit goes into the hold mode when a conversion is initiated. This maintains the selected channel's voltage constant until the ADC has accurately digitized the input. Then, it returns to sample mode to re-acquire the analog signal. Once a conversion has been completed, control logic on the module automatically and simultaneously serially reads the digitized values corresponding to the eight channels. While the digitized values are read the input is in the acquire mode. Digital noise generated by reading the newly digitized values will not be present when the ADC transitions into the hold mode since the analog signal is allowed to settle for an interval after the digitized values are read. This pipelined mode of operation facilitates a maximum system throughput with minimum system noise.

The board contains a very stable and accurate 2.5 volt reference used by the ADC.

32Mbit Serial Flash

The serial FLASH memory provides 32 megabits of non-volatile storage that is used for FPGA configuration, ADC calibration coefficient and identifier string storage.

An AXI Quad SPI v3.2 block provides the interface between the internal AXI bus and the FLASH device.

System Monitor (XADC)

The System Monitor provides status information for the 7 series device. The system monitor is located in the center of the FPGA die. The System Monitor function is built around dual 12-bit, 1-megasamples per second Analog-to-Digital Converter. The system monitor is used to measure FPGA physical

operating parameters such as on-chip power supply voltages and die temperature.

5. SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation for Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the carrier and/or AP module with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag website at www.acromag.com. Our website contains the most up-to-date product and software information.

Go to the "Support" tab or your specific AcroPack model ordering page.

Acromag's application engineers can also be contacted directly for technical assistance via email, telephone, or FAX through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab. When needed, complete repair services are also available.

Phone: 248-295-0310
Email: solutions@acromag.com

6. SPECIFICATIONS

PHYSICAL

Length ..... 70.0 mm (2.756 in)
Width ..... 30.0 mm (1.181 in)
Weight..... 10 g

POWER

Summarized below are the expected current draws for each of the specified power supply voltages.

Power Supply Voltage	Current Draw
3.3 VDC +/- 5%	500 mA typical, 580 mA maximum
1.5 VDC +/- 5%	Not Used
5.0 VDC +/- 5%	35 mA typical, 70 mA maximum
+12 VDC +/- 5%	14 mA typical, 40 mA maximum
-12 VDC +/- 5%	7 mA typical, 20 mA maximum

ENVIRONMENTAL

Operating Temperature ..... -40°C to +80°C
Applications requiring operating temperatures above *70*°C will require purchase of *AcroPack Heatsink Accessory* ***AP-CC-01.*** An air cooled application will require a minimum airflow of 400 LFM.
Relative Humidity..... 5-95% non-condensing
Storage Temperature..... -55 to +125°C
Non-Isolated..... The PCIe bus and the AcroPack module commons have a direct electrical connection. As such unless the AcroPack module provides isolation between the logic and user I/O signals, the user I/O signals are not isolated from the PCIe bus.
EMC Directives ..... AcroPack complies with EMC Directive 2014/30/EU.
Immunity per EN 61000-6-2 ..... This is a Class A product
Electrostatic Discharge Immunity (ESD)
per IEC 61000-4-2.
Radiated Field Immunity (RFI)..... per IEC 61000-4-3.
Electrical Fast Transient Immunity (EFT)
per IEC 61000-4-4
Surge Immunity..... per IEC 61000-4-5.
Conducted RF Immunity (CRFI)..... per IEC 61000-4-6.

Emissions per EN 61000-6-4: ..... This is a Class A product

Enclosure Port ..... per CISPR 16
Low Voltage AC Mains Port..... per CISPR 16.

Vibration and Shock ..... This AcroPack is designed to comply with the following Vibration and Shock standards:
Vibration, Sinusoidal Operating: . Designed to comply with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis
Vibration, Random Operating: .... Designed to comply with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis.
Shock, Operating: ..... Designed to comply with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3mS half sine, 18 shocks at 6 orientations for both test levels.

Reliability Prediction

AP341E-LF

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled,* $G_B G_C$

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	1,756,380	200.5	569.4
40°C	935,673	106.8	1068.8

[1] FIT is Failures in 10^9 hours.

ANALOG INPUTS

Input Channels ..... Two banks of eight channels (channels 0-7 and 8-15). The channels of each bank are simultaneously converted.
FIFO Buffer ..... 1025 samples
Interrupt..... Interrupt on programmed FIFO Threshold Met Condition, CDMA interrupt on completion or error
Input Overvoltage Protection ..... ±25V power ON, ±40V Power OFF
Data Format ..... Binary two's complement, 16-bit
Source Impedance Requirements.

Maximum Source Impedance	Maximum Operating Frequency	Channels in Operation
2.2KΩ	125KHz	0 to 7 & 8 to 15
6KΩ	50KHz	0 to 7 & 8 to 15
25KΩ	12.5KHz	0 to 7 & 8 to 15
50KΩ	6.25KHz	0 to 7 & 8 to 15
100KΩ	3.12KHz	0 to 7 & 8 to 15
1MΩ	125KHz	0 to 7 only

ADC Specifications

Conversion Rate	125KHz
Input Voltage Range	±10 Volts
Data Format	Binary 2's Complement
Device	Analog Devices AD7894
Resolution	14-bits
No Missing Codes	14-bits
Differential Nonlinearity	-1 to +1.5LSB maximum
Gain Error	±6 LSB maximum (software calibration eliminates error)
Bipolar Zero Error	±8 LSB maximum (software calibration eliminates this error)

Instrumentation Amplifier Specifications

Device	INA128
Nonlinearity	±0.001% of FSR maximum
Offset Voltage	±550µV maximum
Gain Error	±0.024% maximum (software calibration eliminates this error)
Settling Time	7µ seconds typical to 0.01%

Maximum Overall Calibrated Error

Maximum Total Error[1] ..... +/-2.8 LSB

The maximum corrected (i.e. calibrated) error is the worst case accuracy possible. It is the sum of error components due to ADC quantization of the low and high calibration signals, instrumentation amplifier and ADC linearity error at 25°C. For critical applications multiple input samples should be averaged to improve performance.

Note:

1. Software calibration must be performed in order to achieve the specified accuracy. Follow the input connection recommendations of Appendix B to keep non-ideal grounds from degrading overall system accuracy.

Input Noise[2] ..... 1 LSB RMS, typical

Note:

2. Reference Test Conditions: Temperature 25°C, 125K conversions/second, using carrier APCe7020E-LF with a 2 meter length cable connection to the field analog input signal.

External Trigger Input/Output

As an Input: Negative edge triggered. Must be an active low 3.3-volt logic CMOS compatible, debounced signal referenced to digital common. Conversions are triggered within 250n seconds of the falling edge. Minimum pulse width is 125n seconds.

As an Output: Active low 3.3-volt logic CMOS compatible output is generated. The trigger pulse is low for typically 250n seconds.

PCIe BUS COMPLIANCE

Compatibility.....	This device meets or exceeds all written PCI Express specifications per revision 2.1 dated March 4, 2009.
Line Speed.....	Gen1 (2.5Gbps) Available through system connector
Lane Operation	1-Lane
8K Memory Space Required.....	One Base Address Register (BAR)

PCIe Bus Data Rates

PCIe Gen 1 (1 lane)	Giga bit / second	Bytes / second
Signaling Rate	2.5 Gb/s	312 Mbyte/s
Ideal Rate[1]	2 Gb/s	250 Mbyte/s
Header Burden plus 4byte Sample Rate[2]	0.332 Gb/s	41.6 Mbyte/s
Actual Measured 4 Byte Read Rate[3]	0.019 Gb/s	2.35 Mbytes/s
Actual Measured DMA 4 Byte Read Rate[4]	0.327 Gb/s	40.9 Mbyte/s
Actual Measured 4 Byte Write Rate[5]	0.320 Gb/s	40 Mbyte/s

Note 1: PCIe x1 Gen 1 = 2.5GT/s (with 10-bit encoding we have a 20% loss in possible throughput due to encoding) giving 2.0 G bits/sec or 250M Bytes/sec.

Note 2: With PCIe we have a header for address and read/write command that is sent with every packet. This header is 20 Bytes with data payload of 4 Bytes (for our typical AcroPack). For each 4 Byte data sample, 24 Bytes are sent.

$\frac{250MByte/s}{24\,Bytes}$ = 10.4 M samples/sec or 41.6 M Bytes/sec or 0.332 G bit/sec

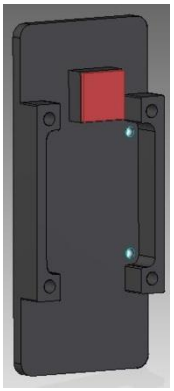
Note 3: For our typical AcroPack have measured back to back 4 Byte read operations completing every 1.7usec. A read operation starts with a host read request. The AcroPack must process the read and fetch the data and then generated the completion back to the host. The host then sends a message back that says I got it. This back and forth hand shaking slows down individual reads.

Note 4: DMA Read of 1024 sample takes 100us. Each sample is 4 Bytes. 100us/1024=0.0977us per sample or 4/0.0977us = 40.94Mbyte/s. We use DMA transfers to improve data transfers on the AP341/2 and AP225/235.

Note 5: Simple write operations are just as fast as DMA read operations. Write data is presented to the AcroPack in one transaction. Measured 4-byte back to back write accesses taking place every 100ns.

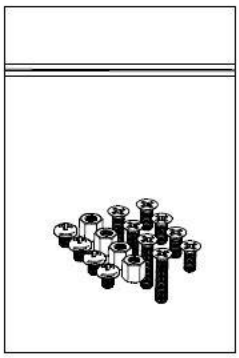
Appendix A

AP-CC-01 Heatsink Kit Installation



Bottom view

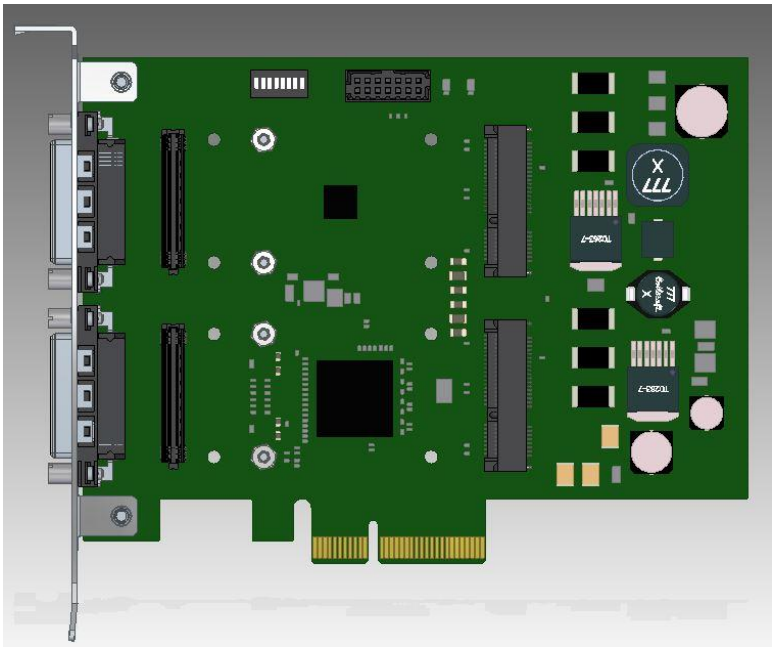
Top view



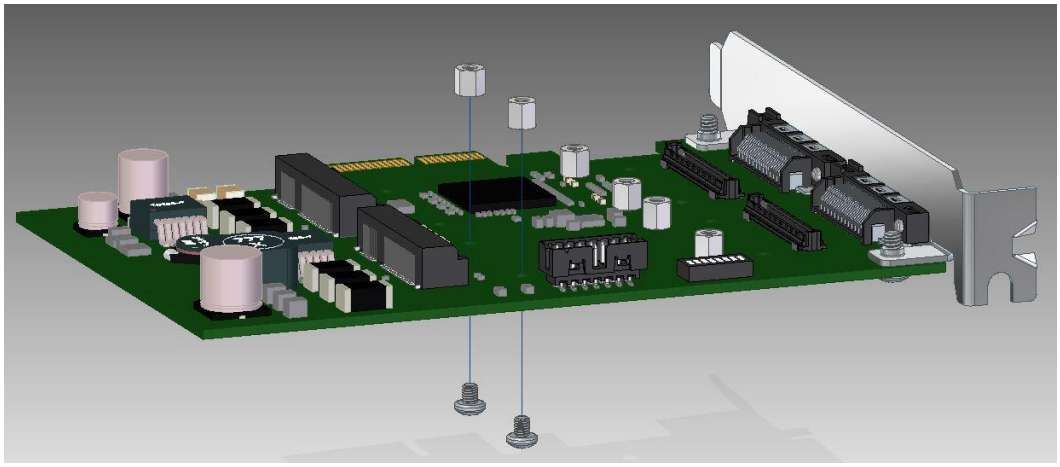
Hardware

AP-CC-01 Heat Sink Kit

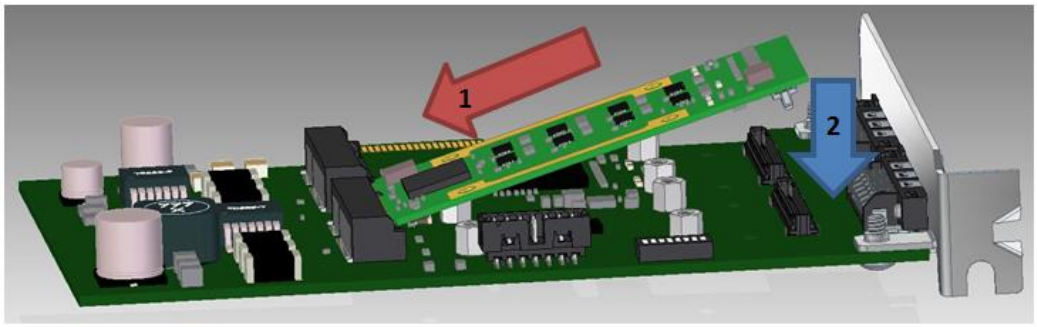
This example will show how to install the AP-CC-01 Heatsink kit with an APCe7020 carrier.



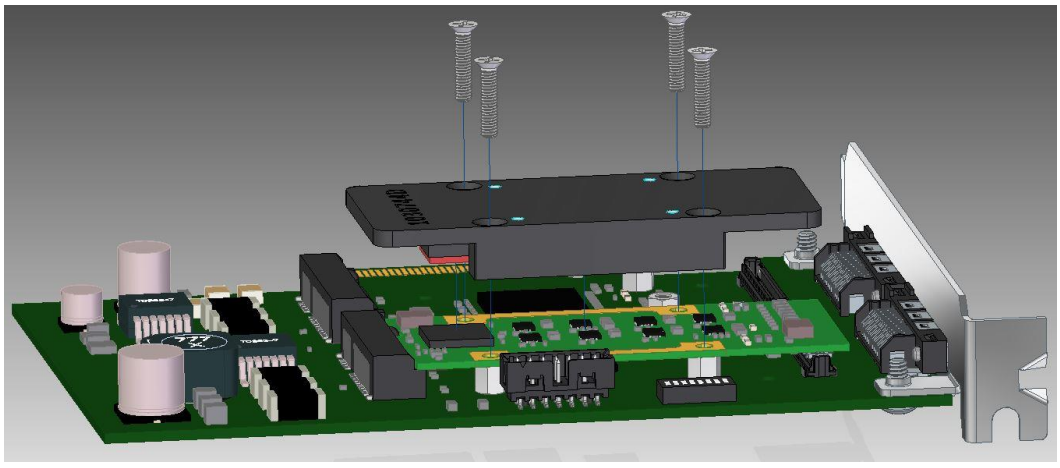
1. Install two standoffs and secure with two screws.



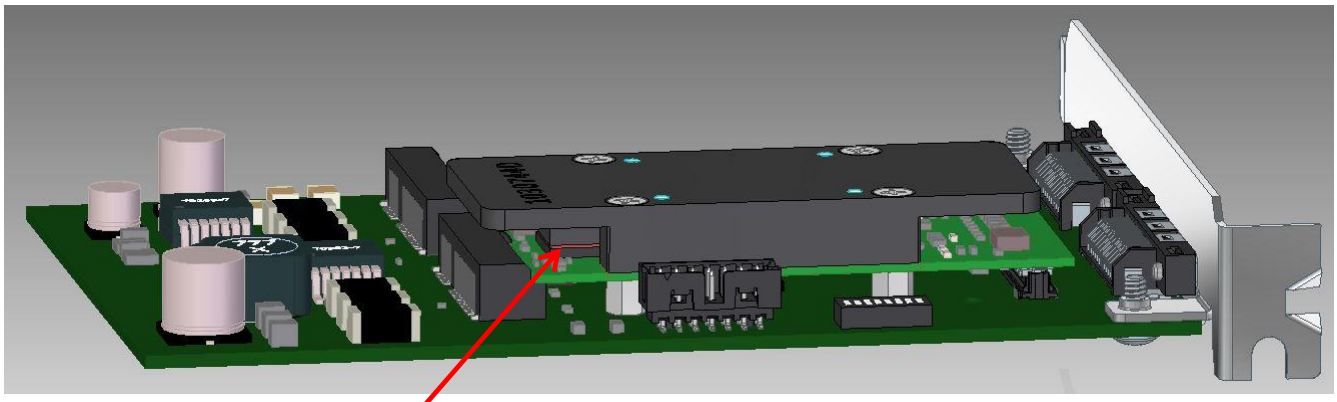
2. Install the AcroPack module.



3. Install the Heatsink and secure with 4 screws.



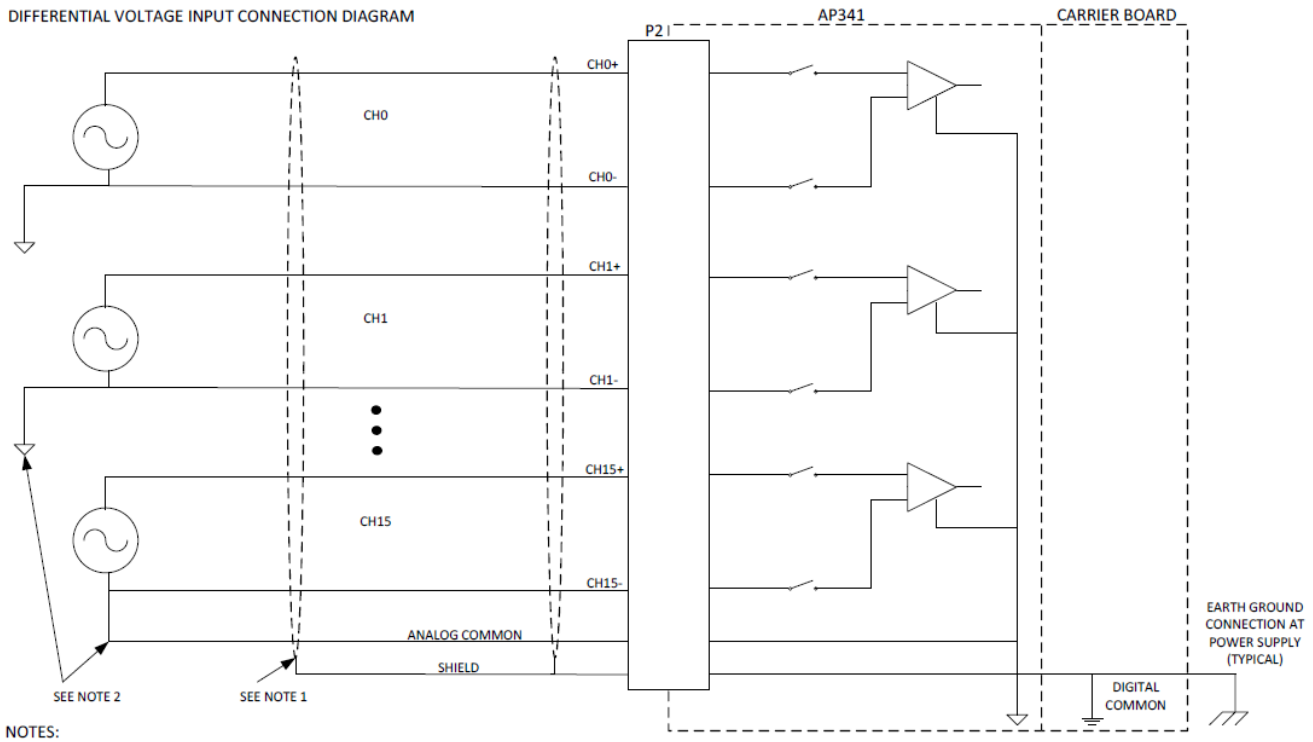
4. AP-CC-01 Installation is complete.



Note: Make sure the thermal pad is making contact with the FPGA IC.

Appendix B

Differential Voltage Input Connection Diagram



NOTES:
1. SHIELDED CABLE IS RECOMMENDED FOR LOWEST NOISE. SHIELD IS CONNECTED TO GROUND REFERENCE AT ONE END ONLY TO PROVIDE SHIELDING WITHOUT GROUND LOOPS.
2. REFERENCE CHANNELS TO ANALOG COMMON IF THEY WOULD OTHERWISE BE FLOATING. CHANNELS ALREADY HAVING A GROUND REFERENCE MUST NOT BE CONNECTED TO ANALOG COMMON, TO AVOID GROUND LOOPS.

Certificate of Volatility

<table>
<tr><th colspan="5">Certificate of Volatility</th></tr>
<tr><td colspan="2">Acromag Models:
AP341E-LF</td><td colspan="3">Manufacturer:
Acromag, Inc.
30765 Wixom Rd
Wixom, MI 48393</td></tr>
<tr><th colspan="5">Volatile Memory</th></tr>
<tr><td colspan="5">Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed)
■ Yes □ No</td></tr>
<tr><td>Type (SRAM, SDRAM, etc.)
FPGA based RAM</td><td>Size:
50 x 36-Kbit</td><td>User Modifiable
■ Yes
□ No</td><td>Function:
Data storage for FPGA</td><td>Process to Sanitize:
Power Down</td></tr>
<tr><th colspan="5">Non-Volatile Memory</th></tr>
<tr><td colspan="5">Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed)
■ Yes □ No</td></tr>
<tr><td>Type (EEPROM, Flash, etc.)
Flash</td><td>Size:
32Meg x 1bit</td><td>User Modifiable
■ Yes
□ No</td><td>Function:
Storage of Code for FPGA</td><td>Process to Sanitize:
Clear Flash memory by erasing all sectors of the Flash</td></tr>
<tr><td>Type (EEPROM, Flash, etc.)
One Time Programmable area in flash device</td><td>Size:
3 x 256-byte</td><td>User Modifiable
□ Yes
■ No</td><td>Function:
The OTP area has been disabled by writing the lock bits with logic 1</td><td>Process to Sanitize:
Not applicable</td></tr>
<tr><th colspan="5">Acromag Representative</th></tr>
<tr><td>Name:
Russ Nieves</td><td>Title:
Dir. of Sales and Marketing</td><td>Email:
solutions@acromag.com</td><td>Office Phone:
248-295-0310</td><td>Office Fax:
248-624-9234</td></tr>
</table>

Revision History

Release Date	Version	EGR/DOC	Description of Revision
14 Dec 2016	Prelim	ENZ/MJO	Preliminary Release.
18 APR 2017	Rev A	ENZ/MJO	Rev A Release
12 JAN 2018	Rev B	LMP/MJO	Added PCIe Bus Data Rates Table.
18 SEPT 2018	Rev C	LMP/MJO	Added Reliability Prediction MTBF Table