Series AP220 AcroPack

12-Bit Analog Output Module

AP231 AcroPack

16-Bit High Density Analog Output Module

USER'S MANUAL

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1. GENERAL INFORMATION

1.1 Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the AcroPack module. It is not intended for a general, non-technical audience that is unfamiliar with AcroPack devices and their application.

1.2 Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag,

1.2.1 Trademark, Trade Name and Copyright Information

1.2.2 Class A Product Warning

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

1.2.3 Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

1.3 AcroPack Information – All Models

The AcroPack IO module are based on the PCI Express Mini Card Electromechanical specification and are 70mm in length with an add 100 pin field I/O connector.

The AcroPack is 19.05mm longer than the full length mini PCIe card at 50.95mm. It has the same mPCIe board width of 30mm and uses the same mPCIe standard board hold down standoff and screw keep out areas.

The AP231 is a 16-bit, high-density, single-width AcroPack module, with the capability to drive up to 16 analog voltage output channels. The AP231 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its high channel density and is an ideal choice for a wide range of industrial control and monitor applications that require high-density, high-reliability, and high-performance at a low cost.

1.3.1 Ordering Information

The AcroPack ordering options are given in the following table.

Model Number	*Description*	*Temp Range*
AP220-16E-LF[1]	*16-Channel 12-Bit Analog Output*	*-40℃ to 85℃*
AP231-16E-LF[1]	*16-Channel 16-Bit Analog Output*	*-40℃ to 85℃*

Note 1: Applications requiring operating temperatures of 70°C to 85°C will require purchase of AcroPack Heatsink Accessory AP-CC-01 and minimum airflow of 400LFM. For temperatures below 70°C the module will require a minimal airflow of 200LFM

AP-CC-01 AcroPack Conduction Cool Kit (See Appendix for installation instructions)

1.3.2 Key Features

- **High Channel Count** – Individual control of up to 16 analog voltage output channels is provided.
- **AP220, 12-Bit Accuracy** - Each channel contains its own 16-bit, Digital to Analog Converter (DAC) with 7.5uS output settling time.
- **AP231, 16-Bit Accuracy** - Each channel contains its own 16-bit, Digital to Analog Converter (DAC) with 7.5uS output settling time.
- **Software selectable outputs** - Provides 6 Unipolar/bipolar voltage range outputs:
    - unipolar, 0V to +10 Volts, 0vV to +5 Volts
    - bipolar, +/-10 Volts, +/-5 Volts, +/-3 Volts, +/- 2.5V to 7.5 Volts
- **Reliable Software Calibration** - Calibration coefficients stored on-board provide the means for accurate software calibration of the module.

- **Individual Output Control** - Output channels can be individually selected and updated with a single channel data write command when using the "transparent" output mode.
- **Simultaneous Output Control** - All output channels can be simultaneously updated with a single software trigger command when using the "simultaneous" output mode (DAC's are double-buffered which allows new data to be written to each channel before the simultaneous trigger updates the outputs).
- **Easy Mode Selection** - Selection of transparent and simultaneous output modes is easily done via software commands.
- **Reset is Failsafe** - Outputs reset to 0 volts following a power up or reset.
- **Alarm** – Software readable, monitor Brownout, short circuit and Die temperature >150C.

1.3.3 Key Features PCIe Interface

- **PCIe Bus** – The AP module includes a PCI Express Generation 1 interface operating at a bus speed of 2.5 Gbps with one lane in each direction.
- **Compatibility** – PCI Express Base Specification v2.1 compliant PCI Express Endpoint.

1.4 Signal Interface Products

This AcroPack Module will mate directly to all Acromag AP carriers. Once connected, the module is accessed via a front panel connector.

The cables and termination panels are also available. For optimum performance with the AP231 analog output module, use of the shortest possible length of shielded I/O cable is recommended.

1.5 Software Support

The AcroPack series products require support drivers specific to your operating system. Supported operating systems include: Linux, Windows, and VxWorks

Windows®

Acromag provides software products (sold separately) to facilitate the development of Windows® applications interfacing with AcroPack modules, VPX I/O board products, and PCIe I/O Cards. This software (model APSW-API-WIN) consists of low-level drivers and Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

VxWorks®

Acromag provides a software product (sold separately) consisting of VxWorks® software. This software (Model APSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

Linux®

Acromag provides a software product consisting of Linux® software. This software (Model APSW-API-LNX) is composed of Linux® libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

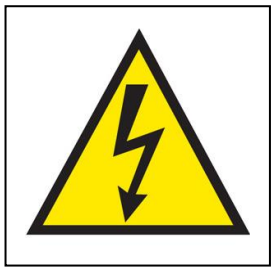
1.6 References

The following resources regarding AcroPack modules are available for download on Acromag's website or by contacting your sales representative.

- PCI Express MINI Card Electromechanical Specification, REV 1.2
  https://www.acromag.com

2.0 PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.

WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

2.1 Unpacking and Inspecting

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

2.2 Installation Considerations

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

Refer to the specifications section for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

In an air cooled assembly, a minimum of 200 LFM of air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If operating in an ambient temperature of > 70°C a heatsink is required as well as 400 LFM of Air circulation. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

In a conduction cooled assembly, adequate thermal conduction must be provided to prevent a temperature rise above the maximum operating temperature.

2.3 Non-Isolation Considerations

The board is non-isolated, since there is electrical continuity between the PCIe bus and AcroPack module grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

2.4 Default Hardware Configuration

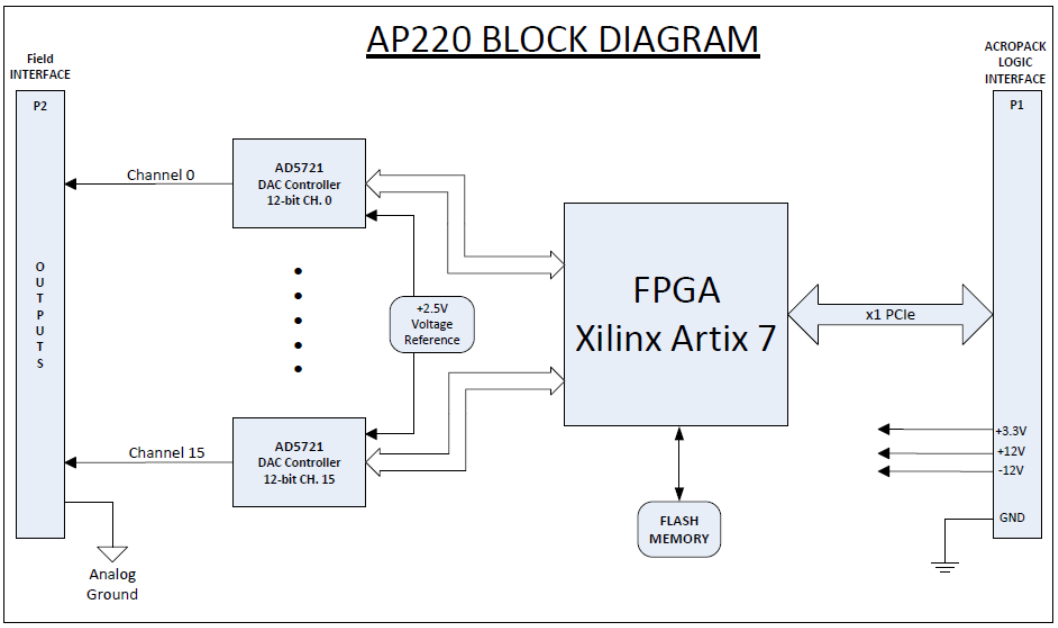
A board is shipped from the factory configured as follows:

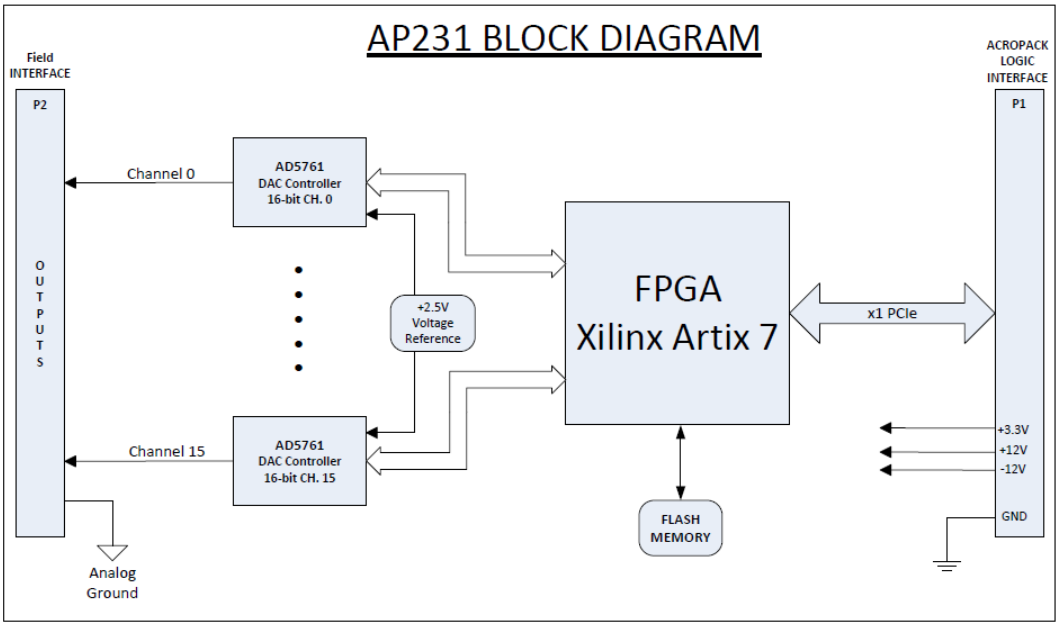
- Internal ± 12 Volt power supplies are used (sourced from PCI Local Bus connectors).
- Analog output bipolar range is -10 to +10 Volts.
- Software programmable register bits are undefined at reset, but the board defaults to 0 Volts on all analog outputs and the Simultaneous Channel Update Mode (see Section 3).

2.5 Programmable Register Configuration

Programmable registers are software configurable. That is, there are no hardware jumpers associated with them. Registers must be accessed to select the desired mode of operation and to update analog outputs (refer to Section 3 for details).

2.6 Functional Block diagram





2.7 Field I/O Connector

A field I/O interface connector provides a mating interface between the AP modules and the carrier board. The 100 pin ST5-50-1.50-L-D-P-TR Samtec connector is used on the AcroPack card as board to board interconnect. This connector will mate with the 100 pin SS5-50-3.00-L-D-K-TR Samtec connector on the carrier. The stack height is 4.5mm.

Threaded metric M2.5 screws and spacers are supplied with the module to provide additional stability for harsh environments.

Pin assignments are unique to each AP model. Table 2.1 lists signal pin assignments for the module field I/O connector. Every other pin of the 100 pin connector is left unconnected in order to meet the minimum distance required for 60 Volt isolation.

Table 2.1 Field I/O Connector Pin Assignments

68 Pin Champ Carrier Connector	50 Pin Champ Carrier Connector[2]	Ribbon Carrier Connector[1]	Module P2 Pin Number	Field I/O Signal
1	1	1	2	CH0+
35	26	2	1	Signal Return
			4	Reserved/isolation
			3	Reserved/isolation
2	2	3	6	CH1+
36	27	4	5	Signal Return
			8	Reserved/isolation
			7	Reserved/isolation
3	3	5	10	CH2+
37	28	6	9	Signal Return
			12	Reserved/isolation
			11	Reserved/isolation
4	4	7	14	CH3+
38	29	8	13	Signal Return
			16	Reserved/isolation
			15	Reserved/isolation
5	5	9	18	CH4+
39	30	10	17	Signal Return
			20	Reserved/isolation
			19	Reserved/isolation
6	6	11	22	CH5+
40	31	12	21	Signal Return
			24	Reserved/isolation
			23	Reserved/isolation
7	7	13	26	CH6+

41	32	14	25	Signal Return
			28	Reserved/isolation
			27	Reserved/isolation
8	8	15	30	CH7+
42	33	16	29	Signal Return
			32	Reserved/isolation
			31	Reserved/isolation
9	9	17	34	CH8+
43	34	18	33	Signal Return
			36	Reserved/isolation
			35	Reserved/isolation
10	10	19	38	CH9+
44	35	20	37	Signal Return
			40	Reserved/isolation
			39	Reserved/isolation
11	11	21	42	CH10+
45	36	22	41	Signal Return
			44	Reserved/isolation
			43	Reserved/isolation
12	12	23	46	CH11+
46	37	24	45	Signal Return
			48	Reserved/isolation
			47	Reserved/isolation
13	13	25	50	CH12+
47	38	26	49	Signal Return
			52	Reserved/isolation
			51	Reserved/isolation
14	14	27	54	CH13+
48	39	28	53	Signal Return
			56	Reserved/isolation
			55	Reserved/isolation
15	15	29	58	CH14+
49	40	30	57	Signal Return
			60	Reserved/isolation
			59	Reserved/isolation
16	16	31	62	CH15+
50	41	32	61	Signal Return
			64	Reserved/isolation
			63	Reserved/isolation
17	17	33	66	
51	42	34	65	
			68	Reserved/isolation
			67	Reserved/isolation
18	18	35	70	

52	43	36	69	
			72	Reserved/isolation
			71	Reserved/isolation
19	19	37	74	
53	44	38	73	
			76	Reserved/isolation
			75	Reserved/isolation
20	20	39	78	
54	45	40	77	
			80	Reserved/isolation
			79	Reserved/isolation
21	21	41	82	
55	46	42	81	
			84	Reserved/isolation
			83	Reserved/isolation
22	22	43	86	
56	47	44	85	
			88	Reserved/isolation
			87	Reserved/isolation
23	23	45	90	
57	48	46	89	
			92	Reserved/isolation
			91	Reserved/isolation
24	24	47	94	EXT_VSS_DAC
58	49	48	93	Signal Return
			96	Reserved/isolation
			95	Reserved/isolation
25	25	49	98	EXT_VDD_DAC
59	50	50	97	Signal Return
			100	Reserved/isolation
			99	Reserved/isolation

2.8 Logic Interface Connector

The AP module logic edge connector interfaces to the mating connector on the carrier board. The pin assignments of this connector are standard for all AP modules according to the PCI Express MINI Card Electromechanical Specification, REV 1.2 (with exceptions shown in Table 2.2 and noted below).

Power supplies +5, +12, and -12 Volt have been assigned to pins that are reserved in the mini-PCIe specification. The Present signal is grounded on the AP module. In addition, COEX1, COEX2 – wireless transmitter control are reassigned to JTAG signals TMS and TCK Lastly, UIM_C4, UIM_C8 – reserved User Identity Module signals are reassigned to JTAG signals TDI and TDO.

Table 2.2 Logic Interface connector Pin Assignments

Pin #	Name	Pin #	Name
51	+5V[1,2]	52	+3.3V[3]
49	+12V[1,2]	50	GND
47	-12V[1,2]	48	N.C. (+1.5V)[1]
45	Present[4]	46	N.C. (LED_WPAN#)[1]
43	GND	44	N.C. (LED_WLAN#)[1]
41	+3.3V[3]	42	N.C. (LED_WWAN#)[1]
39	+3.3V[3]	40	GND
37	GND	38	N.C. (USB_D+)[1]
35	GND	36	N.C. (USB_D-)[1]
33	PETp0	34	GND
31	PETn0	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	N.C. (+1.5V)[1]
25	PERp0	26	GND
23	PERn0	24	+3.3V[3]
21	GND	22	PERST#
19	TDI (UIM_C4)[1]	20	N.C. (W_DISABLE#)[1]
17	TDO (UIM_C8)[1]	18	GND
15	GND	16	N.C. (UIM_VPP)[1]
13	RECLK+	14	N.C. (UIM_RESET)[1]
11	REFCLK-	12	N.C (UIM_CLK)[1]
9	GND	10	N.C. (UIM_DATA)[1]
7	CLKREQ#	8	N.C. (UIM_PWR)[1]
5	TCK (COEX2)[1]	6	N.C. (+1.5V)[1]
3	TMS (COEX1)[1]	4	GND
1	N.C. (WAKE#)[1]	2	+3.3V[3]

Note 1: Signals are not applicable for the AP220 and AP231 implementation. Pins are either "no connects" on the module or are repurposed for JTAG.

Note 2: +5V, +12V, and -12V power supplies have been assigned to pins that are reserved in the mini-PCIe specification.

Note 3: All +3.3Vaux power pins are changed to +3.3V power.

Note 4: The Present signal is tied to circuit common on the AP module.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the AP220 or AP231 module.

The PCIe bus is defined to address three distinct address spaces: I/O, memory, and configuration space. The AcroPack module can be accessed via the PCIe bus memory space and configuration spaces, only.

The AcroPack configuration registers are initialized by system software at power-up to configure the card. The AP220 or AP231 module is a Plug-and-Play PCIe card. As a Plug-and-Play card the board's base address and system interrupt request are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCIe bus configuration access is used to access an AcroPack's configuration registers.

When the computer is first powered-up, the computer's system configuration software scans the PCIe bus to determine what PCIe devices are present. The software also determines the configuration requirements of the PCIe card.

The system software accesses the configuration registers to determine how many blocks of memory space the module requires. It then programs the board's configuration registers with the unique memory base address.

Since this board is not fixed in address space, its device driver must use the mapping information stored in the board's Configuration Space registers to determine where the board is mapped in memory space.

The configuration registers are also used to indicate that the board requires an interrupt request. The system software then programs the configuration registers with the interrupt request assigned to the board.

CONFIGURATION REGISTERS

The PCIe specification requires software driven initialization and configuration via the Configuration Address space. This board provides 512 bytes of configuration registers for this purpose. It contains the configuration registers shown in the following table to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers and the Interrupt Register which must be read to determine the base address assigned to the board and the interrupt request that goes active on a board interrupt request.

Table 3.1 Configuration Registers

Reg. Num.	D31 D24	D23 D16	D15 D8	D7 D0
0	**Device ID** 0x701A AP220 0x701B AP231		**Vendor ID** 16D5	
1	Status		Command	
2	Class Code=118000			Rev ID=00
3	BIST	Header	Latency	Cache
4	64-bit Memory Base Address for Memory Accesses to PCIe interrupt and I/O registers 4K Space **(BAR0)**			
5:10	Not Used			
11	**Subsystem ID** 0x701A AP220 0x701B AP231		**Subsystem Vendor ID** 16D5	
12	Not Used			
13,14	Reserved			
15	Max_Lat	Min_Gnt	Inter. Pin	Inter. Line

This board is allocated a 4K byte block of memory (BAR0), to access the PCIe interrupt and I/O registers. The PCIe bus decodes 4K bytes for BAR0 for this memory space.

The memory space address map for the AP220 or AP231 is shown in Table 3.2. Note that the base address for the board (BAR0) in memory space must be added to the addresses shown to properly access these AP220 and AP231 registers. Register accesses as 32, 16, and 8-bit data in memory space are permitted. All the registers of the AP220 or AP231 are accessed via data lines D0 to D31.

Table 3.2: BAR0 Registers

Note that any registers/bits not mentioned will remain at the default value logic low.

BAR0 Base Address	Bit(s)	Description
0x0000 0000	31:0	Not Used
0x0000 0004	7:0	Location in System Register
0x0000 0008	31:0	DAC Channel 0
0x0000 000C	31:0	DAC Channel 1
0x0000 0010	31:0	DAC Channel 2
0x0000 0014	31:0	DAC Channel 3

0x0000 0018	31:0	DAC Channel 4
0x0000 001C	31:0	DAC Channel 5
0x0000 0020	31:0	DAC Channel 6
0x0000 0024	31:0	DAC Channel 7
0x0000 0028	31:0	DAC Channel 8
0x0000 002C	31:0	DAC Channel 9
0x0000 0030	31:0	DAC Channel 10
0x0000 0034	31:0	DAC Channel 11
0x0000 0038	31:0	DAC Channel 12
0x0000 003C	31:0	DAC Channel 13
0x0000 0040	31:0	DAC Channel 14
0x0000 0044	31:0	DAC Channel 15
0x0000 0048	31:0	Simultaneous Mode
0x0000 004C	31:0	Simultaneous Output Trigger
0x0000 0050	31:0	Not Used
0x0000 0054	31:0	DAC Write Status
0x0000 0058	31:0	DAC Reset Control
0x0000 005C→0x00000084	31:0	Not Used
0x0000 0088		XADC Status/Control Register
0x0000 008C		XADC Address Register
0x0000 0090→0x000001FC		Not Used
0x0000 0200	31:0	Firmware Revision
0x0000 0204	7:0	Flash Data
0x0000 0208	Bit-0	Flash Chip Select
0x0000 020C→0x000007FF	31:0	Not Used

Module Location In System Register (Read Only) - (BAR0 + 0x0000 0004)

This read only register is used identify the module's plugin location in a system.

Table 3.3 Location Register

Note that any registers/bits not mentioned will remain at the default value logic low.

This feature was implemented on the Revision B boards.

Bit(s)	FUNCTION	
2 to 0	Module Site Location Bits. These bits identify the location on the carrier of the AP module.	
	000	Carrier Site A
	001	Carrier Site B
	010	Carrier Site C
	011	Carrier Site D
7 to 3	Module Slot Location Bits. These bits identify the slot location of the AP module in a system. The Carrier may use backplane signals as in a VPX system or a carrier DIP switch to uniquely identify the system location of the carrier.	
	XXXXX	System Slot identification bits are described by the AcroPack carrier card.
31 to 8	Not Used	

DAC Channel Registers (Read/Write) - (BAR0 + 0x0000 0008 to 0x0000 0044)

Sixteen (16) DAC Channels registers are used to write and read the DAC 24-bit control/data values. Writing to the address of the specific register enables transfer of data and control of the DAC. Read of the specified register returns the DAC data or control value as requested. All reads requires write of two read commands to complete serial shift out of the DAC data or control value. Then read the DAC channel register will contain the read data in the lower 16 bits for AP231 and bits-15 to 4 of the AP220. See Table 3.5 for the allowed DAC write and read commands.

The contents of the DAC Channel registers are transferred to their corresponding converter input buffer serially. This serial data transfer take 1.6µs. Thus, a new write of the same DAC register can be performed no sooner then 1.6µs after the previous write. A DAC Write Status register, at base address plus 54H, is available as a write operation busy status indicator. The channels Status bit will be set low upon initiation of a write operation and will remain low until the requested write operation has completed. New write accesses to the same DAC Channel register, should not be initiated unless its write busy status bit is set high. Read of the DAC registers must also wait 1.6µs after issue of two read commands. Thus you avoid read of the register as it is being serially shift out.

Table 3.4 DAC Channel Register

Bit(s)	FUNCTION	
15 to 0	Data 16-bits or Control register data with issue of 0100 commend or DAC data when issued of 0001 or 0011.	
19 to 16	Address 4-bits	
	0000	No Operation
	0001	**Write to input register** (no DAC output update input register only written.) Used for simultaneous mode

	0010	**Update DAC register from input register** (Updates DAC output voltage). Software equivalent of LDAC
	0011	**Write and update DAC register** (Updates the input register and DAC register irrespective of LDAC) Use for transparent mode
	0100	**Write to control register**
	0101	No operation
	0110	No operation
	0111	**Software data reset** (Reset to zero scale, midscale, or full scale as specified by PV1 and PV0 bits of control.)
	1000	Reserved
	1001	**Disable daisy-chain functionality** (Default enabled) Leave enabled for SDO read-back operation.
	1010	**Readback input register** (Provides contents of input register after issue of two commands and 1.6µs.)
	1011	**Readback DAC register** (Provides contents of DAC register after issue of two commands and 1.6µs.)
	1100	**Readback control register** (Provides contents of control register after issue of two commands and 1.6µs. See Table 3.6 for description of DAC Control register.)
	1101	No operation
	1110	No operation
	1111	**Software full reset** (Device set to power up state, output at AGND and output buffer is powered down.)
20	0 (This bit must be fixed at 0)	
31 to 21	Not Used	

Table 3.5 DAC Channel Control Register

Bit(s)	FUNCTION	
2 to 0	3-bits Output Range (Software full reset is also issued when the output range is reconfigured.)	
	000	-10V to +10V
	001	0V to +10V
	010	-5V to +5V
	011	0V to +5V
	100	-2.5V to +7.5V
	101	-3V to +3V
	110	0V to 16V (external power supply, contact Acromag)
	111	0V to 20V (external power supply, contact Acromag)
4 to 3	2-bits Power-up Voltage	
	00	Zero scale
	01	Midscale
	10	Full scale
	11	Full scale

5	0	Fixed at 0
6	Thermal shutdown alert	
	0	Die temperature > 150C do not power down
	1	Die temperature > 150C power down
7	Data Format Control Bit When a channel is configured for 0-10 or 0-5 ranges, this bit is ignored and anything written to the DAC is treated as straight binary. See Table 3.6 for example corresponding codes.	
	0	Straight binary coded or Bipolar Offset Binary coded
	1	Twos complement coded
8	5% Over-range	
	0	5% over-range disable
	1	5% over-range enable
10 to 9	2-bits Clear voltage selection	
	00	Zero scale
	01	Midscale
	10	Full scale
	11	Full scale
11	Brownout condition status on readback	
	0	No brownout condition
	1	Brownout condition detected
12	Short-circuit condition status on readback	
	0	No short circuit condition
	1	Short-circuit condition detected
15 to 13	Not Used	

Output Data Format

The default bipolar output range (-10 to +10 Volts) is programmed with straight binary with default setting. However, twos complement can also be select via the write to DAC control register. The following table indicates the relationship between the data format and the ideal analog output voltage from the module.

Table 3.6 DAC Channel Data Format

Straight Binary	Decimal Code	Twos Complement
1111	+7	0111
1110	+6	0110
1101	+5	0101
1100	+4	0100
1011	+3	0011
1010	+2	0010

1001	+1	0001
1000	0	0000
0111	-1	1111
0110	-2	1110
0101	-3	1101
0100	-4	1100
0011	-5	1011
0010	-6	1010
0001	-7	1001
0000	-8	1000

Transparent Mode

The Transparent Mode is available with DAC **Write and update DAC register command 0011.**

Simultaneous Mode (Read/Write) - (BAR0 + 0x0000 0048)

The Simultaneous Mode is a write-only register that is used to select the simultaneous type of data transfer. Once Simultaneous Mode is selected, digital data written should use **Write to input register** DAC Command 0001 to the address specific channel's input latch. Data will not show up at the output until the Simultaneous Output Trigger register is written. The data, of all the channels, is simultaneously transferred, **once per simultaneous trigger,** from the DAC input latch to the output (and analog output) updated only when the Simultaneous Output Trigger register is enabled. The data written to this location must have bit-0 set to logic '1' in order to select Simultaneous Mode.

RESET CONDITION: Defaults to Simultaneous Mode. All analog output channels are set to "0 Volts".

Note: The reset function resets only the DAC output latch of the input double buffer. Therefore, after a reset, good data must be written (using **Write to input register** DAC Command 0001) to all the input latches before enabling the Simultaneous Output Trigger for a DAC output update. Otherwise, old or unknown data present in the input latches will be transferred to the DAC output latch producing an undesired analog output.

Simultaneous Output Trigger (Write Only) - (BAR0 + 0x0000 004C)

Simultaneous Output Trigger is a write-only register that produces the pulse needed to trigger simultaneous data transfer. Simultaneous Output Trigger register works in conjunction with the Simultaneous Mode register to simultaneously transfer all the channels' digital data from the DAC input latch to the output latch (and update the analog output) at a specific time. The Simultaneous Mode register must be written to first. Then, writing to the Simultaneous Output Trigger register creates the trigger for digital data to be converted and transferred to the board's field connector. The digital

data written to the address specific channel's input latch will continue to be held until the Simultaneous Output Trigger register is written.

This will trigger the transfer of digital data from the D/A input latch to the output latch and the digital to analog conversion producing the updated analog output. The data written to this location is immaterial, since the write is sufficient to complete the action.

RESET CONDITION: Defaults to Simultaneous Mode. All analog output channels are set to "0 Volts".

Note: The reset function resets only the DAC output latch of the input double buffer. Therefore, after a reset, good data must be written to all the input latches before enabling the Simultaneous Output Trigger for a DAC output update. Otherwise, old or unknown data present in the input latches will be transferred to the DAC output latch producing an undesired analog output.

DAC Write Status Register (Read Only) - (BAR0 + 0x0000 0054)

This DAC Write Status register can be read to monitor the busy status after a write to a DAC channel. New write of a DAC Channel register can be performed no sooner than 1.6µs after the previous DAC write command is executed.

The status of 16 DAC channels numbered 0 through 15 may be monitored via this register. Data bits 0 to 15 reflect the status of DAC channels 0 to 15. The channels corresponding status bit will be set low upon initiation of a write operation and will remain low until the requested write operation has completed. New write accesses to the DAC Channel register should not be initiated unless its write busy status bit is set high.

Control Register (Write Only) - (BAR0 + 0x0000 0058)

Asserting bit-0 of this register to logic "1" returns the DACs to their default power-on status where the output is clamped to ground and the output buffer is powered down.

Asserting bit-1 of this register to logic "1" sets the DAC register to zero-scale, midscale, or full-scale code (user selectable) and updates the DAC output.

Asserting bit-7 of this register to logic "1" issues a software reset to the module.

Bit-7 resets only the DAC output latch of the input double buffer. Therefore, after a reset, good data must be written to all the input latches before enabling the Transparent Mode or enabling the Simultaneous Output Trigger for a DAC output update. Otherwise, old data or unknown data present in the input latches will be transferred to the DAC output latch producing an undesired analog output.

XADC Status/Control Register (Read/Write) - (BAR0 + 0x0000 0088)

This read/write register will access the XADC register at the address set in the XADC Address Register.

For example, the address of the XADC Status register that is to be accessed is first set via the XADC Address register at BAR0 plus 0x8CH. Next, this register at BAR0 plus 0x88H is read. Bits 22 to 16 of this register hold the address of the XADC register that is accessed. Data bits 15 to 6 of this register hold the "ADCcode" temperature, Vccint, or Vccaux value. Data bits 5 to 0 are not used. Valid addresses are given in column one of the table below.

Reading or writing this register is possible via 32-bit data transfers.

The 10-bits digitized and output from the ADC can be converted to temperature by using the following equation.

$$Temperature(°C) = \frac{ADCcode \times 503.975}{1024} - 273.15$$

The 10-bits digitized and output from the ADC can be converted to voltage by using the following equation.

$$SupplyVoltage(volts) = \frac{ADCcode}{1024} \times 3V$$

XADC Address Register (Write Only) - (BAR0 + 0x0000 008C)

This write only register is used to set the XADC address register with a valid address for the XADC internal status or control registers. Valid addresses are given in the following table. Additional addresses can be found in the Xilinx XADC document UG480 (available from Xilinx). Writing this register is possible via 32-bit data transfers.

The address value written to this register can be read on bits 22 to 16 of the XADC Status/Control register at BAR0 plus 0x48H.

Table 3.7: System Monitor Register Map

Address	Status Register
0x00	Temperature
0x01	Vccint
0x02	Vccaux
0x20	Maximum Temperature
0x21	Maximum Vccint
0x22	Maximum Vccaux
0x24	Minimum Temperature
0x25	Minimum Vccint
0x26	Minimum Vccaux

Firmware Revision Register (Read Only) - (BAR0 + 0x0000 0200)

This is a read only register. The ASCII code representing the current revision of the MCS firmware file is readable from this location. For example, if the firmware is at revision A then this register will read 0x41 in the least significant byte or B= 0x42, C=0x43, etc.

Flash Data Register (Read/Write) - (BAR0 + 0x0000 0204)

A byte write to this address triggers a write/read serial transfer to/from the serial FLASH device. A byte read from this address returns the data read from a previous write/read serial transfer.

WARNING: Factory calibration data is stored in FLASH. Writing to FLASH could result in loss of factory calibration data. See Table 3.7 Flash Memory Map.

Note that the Flash chip select must be set prior to the start of any instruction. Flash chip select must also be driven high after the instruction is issued.

Table 3.8 Flash Data Register

Note that any registers/bits not used will remain at the default value logic low.

BIT	Function
31 - 8	Unused
7 - 0	Flash Data

Flash Chip Select (Write Only) - (BAR0 + 0x0000 0208)

Asserting bit-0 to logic "0" drive the Flash chip select signal active. The default state of this bit is logic "1" which is the inactive state of the Flash chip select signal.

Note that the Flash chip select must be set prior to the start of Flash memory instruction. Flash chip select must also be driven high after the instruction is issued.

Flash Coefficient Memory Map

Table 3.9 Flash Coefficient Memory Map

Flash Coefficient Memory starts at the second from the last sector SA1022. This corresponds to Flash address range of 3FE000 to 3FEFFF.

Channel 1 coefficients start at **0x3F E100** to **0x3F E117.**

Channel 2 coefficients start at **0x3F E200** to **0x3F E217.**

Etc.

Channel 15 coefficients start at **0x3F EF00** to **0x3F EF17.**

Note that the coefficients are stored as 2's complement to allow of plus and minus values.

Flash Address	Bit(s)	Range	Description
0x3F E000	7:0	-10 to 10V	Channel 0 OffsetCoef LSB
0x3F E001	7:0	-10 to 10V	Channel 0 OffsetCoef MSB
0x3F E002	7:0	-10 to 10V	Channel 0 GainCoef LSB
0x3F E003	7:0	-10 to 10V	Channel 0 GainCoef MSB
0x3F E004	7:0	0 to 10V	Channel 0 OffsetCoef LSB
0x3F E005	7:0	0 to 10V	Channel 0 OffsetCoef MSB
0x3F E006	7:0	0 to 10V	Channel 0 GainCoef LSB
0x3F E007	7:0	0 to 10V	Channel 0 GainCoef MSB
0x3F E008	7:0	-5 to 5V	Channel 0 OffsetCoef LSB
0x3F E009	7:0	-5 to 5V	Channel 0 OffsetCoef MSB
0x3F E00A	7:0	-5 to 5V	Channel 0 GainCoef LSB
0x3F E00B	7:0	-5 to 5V	Channel 0 GainCoef MSB
0x3F E00C	7:0	0 to 5V	Channel 0 OffsetCoef LSB
0x3F E00D	7:0	0 to 5V	Channel 0 OffsetCoef MSB
0x3F E00E	7:0	0 to 5V	Channel 0 GainCoef LSB
0x3F E00F	7:0	0 to 5V	Channel 0 GainCoef MSB
0x3F E010	7:0	-2.5 to 7.5V	Channel 0 OffsetCoef LSB
0x3F E011	7:0	-2.5 to 7.5V	Channel 0 OffsetCoef MSB
0x3F E012	7:0	-2.5 to 7.5V	Channel 0 GainCoef LSB
0x3F E013	7:0	-2.5 to 7.5V	Channel 0 GainCoef MSB
0x3F E014	7:0	-3 to 3V	Channel 0 OffsetCoef LSB
0x3F E015	7:0	-3 to 3V	Channel 0 OffsetCoef MSB
0x3F E016	7:0	-3 to 3V	Channel 0 GainCoef LSB

0x3F E017	7:0	-3 to 3V	Channel 0 GainCoef MSB
0x3F E018 ->	7:0	Reserved	Reserved
0x3F E0FF	7:0	Reserved	Reserved

Table 3.10 Flash Coefficient Memory Map ASCII String Location

ASCII code for AP231 or AP220 starting at address 0x3F EFF0 is present to indicate valid calibration data.

Flash Address	Bit(s)	AP231 Model	AP220 Model
0x3F EFF0	7:0	A = 0x41	A = 0x41
0x3F EFF1	7:0	P = 0x50	P = 0x50
0x3F EFF2	7:0	2 = 0x32	2 = 0x32
0x3F EFF3	7:0	3 = 0x33	2 = 0x32
0x3F EFF4	7:0	1 = 0x31	0 = 0x30
0x3F EFF5	7:0	0 (null Character)	0 (null Character)
0x3F EFF6->	7:0	Reserved	Reserved
0x3F EFFF	7:0	Reserved	Reserved

4.0 USE OF CALIBRATION DATA

Calibration data is provided in the form of calibration coefficients, so the user can adjust and improve the accuracy of the analog output voltage over the uncalibrated state. Each channel's unique offset and gain calibration coefficients are stored in Flash memory. The use of software calibration allows the elimination of hardware calibration potentiometers traditionally used in producing precision analog outputs. A comparison of the uncalibrated and software calibrated performance is shown to illustrate the importance of the software calibration.

Software calibration uses some fairly complex equations. Acromag provides software products (sold separately) to make communication with the board and calibration easy. It relieves you from having to turn the equations of the following sections into debugged software calibration code.

4.1 Uncalibrated Performance

The uncalibrated performance is affected by two primary error sources. These are the channel's offset and gain errors. The use of channel specific calibration coefficients to accurately adjust offset and gain is important because the worst case uncalibrated error can be significant (although the typical uncalibrated errors observed may be much less). The maximum uncalibrated error is summarized as follows.

AP231 Model

AD5761 @ -40^{O}C to 85^{O}C:

Linearity Error is +/- 0.003% FSR maximum (i.e. +/-2 LSB).

Offset Error is +/- 0.05% FSR (i.e. 20V SPAN) maximum.

Gain Error is +/- 0.1% FSR maximum.

Total Error +/- 0.153% FSR maximum (+/-98.5 LSB)

AP220 Model

AD5721 @ -40^{O}C to 85^{O}C:

Linearity Error is +/- 0.0122% FSR maximum (i.e. +/-0.5 LSB).

Offset Error is +/- 0.05% FSR (i.e. 20V SPAN) maximum.

Gain Error is +/- 0.1% FSR maximum.

Total Error +/- 0.1622% FSR maximum (+/-6.64 LSB)

Typically, each error component is much less than its maximum and all error components do not reinforce each other. Thus, typical errors are much less than that shown above.

4.2 Calibrated Performance

Accurate calibration of the AP231 or AP220 can be accomplished through software control by using calibration coefficients to adjust the analog output voltage. Unique calibration coefficients are stored in Flash memory as 1/16 LSB's for each specific channel. Once retrieved, the channel's unique offset and gain coefficients can be used to correct the data value sent to the DAC channel to accurately generate the desired output voltage.

The maximum calibrated error combining the linearity and adjusted offset and gain errors:

AP231 Model

AD5761 @ -40^{O}C to 85^{O}C:

Linearity Error is +/-2 LSB

Offset Error is +/-0.0625 LSB

Gain Error is +/-0.0625 LSB

Total Error +/-2.125 LSB (+/- 0.0032% FSR) maximum

AP220 Model

AD5721 @ -40^{O}C to 85^{O}C:

Linearity Error is +/-0.5 LSB

Offset Error is +/-0.0625 LSB

Gain Error is +/-0.0625 LSB

Total Error +/-0.625 LSB (+/- 0.0152% FSR) maximum

Thus, correcting the value programmed to the DAC Channel Register using the stored calibration coefficients provides the means to obtain excellent accuracy.

Data is corrected using a couple of formulas. Equation (1) expresses the ideal relationship between the value (*IdealCode*) written to the 16-bit DAC to achieve a specified voltage within output range assuming Straight Binary (also called Bipolar Offset Binary) or 2's Complement data format (see Table 3.11 and 3.12).

Equation (1):

$$IdealCode = [IdealSlope \times DesiredVoltage] + IdealZeroCode$$

where,

Table 3.11 AP231 Model

Ideal slope and zero values for supported ranges.

Range	*IdealSlope*	*IdealZeroCode* *Straight Binary(2's Comp)*
-10 to 10V	3276.8	32768 (0)
-5 to 5V	6553.6	32768 (0)
-3 to 3V	10922.67	32768 (0)
-2.5 to 7.5V	6553.6	16384 (-16384)
0 to 10V	6553.6	0 (-32768)
0 to 5V	13107.2	0 (-32768)

Table 3.12 AP220 Model

Ideal slope and zero values for supported ranges.

Range	*IdealSlope*	*IdealZeroCode* *Straight Binary(2's Comp)*
-10 to 10V	204.8	2048 (0)
-5 to 5V	409.6	2048 (0)
-3 to 3V	682.6	2048 (0)
-2.5 to 7.5V	409.6	1024 (-1024)
0 to 10V	409.6	0 (-2048)
0 to 5V	819.2	0 (-2048)

Using equation (1), one can determine the *IdealCode* for any desired voltage within the range. For example, if it is desired to output a voltage of +5 Volts for -10 to 10V range, equation (1) returns the result 49,152 for *IdealCode* for Model AP231. If this value is used to program the DAC output (following conversion to Hex 0xC000), the output value will approach +5 Volts to within the uncalibrated error. This will be acceptable for some applications.

For applications needing better accuracy, the software calibration coefficients should be used to correct the *IdealCode* into the CorrectedCode required to accurately produce the output voltage. This is illustrated in equation (2):

Equation (2) AP231 Model

$$\text{CorrectedCode} = \left(\frac{\text{GainCoef}}{65536 \times 16} + 1\right)[\text{IdealSlope} \times \text{DesiredVoltage}] + \text{IdealZeroCode} + \frac{\text{OffsetCoef}}{16}$$

The GainCoef and OffsetCoef are stored and retrieved from Flash memory at the addresses shown in Table 3.7. Coefficients are unique to each of the 16 channels. The GainCoef and OffestCoef values are calculated using the following equations at room temperature and then stored in Flash memory at the location identified in Table 3.7. Note that the coefficients are stored as 2's complement to allow of plus and minus values.

AP231 Model

$$\text{GainCoef} = 65536 \times 16\left(\frac{ActualSlope}{IdealSlope} - 1\right)$$

$$\text{OffsetCoef} = (\text{ActualZeroCode} - \text{IdealZeroCode}) \times 16$$

$$\text{ActualSlope} = \left(\frac{Code2 - Code1}{MeasuredV2 - MeasuredV1}\right)$$

$$\text{ActualZeroCode} = \text{Code1} - (\text{ActualSlope} \times MeasuredV1)$$

Where:

Code1 = 655(0x28F hex)

Code2 = 64880 (0xFD70 hex)

Measured values ($MeasuredV2\ and\ MeasuredV1$)are taken using data averaging.

Equation (3) AP220 Model

$$\text{CorrectedCode} = \left(\frac{\text{GainCoef}}{4096 \times 16} + 1\right)[\text{IdealSlope} \times \text{DesiredVoltage}] + \text{IdealZeroCode} + \frac{\text{OffsetCoef}}{16}$$

AP220 Model

$$\text{GainCoef} = 4096 \times 16\left(\frac{ActualSlope}{IdealSlope} - 1\right)$$

$$\text{OffsetCoef} = (\text{ActualZeroCode} - \text{IdealZeroCode}) \times 16$$

$$\text{ActualSlope} = \left(\frac{Code2 - Code1}{MeasuredV2 - MeasuredV1}\right)$$

$$\text{ActualZeroCode} = \text{Code1} - (\text{ActualSlope} \times MeasuredV1)$$

Where:

Code1 = 40 (0x28 hex)

Code2 = 4055 (0xFD7 hex)

Measured values ($MeasuredV2\ and\ MeasuredV1$)are taken using data averaging.

5.0 SERVICE AND REPAIR

5.1 Service and Repair Assistance

Surface-Mounted Technology (SMT) boards like the AcroPack family of carrier boards are generally difficult to repair. The board can be easily damaged unless special SMT repair and service tools are used. For these and other reasons, it is strongly recommended that a non-functioning board be returned to Acromag for repair. Acromag has automated diagnostic and test equipment that thoroughly checks the performance of suspect boards. Furthermore, when any repair is made, the board is retested before return shipment to the customer.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts, or return parts for repair.

5.2 Preliminary Service Procedure

CAUTION: POWER MUST BE TURNED OFF BEFORE SERVICING BOARDS

Before beginning repair, be sure that all of the procedures in the "Preparation for Use" section have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique for isolating a faulty part.

5.3 Where to Get Help

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at https://www.acromag.com. Our web site contains the most up-to-date product and software information.

Go to the "Support" tab to access:

- Application Notes
- Frequently Asked Questions (FAQ's)
- Product Knowledge Base
- Tutorials
- Software Updates/Drivers

Acromag's application engineers can also be contacted directly for technical assistance via email, telephone, or FAX through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab. When needed, complete repair services are also available.

- Email: solutions@acromag.com
- Phone: 248-295-0310

6.0 SPECIFICATIONS

6.1 Physical

Height: 12.5 mm (0.4921 in)

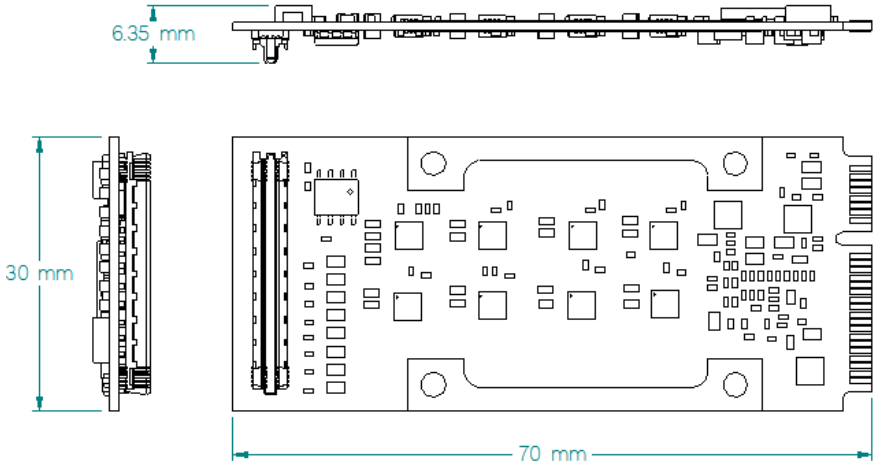
Height defines Carrier to Module Maximum component height

Board Thickness 1.0 mm (0.03937 in)

- AcroPack L x W: 70 mm x 30.00 mm (2.76 in x 1.18 in)

Unit Weight (does not include shipping material):

- AcroPack 0.016 lbs (0.0074 kg)



6.2 Power Requirements

Summarized below are the expected current draws for each of the specified power supply voltages. (The current draw is the same for both AP220E and AP231E)

Power Supply Voltage	Current Draw
• +3.3 VDC +/- 5%[1]	400 mA Typical, 480 mA maximum
• +12 VDC +/- 5%[1]	85 mA Typical, 275 mA maximum
• -12 VDC +/- 5%[1]	50 mA Typical, 200 mA maximum

Note 1: *Typical current draw is using an AP220E with APCe7020E-LF*

6.3 Environmental Considerations

Summarized below are the operating temperature range, airflow and other environmental requirements and applicable standards for the AcroPack module.

6.3.1 Operating Temperature

Model Number	***Description***	***Temp Range***
AP220E-LF	*16 Channels of 12-bit Analog Output*	*-40℃ to 85℃*[1]
AP231E-LF	*16 Channels of 16-bit Analog Output*	*-40℃ to 85℃*[1]

Note 1: Applications requiring operating temperatures of 70°C to 85°C will require purchase of AcroPack Heatsink Accessory AP-CC-01 and minimum airflow of 400LFM. For temperatures below 70°C the module will require a minimum airflow of 200LFM

AP-CC-01 AcroPack Conduction Cool Kit (See Appendix for installation instructions)

6.3.2 Other Environmental Requirements

6.3.2.1 Relative Humidity

The range of acceptable relative humidity is 5% to 95% non-condensing.

6.3.2.2 Isolation

The PCIe bus and field commons are non-isolated and have a direct electrical connection.

6.3.3 Vibration and Shock Standards

The AcroPack is designed to pass the following Vibration and Shock standards.

Vibration, Operating: MIL-STD-810G, Method 514.6
Procedure I (General Vibration)
Category 20 (Ground vehicles/ground mobile)
8-500Hz, Sinusoidal 5Grms X, Y and Z axis. 1hr per axis (15 minute sweep up / 15 minute sweep down test duration)
Shock, Operating: MIL-STD-810G, Method 516.6
Procedure I (functional Shock)
50g, 11ms half-sine 3 positive/negative per axis (Total of 18 drops)

6.3.4 EMC Directives

The AcroPack is designed to comply with EMC Directive 2004/108/EC.

- **Immunity per EN 61000-6-2:**
  Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2.
  Radiated Field Immunity (RFI), per IEC 61000-4-3.
  Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4.
  Surge Immunity, per IEC 61000-4-5.
  Conducted RF Immunity (CRFI), per IEC 61000-4-6.
- **Emissions per EN 61000-6-4:**
  Enclosure Port, per CISPR 16.
  Low Voltage AC Mains Port, per CISPR 16.
  Note: This is a Class A product

6.4 Reliability Prediction

AP220-16E

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled, G_BG_C*

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	1,373,772	156.8	727.9
40°C	792,959	90.5	1,261.1

[1] FIT is Failures in 10^9 hours.

AP231-16E

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. Per MIL-HDBK-217, Ground Benign, Controlled, GBGC

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	2,190,883	250.1	456.4
40°C	1,241,382	141.7	805.6

[1] FIT is Failures in 109 hours.

6.5 PCIe Bus Specifications

Compatibility	Conforms to PCI Express Base Specification, Revision 2.1
Line Speed	Gen1 (2.5Gbps) Available through front connector
Lane Operation	1-Lane
4K Memory Space Required	One Base Address Register

Table 6.5 PCIe Bus Data Rates

PCIe Gen 1 (1 lane)	Giga bit / second	Bytes / second
Signaling Rate	2.5 Gb/s	312 Mbyte/s
Ideal Rate[1]	2 Gb/s	250 Mbyte/s
Header Burden plus 4byte Sample Rate[2]	0.332 Gb/s	41.6 Mbyte/s
Actual Measured 4 Byte Read Rate[3]	0.019 Gb/s	2.35 Mbytes/s
Actual Measured DMA 4 Byte Read Rate[4]	0.327 Gb/s	40.9 Mbyte/s
Actual Measured 4 Byte Write Rate[5]	0.320 Gb/s	40 Mbyte/s

Note 1: PCIe x1 Gen 1 = 2.5GT/s (with 10-bit encoding we have a 20% loss in possible throughput due to encoding) giving 2.0 G bits/sec or 250M Bytes/sec.

Note 2: With PCIe we have a header for address and read/write command that is sent with every packet. This header is 20 Bytes with data payload of 4 Bytes (for our typical AcroPack). For each 4 Byte data sample, 24 Bytes are sent.

$\frac{250MByte/s}{24\ Bytes}$ = 10.4 M samples/sec or 41.6 M Bytes/sec or 0.332 G bit/sec

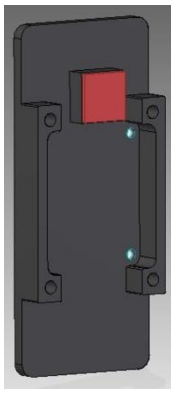
Note 3: For our typical AcroPack have measured back to back 4 Byte read operations completing every 1.7usec. A read operation starts with a host read request. The AcroPack must process the read and fetch the data and then generated the completion back to the host. The host then sends a message back that says I got it. This back and forth hand shaking slows down individual reads.

Note 4: DMA Read of 1024 sample takes 100us. Each sample is 4 Bytes. 100us/1024=0.0977us per sample or 4/0.0977us = 40.94Mbyte/s. We use DMA transfers to improve data transfers on the AP341/2 and AP225/235.

Note 5: Simple write operations are just as fast as DMA read operations. Write data is presented to the AcroPack in one transaction. Measured 4-byte back to back write accesses taking place every 100ns.

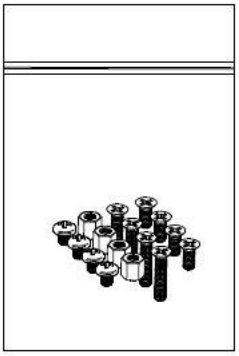
Appendix

AP-CC-01 Heatsink Kit Installation



Bottom view

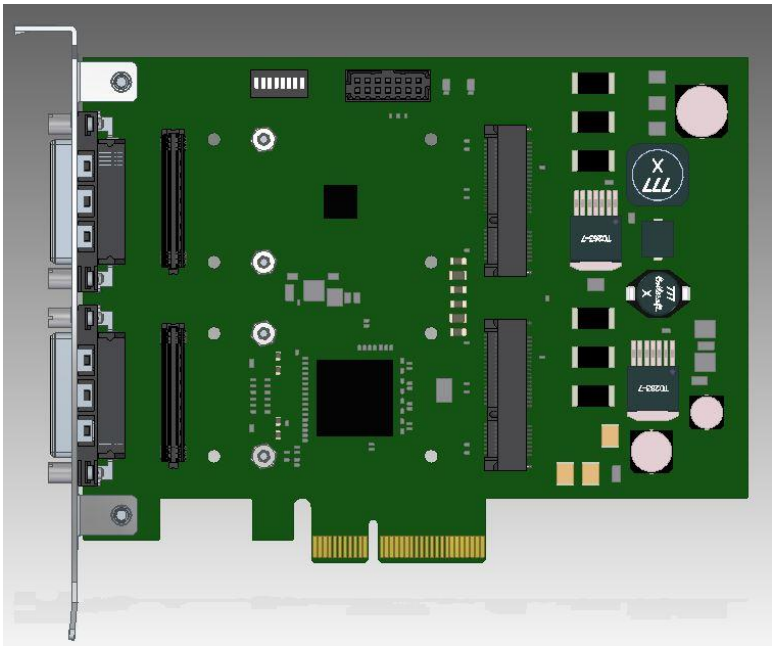
Top view



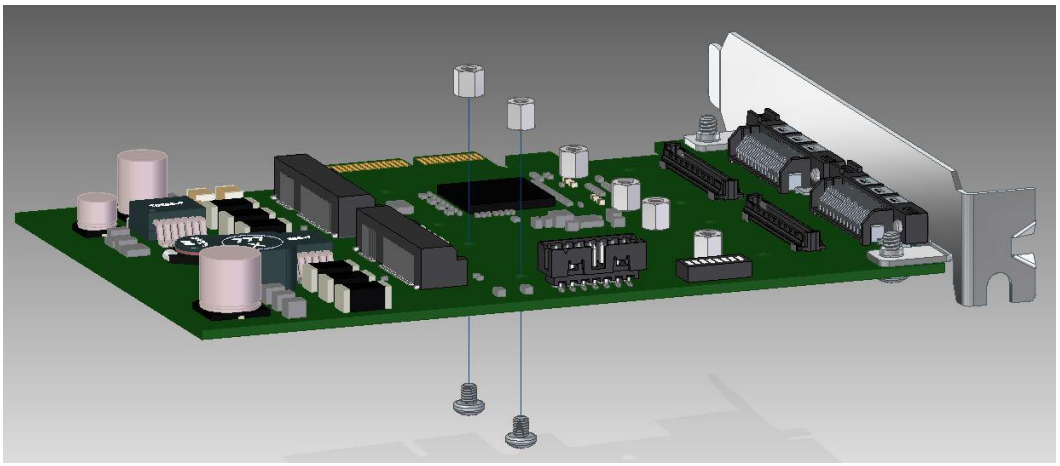
Hardware

AP-CC-01 Heat Sink Kit

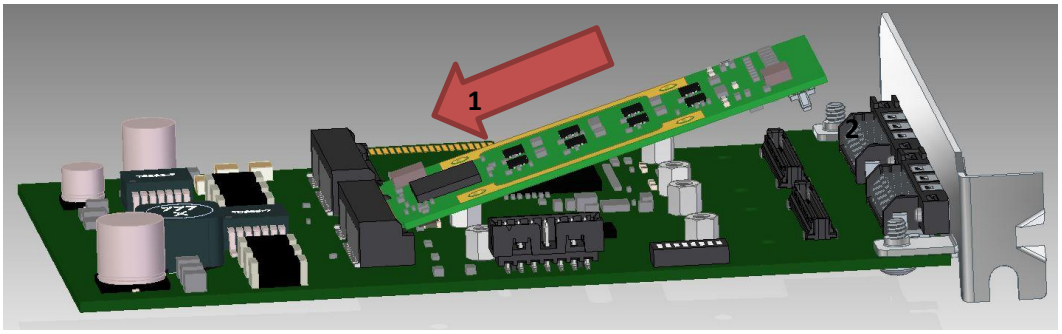
This example will show how to install the AP-CC-01 Heatsink kit with an APCe7020 carrier.



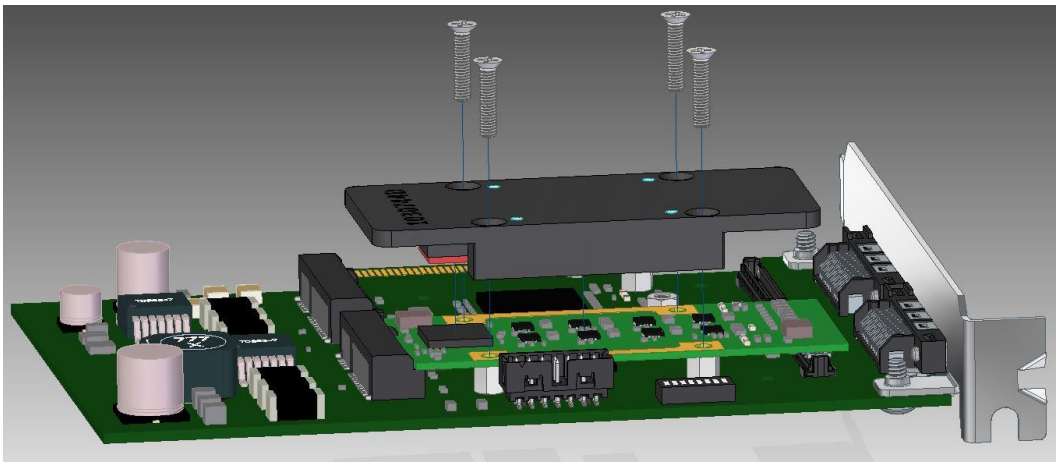
1. Install two standoffs and secure with two screws.



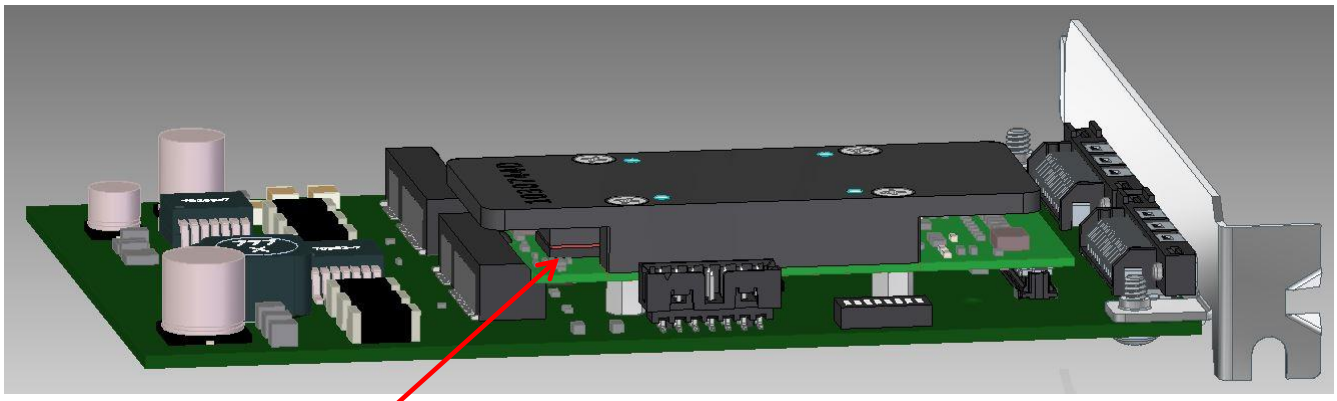
2. Install the AcroPack module.



3. Install the Heatsink and secure with 4 screws.



4. AP-CC-01 Installation is complete.



Note: Make sure the thermal pad is making contact with the FPGA IC.

Certificate of Volatility

Acromag Model AP231E-LF	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) ■ Yes □ No				
Type (SRAM, SDRAM, etc.) Configurable Logic Blocks	Size: 16,640 Logic Cells	User Modifiable ■ Yes □ No	Function: FPGA logic blocks	Process to Sanitize: Power Down
Type (SRAM, SDRAM, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No				
Type(EEPROM, Flash, etc.)	Size: 32 Meg x 1bit	User Modifiable ■ Yes □ No	Function: Data storage for FPGA	Process to Sanitize: Erase using JTAG
Type(EEPROM, Flash, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:

Acromag Representative				
Name:	Title: Sales and Marketing	Email: solutions@acromag.com	Office Phone: 248-295-0310	Office Fax: 248-624-9234

Revision History

The revision history for this document is summarized in the table below.

Release Date	Version	EGR/DOC	Description of Revision
25 MAY 16	Preliminary	PDG/PDG	Preliminary Document Publication
29 JUN 16	A	PDG/ARP	Initial Release
09 MAR 17	B	PDG/ARP	Added module location feature (sec 3.3)
21 Sept 17	C	PDG/ARP	Update the BAR0 Base Address Description (Table 3.2)
16 JAN 2018	D	LMP/ARP	Add Table 6.5 PCIe Bus Data Rates.
03 JULY 2018	E	LMP/ARP	Add 68-pin Champ Connector to Table 2.1
04 DEC 2020	F	ENZ/AMM	Updated MTBF Numbers.
10 MAR 2021	G	LMP/AMM	Removed "50-Pin" in reference to the Front Panel Connector.