ACPS3320 CompactPCI-Serial AcroPack Carrier Board

USER'S MANUAL

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1. GENERAL INFORMATION

Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the AcroPack module.

Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag.

Trademark, Trade Name and Copyright Information

Radio Frequency Interference Statement

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

ACPS3320 Overview

The ACPS3320 is a Compact Peripheral Component Interconnect – Serial (CPCI-S) card and is a carrier for mini-PCIe or AcroPack mezzanine modules. This carrier board provides a modular approach to system assembly, since each carrier can be populated with any combination of analog input/output, digital input/output, communication, etc. AcroPack modules. Thus, the user can create a board which is customized to the application. This saves money and space - a single carrier board populated with AcroPack modules may

replace several dedicated function PCI or PCIe bus boards. The ACPS3320 non-intelligent carrier board provides impressive functionality at low cost.

Model	Input/Output	AcroPack Slots	Operating Temperature Range
ACPS3320	Rear I/O	2 (A, B)	-40 to +85°C (with 200 LFM airflow)

KEY ACPS3320 FEATURES

Interface for AcroPack modules – The ACPS3320 provides an electrical and mechanical interface for up to two industry standard mini-PCIe or AcroPack modules. AcroPack modules are available from Acromag. Mini-PCIe cards are available from other vendors in a wide variety of input/output configurations to meet the needs of varied applications.

PCI Express Version 2.1 Compliant Carrier: - Includes a PCIe switch to allow two PCIe devices (AcroPack or mini-PCIe) to share a single 4HP peripheral board slot in a CPCI-S chassis.

Board Identification – A unique carrier and site number is determined from geographical addressing signals GA0-GA3 from the backplane. This feature provides the capability to distinguish a particular carrier and AcroPack module from others when multiple instances of the same carrier and/or module are used in a system.

JTAG Programming Header – A standard 14-pin Xilinx JTAG programming header is provided for programming and debugging the FPGA on some AcroPack modules. The JTAG ports of the two AcroPack modules are daisy-chained.

Individually Fused Power - Fused +1.5V, +3.3V, +5V, +12V, and -12V DC power is provided. A fuse is present on each supply line serving each AcroPack module. Fuses F1-F3 and F7-F9 are user replaceable. Fuses F4-F6 and F10-F12 are not user replaceable, you must return the board to Acromag to replace these fuses.

Software Support

The AcroPack series products require support drivers specific to your operating system. Supported operating systems include: Linux®, Windows®, and VxWorks®.

Windows®

Acromag provides software products (sold separately) to facilitate the development of Windows® applications interfacing with AcroPack modules. This software (model APSW-API-WIN) consists of low-level drivers and Dynamic Link Libraries (DLLs) that are compatible with a number of programming environments. The DLL functions provide a high-level interface to boards eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

VxWorks®

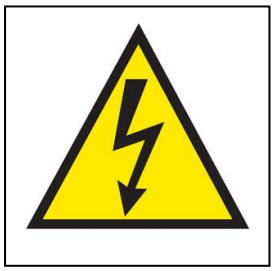
Acromag provides a software product (sold separately) consisting of VxWorks® software. This software (Model APSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of “C” functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

Linux®

Acromag provides a software product consisting of Linux® software. This software (Model APSW-API-LNX) is composed of Linux® libraries for all AcroPack modules, VPX I/O board products, and PCIe I/O Cards. The software is implemented as a library of “C” functions which link with existing user code to make possible simple control of all Acromag AcroPack modules.

2. PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.

WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

WARNING: This AcroPack carrier does not provide isolation between the AcroPack Field I/O signals and the host. It is not intended to be used with isolated AcroPack modules.

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

BOARD CONFIGURATION

Power should be removed from the carrier board when installing AcroPack modules, cables, termination panels, and field wiring.

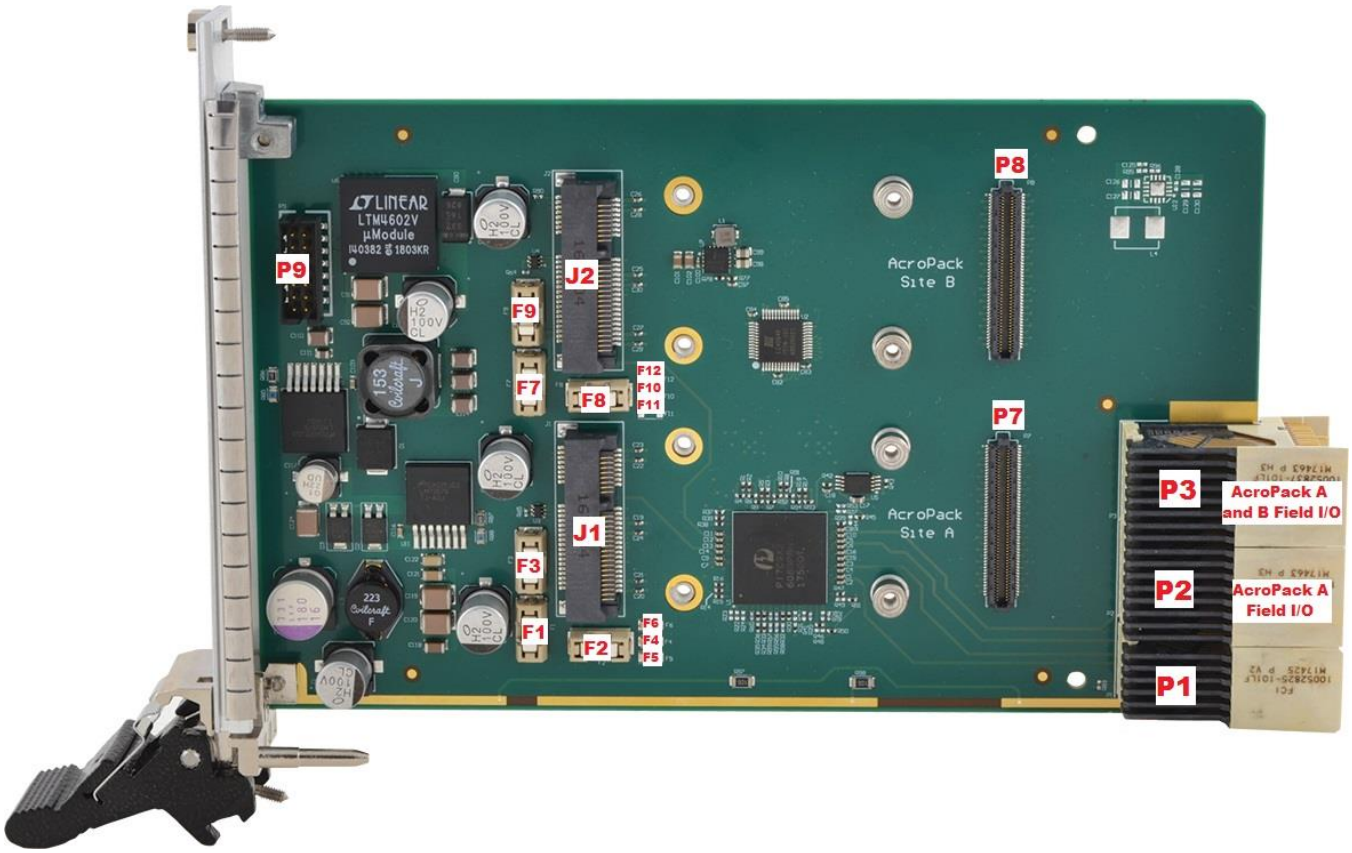


Figure 1 Connector and Fuse Locations

Power and Cooling Considerations

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed AcroPack modules within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The lack of air circulation within some CPCI-S chassis could be a cause for some concern. The dense packing of the AcroPack modules to the carrier board alone results in elevated module and carrier board temperatures, and the restricted air flow within the chassis aggravates this problem. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

Carrier Fuses

CAUTION: Acromag has used pins labeled as reserved in the Mini-PCIe specification for additional power connections. If you are installing a Mini-PCIe card from another manufacturer in slot A remove fuses F1(+12V), F2(+5V) and F3 (-12V). When installing a Mini-PCIe card in from another manufacturer in slot B remove fuses F7(+12V), F8(+5V) and F9 (-12V). Fuse locations are shown in Figure 1.

Other fuses present on the board include +1.5V Fuses F6 (slot A) and F12 (slot B). Also present on the board are +3.3V Fuses F4 (slot A) and F10 (slot B). These fuses are not user replaceable. Return the carrier board to Acromag to replace these fuses. Both Mini-PCIe cards from other manufacturers and the AcroPack modules can use +1.5V and +3.3V power.

Fuses not present on the board include +3.3V Aux Fuses F5 (slot A), F11 (slot B). Some standard Mini PCIe cards may require +3.3V Aux to power the module. For a site using such a module the +3.3V fuse will need to be removed and the +3.3 Aux fuse will need to be installed, along with a regulator to convert +5V standby from the CPCI-S backplane to +3.3V Aux. Return the carrier board to Acromag to remove and install these parts.

ACROPACK MODULE INSTALLATION

Power should be removed from the carrier board when installing AcroPack modules, cables, termination panels, and field wiring. Refer to Figure 2 while reading this section. To install, first insert the edge of the AcroPack module into the carrier connector at an angle similar to that shown in the figure. Next, using a rocking motion while gently applying force to keep the edge of the board against the back of the carrier connector, position the module such that the field I/O connector is just above the mating connector. Verify that the two connectors are properly aligned. Once alignment is achieved, you can fully seat the connector. It will snap into place. Install two M2.5 screws as shown.

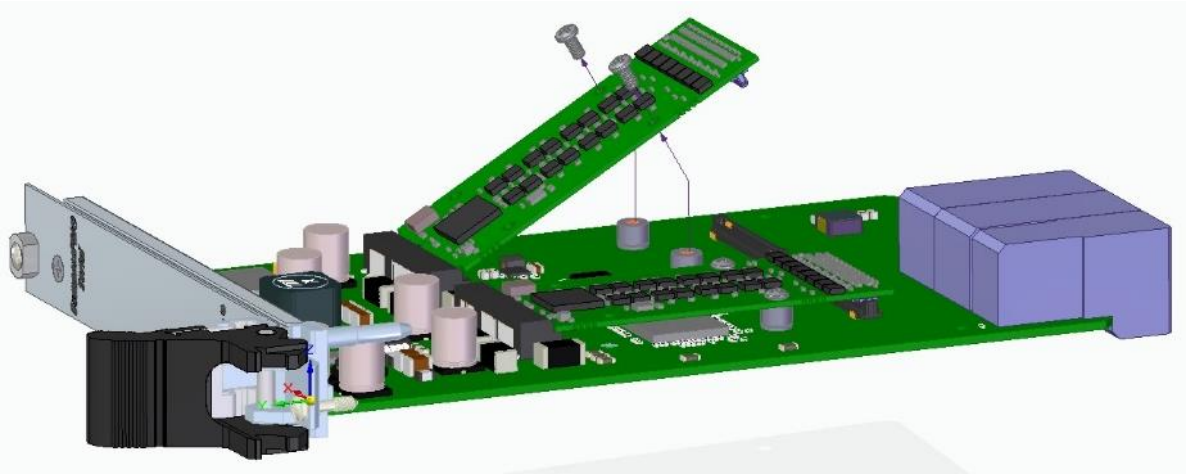


Figure 2 AcroPack Module Installation

FIELD GROUNDING CONSIDERATIONS

This board is non-isolated, since there is electrical continuity between the PCIe bus and AcroPack module grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

CONNECTORS

The ACPS3320 carrier uses two AcroPack module field I/O connectors, two mini-PCIe connectors, and three CompactPCI-Serial backplane connectors. These are discussed in the following sections.

AcroPack Field I/O Connectors

The field side connector of AcroPack modules mate to Samtec SS5-50-3.00-L-D-K-TR socket connectors on the carrier board.

This provides excellent connection integrity due to the gold plating in the mating area. M2.5 screws and spacers provide additional stability for harsh environments.

The functions of each of the Field I/O signals are defined by the installed AcroPack model.

Table 1 Field I/O Pin Assignments

Carrier P7, P8	Module Pin Number	Field I/O Signal
2	2	Field I/O 1
1	1	Field I/O 2
4	4	Reserved/isolation
3	3	Reserved/isolation
6	6	Field I/O 3
5	5	Field I/O 4
8	8	Reserved/isolation
7	7	Reserved/isolation
10	10	Field I/O 5
9	9	Field I/O 6
12	12	Reserved/isolation
11	11	Reserved/isolation
14	14	Field I/O 7
13	13	Field I/O 8
16	16	Reserved/isolation
15	15	Reserved/isolation

Carrier P7, P8	Module Pin Number	Field I/O Signal
18	18	Field I/O 9
17	17	Field I/O 10
20	20	Reserved/isolation
19	19	Reserved/isolation
22	22	Field I/O 11
21	21	Field I/O 12
24	24	Reserved/isolation
23	23	Reserved/isolation
26	26	Field I/O 13
25	25	Field I/O 14
28	28	Reserved/isolation
27	27	Reserved/isolation
30	30	Field I/O 15
29	29	Field I/O 16
32	32	Reserved/isolation
31	31	Reserved/isolation
34	34	Field I/O 17
33	33	Field I/O 18
36	36	Reserved/isolation
35	35	Reserved/isolation
38	38	Field I/O 19
37	37	Field I/O 20
40	40	Reserved/isolation
39	39	Reserved/isolation
42	42	Field I/O 21
41	41	Field I/O 22
44	44	Reserved/isolation
43	43	Reserved/isolation
46	46	Field I/O 23
45	45	Field I/O 24
48	48	Reserved/isolation
47	47	Reserved/isolation
50	50	Field I/O 25
49	49	Field I/O 26
52	52	Reserved/isolation

Carrier P7, P8	Module Pin Number	Field I/O Signal
51	51	Reserved/isolation
54	54	Field I/O 27
53	53	Field I/O 28
56	56	Reserved/isolation
55	55	Reserved/isolation
58	58	Field I/O 29
57	57	Field I/O 30
60	60	Reserved/isolation
59	59	Reserved/isolation
62	62	Field I/O 31
61	61	Field I/O 32
64	64	Reserved/isolation
63	63	Reserved/isolation
66	66	Field I/O 33
65	65	Field I/O 34
68	68	Reserved/isolation
67	67	Reserved/isolation
70	70	Field I/O 35
69	69	Field I/O 36
72	72	Reserved/isolation
71	71	Reserved/isolation
74	74	Field I/O 37
73	73	Field I/O 38
76	76	Reserved/isolation
75	75	Reserved/isolation
78	78	Field I/O 39
77	77	Field I/O 40
80	80	Reserved/isolation
79	79	Reserved/isolation
82	82	Field I/O 41
81	81	Field I/O 42
84	84	Reserved/isolation
83	83	Reserved/isolation
86	86	Field I/O 43
85	85	Field I/O 44

Carrier P7, P8	Module Pin Number	Field I/O Signal
88	88	Reserved/isolation
87	87	Reserved/isolation
90	90	Field I/O 45
89	89	Field I/O 46
92	92	Reserved/isolation
91	91	Reserved/isolation
94	94	Field I/O 47
93	93	Field I/O 48
96	96	Reserved/isolation
95	95	Reserved/isolation
98	98	Field I/O 49
97	97	Field I/O 50
100	100	Reserved/isolation
99	99	Reserved/isolation

Mini-PCIe Connectors

The AcroPack Mini-PCIe connectors mate to TE Connectivity 1759457-1 connectors on the carrier board. AcroPack locations are labeled on the board for easy identification.

Pin assignments for these connectors are based on the Mini-PCIe specification with the exceptions noted in Table 2.

Table 2 Mini-PCIe Connectors J1 and J2 Pin Assignments

Pin #	Name	Pin #	Name
51	**+5V**[3]	52	+3.3V[4]
49	**+12V**[3]	50	GND
47	**-12V**[3]	48	+1.5V
45	**Present**	46	N.C. (LED_WPAN#)[1]
43	GND	44	N.C. (LED_WLAN#)[1]
41	+3.3V[4]	42	N.C. (LED_WWAN#)[1]
39	+3.3V[4]	40	GND
37	GND	38	USB_D+[6]
35	GND	36	USB_D-[6]
33	PETp0	34	GND
31	PETn0	32	SMB_DATA[5]
29	GND	30	SMB_CLK[5]
27	GND	28	+1.5V
25	PERp0	26	GND
23	PERn0	24	+3.3V[4]
21	GND	22	PERST#
19	**TDI** (UIM_C4)[1,2]	20	N.C. (W_DISABLE#)[1]
17	**TDO** (UIM_C8)[1,2]	18	GND
15	GND	16	UIM_VPP[1]
13	RECLK+	14	UIM_RESET[1]
11	REFCLK-	12	UIM_CLK[1]
9	GND	10	UIM_DATA[1]
7	CLKREQ#	8	UIM_PWR[1]
5	**TCK** (COEX2)[1]	6	+1.5V
3	**TMS** (COEX1)[1]	4	GND
1	N.C. (WAKE#)[1]	2	+3.3V[4]

Notes:

1. The following mini-PCIe signals are not supported: WAKE#, LED_WPAN#, LED_WLAN#, LED_WWAN#, W_DISABLE#, COEX1, COEX2, UIM_C4, UIM_C8, UIM_VPP, UIM_RESET, UIM_CLK, UIM_DATA, UIM_PWR.
2. TDI is tied to TDO on modules that do not use JTAG.
3. +5, +12, and -12 Volt power supplies have been assigned to pins that are reserved in the mini-PCIe specification. Remove the fuses on these power supplies for mini-PCIe cards from other vendors that cannot tolerate power applied to these reserved pins.
4. All +3.3Vaux power pins are changed to system +3.3V power.
5. The SM bus signals SMB_CLK and SMB_DATA are used to communicate with a CPLD on the carrier that reports slot ID. These signals will be under the control of the AcroPack module.
6. USB_D+ and USB_D- is N.C. on AcroPack/mini-PCIe site A and connected to CPCI-S connector P1 to support USB-based mPCIe cards in AcroPack/mini-PCIe site B.

CompactPCI-Serial Backplane Connections

Table 4 indicates the pin assignments for the CPCI-S signals on the backplane connector P1.

Refer to the PICMG CPCI-S specification for additional information on the CPCI-S signals.

Table 3 CPCI-S P1 CONNECTIONS

Pin	A	B	C
01	+12V	STANDBY	GND
02	GND	I^2C_SCL	I^2C_SDA
03	***1_USB3_Tx+***	***1_USB3_Tx-***	GA0
04	GND	1_USB2+	1_USB2-
05	1_PE_Tx00+	1_PE_Tx00-	GND
06	GND	1_PE_Tx02+	1_PE_Tx02-
	D	**E**	**F**
01	+12V	+12V	GND
02	GND	reserved	reserved
03	***1_USB3_Rx+***	***1_USB3_Rx-***	GA1
04	GND	PE_CLKIN+	PE_CLKIN-
05	1_PE_Rx00+	1_PE_Rx00-	GND
06	GND	1_PE_Rx02+	1_PE_Rx02-
	G	**H**	**I**
01	+12V	+12V	GND
02	GND	RST#	WAKE_OUT#
03	***SATA_SDI***	***SATA_SDO***	GA2
04	GND	***1_SATA_Tx+***	***1_SATA_Tx-***
05	1_PE_Tx01+	1_PE_Tx01-	GND
06	GND	1_PE_Tx03+	1_PE_Tx03-
	J	**K**	**L**
01	+12V	+12V	GND
02	GND	PCIE_EN#	SYSEN#
03	***SATA_SCL***	***SATA_SL***	GA3
04	GND	***1_SATA_Rx+***	***1_SATA_Rx-***
05	1_PE_Rx01+	1_PE_Rx01-	GND
06	GND	1_PE_Rx03+	1_PE_Rx03-

Notes (Table 3):

1. Hash (#) is used to indicate an active-low signal.
2. BOLD ITALIC Logic Lines are NOT USED by the carrier board.

The ACPS3320 field I/O connections are made through the CPCI-S rear backplane connectors P2 and P3. Tables 5 and 6 indicate the pin assignments for P2 and P3.

Table 5 CPCI-S P2 CONNECTIONS

Pin	A	B	C
01	N.C.[1]	N.C.[1]	GND
02	GND	N.C.[1]	N.C.[1]
03	Site A Field I/O 49	Site A Field I/O 50	GND
04	GND	Site A Field I/O 41	Site A Field I/O 42
05	Site A Field I/O 33	Site A Field I/O 34	GND
06	GND	Site A Field I/O 25	Site A Field I/O 26
07	Site A Field I/O 17	Site A Field I/O 18	GND
08	GND	Site A Field I/O 9	Site A Field I/O 10
	D	**E**	**F**
01	N.C.[1]	N.C.[1]	GND
02	GND	N.C.[1]	N.C.[1]
03	Site A Field I/O 47	Site A Field I/O 48	GND
04	GND	Site A Field I/O 39	Site A Field I/O 40
05	Site A Field I/O 31	Site A Field I/O 32	GND
06	GND	Site A Field I/O 23	Site A Field I/O 24
07	Site A Field I/O 15	Site A Field I/O 16	GND
08	GND	Site A Field I/O 7	Site A Field I/O 8
	G	**H**	**I**
01	N.C.[1]	N.C.[1]	GND
02	GND	N.C.[1]	N.C.[1]
03	Site A Field I/O 45	Site A Field I/O 46	GND
04	GND	Site A Field I/O 37	Site A Field I/O 38
05	Site A Field I/O 29	Site A Field I/O 30	GND
06	GND	Site A Field I/O 21	Site A Field I/O 22
07	Site A Field I/O 13	Site A Field I/O 14	GND
08	GND	Site A Field I/O 5	Site A Field I/O 6
	J	**K**	**L**
01	N.C.[1]	N.C.[1]	GND
02	GND	N.C.[1]	N.C.[1]
03	Site A Field I/O 43	Site A Field I/O 44	GND
04	GND	Site A Field I/O 35	Site A Field I/O 36
05	Site A Field I/O 27	Site A Field I/O 28	GND
06	GND	Site A Field I/O 19	Site A Field I/O 20
07	Site A Field I/O 11	Site A Field I/O 12	GND
08	GND	Site A Field I/O 3	Site A Field I/O 4

Notes (Table 5):

1. N.C. – not connected

Table 6 CPCI-S P3 CONNECTIONS

Pin	A	B	C
01	Site A Field I/O 2	Site A Field I/O 1	GND
02	GND	N.C.[1]	N.C.[1]
03	Site B Field I/O 41	Site B Field I/O 42	GND
04	GND	Site B Field I/O 33	Site B Field I/O 34
05	Site B Field I/O 25	Site B Field I/O 26	GND
06	GND	Site B Field I/O 17	Site B Field I/O 18
07	Site B Field I/O 9	Site B Field I/O 10	GND
08	GND	Site B Field I/O 1	Site B Field I/O 2
	D	**E**	**F**
01	N.C.[1]	N.C.[1]	GND
02	GND	N.C.[1]	N.C.[1]
03	Site B Field I/O 43	Site B Field I/O 44	GND
04	GND	Site B Field I/O 35	Site B Field I/O 36
05	Site B Field I/O 27	Site B Field I/O 28	GND
06	GND	Site B Field I/O 19	Site B Field I/O 20
07	Site B Field I/O 11	Site B Field I/O 12	GND
08	GND	Site B Field I/O 3	Site B Field I/O 4
	G	**H**	**I**
01	N.C.[1]	N.C.[1]	GND
02	GND	N.C.[1]	N.C.[1]
03	Site B Field I/O 45	Site B Field I/O 46	GND
04	GND	Site B Field I/O 37	Site B Field I/O 38
05	Site B Field I/O 29	Site B Field I/O 30	GND
06	GND	Site B Field I/O 21	Site B Field I/O 22
07	Site B Field I/O 13	Site B Field I/O 14	GND
08	GND	Site B Field I/O 5	Site B Field I/O 6
	J	**K**	**L**
01	N.C.[1]	N.C.[1]	GND
02	GND	Site B Field I/O 49	Site B Field I/O 50
03	Site B Field I/O 47	Site B Field I/O 48	GND
04	GND	Site B Field I/O 39	Site B Field I/O 40
05	Site B Field I/O 31	Site B Field I/O 32	GND
06	GND	Site B Field I/O 23	Site B Field I/O 24
07	Site B Field I/O 15	Site B Field I/O 16	GND
08	GND	Site B Field I/O 7	Site B Field I/O 8

Notes (Table 6):

1. N.C. – not connected

JTAG Programming/Debug Connector

A JTAG programming/debug connector is provided for developing applications that use Acromag's FPGA AcroPack modules. See reference designator P9 in

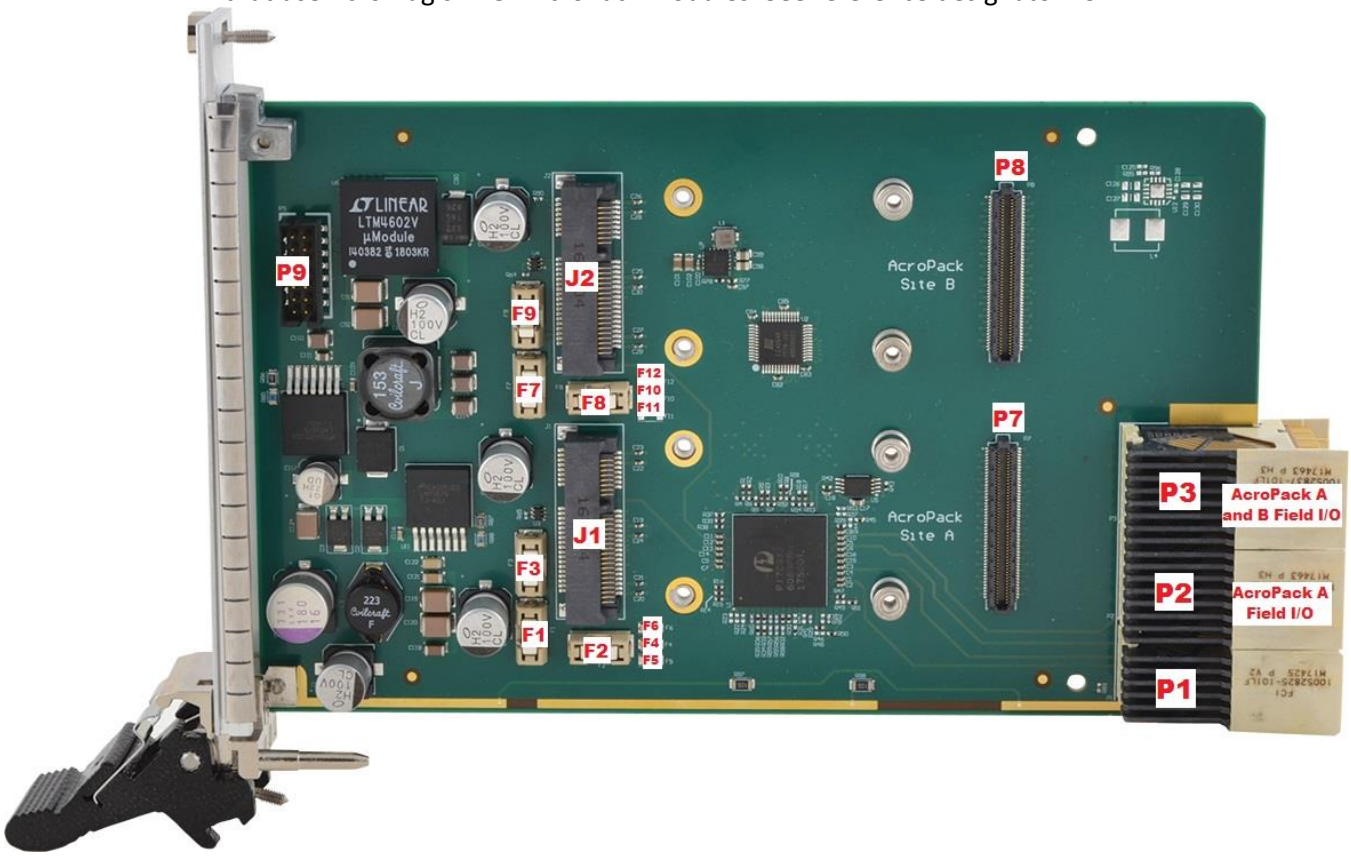


Figure 1. This is a standard 14-pin Xilinx programming header for connecting a Xilinx Platform USB II programming device (or equivalent). The pin assignment for P9 is shown in 7. A bypass circuit is included that will detect a vacant AcroPack site and close a switch to bypass the TDI and TDO signals. A CPLD on the carrier is included in the JTAG chain. The Xilinx Vivado tools can detect the presence of the CPLD in the JTAG chain and skip it when accessing the FPGAs on the AcroPack modules.

Table 7 JTAG Programming/Debug Connector Pin Assignment

Signal	Pin	Pin	Signal
N.C.[1]	1	2	_+3.3V
GND	3	4	TMS
GND	5	6	TCK
GND	7	8	TDO
GND	9	10	TDI
GND	11	12	N.C.[1]
N.C.[1]	13	14	N.C.[1]

Notes (Table 7):

1. N.C. – not connected

TMS – **JTAG Test Mode Select**. This pin is the JTAG mode signal establishing appropriate TAP state transitions for target ISP devices sharing the same data stream.

TCK – **JTAG Test Clock**. This pin is the clock signal for JTAG operations and should be connected to the TCK pin on all target ISP devices sharing the same data stream.

TDO – **JTAG Test Data Out**. This pin is the serial data stream received from the TDO pin on the last device in a JTAG chain.

TDI – **JTAG Test Data In**. This pin outputs the serial data stream transmitted to the TDI pin on the first device in a JTAG chain.

+3.3V – The target reference voltage V_{REF} is 3.3 Volts

GND – Ground.

3. THEORY OF OPERATION

This section describes the functionality of the circuitry used on the carrier board. Refer to Figure 3 as you read this section.

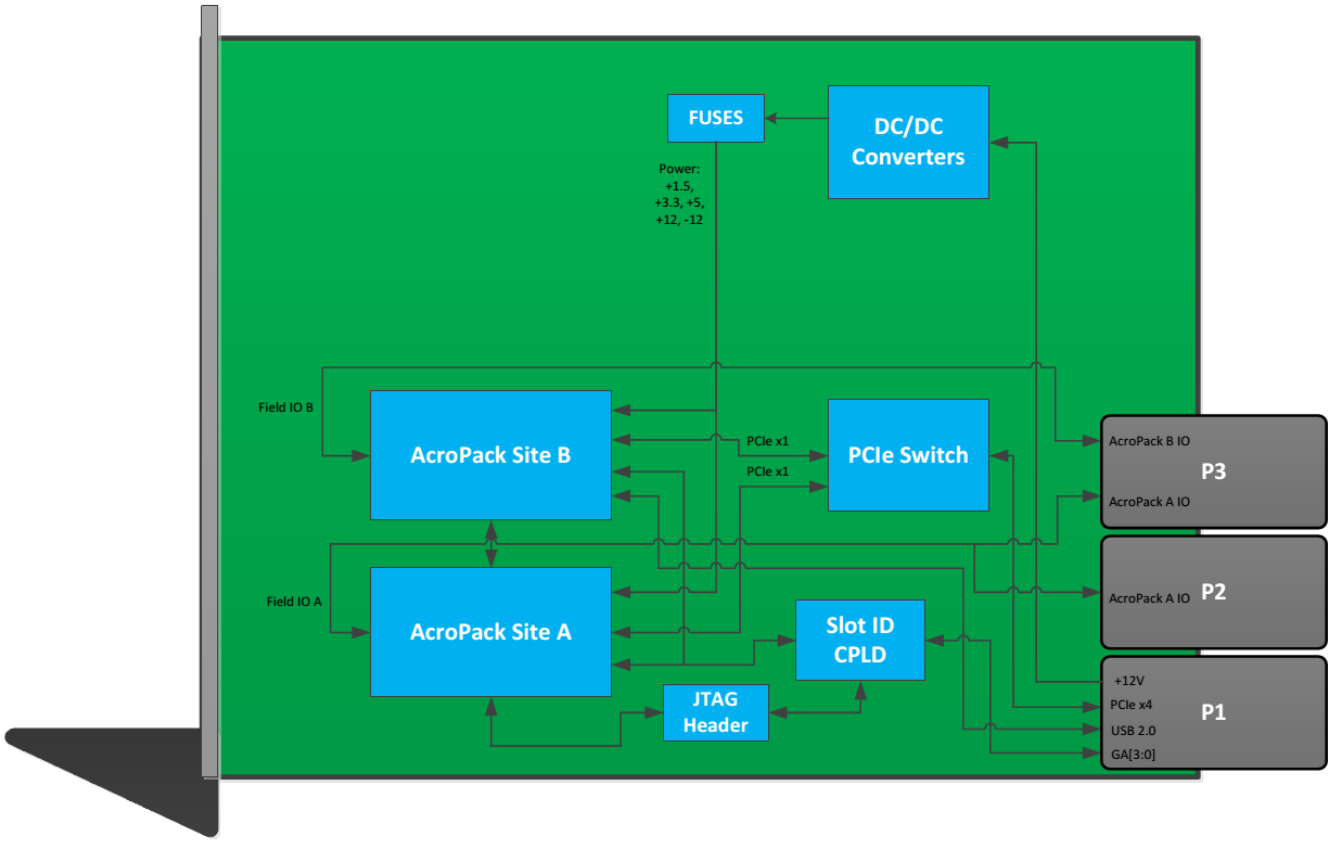


Figure 3 ACPS3320 AcroPack Carrier Block Diagram

PCIe Switch

The PCIe switch is a 6 port 8 lane PCIe Gen 2 switch. It expands the single host PCIe port to two ports, one for each AcroPack site. The host port consists of four PCIe lanes or one PCIe lane (depending on CPCI-S slot), each of the AcroPack sites have one lane each.

Important Note: The ACPS3320 board is not hot-swappable.

DC/DC Converter

The ACPS3320 has four DC/DC converters to provide the power supply voltages to the AcroPack modules that are not present on the CPCI-S backplane. The +3.3 Volt, +5 Volt and -12 Volt supplies are sourced from +12 Volt power. The +1.5 Volt supply is sourced from the +3.3 Volt supply. Also, if the regulator is populated, +5V standby from the backplane will be converted to +3.3V Aux. This part is not populated by default.

Slot Addressing

The ACPS3320 carrier unique slot address is dependent upon the geographical addressing signals (GA0-GA3) from the backplane. The slot address is 5 bits long and consists of 1 bit to identify the site on the carrier where the AcroPack modules is installed and 4 bits that are determined by the GA signals. The CPLD will serialize the slot address and transmit the address to the AcroPack module as requested by the AcroPack module. The process of reading the slot address is typically initiated by host software.

JTAG

A JTAG interface is provided for programming and debugging FPGAs on AcroPack modules. It is intended to be used with a Xilinx Platform USB II programming device. A bypass circuit is included that will detect a vacant AcroPack site and close a switch to complete the JTAG chain. When two AcroPack modules with Xilinx FPGAs are installed on the carrier the module in slot B appears first in the chain followed by the module in slot A. The slot address CPLD is also included in the JTAG chain for factory programming.

Power Supply Fuses

The power supplies to each AcroPack module are individually fused. A blown fuse can be identified by visible inspection or by use of an ohm meter. The

fuse locations are shown in

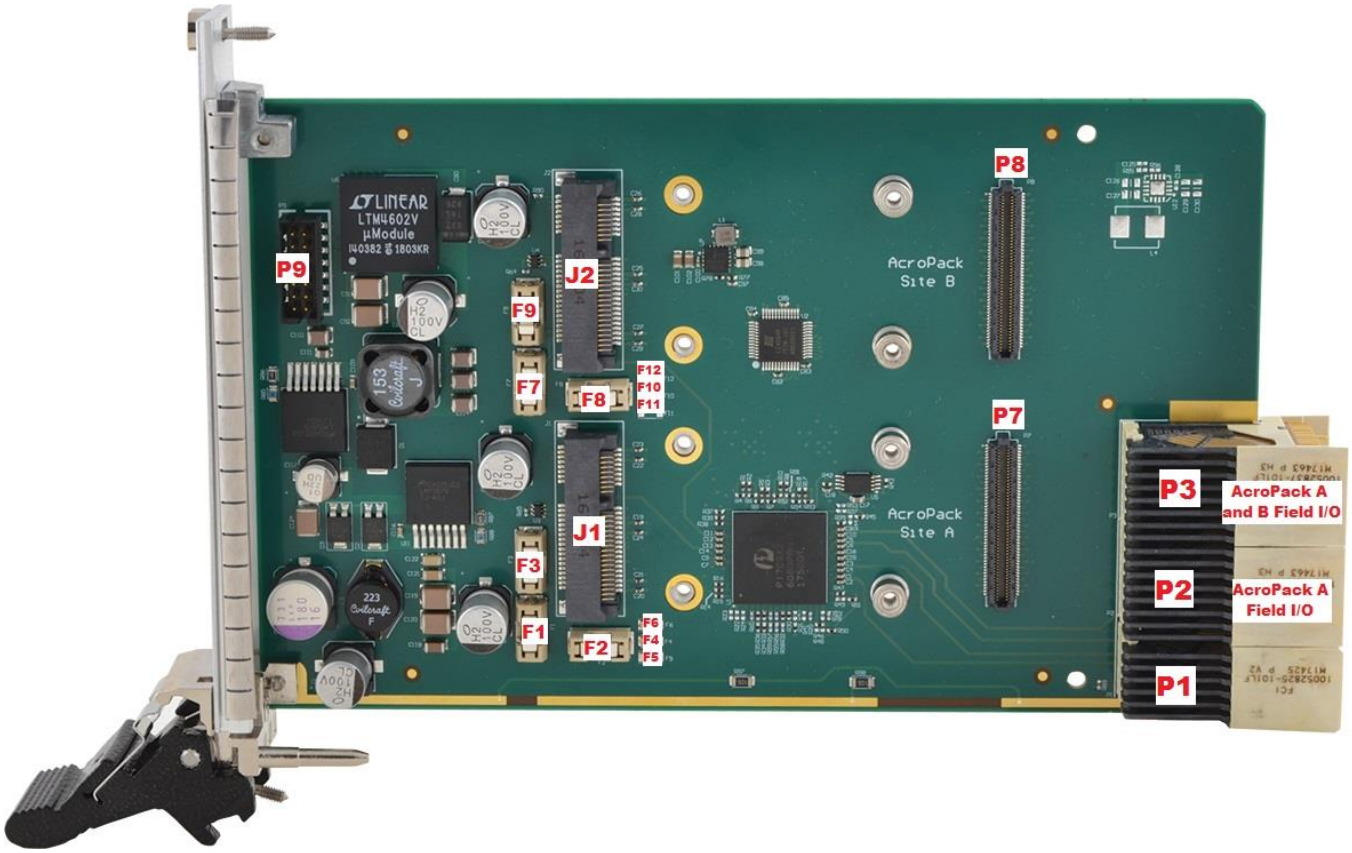


Figure 1. The current rating for each of the fuses is listed in the Fuses paragraph in section 5.

4. SERVICE AND REPAIR

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all the procedures in Section 2, Preparation for Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag website at https://www.acromag.com/. Our website contains the most up-to-date product and software information.

Go to the “Support” tab or your specific AcroPack model ordering page.

Acromag’s application engineers can also be contacted directly for technical assistance via email, telephone, or FAX through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the “Contact Us” tab. When needed, complete repair services are also available.

Phone: 248-295-0310
Email: solutions@acromag.com

5. SPECIFICATIONS

PHYSICAL

Physical Configuration

Length (ACPS3320) .....6.299 inches (160.00 mm)
Height.....3.937 inches (100.00 mm)
Board thickness.....0.063 inches (1.60 mm)
Max component height .....0.402 inches (10.21 mm)
Max component height under AcroPack modules
0.0789 inches (2.00 mm)
Weight.....5.75 oz. (163 g)

Connectors

P1 (CPCI-S) .....72-pin header, AIRMAX (Amphenol 10052825-101LF)
P2, P3 (CPCI-S).....96-pin header, AIRMAX (Amphenol 10052837-101LF)
P7, 8 (AcroPack Field I/O) .....100-pin socket (Samtec SS5-50-3.00-L-D-K-TR)
J1, 2 (Mini-PCIe).....52-pin socket (TE Connectivity 1759457-1)
P9 (JTAG).....14-pin header (Molex 87832-1420)

Isolation

This AcroPack carrier does not provide isolation between the AcroPack Field I/O signals and the host. It is not intended to be used with isolated AcroPack modules.

Power

Board power requirements are a function of the installed AcroPack modules. This specification below lists current specified is for the ACPS3320 carrier board only.

+12 Volts (±8 %) 0.292A Typical

Add the current for each of the AcroPack modules to calculate the total current required from each supply. The carrier is designed to provide the following voltage and currents to each AcroPack module.

Supply Voltage	Current (Max)
+12V +/- 8% (max)	0.5 A
-12V +/- 8% (max)	0.5 A
+5V +/- 5% (max)	0.5 A
+3.3V +/- 5% (max)	1.1 A
+1.5V +/- 5% (max)	0.5 A
+3.3Vaux +/- 9% (max)	100mA

The carrier board provides +1.5V, +3.3V, +5V, +12V and -12V power to each AcroPack module. The ACPC3310 utilizes DC/DC converters to generate the +1.5V, +3.3V, +5V and -12V supplies from the +12V on the CPCI-S backplane. An additional regulator and fuse can be populated to supply +3.3Vaux from the +5V standby on the CPCI-S backplane.

Fuses

+1.5 .....1.1 Amps (F5, F10) Raychem NANOSMDC110F-2
+3.3V..... 3 Amps (F4, F9) Littelfuse 0466003.NR
+5V, +12V, -12V ..... 2 Amps (F1, F2, F3, F6, F7, F8) Littelfuse 0453002.MR

CPCI-S COMPLIANCE

Specification.....This device meets or exceeds all written CompactPCI Serial specifications per revision 2.0. (PICMG CPCI-S.0 R2.0)

ENVIRONMENTAL

Operating Temperature.....-40 to +85°C (with 200 LFM airflow)
Relative Humidity.....5-95% non-condensing
Storage Temperature.....-55 to +125°C.

EMC Compliance

The ACPS3320 complies with EMC Directive 2004/108/EC.
Immunity.....per EN 61000-6-2
Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2
Radiated Field Immunity (RFI), per IEC 61000-4-3
Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4
Surge Immunity, per IEC 61000-4-5
Conducted RF Immunity (CRFI), per IEC 61000-4-6
Emissions .....per EN61000-6-4
Enclosure Port, per CISPR 16
Low Voltage AC Mains Port, per CISPR 16
Note: This is a Class A product

Vibration and Shock Standard

The ACPS3320 is designed to pass the following Vibration and Shock standards.
Vibration, Sinusoidal Operating.....Designed to comply with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis
Vibration, Random Operating.....Designed to comply with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis
Shock, Operating.....Designed to comply with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3ms half sine, 18 shocks at 6 orientations for both test levels

Reliability Prediction

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled, G_BG_C*

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	1,930,688	220.4	518.0
40°C	1,191,422	136.0	839.3

[1] FIT is Failures in 10^9 hours.

6. CERTIFICATE OF VOLATILITY

<table>
<tr><th colspan="6">Certificate of Volatility</th></tr>
<tr><td colspan="2">Acromag Model
ACPS3320</td><td colspan="4">Manufacturer:
Acromag, Inc.
30765 Wixom Rd
Wixom, MI 48393</td></tr>
<tr><th colspan="6">Volatile Memory</th></tr>
<tr><td colspan="6">Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed)
□ Yes ■ No</td></tr>
<tr><th colspan="6">Non-Volatile Memory</th></tr>
<tr><td colspan="6">Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed)
■ Yes □ No</td></tr>
<tr><td>Type (EEPROM, FLASH etc.)

FLASH</td><td>Size:

1 Mbit</td><td>User Modifiable
Yes</td><td>Function:

PCIe switch configuration</td><td colspan="2">Process to Sanitize:

Overwrite FLASH contents.</td></tr>
<tr><th colspan="6">Acromag Representative</th></tr>
<tr><td>Name:
Russ Nieves</td><td colspan="2">Title:
Director of Sales and Marketing</td><td>Email:
rnieves@acromag.com</td><td>Office Phone:
248-295-0838</td><td>Office Fax:
248-624-9234</td></tr>
</table>

7. ACPS3320-RTM Rear Transition Accessory Module

The optional ACPS3320-RTM module may be installed into the slot directly behind the ACPS3320 to easily access AcroPack Field I/O on the ACPS3320's P2 and P3 connectors. The I/O is routed to one 68 pin dual stack 0.8mm Champ connector mounted on the front panel of the ACPS3320-RTM. The AcroPack module identifier is marker on the front panel for easy identification. Cables and termination panels (or user defined terminations) can be quickly mated to the field I/O connectors. Pin assignments are defined by the installed AcroPack module. Refer to Figure 4 for a block diagram.

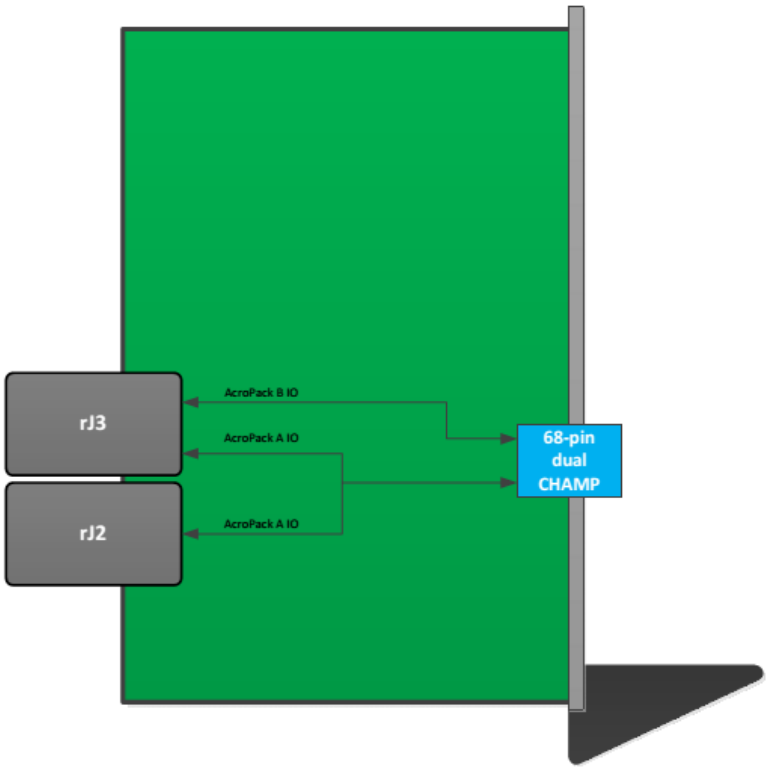


Figure 4 ACPS3320-RTM Block Diagram

7.1 Ordering Information

Model	Operating Temperature Range
ACPS3320-RTM	-40 to +85°C

SIGNAL INTERFACE PRODUCTS

Cable

Model 5028-420 Round cable, shielded, 34 twisted pairs, male SCSI-3 connector to 68-pin CHAMP 0.8mm, 2 meters long.

Model 5028-615 Cable, 68-pin CHAMP to pigtail, 36 inches long.

Model 5028-616 Cable, 68-pin CHAMP to pigtail, 70 inches long.

Termination Panel

Model 5025-288 DIN-rail mountable panel provides 68 screw terminals for universal field I/O termination, SCSI-3 connector.

7.2 Specifications

Physical Configuration

Length (ACPS3320-RTM).....3.150 inches (80.00 mm)
Height.....3.937 inches (100.00 mm)
Board thickness.....0.063 inches (1.60 mm)
Max component height .....0.402 inches (10.21 mm)
Weight.....3.63 oz. (103 g)

Connectors

7.2.1 rJ2 CPCI-S Connector

This connector is a 72-position Type H AirMax receptacle (10114633-101LF) specified by CPCI-S standard. The pinout is as shown in the table below.

Pin	A	B	C
01	Site A Field I/O 49	Site A Field I/O 50	GND
02	GND	Site A Field I/O 41	Site A Field I/O 42
03	Site A Field I/O 33	Site A Field I/O 34	GND
04	GND	Site A Field I/O 25	Site A Field I/O 26
05	Site A Field I/O 17	Site A Field I/O 18	GND
06	GND	Site A Field I/O 9	Site A Field I/O 10
	D	**E**	**F**
01	Site A Field I/O 47	Site A Field I/O 48	GND
02	GND	Site A Field I/O 39	Site A Field I/O 40
03	Site A Field I/O 31	Site A Field I/O 32	GND
04	GND	Site A Field I/O 23	Site A Field I/O 24
05	Site A Field I/O 15	Site A Field I/O 16	GND
06	GND	Site A Field I/O 7	Site A Field I/O 8
	G	**H**	**I**
01	Site A Field I/O 45	Site A Field I/O 46	GND
02	GND	Site A Field I/O 37	Site A Field I/O 38
03	Site A Field I/O 29	Site A Field I/O 30	GND
04	GND	Site A Field I/O 21	Site A Field I/O 22
05	Site A Field I/O 13	Site A Field I/O 14	GND
06	GND	Site A Field I/O 5	Site A Field I/O 6
	J	**K**	**L**
01	Site A Field I/O 43	Site A Field I/O 44	GND
02	GND	Site A Field I/O 35	Site A Field I/O 36
03	Site A Field I/O 27	Site A Field I/O 28	GND

Pin	A	B	C
04	GND	Site A Field I/O 19	Site A Field I/O 20
05	Site A Field I/O 11	Site A Field I/O 12	GND
06	GND	Site A Field I/O 3	Site A Field I/O 4

7.2.2 rJ3 CPCI-S Connector

This connector is a 96-position Type G AirMax receptacle (10060905-101LF) specified by CPCI-S standard. The pinout is as shown in the table below.

Pin	A	B	C
01	Site A Field I/O 2	Site A Field I/O 1	GND
02	GND	N.C.[1]	N.C.[1]
03	Site B Field I/O 41	Site B Field I/O 42	GND
04	GND	Site B Field I/O 33	Site B Field I/O 34
05	Site B Field I/O 25	Site B Field I/O 26	GND
06	GND	Site B Field I/O 17	Site B Field I/O 18
07	Site B Field I/O 9	Site B Field I/O 10	GND
08	GND	Site B Field I/O 1	Site B Field I/O 2
	D	**E**	**F**
01	N.C.[1]	N.C.[1]	GND
02	GND	N.C.[1]	N.C.[1]
03	Site B Field I/O 43	Site B Field I/O 44	GND
04	GND	Site B Field I/O 35	Site B Field I/O 36
05	Site B Field I/O 27	Site B Field I/O 28	GND
06	GND	Site B Field I/O 19	Site B Field I/O 20
07	Site B Field I/O 11	Site B Field I/O 12	GND
08	GND	Site B Field I/O 3	Site B Field I/O 4
	G	**H**	**I**
01	N.C.[1]	N.C.[1]	GND
02	GND	N.C.[1]	N.C.[1]
03	Site B Field I/O 45	Site B Field I/O 46	GND
04	GND	Site B Field I/O 37	Site B Field I/O 38
05	Site B Field I/O 29	Site B Field I/O 30	GND
06	GND	Site B Field I/O 21	Site B Field I/O 22
07	Site B Field I/O 13	Site B Field I/O 14	GND
08	GND	Site B Field I/O 5	Site B Field I/O 6
	J	**K**	**L**
01	N.C.[1]	N.C.[1]	GND
02	GND	Site B Field I/O 49	Site B Field I/O 50
03	Site B Field I/O 47	Site B Field I/O 48	GND
04	GND	Site B Field I/O 39	Site B Field I/O 40

Pin	A	B	C
05	Site B Field I/O 31	Site B Field I/O 32	GND
06	GND	Site B Field I/O 23	Site B Field I/O 24
07	Site B Field I/O 15	Site B Field I/O 16	GND
08	GND	Site B Field I/O 7	Site B Field I/O 8

1. N.C. – not connected

7.2.3 J1 Field I/O Connector

This connector is a 68-pin dual stack 0.8mm Champ cable connector which is mounted on the front panel of the ACPS3320-RTM. The pinout is as follows in the table below.

J1 and Termination Panel	AcroPack Field I/O Signal
1	Field I/O 1
35	Field I/O 2
	Reserved/isolation
	Reserved/isolation
2	Field I/O 3
36	Field I/O 4
	Reserved/isolation
	Reserved/isolation
3	Field I/O 5
37	Field I/O 6
	Reserved/isolation
	Reserved/isolation
4	Field I/O 7
38	Field I/O 8
	Reserved/isolation
	Reserved/isolation
5	Field I/O 9
39	Field I/O 10
	Reserved/isolation
	Reserved/isolation
6	Field I/O 11
40	Field I/O 12
	Reserved/isolation
	Reserved/isolation
7	Field I/O 13
41	Field I/O 14
	Reserved/isolation

J1 and Termination Panel	AcroPack Field I/O Signal
	Reserved/isolation
8	Field I/O 15
42	Field I/O 16
	Reserved/isolation
	Reserved/isolation
9	Field I/O 17
43	Field I/O 18
	Reserved/isolation
	Reserved/isolation
10	Field I/O 19
44	Field I/O 20
	Reserved/isolation
	Reserved/isolation
11	Field I/O 21
45	Field I/O 22
	Reserved/isolation
	Reserved/isolation
12	Field I/O 23
46	Field I/O 24
	Reserved/isolation
	Reserved/isolation
13	Field I/O 25
47	Field I/O 26
	Reserved/isolation
	Reserved/isolation
14	Field I/O 27
48	Field I/O 28
	Reserved/isolation
	Reserved/isolation
15	Field I/O 29
49	Field I/O 30
	Reserved/isolation
	Reserved/isolation
16	Field I/O 31
50	Field I/O 32
	Reserved/isolation

J1 and Termination Panel	AcroPack Field I/O Signal
	Reserved/isolation
17	Field I/O 33
51	Field I/O 34
	Reserved/isolation
	Reserved/isolation
18	Field I/O 35
52	Field I/O 36
	Reserved/isolation
	Reserved/isolation
19	Field I/O 37
53	Field I/O 38
	Reserved/isolation
	Reserved/isolation
20	Field I/O 39
54	Field I/O 40
	Reserved/isolation
	Reserved/isolation
21	Field I/O 41
55	Field I/O 42
	Reserved/isolation
	Reserved/isolation
22	Field I/O 43
56	Field I/O 44
	Reserved/isolation
	Reserved/isolation
23	Field I/O 45
57	Field I/O 46
	Reserved/isolation
	Reserved/isolation
24	Field I/O 47
58	Field I/O 48
	Reserved/isolation
	Reserved/isolation
25	Field I/O 49
59	Field I/O 50
	Reserved/isolation

J1 and Termination Panel	AcroPack Field I/O Signal
	Reserved/isolation

Isolation

This rear-transition module does not provide isolation between the AcroPack Field I/O signals and the host. It is not intended to be used with isolated AcroPack modules.

CPCI-S Compliance

Specification.....This device meets or exceeds all written CompactPCI Serial specifications per revision 2.0. (PICMG CPCI-S.0 R2.0)

ENVIRONMENTAL

Operating Temperature.....-40 to +85°C (with 200 LFM airflow)
Relative Humidity.....5-95% non-condensing
Storage Temperature.....-55 to +125°C.

EMC Compliance

The ACPS3320-RTM complies with EMC Directive 2004/108/EC.
Immunity.....per EN 61000-6-2
Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2
Radiated Field Immunity (RFI), per IEC 61000-4-3
Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4
Surge Immunity, per IEC 61000-4-5
Conducted RF Immunity (CRFI), per IEC 61000-4-6
Emissions .....per EN61000-6-4
Enclosure Port, per CISPR 16
Low Voltage AC Mains Port, per CISPR 16
Note: This is a Class A product

Vibration and Shock Standard

The ACPS3320-RTM is designed to pass the following Vibration and Shock standards.
Vibration, Sinusoidal Operating.....Designed to comply with IEC 60068-2-6: 10-500Hz, 5G, 2 Hours/axis
Vibration, Random Operating.....Designed to comply with IEC 60068-2-64: 10-500Hz, 5G-rms, 2 Hours/axis
Shock, Operating.....Designed to comply with IEC 60068-2-27: 30G, 11ms half sine, 50G, 3ms half sine, 18 shocks at 6 orientations for both test levels

Reliability Prediction

MTBF (Mean Time Between Failure): MTBF in hours using MIL-HDBK-217F, FN2. *Per MIL-HDBK-217, Ground Benign, Controlled,* G_BG_C

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
25°C	54,195,548	6,186.7	18.45

Temperature	MTBF (Hours)	MTBF (Years)	Failure Rate (FIT[1])
40°C	54,011,721	6,165.7	18.51

1 FIT is Failures in 10^9 hours.

7.3 CERTIFICATE OF VOLATILITY

<table>
<tr><th colspan="5">Certificate of Volatility</th></tr>
<tr><td colspan="2">Acromag Model
ACPS3320-RTM</td><td colspan="3">Manufacturer:
Acromag, Inc.
30765 Wixom Rd
Wixom, MI 48393</td></tr>
<tr><th colspan="5">Volatile Memory</th></tr>
<tr><td colspan="5">Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed)
□ Yes ■ No</td></tr>
<tr><th colspan="5">Non-Volatile Memory</th></tr>
<tr><td colspan="5">Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed)
□ Yes ■ No</td></tr>
<tr><th colspan="5">Acromag Representative</th></tr>
<tr><td>Name:
Russ Nieves</td><td>Title:
Director of Sales and Marketing</td><td>Email:
rnieves@acromag.com</td><td>Office Phone:
248-295-0838</td><td>Office Fax:
248-624-9234</td></tr>
</table>

8. REVISION HISTORY

The following table shows the revision history for this document:

Release Date	Version	EGR/DOC	Description of Revision
26-JUL-2018		ENZ	Preliminary release.
23-APR-2019	A	ENZ/ARP	Release.