Acromag®

Series APC8640 Industrial I/O Pack

PCI Bus Non-Intelligent Carrier Board

USER'S MANUAL

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Table of Contents **Page**

DRAWINGS **Page**

IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The APC8640 card is a personal computer Peripheral Component Interconnect (PCI) bus card and is a carrier for the Industrial I/O Pack (IP) mezzanine board field I/O modules. The carrier board provides a modular approach to system assembly, since each carrier can be populated with any combination of analog input/output, digital input/output, communication, etc. IP modules. Thus, the user can create a board which is customized to the application. This saves money and space - a single carrier board populated with IP modules may replace several dedicated function PCI bus boards. The APC8640 non-intelligent carrier board provides impressive functionality at low cost.

Model	Board Size (Length)	Supported IP Slots	Operating Temperature Range
APC8640	Long (12.283")	5(A,B,C,D,E)	0 to +70°C

KEY APC8640 FEATURES

- **PCI Specification Version 2.2 Compliant Slave Carrier: -** Provides a PCI bus interface to control and communicate with industry standard IP modules.
- **Interface for IP Modules** – APC8640 provides an electrical and mechanical interface for up to five industry standard IP modules. IP Modules are available from Acromag and other vendors in a wide variety of Input/Output configurations to meet the needs of varied applications.
- **Plug-And-Play PCI bus Carrier** - The carrier card contains standard PCI bus configuration memory. Upon power-up the system auto-configuration process assigns the carrier's base address in memory space.
- **Plug-And-Play Interrupt Support** - The personal computer system software will allocate one interrupt line to the carrier. The carrier's interrupt pending register can be used to quickly identify IP module pending interrupts.
- **Supports Two Interrupt Channels per IP** - Up to two interrupt requests are supported for each IP. Additional registers are associated with each interrupt request for control and status monitoring.

- **Full IP Register Access** - Makes maximum use of logically organized programmable registers on the carrier boards to provide for easy configuration and control of IP modules. Supports accesses to IP input/output, interrupt, ID ROM, and Memory data spaces.
- **IP Module Access Time Out** - Allows access to empty IP slots without system failure. If the IP module accessed does not respond within 32u seconds the bus access is terminated without system failure. This allows each IP slot to be probed to determine if an IP is installed. A control register bit will be set and/or issue of an interrupt request to indicate IP module time out access has occurred.
- **IP Module Selectable Clock** - Allows for each IP module to be individual configured to an 8MHz or 32MHz clock.
- **Optional Screw Termination Panel** - Model supports field connection via screw terminals using the optional DIN rail mount termination panels.
- **Connectors Access I/O** - Access to field I/O signals is provided via 3M Low Profile 50-pin headers with cable ejector latches. A separate header is provided for each IP module.
- **Supervisory Circuit for Reset Generation** - A microprocessor supervisor circuit provides power-on, power-off, and low power detection reset signals to the IP modules per the IP specification.
- **Individually Filtered Power** - Filtered +5V, +12V, and -12V DC power is provided to the IP modules via passive filters present on each supply line serving each IP. This provides optimum filtering and isolation between the IP modules and the carrier board and allows analog signals to be accurately measured or reproduced on IP modules without signal degradation from the carrier board logic signals.
- **Individually Fused Power** - Fused +5V, +12V, and -12V DC power is provided. A fuse is present on each supply line serving each IP module.
- **DLL Software is Available** - Acromag provides Windows 32 Dynamic Link Libraries (DLLS) controls software for Windows 98/Me/2000/XP®. This software (Model IPSW-API-WIN) provide a high-level interface to the carriers and IP modules. They are also compatible with a number of programming environments including Visual C++, Visual Basic, Borland C++ Builder and others.

PCI BUS INTERFACE FEATURES

- **Slave Module**- All read and write accesses are implemented as either a 32-bit, 16-bit or 8-bit single data transfer.
- **Immediate Disconnect on Read** - The PCI bus will immediately disconnect after a read. The read data is then stored in a read FIFO. Data in the read FIFO is then accessed by the PCI bus when the read cycle is retried. This allows the PCI bus to be free for other system operations while the read data is moved to the read FIFO.
- **Interrupt Support** - PCI bus INTA# interrupt request is supported. All IP module interrupts are mapped to INTA#. Carrier board software programmable registers are utilized as interrupt request control and status monitors.

SIGNAL INTERFACE PRODUCTS

This IP carrier board will mate directly to all industry standard IP modules. Acromag provides the following interface products (all connections to field signals are made through the carrier board which passes them to the individual IP modules):

Cables:

Cables are assembled using 3M wire-mount connector: P25LE-050S-DA. Shielded Cable should be assembled using 3M Part #: 90101/50. Each end of the cable should be stripped a minimum of 0.5” from the connector to allow for strain relief. Unshielded cable should be assembled using 3M Part #: 3756/50. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.

IP MODULE Win32 DRIVER SOFTWARE

Acromag provides a software product (sold separately) to facilitate the development of Windows (98/Me/2000/XP®) applications accessing Industry Pack modules installed on Acromag PCI Carrier Cards and CompactPCI Carrier Cards. This software (Model IPSW-API-WIN) consists of low-level drivers and Windows 32 Dynamic Link Libraries (DLLS) that are compatible with a number of programming environments including Visual C++, Visual Basic, Borland C++ Builder and others. The DLL functions provide a high-level interface to the carriers and IP modules eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

IP MODULE QNX SOFTWARE

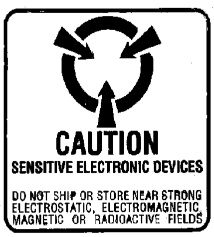
Acromag provides a software product (sold separately) consisting of board QNX® software. This software (Model IPSW-API-QNX) is composed of QNX® (real time operating system) libraries for all Acromag IP modules and carriers including the AVME9670, AVME9660/9630, APC8620A/21A, APC8640, ACPC8630/35, and ACPC8625. The software supports X86 PCI bus only and is implemented as library of “C” functions. These functions link with existing user code to make possible simple control of all Acromag IP modules and carriers.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.



This board is physically protected with packing material and electrically protected with an anti static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The lack of air circulation within the computer chassis is a cause for some concern. Most, if not all, computer chassis do not provide a fan for cooling of add-in boards. The dense packing of the IP modules to the carrier board alone results in elevated IP module and carrier board temperatures, and the restricted air flow within the chassis aggravates this problem. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

The carrier board is plug-and-play compatible and, as such, its board addresses are automatically assigned by the system auto-configuration routine upon power-up. The base address of the carrier board’s configuration registers in memory space and I/O space is assigned. In addition, the base addresses of the IP modules and carrier board registers are assigned in 32-bit memory space.

Power should be removed from the board when changing jumper configurations or when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-672 and your IP module documentation for specific configuration and assembly instructions.

IP Memory Space Configuration

A configuration jumper must be set on the carrier, prior to power-up, to enable IP Memory Space. Setting this jumper will allow each IP module to use up to 8M bytes of Memory Space. Note that the board will request 64M bytes of system memory during PCI configuration. This value cannot be altered.

See diagram 4502-114 located in the drawings portion of this manual for jumper location and settings. **The jumper must be present in one of the two configurations for proper board operation. Factory default is memory space disabled.**

Interrupt Configuration

No hardware jumper configuration is required for interrupts. Interrupt enables and status flags are configured or viewed via programmable registers on the carrier board (see Section 3 for programming details). The carrier board passes interrupt requests from the IP modules to the PCI bus. Refer to the IP modules for their specific configuration requirements.

CONNECTORS

Connectors of the APC8640 carrier consist of five carrier IP module field I/O connectors, five IP module logic connectors, and one PCI bus interface connector. These interface connectors are discussed in the following sections.

Carrier Field I/O Connectors (IP modules A through E)

Field I/O connections are made via 50 pin 3M ribbon cable connectors A, B, C, D, and E for IP modules in positions A through E. IP module assignment is marked on the board for easy identification (see IP location drawing 4502-114 for physical locations of the IP modules). Flat cable assemblies and termination panels (or user defined terminations) can be quickly mated to the field I/O connectors. Pin assignments are defined by the IP module employed since the pins from the IP module field side correspond identically to the pin numbers of the 50 pin connectors.

Carrier field I/O connectors A through E are 3M Low Profile 50-pin headers (3M P/N P50LE-050P1-R1-DA) and they mate to ejector equipped ribbon cable connectors (P25LE-050S-DA).

IP Field I/O Connectors (IP modules A through E)

The field side connectors of IP modules A through E mate to AMP 173280-3 connectors P4, P5, P9, P12, and P15 respectively, on the carrier board. IP locations are labeled on the board for easy identification. Field and logic side connectors are keyed to avoid incorrect assembly.

The AMP 173280-3 connectors mate to AMP 173279-3 connectors (or similar) on the IP modules. This provides excellent connection integrity and utilizes gold plating in the mating area. Threaded metric M2 screws and spacers (supplied with Acromag IP modules) provide additional stability for harsh environments (see Drawing 4501-672 for assembly details).

Pin assignments for these connectors are made by the specific IP model used and correspond identically to the pin numbers of the front panel connectors.

IP Logic Interface Connectors (IP modules A through E)

The logic interface sides of IP modules A through E mate to AMP 173280-3 connectors P6, P7, P10, P13, and P16, respectively, on the carrier board. IP locations are labeled on the board for easy identification. Field and logic side connectors are keyed to avoid incorrect assembly.

The AMP 173280-3 connectors mate to AMP 173279-3 connectors (or similar) on the IP modules. This provides excellent connection integrity and utilizes gold plating in the mating area. Threaded metric M2 screws and spacers (supplied with Acromag IP modules) provide additional stability for harsh environments (see Drawing 4501-672 for assembly details).

Pin assignments for these connectors are defined by the IP module specification and are shown in Table 2.1.

IP Logic Strobe Connectors

Each IP module has an uncommitted Strobe signal on the logic interface connector (pin 46). The Strobe signal may be used as an optional input or output from the IP module. On the APC8640 the Strobe signals for each of the five IP modules are routed to 0 Ohms resistors. Contact Acromag for further information on using the Strobe signals.

PCI Bus Connections

Table 2.2 indicates the pin assignments for the PCI bus signals at the card edge connector. Connector pins are designated by a letter and a number. The letter indicates which side of a particular connector the pin contact is on. “B” is on the component side of the carrier board while “A” is on the solder side. Connector “gold finger” numbers increase with distance from the bracket end of the printed circuit board.

Refer to the PCI bus specification for additional information on the PCI bus signals.

Table 2.1: Standard IP Logic Interface Connections

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSel*	29
D01	5	***DMAReq0****	30
D02	6	MEMSel*	31
D03	7	***DMAReq1****	32
D04	8	IntSel*	33
D05	9	***DMAck0****	34
D06	10	IOSEL*	35
D07	11	***RESERVED***	36
D08	12	A1	37
D09	13	***DMAEnd****	38
D10	14	A2	39
D11	15	ERROR*	40
D12	16	A3	41
D13	17	INTReq0*	42
D14	18	A4	43
D15	19	INTReq1*	44
BS0*	20	A5	45
BS1*	21	STROBE*	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	***RESERVED***	49
GND	25	GND	50

Asterisk (*) is used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by the carrier board.

TABLE 2.2: PCI Bus P1 CONNECTIONS

Signal	Pin	Pin	Signal
-12V	B01	A01	***TRST#***
TCK	B02	A02	+12V
Ground	B03	A03	***TMS***
TDO	B04	A04	TDI
+5V	B05	A05	+5V
+5V	B06	A06	INTA#
INTB#	B07	A07	***INTC#***
INTD#	B08	A08	+5V
PRSNT1#	B09	A09	***Reserved***
Reserved	B10	A10	V I/O[1]
PRSNT2#	B11	A11	***Reserved***
KEYWAY	B12	A12	KEYWAY
KEYWAY	B13	A13	KEYWAY
Reserved	B14	A14	***Reserved***
Ground	B15	A15	RST#
CLK	B16	A16	+5V
Ground	B17	A17	***GNT#***
REQ#	B18	A18	Ground
V I/O[1]	B19	A19	***Reserved***
AD[31]	B20	A20	AD[30]
AD[29]	B21	A21	+3.3V
Ground	B22	A22	AD[28]
AD[27]	B23	A23	AD[26]
AD[25]	B24	A24	Ground
+3.3V	B25	A25	AD[24]
C/BE[3]#	B26	A26	IDSEL
AD[23]	B27	A27	+3.3V
Ground	B28	A28	AD[22]
AD[21]	B29	A29	AD[20]
AD[19]	B30	A30	Ground

Signal	Pin	Pin	Signal
+3.3V	B31	A31	AD[18]
AD[17]	B32	A32	AD[16]
C/BE[2]#	B33	A33	+3.3V
Ground	B34	A34	FRAME#
IRDY#	B35	A35	Ground
+3.3V	B36	A36	TRDY#
DEVSEL#	B37	A37	Ground
Ground	B38	A38	STOP#
LOCK#	B39	A39	+3.3V
PERR#	B40	A40	***SDONE***
+3.3V	B41	A41	***SBO#***
SERR#	B42	A42	Ground
+3.3V	B43	A43	PAR
C/BE[1]#	B44	A44	AD[15]
AD[14]	B45	A45	+3.3V
Ground	B46	A46	AD[13]
AD[12]	B47	A47	AD[11]
AD[10]	B48	A48	Ground
Ground	B49	A49	AD[09]
KEYWAY			KEYWAY
KEYWAY			KEYWAY
AD[08]	B52	A52	C/BE[0]#
AD[07]	B53	A53	+3.3V
+3.3V	B54	A54	AD[06]
AD[05]	B55	A55	AD[04]
AD[03]	B56	A56	Ground
Ground	B57	A57	AD[02]
AD[01]	B58	A58	AD[00]
V I/O[1]	B59	A59	V I/O[1]
ACK64#	B60	A60	***REQ64#***
+5V	B61	A61	+5V
+5V	B62	A62	+5V

Notes (Table 2.2):
(#) s used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by the carrier board.
1. V I/O may be either +3.3V or +5V.

DATA TRANSFER TIMING

All PCI bus read or write cycles to the APC8640 are typically implemented within 150n seconds (FRAME# active to TRDY# active). After 150n seconds the PCI bus is available to the system for other PCI bus activity. As the PCI bus is released, the APC8640 completes the read or write cycle to the targeted IP module or carrier register within the access times given in Table 2.3.

FIELD GROUNDING CONSIDERATIONS

Carrier boards are designed with passive filters on each supply line to each IP module. This provides maximum filtering and signal decoupling between the IP modules and the carrier board. However, the boards are considered non-isolated, since there is electrical continuity between the PCI bus and the IP grounds. Therefore, unless isolation is provided on the IP module itself, the field I/O connections are not isolated from the PCI bus. Care should be taken in designing installations without isolation to avoid ground loops and noise pickup. This is particularly important for analog I/O applications when a high level of accuracy/resolution is needed (12-bits or more). Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the IP input/output modules.

TABLE 2.3: APC8640 Write and Read Complete Time

Register	Data Transfer Time
Carrier Registers Write	300ns, Typical[1]
Carrier Register Read	250ns, Typical[1]
8MHz IP Opertaion	
8 and 16-bit IP Write	525ns, Typical[1,2]
32-bit IP Write	900ns, Typical[1,2]
8 and 16-bit IP Read	500ns, Typical[1,2]
32-bit IP Read	850ns, Typical[1,2]
32MHz IP Opertaion	
8 and 16-bit IP Write	350ns, Typical[1,3,4]
32-bit IP Write	550ns, Typical[1,3,5]
8 and 16-bit IP Read	300ns, Typical[1,3,4,4]
32-bit IP Read	500ns, Typical[1,3,5]

Notes (Table 2.3):

1. The data transfer times given in table 2.3 are measured from the falling edge of FRAME# to the falling edge of READY#. The PCI bus starts a data transfer cycle by driving FRAME# low. The APC8640 signals the completion of a read or write cycle by driving READY# low. Note that an additional delay will occur during read cycles as the data is transferred to the PCI Bus. These values may vary up to 125ns due to the asynchronous relationship between the PCI bus clock and the local clock.
2. This access time assumes zero IP module wait states. For each IP module wait state 125n seconds must be added to this value.
3. This access time assumes zero IP module wait states. For each IP module wait state 31.25n seconds must be added to this value.
4. 8 or 16-bit IP Memory Space accesses require an additional 31.25ns when the IP is operating at 32MHz.
5. 32-bit IP Memory Space accesses require an additional 62.5ns when the IP is operating at 32MHz.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the APC8640 non-intelligent carrier board.

This Acromag APC8640 is a PCI Specification version 2.2 compliant PCI bus slave carrier board. The carrier connects a PCI host bus to the IP module's 16-bit data bus per the Industrial I/O Pack logic interface specification on the mezzanine (IP) boards that are installed on the carrier.

The PCI bus is defined to address three distinct address spaces: I/O, memory, and configuration space. **The IP modules can be accessed via the PCI bus memory space only.**

The PCI card's configuration registers are initialized by system software at power-up to configure the card. The PCI carrier is a Plug-and-Play PCI card. As a Plug-and-Play card the board's base address and system interrupt request line are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCI bus configuration access is used to access a PCI card's configuration registers.

PCI Configuration Address Space

When the computer is first powered-up, the computer's system configuration software scans the PCI bus to determine what PCI devices are present. The software also determines the configuration requirements of the PCI card.

The system software accesses the configuration registers to determine how many blocks of memory space the carrier requires. It then programs the carrier's configuration registers with the unique memory address range assigned.

The configuration registers are also used to indicate that the PCI carrier requires an interrupt request line. The system software then programs the configuration registers with the interrupt request line assigned to the PCI carrier.

Since this PCI carrier is portable and not hardwired in address space, this carrier's device drive provided by Acromag uses the mapping information stored in the carrier's Configuration Space registers to determine where the carrier is mapped in memory space and which interrupt line will be used.

Configuration Transactions

The PCI bus is designed to recognize certain I/O accesses initiated by the host processor as a configuration access. Configuration uses two 32-bit I/O ports located at addresses 0CF8 and 0CFC hex. These two ports are:

- 32-bit configuration address port, occupying I/O addresses 0CF8 through 0CFB hex.
- 32-bit configuration data port, occupying I/O addresses 0CFC through 0CFF hex.

Configuration space, shown in Table 3.1, is accessed by writing a 32-bit long-word into the configuration address port that specifies the PCI bus, the carrier board on the bus, and the configuration register on the carrier being accessed. A read or write to the configuration data port will then cause the configuration address value to be translated to the requested configuration cycle on the PCI bus. Accesses to the configuration data port determine the size of the access to the configuration register addressed and can be an 8, 16, or 32-bit operation.

Any access to the Configuration address port that is not a 32-bit access is treated like a normal computer I/O access. Thus, computer I/O devices using 8 or 16-bit registers are not affected because they will be accessed as expected.

Configuration Registers

The PCI specification requires software driven initialization and configuration via the Configuration Address space. This PCI carrier provides 256 bytes of configuration registers for this purpose. The PCI carrier contains the configuration registers, shown in Table 3.2, to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers and the Interrupt Line Register, which must be read to determine the base address, assigned to the carrier and the interrupt request line that goes active on a carrier interrupt request.

Table 3.1: Configuration Address Port

BIT	FUNCTION
31	Enables accesses to Configuration Data to be translated to configuration cycles on the PCI bus.
30-24	Reserved, Return 0 when read.
23-16	Bus Number Choose a specific PCI bus in the system. Zero if only one PCI bus.
15-11	Device Number Choose a specific device/PCI board on the bus.
10-8	Function Number Choose a specific function in a device. Function number is zero for the APC8640
7-2	Register Number Used to indicate which PCI Configuration Register to access. The Configuration Registers and their corresponding register numbers are given in Table 3.2.
1-0	Read Only bits that return 0.

Table 3.2: Configuration Registers

Reg. Num.	D31 D24	D23 D16	D15 D8	D7 D0
0	Device ID=1024		Vendor ID= 10B5	
1	Status		Command	
2	Class Code			Rev ID
3	BIST	Header	Latency	Cache
4	Base Addr. Memory Mapped Configuration Registers			
5	Base Address for I/O Mapped Configuration Registers			
6	*PCIBar2:* Base Address for Carrier/IO/ID/INT Space			
7	*PCIBar3:* Base Address for Memory Space [1]			
8:10	Not Used			
11	Subsystem ID		Subsystem Vendor ID	
12	Not Used			
13	Reserved			
14	Reserved			
15	Max_Lat	Min_Gnt	Inter. Pin	Inter. Line

1. Optional address space that is enabled/disabled via a jumper prior to power-up.

MEMORY MAP

This board consumes a 1K byte block and an optional 64M byte block that is enabled via configuration jumper prior to power-up. The 1K byte block of memory consumed by the board is composed of blocks of memory for the ID, I/O and INT spaces corresponding to five IP modules. In addition, a small portion of the 1K byte address space contains registers specific to the function of the carrier board. The 64M byte block of memory is composed of the Memory Space for up to five IP modules.

The carrier is configured to map this 1K byte and 64M byte block of memory into 32-bit memory space. The system configuration software will allocate space by writing the assigned addresses into the corresponding Base Address registers of the Configuration Registers. The memory map for APC8640 is shown in Tables 3.3.

Table 3.3: APC8640 Carrier Board Memory Map

PCIBar2 + (Hex)	High Byte D15 D08	Low Byte D07 D00	PCIBar2 + (Hex)
0001	Carrier Board Status / Control Register		**0000**
0003	IP Interrupt Pending Register		**0002**
0005	IP A Interrupt 0 Select Space		**0004**
0007	IP A Interrupt 1 Select Space		**0006**
0009	IP B Interrupt 0 Select Space		**0008**
000B	IP B Interrupt 1 Select Space		**000A**
000D	IP C Interrupt 0 Select Space		**000C**
000F	IP C Interrupt 1 Select Space		**000E**
0011	IP D Interrupt 0 Select Space		**0010**
0013	IP D Interrupt 1 Select Space		**0012**
0015	IP E Interrupt 0 Select Space		**0014**
0017	IP E Interrupt 1 Select Space		**0016**
0019	Clock Control Register		**0018**
001B ↓ **003F**	Not Used[1]	Not Used[1]	**001A** ↓ **003E**
0041 ↓ **007F**	IP A ID Space	IP A ID Space	**0040** ↓ **007E**
0081 ↓ **00BF**	IP B ID Space	IP B ID Space	**0080** ↓ **00BE**
00C1 ↓ **00FF**	IP C ID Space	IP C ID Space	**00C0** ↓ **00FE**
0101 ↓ **013F**	IP D ID Space	IP D ID Space	**0100** ↓ **013E**
0141 ↓ **017F**	IP E ID Space	IP E ID Space	**0140** ↓ **017E**
0181 ↓ **01FF**	IP A I/O Space	IP A I/O Space	**0180** ↓ **01FE**
0201 ↓ **027F**	IP B I/O Space	IP B I/O Space	**0200** ↓ **027E**
0281 ↓ **02FF**	IP C I/O Space	IP C I/O Space	**0280** ↓ **02FE**
0301 ↓ **037F**	IP D I/O Space	IP D I/O Space	**0300** ↓ **037E**
0381 ↓ **03FF**	IP E I/O Space	IP E I/O Space	**0380** ↓ **03FE**

1. The board will return "0" for all address that are not used.

Table 3.3: APC8640 Carrier Board Memory Map

PCIBar3 + (Hex)	High Byte D15 D08	Low Byte D07 D00	PCIBar3+ (Hex)
0000001 ↓ **07FFFFF**	IP A Memory Space		**0000000** ↓ **07FFFFE**
0800001 ↓ **0FFFFFF**	IP B Memory Space		**0800000** ↓ **0FFFFFE**
1000001 ↓ **17FFFFF**	IP C Memory Space		**1000000** ↓ **17FFFFE**
1800001 ↓ **1FFFFFF**	IP D Memory Space		**1800000** ↓ **1FFFFFE**
2000001 ↓ **27FFFFF**	IP E Memory Space		**2000000** ↓ **27FFFFE**
2800001 ↓ **3FFFFFF**	Not Used[1]		**2800000** ↓ **3FFFFFE**

Note: Shaded areas not used by APC8621A carrier.
1. The board will return "0" for all address that are not used.

The APC8640 base addresses are determined through the PCI Configuration Registers. The addresses given in the memory map are relative to the base addresses (PCIBar2, PCIBar3) of the APC8640 carrier as shown in Table 3.2. The addresses within each IP's own space are specific to that IP module. Refer to the IP module's User Manual for information relating to the IP specific addressing.

The Carrier registers, IP Identification (ID) spaces, IP Input/Output (IO), IP Interrupt spaces, and Memory (MEM) spaces are accessible via the PCI bus space as given in Tables 3.3. A 32-bit PCI bus access will result in two 16-bit accesses to the IP module. A 16-bit or 8-bit PCI bus access results in a single 16-bit or 8-bit access to the IP module respectively.

Carrier Status/Control Register - (Read/Write, PCIBar2 + 00H)

The Carrier Board Status Register reflects and controls functions globally on the carrier board. This includes monitoring the IP Error signal, enabling, disabling, or monitoring IP and timeout interrupts, performing a software reset including the carrier and IP modules, and identifying if memory space is enabled.

BIT	FUNCTION
15-12	Carried Identification: These bits are used for carrier identification. Writing to these bits will result in the data being stored. Reading these bits will result in the inverse of the stored value. Reset Condition: "1010" if Memory Space is not supported. "1011" if memory space is supported. *Memory space support is controlled via a configuration jumper.*
11-09	Not Used (bits read as logic "0")
08 Write Only	Software Reset Writing a "1" to this bit causes a software reset. Writing a "0" or reading this bit has no effect. When set, the software reset pulse will have a duration of 1μs (microsecond).
07-06	Not Used (bits read as logic "0")
05 Read And Write	IP Module Access Time Out Interrupt Pending This bit will be "1" when there is a IP Module Access Time Out interrupt pending. This bit will be "0" when there is no interrupt pending. Reset condition: Set to "0". Writing a "1" to this bit will release the pending interrupt.
04 Read Only	IP Module Access Time Out Status Status bit to indicated that the last IP module access has timed out. This bit only reflects the last IP module access. "0" if last IP module access did not time out. "1" if last IP module access did time out.
03 Read And Write	Time Out Interrupt Enable When set to "1", this bit will enable the carrier board to generate an interrupt upon time out of an IP module access. The default setting or reset condition is "0" (interrupt generation upon time out disabled). The interrupt service routine, in responding to the Time Out Access interrupt, will need to set this bit to 0 to clear the pending interrupt request.
02 Read And Write	IP Module Interrupt Enable When set to "1", this bit will enable the generation of IP module interrupts. The default setting or reset condition is "0" (IP module interrupt generation disabled). Interrupts must also be supported and configured at the IPs.
01 Read Only	IP Module Interrupt Pending This bit will be "1" when there is an interrupt pending. This bit will be "0" when there is no interrupt pending. Polling this bit will reflect the IP Module's pending interrupt status, even if the IP Module Interrupt Enable bit is set to "0". Reset condition: Set to "0".
00 Read Only	IP Module Error This bit will be "1" when there is an active IP Module Error signal. This bit will be "0" when all IP module Error signals are inactive. This bit allows the user to monitor the Error signals of IP modules A through E. The IP specification states that the error signals indicate a non-recoverable error from the IP (such as a component failure or hard-wired configuration error). Refer to your IP specific documentation to see if the error signal is supported and what it indicates. Reset condition: Set to "0".

IP Interrupt Pending Register - (Read, PCIBar2 + 02H)

The IP Interrupt Pending Register is used to individually identify pending IP interrupts or a pending carrier generated interrupt as a result of IP module time out access. If multiple IP interrupts are pending, software must determine the order in which they are serviced.

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
IP D Int1 Pend	IP D Int0 Pend	IP C Int1 Pend	IP C Int0 Pend	IP B Int1 Pend	IP B Int0 Pend	IP A Int1 Pend	IP A Int0 Pend

MSB D15	D14	D13	D12	D11	D10	D9	LSB D8
Not Used (bits read as logic "0")					Time Out Interrupt Pend	IP E Int1 Pend	IP E Int0 Pend

Where:

All Bits IP Interrupt Pending (Read)	A bit will be a "1" when the corresponding interrupt is pending. A bit will be a "0" when its corresponding interrupt is <u>not</u> pending. Polling this bit will reflect the IP module's pending interrupt status, even if the IP interrupt enable bit is set to "0". Reset Condition: Set to "0". An IP module pending interrupt bit will be cleared if its correspond interrupt request signal is inactive.

Clock Control Register - (Read/Write, PCIBar2 + 018H)

The Clock Control Register is used to select the operational frequency of the individual IP modules. A "0" (default) indicates that the IP module is supplied with an 8MHz clock. A "1" indicates that the IP module is supplied a 32MHz clock. A reset will set all bits of this register to "0".

MSB D15 -- D5	D4	D3	D2	D1	LSB D0
Not Used	IP E CLK	IP D CLK	IP C CLK	IP B CLK	IP A CLK

IP Module Interrupt Space - (Read Only)

The Interrupt space for each IP module is fixed at two 16-bit words. Interrupt 0 select space is read, typically by an interrupt service routine, to respond to an interrupt request via the IP Module's INTREQ0* signal. Likewise interrupt 1 select space is read to respond to an interrupt request via the IP Module's INTREQ1* signal. An access to an interrupt select space results in the IP module serving up an interrupt vector. In addition, access to the interrupt space will cause some IP modules to release their interrupt request. See each IP module's User Manual for details.

IP Module ID Space- (Read Only)

Each IP contains identification (ID) information that resides in the ID space per the IP specification. This area of memory contains either 32 bytes (Format I ID) or 64 bytes (Format II ID) of information, at most. Format I requires read of only the least significant byte. Format II requires read of a 16-bit value. The carrier will implement 16-bit reads to the ID space to allow support for either Format I or Format II. Both fixed and variable information may be present within the ID ROM. Variable information may include unique information required for the module. The identification Section for each IP module is located in the carrier board memory map per Table 3.3. Refer to the documentation of your IP module for specific information about each IP module's ID Space contents.

IP Module I/O Space - (Read/Write)

The I/O space on each IP module is fixed at 128, 16-bit words (256 bytes). The five IP module I/O spaces are accessible at fixed offsets from PCIBar2. IP modules may not fully decode their I/O space and may use byte or word only accesses. See each IP module's User Manual for details.

IP Module Memory Space - (Read/Write)

Each IP module may contain up to 8M bytes of Memory Space arranged into 16-bit words. The five IP module Memory spaces are accessible at fixed offset from PCIBar3. IP modules may not fully decode their Memory space and may use only byte or word accesses. See each IP module's User Manual for details.

GENERATING INTERRUPTS

Interrupt requests originate from the carrier board in the case of an access time out and from the IP modules. Each IP may support 0, 1, or 2 interrupt requests. Upon an IP module interrupt request the carrier passes the interrupt request onto the host, provided that the carrier board is enabled for interrupts within the Carrier Board Status Register.

Sequence of Events For an Interrupt

1. Clear the interrupt enable bits in the Carrier Board Status Register by writing a "0" to bit 2/bit 3.
2. Write interrupt vector to the location specified on the IP and perform any other IP specific configuration required - do for each supported IP interrupt request.
3. Determine the IRQ line assigned to the carrier during system configuration (within the configuration register).
4. Set up the PC/AT's interrupt vector for the appropriate interrupt.
5. Unmask the IRQ on the PC/AT's 8259 interrupt controller.
6. The IP asserts an interrupt request to the carrier board (asserts interrupt request line IntReq0* or IntReq1*).
7. The carrier drives PCI bus interrupt request signal INTA# active.
8. PC/AT's drives the IRQ line assigned to the active carrier.
9. The interrupt service routine pointed to by the vector set up in step 4 starts.
10. Interrupt service routine determines which IP module caused the interrupt by reading the carrier interrupt pending register. If multiple interrupts are pending the interrupt service routine software determines which IP module to service first. In a PC interrupts are shared and can be from any slot on the backplane or from the mother board itself. The driver must first check that the interrupt came from the PCI carrier by reading the carrier interrupt pending register.
11. The interrupt service routine accesses the interrupt space of the IP module selected to be serviced. Note that the interrupt space accessed must correspond to the interrupt request signal driven by the IP module.
12. The carrier board will assert the INTSEL* signal to the appropriate IP together with (carrier board generated) address bit A1 to select which interrupt request is being processed (A1 low corresponds to INTREQ0*; A1 high corresponds to INTREQ1*).
13. The IP module receives an active INTSEL* signal from the carrier and supplies its interrupt vector to the host system during this interrupt acknowledge cycle. An IP module designed to release its interrupt request on acknowledge will release its interrupt request upon receiving an active INTSEL* signal from the carrier. If the IP module is designed to release it's interrupt request on register access the interrupt service routine must access the required register to clear the interrupt request.
14. Write "End-Of-Interrupt" command to PC/AT's 8259.
15. If the IP interrupt stimulus has been removed and no other IP modules have interrupts pending, the interrupt cycle is completed (i.e. the carrier board negates its interrupt request INTA#).

4.0 THEORY OF OPERATION

This section describes the basic functionality of the circuitry used on the carrier board. Refer to the Block Diagram shown in the Drawing 4502-113 as you review this material.

CARRIER BOARD OVERVIEW

The carrier board is a PCI bus slave/target board providing up to five industry standard IP module interfaces. The carrier board's PCI bus interface allows an intelligent single board computer (PCI bus Master) to control and communicate with IP modules that are present on the PCI bus carrier. IP module field I/O connections link to the field I/O connections of the carrier, which in turn are used to connect field electronic hardware to the carrier board via ribbon cable.

The PCI bus and IP module logic commons have a direct electrical connection (i.e., they are not electrically isolated). However, the field I/O connections can be isolated from the PCI bus if an IP module that provides this isolation (between the logic and field side) is utilized. A wide variety of IP modules are currently available (from Acromag and other vendors) that allow interface to many external devices for digital I/O, analog I/O, and communication applications.

PCI Bus Interface

The carrier board's PCI bus interface is used to program and monitor carrier board registers for configuration and control of the board's documented modes of operation (see section 3). In addition, the PCI bus interface is also used to communicate with and control external devices that are connected to an IP module's field I/O signals (assuming an IP module is present on the carrier board).

The PCI bus interface is implemented in the logic of the carrier board's PCI bus target interface chip. The PCI bus interface chip implements PCI specification version 2.2 as an interrupting slave including 8-bit and 16-bit data transfers to the IP modules. 32-bit IP data transfers will be treated as two 16-bit data transfers.

Note the APC8640 requires that system 3.3 volts is present on the PCI bus 3.3V pins. There are some older systems that do not provide 3.3 Volts on the PCI bus 3.3 volt pins. The APC8640 boards will not work in these systems.

Note that the APC8640 board is not hot-swapable

The carrier board's PCI bus data transfer rates are shown in Table 2.3.

Carrier Board Registers

The carrier board registers (presented in section 3) are implemented in the logic of the carrier board's FPGA. An outline of the functions provided by the carrier board registers includes:

- Identifying if memory space is enabled in the **Carrier Identification Bits**.
- Selecting either an 8MHz or 32MHz clock for each IP module in the **Clock Control Register**.
- Monitoring the error signal received from each IP module is possible via the **IP Error Bit**.
- Enabling of PCI bus interrupt requests from each IP module is possible via the **IP Module Interrupt Enable Bit**.
- Enabling of interrupt generation upon an IP module access time out is implemented via the **Time Out Interrupt Enable Bit.**
- Monitoring an IP module access time out is possible via the **IP Module Access Time Out Status Bit.**
- Identify pending interrupts via the carrier's **IP Module Interrupt Pending Bit**.
- Lastly, pending interrupts can be individually monitored via the **IP Module Interrupt Pending register**.

IP Logic Interface

The IP logic interface is also implemented in the logic of the carrier board's FPGA. The carrier board implements ANSI/VITA 4 1995 Industrial I/O Pack logic interface specification and includes five IP logic interfaces. The PCI bus address and data lines are linked to the address and data of the IP logic interface. This link is implemented and controlled by the carrier board's FPGA.

The PCI bus to IP logic interface link allows a PCI bus master to:

- Access up to 64 ID Space bytes for IP module identification via 8-bit or 16-bit data transfers using PCI bus.
- Access up to 128 I/O Space bytes of IP data via 8-bit or 16-bit data transfers.
- Access up to 8M byes of Memory Space data via 8-bit or 16-bit data transfers.
- Access IP module interrupt space via 8-bit or 16-bit PCI bus data transfers.
- Respond to two IP module interrupt requests per IP module.

As per the ANSI/VITA 4 1995 Industrial I/O Pack logic interface specification only 4 IP modules may be running at 32MHz on the APC8640 to comply with bus loading requirements.

When an IP module places data on the bus, for all data read cycles, any undriven data lines are read by the PCI bus as high because of pull-up resisters on the carrier board's data bus.

Carrier Board Clock Circuitry

A 32MHz clock, obtained from a multiplied 8MHz clock, is used to control the FPGA and the local bus. Clocks are then driven to each IP module via a high speed transceiver to allow for a module independent selectable clock. All clock lines include series damping resistors to reduce clock overshoot and undershoot.

PCI Interrupter

Interrupts are initiated from an interrupting IP module. However, the carrier board will only pass an interrupt generated by an IP module to the PCI bus if the carrier board has been first enabled for interrupts. Each IP module can initiate two interrupts which can be individually monitored on the carrier board. After interrupts are enabled on the carrier board via the Interrupt Enable Bits (see section 3 for programming details), an IP generated interrupt is recognized by the carrier board and is recorded in the carrier board's Interrupt Pending Register.

A carrier board pending interrupt will cause the board to pass the interrupt to the PCI bus provided the Interrupt Enable bits of the carrier's Status Register have been enabled (see section 3 for programming details). The PC interrupt request line assigned by the system configuration software will then be asserted. The PC/AT will respond to the asserted interrupt line by executing the interrupt service routine corresponding to the interrupt line asserted. The interrupt service routine is executed only if the IRQ on the PC/AT's 8259 interrupt controller has been previously unmasked (see section 3 for programming details).

The interrupt service routine should respond to an interrupt by accessing IP Interrupt Select (INTSEL*) space. The interrupt service routine should also conclude the interrupt routine by writing the "End-Of-Interrupt" command to the PC/AT's 8259 interrupt controller (see section 3 for more details).

Power Failure Monitor

The carrier board contains a 5 volts undervoltage monitoring circuit which provides a reset to the IP modules when the 5 volt power drops below 4.38 volts typical / 4.31 volts minimum. This circuitry is implemented per the Industrial I/O Pack specification.

Power-On Reset

The carrier board will provide an asynchronous reset signal to all IP modules for at least 200ms following power-up. The IP reset signal will remain active until the FPGA is initialized.

Power Supply Fuses

The +5V, supply lines to each of the IP modules are individually fused with a current limit of, at minimum, 2 amps imposed by the fuses. In addition, the +12, and -12 supply lines to each of the IP modules are individually fused with a current limit of, at minimum, 1 amp imposed by the fuses. A blown fuse can be identified by visible inspection or by use of an ohm meter. The fuses are located under each IP slot near the "logic connectors" (see figure 4502-114). Note that fuse type and current limit may vary. Contact Acromag for further details.

Power Supply Filters

Power line filters are dedicated to each IP module for filtering of the +5, +12, and -12 volt supplies. The power line filters are a "T" type filter circuit comprising ferrite bead inductors and a feed-through capacitor. The filters provide improved noise performance as is required on precision analog IP modules.

Software Compatibility to the APC8620/APC8621

To provide backwards compatibility with all software for the APC8620/8621, the APC8640 has the same PCI Device and Vendor ID and the option to disable IP Memory space. A jumper, set prior to power-up, is used to select between one of two configurations to load into the PCI interface chip. Note that 32MHz clock support is available with both of the APC8640 configurations. In order to determine the current configuration of the hardware use either the PCI configuration register PCIBar3 address and/or the Carrier Identification Register as outlined in table 4.1. The default factory jumper configuration is to disabled memory space.

Table 4.1

	PCIBar3	**Carrier Identification Register: PCIBar2 + 0H Bits 15-12**
APC8620/8621	0x00000000 (Not used)	Write: no effect Read: undefined Reset: undefined
APC8640 without Memory support	0x00000000 (Not used)	Write: register data Read: return inverse of registered data Reset: Set to "A"
APC8640 with Memory support	Valid address	Write: register data Read: return inverse of registered data Reset: Set to "B"

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Verify that there are no blown fuses. Replacement of the carrier and/or IP with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

Go to the "Support" tab to access:

- Application Notes
- Frequently Asked Questions (FAQ's)
- Product Knowledge Base
- Tutorials
- Software Updates/Drivers

An email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab.

Acromag's application engineers can also be contacted directly for technical assistance via telephone or FAX through the numbers listed below. When needed, complete repair services are also available.

Phone: 248-624-1541
Fax: 248-624-9234
Email: solutions@acromag.com

6.0 SPECIFICATIONS

PHYSICAL

Physical Configuration....................PCI 5/3.3V (dual) Card
Length (APC8640)....................12.283 inches (312.0 mm)
Height.......................................4.200 inches (106.68 mm)
Board Thickness.....................0.063 inches (1.60 mm)
Max Component Height............0.380 inches (9.65 mm)
Max Component Height Under IP Modules.........0.180 inches (4.57 mm)

Connectors:
P1 (PCI Bus)...........................PCI Specification 2.2 5/3.3V (dual) board card edge "finger" spacing
A-E (Carrier Field I/O)..............50-pin Low Profile Male Header (3M P50LE-050P1-R1-DA).
P4,5, 9, 12, 15 (IP Field I/O).....50-pin male plug header
P6, 7, 10, 13, 16 (IP Logic)......50-pin male plug header (AMP 173280-3 or equivalent).

Power:

Board power requirements are a function of the installed IP modules. This specification lists currents for the carrier board only. The carrier board provides +5V, +12V and -12V power to each IP from the PCI bus. Each IP module supply line is individually filtered and fused. In addition the carrier board utilizes 3.3 Volts and 5 Volts for hardware. Note that the maximum amount of current provided to the carrier card via the PCI bus varies with each system. Refer to your system documentation for more information on PCI power specifications.

Fuses: +5 volts, 2 amps (minimum) per slot
±12 volts, 1 amp (minimum) per slot

Note that fuse type and current limit may vary. Contact Acromag for further details.

The power failure monitor circuit provides a reset to IP modules when the 5 volt power drops below 4.38 volts typically / 4.31 volts minimum.

Currents specified are for the carrier board only for Models APC8640, add the IP module currents for the total current required from each supply.

+3.3 Volts (±10%)………………130mA, Typical
200mA, Maximum.
+5 Volts (±5%)………………….30mA, Typical
50mA, Maximum.
+12 Volts (±5%)………………..0mA (Not Used)
-12 Volts (±5%)…………………0mA (Not Used)

PCI BUS COMPLIANCE

Specification..................................This device meets or exceeds all written PCI Local Bus specifications per revision 2.2 dated December 1998.

Data Transfer Bus.........................Slave with 32-bit, 16-bit, and 8-bit data transfer operation. 32-bit read or write accesses are implemented as two 16 bit transfers to the IP modules.

PCI bus Write Cycle Time...........150nS Typical measured from falling edge of FRAME# to the falling edge of TRDY#.

PCI bus Read Cycle Time………..150nS Typical; The carrier issues a RETRY which frees the PCI bus while the read request is completed. The PCI bus will repeat the same read request until it completes with the requested data.

Write Complete Time………….…Time from FRAME# active until LRDYi# active. All values assume 0 IP module wait states
300nS Typical carrier register
525nS Typical 8MHz 8-bit and 16-bit IP module write.
900nS Typical 8MHz 32-bit IP module write.
350nS Typical 32MHz 8-bit and 16-bit IP module write.
550nS Typical 32MHz 32-bit IP module write.

Read Complete Time…………….Time from FRAME# active until LRDYi# active. All values assume 0 IP module wait states
250nS Typical carrier register
500nS Typical 8MHz 8-bit and 16-bit IP module read.
850nS Typical 8MHz 32-bit IP module read.
300nS Typical 32MHz 8-bit and 16-bit IP module read.
500nS Typical 32MHz 32-bit IP module read.

Interrupts.....................................PCIbus INTA# interrupt signal Up to two requests sourced from each IP mapped to INTA#. Interrupt vectors come from IP modules via access to IP module INT space.

32-bit Memory Space...................Upon power-up the system auto- configuration process (plug & play) maps the carriers base addresses (for a 1K byte and if necessary 64M byte block of memory) into the PCI bus 32-bit Memory Space.

INDUSTRIAL I/O PACK COMPLIANCE

Specification...................................This device meets or exceeds all written Industrial I/O Pack specifications per ANSI/VITA 4 1995 for 8MHz and 32MHz operation with a maximum of four IP modules. Supports Type I and Type II ID space formats.

Mechanical Interface (For APC8640)……………...Carrier supports five single-size IP modules (A-E), or two double-size and one single size IP module. 32-bit IP modules are not supported.

Electrical Interface………………...Carrier drivers use 3.3V CMOS logic. The carrier may not be compatible with IP module inputs that require 5V CMOS switching thresholds.

IP Clocks……………………………Support 8MHZ (default) or 32MHz IP clocks that are independently selected per each IP slot.

I/O Space.......................................16-bit and 8-bit: Supports 128 byte values per IP module.

ID Space...16 and 8-bit; Supports Type 1 32 bytes per IP (consecutive odd byte addresses). Also supports Type II 32 words per IP via D16 data transfers.

Memory Space...............................16 and 8-bit: Supports up to 8M bytes per IP. Disabled/enabled via a jumper (J1).

Interrupts.......................................Supports two interrupt requests per IP and interrupt acknowledge cycles via access to IP INT space.

ENVIRONMENTAL

Operating Temperature................0 to +70°C

Relative Humidity.........................5-95% non-condensing

Storage Temperature...................-55 to +125°C.

Non-Isolated..................................PCI bus and IP module logic commons have a direct electrical connection. As such, unless the IP module provides isolation between the logic and field side, the field I/O signals are not isolated from the PCI bus.

Radiated Field Immunity (RFI)...... Complies with EN61000-4-3 (3V/m, 80 to 1000MHz and 1.4GHz to 2.0GHz, 1V/m, 2.0GHz to 2.7GHz.) and European Norm EN50082-1 with no register upsets.

Conducted RF Immunity (CRFI)….Complies with EN61000-4-6 3V/rms, 150KHz to 80MHz) and European Norm EN50082-1 with no register upsets.

Electromagnetic Interference Immunity (EMI)…..........................No digital upset under the influence of EMI from switching solenoids, commutator motors, and drill motors.

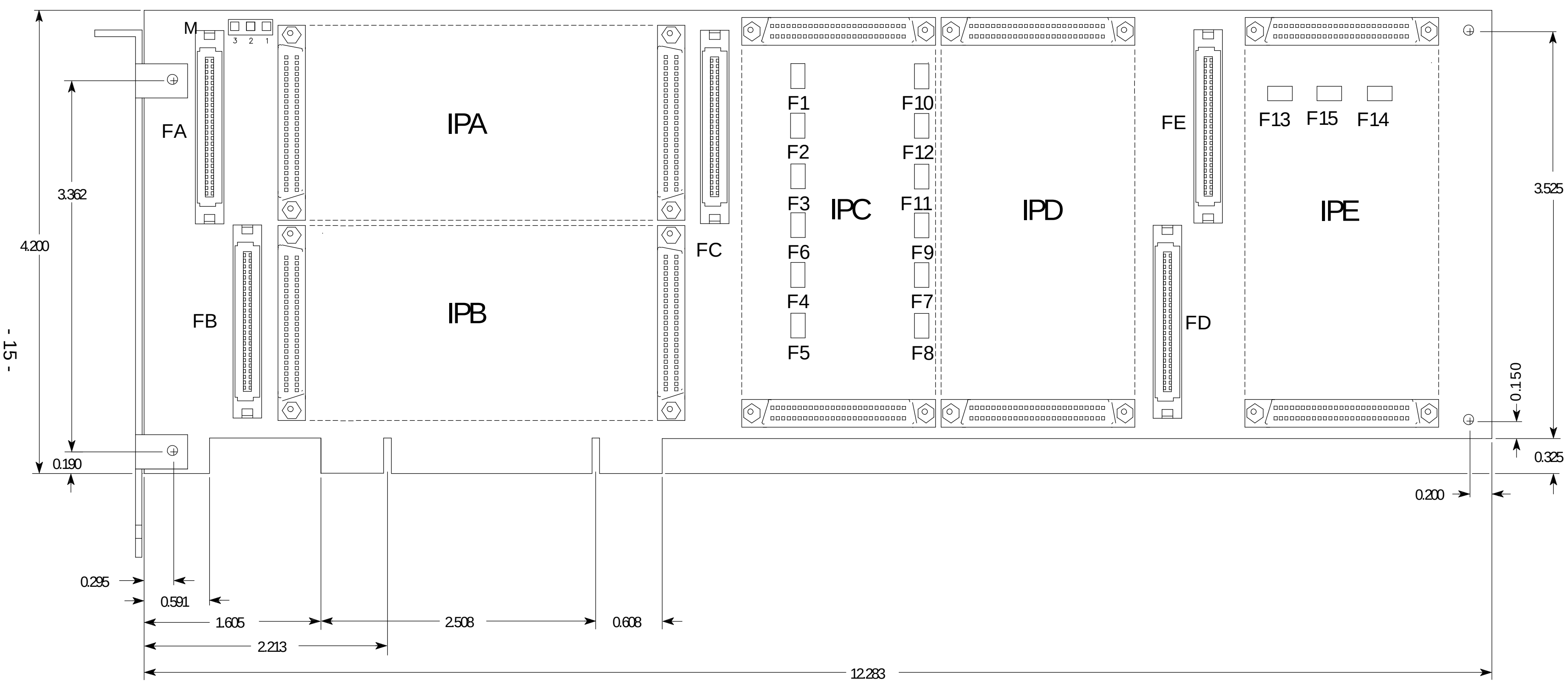
Electrostatic Discharge Immunity (ESD)…....................... Complies with EN61000-4-2 Level 3 (8KV enclosure port air discharge) and Level 2 (4KV enclosure port contact discharge) and European Norm EN50082-1.

Surge Immunity……………………Not required for signal I/O per European Norm EN50082-1.

Electric Fast Transient Immunity EFT…………………..... Complies with EN61000-4-4 Level 2 (0.5KV at field I/O terminals) and European Norm EN50082-1.

Radiated Emissions……….…… Meets or exceeds European Norm EN50081-1 for class B equipment. Shielded cable with I/O connections in shielded enclosure are required to meet compliance.

APC8640 LOCATION DIAGRAM



4502-114

JUMPER SETTINGS

DISABLE Memory Space	M (3 2 1)
ENABLE Memory Space	M (3 2 1)

FUSE IDENTIFICATION

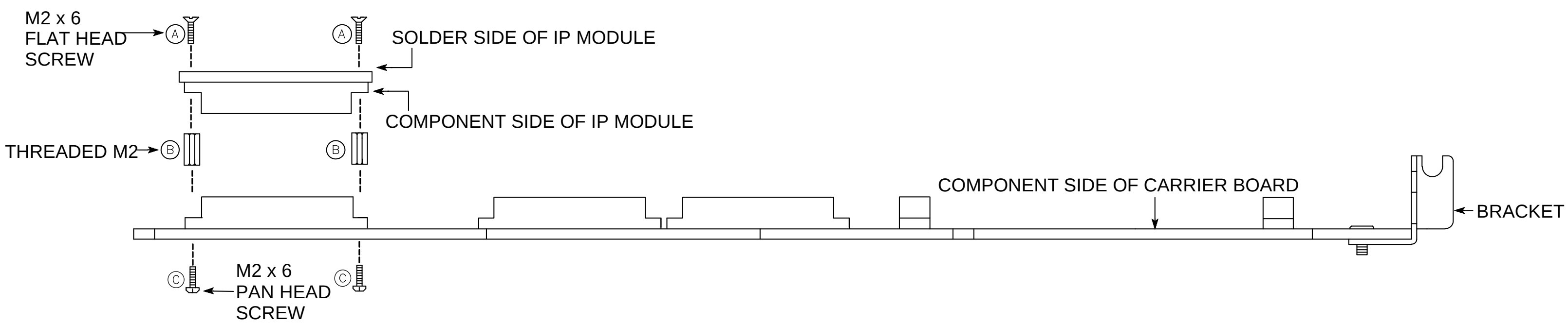
	IPA	IPB	IPC	IPD	IPE
+5V(2 AMP)*	F1	F6	F9	F10	F13
+12V(1 AMP)*	F2	F4	F7	F12	F15
-12V(1 AMP)*	F3	F5	F8	F11	F14

* Minimum Current Rating

IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY

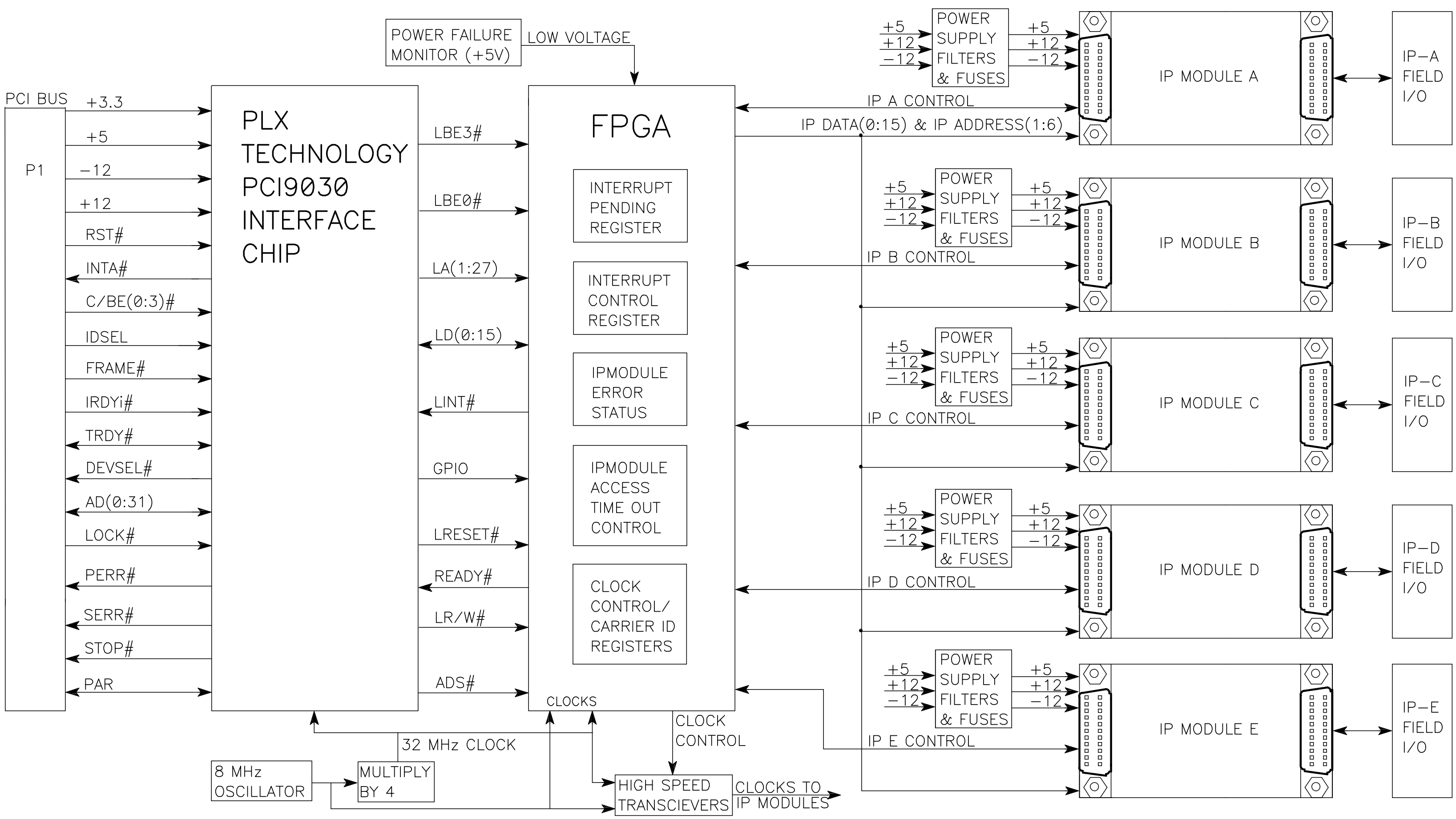
ASSEMBLY PROCEDURE:

1. THREADED SPACERS ARE PROVIDED BY ACROMAG IN TWO DIFFERENT LENGTHS WITH IP MODULES. THE SHORTER LENGTH IS FOR USE WITH APC8620 CARRIER BOARD (SHOWN).
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES).

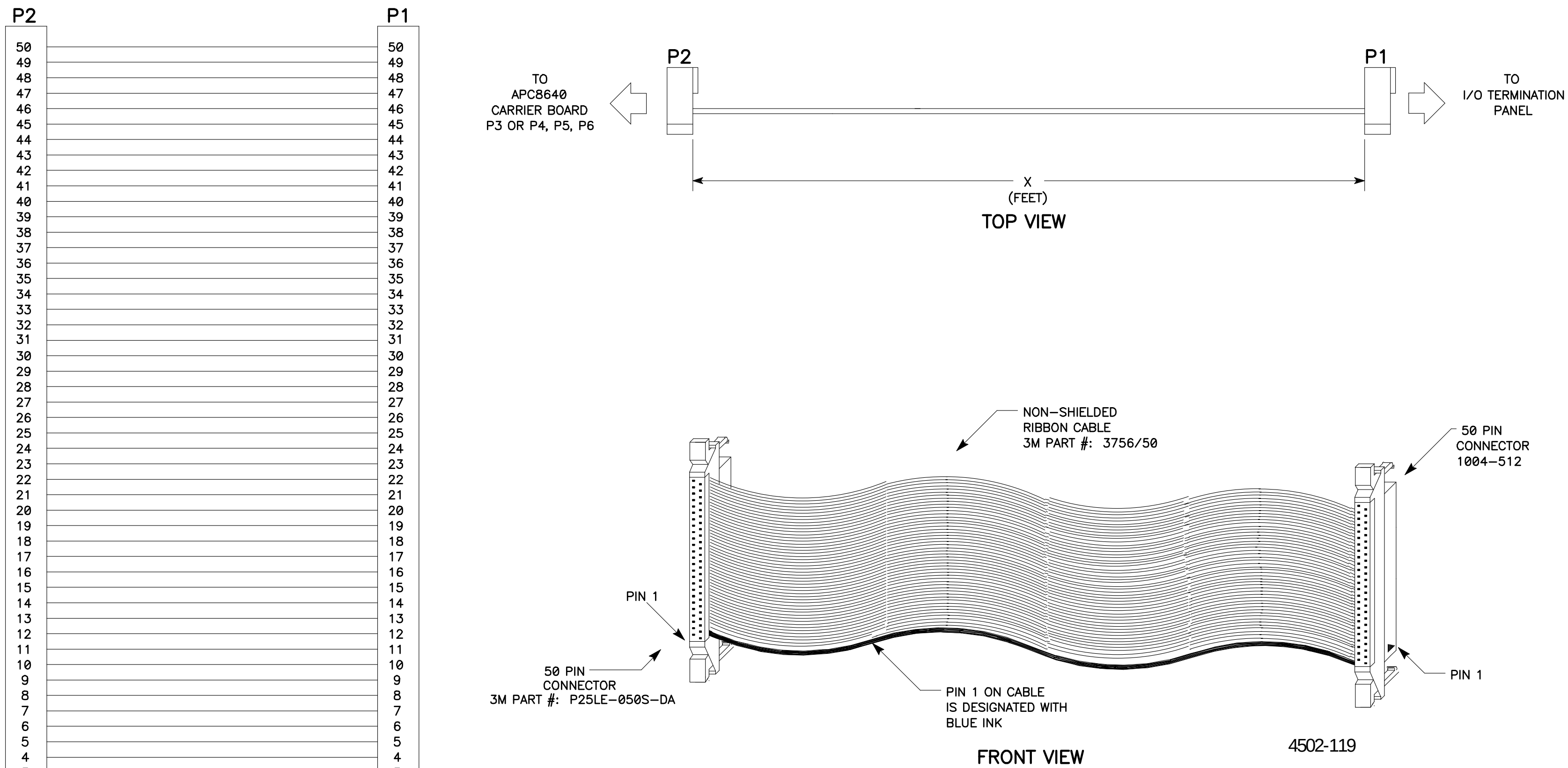


4501-672A

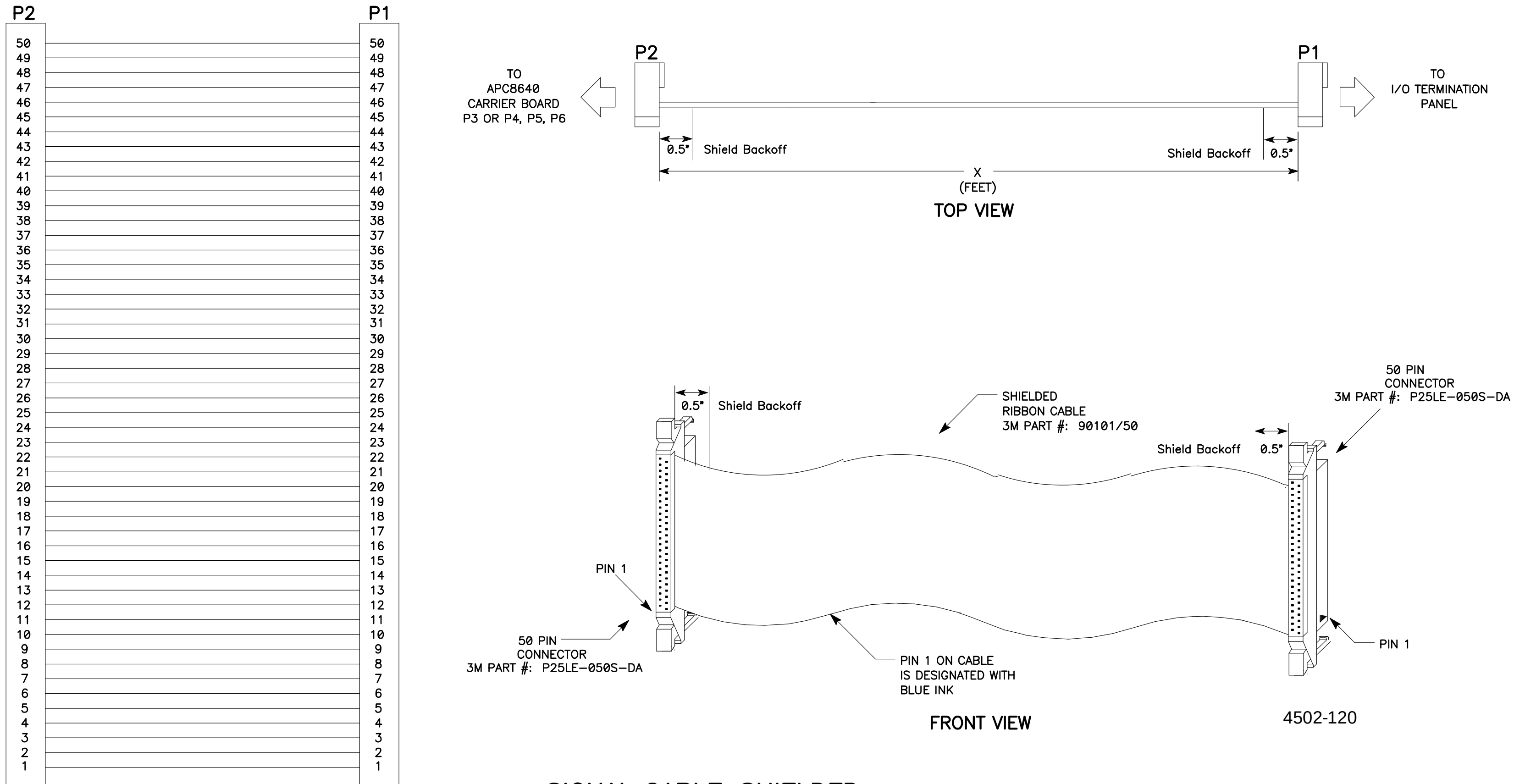
APC8640 BLOCK DIAGRAM



4502-113



SIGNAL CABLE, NON–SHIELDED



SIGNAL CABLE, SHIELDED